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Modulation Index Variation Effect on Harmonic Behavior of Fifteen Multilevel Inverter Neutral-Point-Clamped Topology

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ABSTRACT

The Market for photovoltaic cells (PV) has grown fast due to a higher demand on PV applications. However, there are still the transport and connection problems of the PV systems to the grid because of the difference in the current form. To assure the adequate connection between the PV sources and the network, the conversion of direct current (DC) to an alternative current (AC) is required and provided by an electronic device known as the inverter. In this last years, the conventional inverter structure reached its limits in power level and conversion performance. The multilevel inverter (MLI) structure was introduced and widely used in high power and high voltage applications to solve the conventional inverter limitation problem. In this paper, the Neutral-Point-Clamped (NPC) topology of the MLI was simulated to evaluate the effect of modulation index variation of the control technique on the harmonic behavior of the fifteen-level NPC. The simulation results were useful for the optimization of the MLI control technique toward the decrease of the harmonic (THD) effect on the NPC MLI.

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1. INTRODUCTION

Photovoltaic (PV) systems world market know a fast growth during the last year due to the necessity of developing the renewable energy to replace the fossil fuels [1]. However, this rapid growth required in parallel the improvement of the PV chain efficiency such as the PV generator energy yielding, the electrical power transport performance and the adequate connection to the grid [2]. One of the important parts of the conversion chain devices is the inverter which allows the conversion of DC signal to AC signal in purpose to permit the distribution and connection of the output electrical energy of the PV generator to the network [3]. In addition to PV conversion chain, inverters are used in power system applications and uninterrupted power supplies industries [4]. The inverters power efficiency to feed the different type of loads of the grid reach the max level and it is due to the increase of inductive load usage. More inductive loads mean more harmonics and less conversion efficiency [5]. Improvement of the output power quality of the inverter required reducing its total harmonic distortion (THD) content and decrease the size of the filter used [6]. As a solution for this requirement, a new family of the inverter has emerged and known as the multilevel inverter [7]. Multilevel Inverter (MLI) technology assures some advantages comparably to the conventional technology and deals with higher power applications which make it much easier to deal with lower power applications such as the PV systems [8-19]. One of the main advantages of the MLI structure is the improvement of the output voltage waveform by approaching the sinusoidal waveform which implicates reducing the harmonic stress

and noises on the switches, usage of smaller filter size and lower output power losses. MLI can be divided into three main topologies, neutral-point-, flying capacitor (FC) and H-bridge cascaded. Moreover, many deviated topologies are emerging every day [20]. The advantages of multilevel inverters have been well known since the first NPC inverter was proposed in 1981 by *Nabae et al*. [21]. This particular topology increases the power rating because the blocking voltage of each switch is one-half of the dc-bus voltage. Moreover, their output voltage harmonic content is much smaller than that of the conventional inverters with the same switching frequency owing to the output voltage waveform improvements [22]. Many switches strategies are used for the control of the NPC topology and can be divided into two categories, strategies dealing with high switching frequencies such as sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM) and methods dealing with lower switching frequencies such as space vector control (SVC) and optimized harmonic stepped waveform (OHSW). SPWM is a very popular method in industrial application and it is based on the classic comparison of the triangular carrier with the sinusoidal pulse width modulation which is used to reduce the THD in the output voltage [23]. However, optimization of this controlling method is required to assure a lower harmonic stress on the switches operating. In this paper, the NPC topology of the MLI was simulated and controlled by the SPWM strategy. The modulation index comparing the carrier waveform with the sinusoidal fundamental form was variated on its dependency with THD was optimized.

2. SYSTEM DESCRIPTION

Fifteen-level multilevel NPC topology was reviewed in this paper. The NPC structure has the advantage of lowering the electromagnetic interference (EMI) effect on the output voltage of the loads. Combining this topology with an adequate control strategy such as the SPWM it maybe will lead to emerging new advantages such as THD reducing and waveform output improvement.

2.1. MLI Circuit Schematic

Figure 1 illustrates the circuit schematic of the fifteen-level NPC topology. This structure is powered up using fourteen power sources and one leg of the three phase circuit consist of 28 principal dispositive of commutation (IGBTs) and 54 diodes to assume the control of the IGBTs. The components number of this topology was calculated as shown in Table 1.

One of the merits of the NPC topology is the absence of capacitors in the circuit which decrease the circuit reaction time as shown in Table 1. The 28 IGBTs are divided into two groups (S) and (S') in one leg, and each pair was operated in complementary mode (Sa1, S'a1) to (Sa14, S'a14). The operating detail and the logical diagram of the SPWM are discussed in the next subsection.

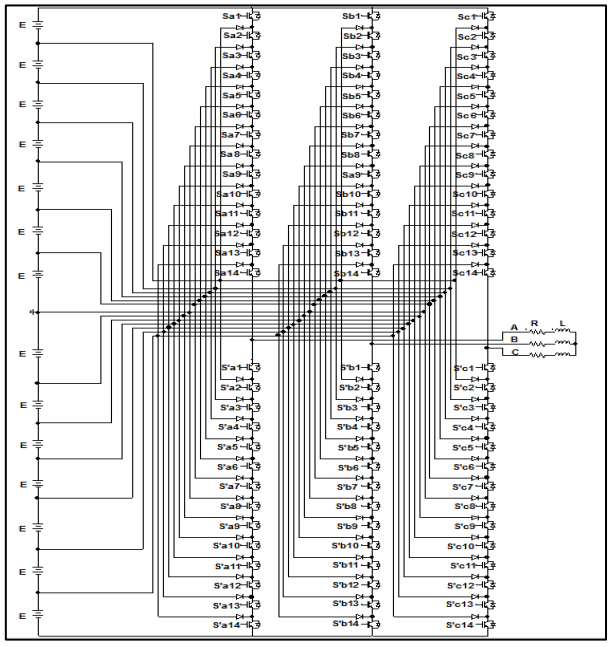

Figure 1. Three phase fifteen-level NPC inverter schematic circuit

Table 1. Components number of the NPC topology (Number of switches, Number of Diodes, Number of Capacitors)

	Topology	
	NPC m level (3Ø)	Studied 15-level NPC (3Ø)
Power Source	m-1	14
Principal dispositive of commutation	6(m-1)	84
Diodes	6(2m-3)	162
Capacitors	0	0
Total number of components	19m-25	260

2.2. Control Strategy SPWM

The sinusoidal pulse width modulation is based on high-frequency switching as already discussed above, it consists of comparing the fundamental frequency sinusoidal signal with a high-frequency carrier waveform. The logical control of the SPWM is based on the phase equality of all carriers known as the PD control as shown in Figure 2.

One triangular signal carrier is compared to a sinusoidal signal an each interactions give a signal, while the dc generator is used to shift the output signal from the comparison depending on the number of impulsion required to control one hand of the inverter.

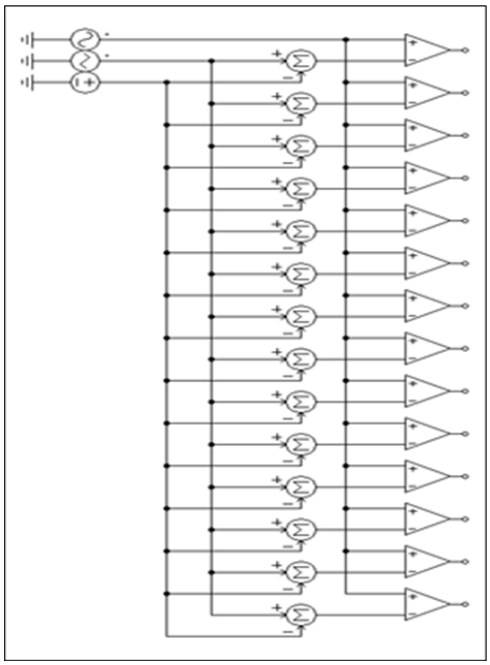

Figure 2. SPWM Logical Controlling Diagram for One Leg 15-level inverter

Each intersection between the sinusoidal and the carriers signals results in a command order. In this case study, the sinusoidal signal is compared to 9 carrier's signals in phase as shown in Figure 3. The PD control has the advantage of decreasing the THD factor by reducing the harmonic stress on the switches. The control signal G1 to G14 are generated by the intersection of the triangular carriers signal C1 to C14 with the fundamental frequency sinusoidal signal.

The switches operating is done by execution of few logical process, and the control result of the switches is shown in Table 2. The control is done in complementary mode which means each pair of interrupters could have two specific value such as 1 (On) for the first such as Sa1 and 0 (Off) for S'a1.

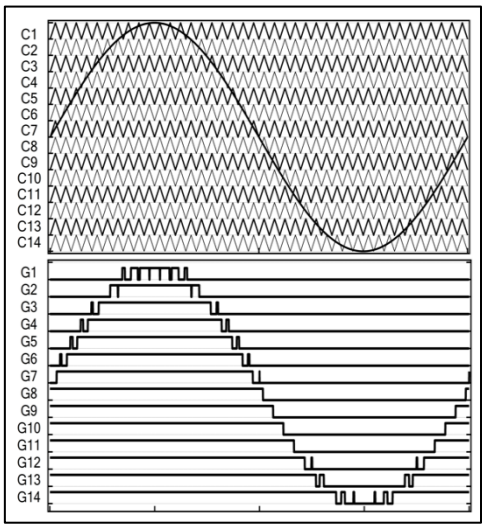

Figure 3. Switching Control Patterns SPWM 15-level

Table 2. Different Switching Stages for one Leg (1=ON, 0=OFF)

VAO	7E	6E	5E	4E	3E	2E	E	0	-E	-2E	-3E	-4E	-5E	-6E	-7E
Sa1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Sa2	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
Sa3	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Sa4	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
Sa5	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
Sa6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
Sa7	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
Sa8	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Sa9	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Sa10	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Sa11	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Sa12	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Sa13	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Sa14	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S'a1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S'a2	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
S'a3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
S'a4	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
S'a5	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
S'a6	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S'a7	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S'a8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S'a9	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
S'a10	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S'a11	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
S'a12	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S'a13	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
S'a14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The amplitude modulation index also is known as the modulation factor which describes the relationship between the carriers amplitude (Ac) with the sinusoidal amplitude (Am) is given by Eq. (1), where m is the number of level of the inverter, and its variation is shown in Table 3.

$$m_i = \frac{A_m}{(m-1)A_C} \quad (1)$$

Table 3. Modulation Index Variation

Carrier Amplitude	Sinusoidal Amplitude	Modulation factor
	1.76	0.88
	1.78	0.89
	1.8	0.9
	1.82	0.91
	1.84	0.92
	1.86	0.93
	1.88	0.94
	1.90	0.95
	1.92	0.96
	1.94	0.97
	1.96	0.98
	1.98	0.99
0.143	2	1
	2.02	1.01
	2.04	1.02
	2.06	1.03
	2.08	1.04
	2.1	1.05
	2.12	1.06
	2.14	1.07
	2.16	1.08
	2.18	1.09
	2.2	1.1
	2.22	1.11
	2.24	1.12

3. SIMULATION AND RESULTS DISCUSSION

Figure 4 shows the phase output voltages and line-to-line voltages V_{AB}, V_{BC} and V_{CA}. Moreover, they are deducted from the pole output voltages as illustrated in Equation (2).

$$\begin{aligned} V_{AB} &= V_{A0} - V_{B0} \\ V_{BC} &= V_{B0} - V_{C0} \\ V_{CA} &= V_{C0} - V_{A0} \end{aligned} \quad (2)$$

The line-to-line voltages are shifted by 120° between each other's, the 15 level line-to-line voltages (7E, 6E, 5E, 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E, -5E, -6E, -7E) are produced from 13 level pole figure related by the pole voltage number [m-2] (where m is the number of MLI levels) is used to get [m] line-to-line output voltages. Figure 5 illustrates the simulation results of the phases currents shifted by 120° and in the case of pure inductive load, the current shape was stable and had a smoother waveform, and it is due to the induction filtering comparable to the pure capacitive load (b). Smoother waveform and its due to the induction filtering of the harmonic component.

Furthermore, the variation effect of the modulation factor on the THD is illustrated in Figure 6. The change of the modulation index has an impact on the THD value, and these results prove that a specific value of the modulation factor corresponds to the lower value of THD. In this case, the optimum condition for lowering THD required that the amplitude of the sinusoidal signal be in [1.05-1.07] times the carriers signal amplitude. These results can be explained as the larger amplitude of the sinusoidal waveform will interact more and in an efficient way leading to reduce the harmonic stress on the controlling switches (IGBTs).

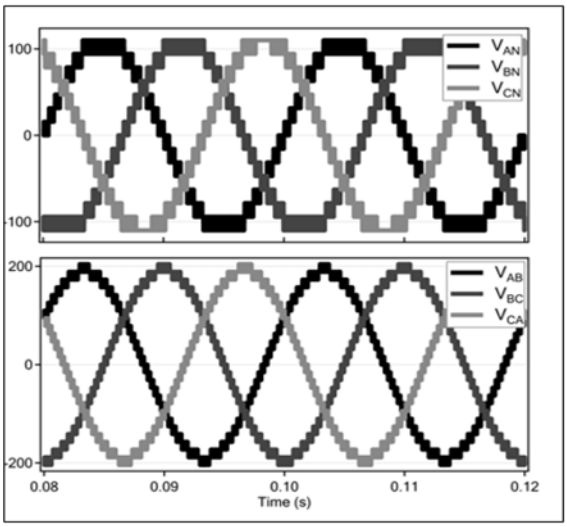

Figure 4. Inverter Output (a) Pole voltages, (b) Line-to-line voltages

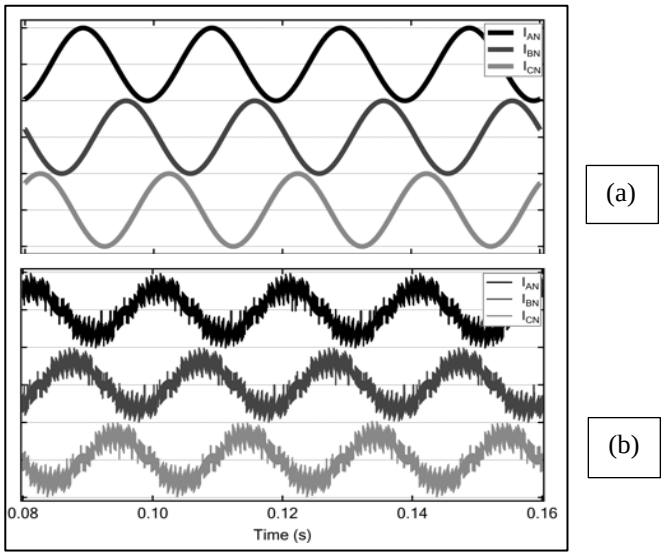

Figure 5. Inverter Output phase current (a) Pure Inductive charge (R=20 Ω, XL=63 Ω) (b) Pure Capacitive charge (R=20Ω, XC=63 Ω)

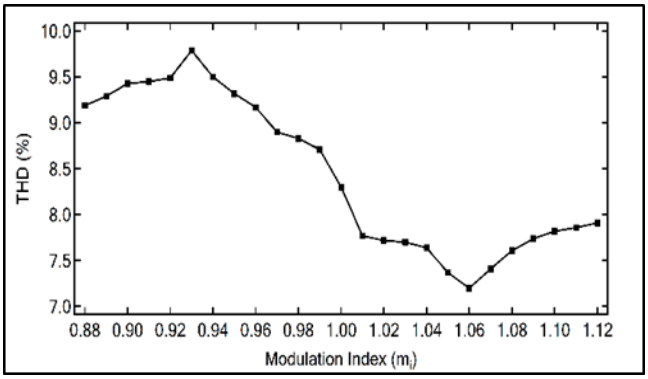

Figure 6. Total Harmonic Distortion (THD) dependecy on the variation of the modualtion index

4. CONCLUSION

In this paper, the simulation of the MLI NPC topology was discussed with the fifteen-level output voltage.The improvement of the SPWM control strategy was discussed in term of waveform amplitudes. The modulation index describing the amplitude relationship between the sinusoidal signal amplitude and the triangular waveform amplitude was optimized based on its dependency to the THD changing. Lower THD values were observed for small variation range of the amplitude modulation index.

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