Event-focused control strategy for a SiC-based synchronous boost converter working at different conduction modes.

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***Abstract*— A SiC-based synchronous boost DC/DC converter rated for 400V to 800V and 10kW with high efficiency, especially at medium and light load, is designed and developed. The better switching performance of SiC MOSFETs allows the use of high switching frequency operation modes even at voltage close to 1kV (previously avoided due to the high switching losses introduced by silicon IGBTs). Evaluation of all the power losses in the converter for different conduction modes is fulfilled. Since the model of losses predicts suitable performance of QSW-ZVS conduction mode for low and medium loads, an event control strategy will be detailed taking advantage of digital control. This methodology will also allow self-regulating modifications of the operation mode in order to optimize the efficiency for different loads. Consequently, a control strategy based on events and switching among modes is proposed to maintain high efficiency in a wide power range.**

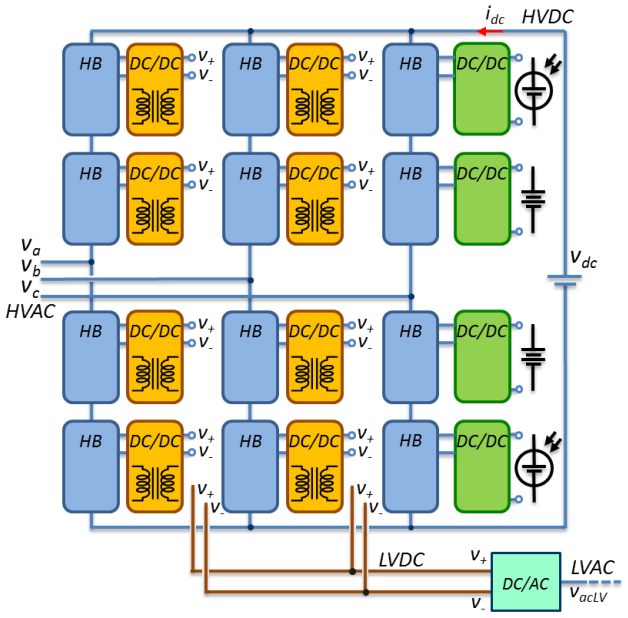
Keywords*— *light load, conduction modes, QSW, SiC MOSFETs, events control

I. INTRODUCTION

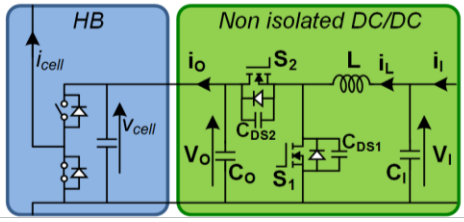
Power Electronics Transformers (PETs) have been proposed as a semiconductor based alternative to conventional Line-Frequency Transformers (LFTs) [1]-[3]. A fully modular three stage approach (AC/DC + DC/DC + DC/AC) appears to be the most popular choice [2], [4]-[6], being very common the use of multilevel converters to develop the AC/DC stage of the PET, as in the case CHB-based PET [6] and MMC-based PET [7] (Fig. 1a). It is possible to integrate storage systems at the cell level (or other low voltage dc or ac power sources, such as PV panels or wind turbines) [8], [9]. However, if the voltage level of the cell (usually, around 1 kV) and the voltage level of the storage system are different, the use of bidirectional power converters is mandatory to adapt the energy format (Fig. 1b). The power converter connecting the battery with the PET cell must withstand high voltage providing high efficiency over a wide power range.

Nowadays, most of the high-power converters are digitally controlled, making possible modifications of the operation mode. In this paper, a control strategy, based on theoretical efficiency models, that changes the conduction mode to achieve the maximum attainable performance of a Silicon Carbide (SiC)-based synchronous boost converter is proposed. Although this work is oriented to develop a bidirectional converter able to provide energy storage capability to a PET, the extracted conclusions can also be applied to other applications where a bidirectional converter with high efficiency and high voltage operation is needed.

This paper is organized as follows. Section II outlines the main characteristics of the different conduction modes proposed in this work. In Section III an extensive description of the whole topology is presented, highlighting the event-focused strategy followed to achieve automatic Quasi-Square Wave mode with Zero Voltage Switching and the approach taken to alternate among modes. Section IV shows the most relevant experimental results obtained. Finally, conclusions are drawn in Section V.

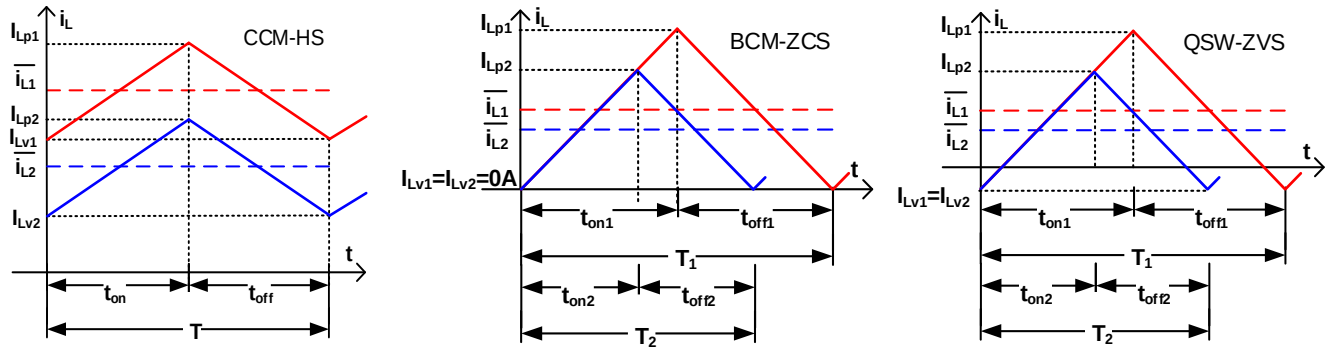


(a)



(b)

Fig. 1 (a) Distributed energy sources integration in a MMC-based PET. (b) Structure of the cell.



(a) (b) (c)

Fig. 2 Inductor current waveform for two different power levels.

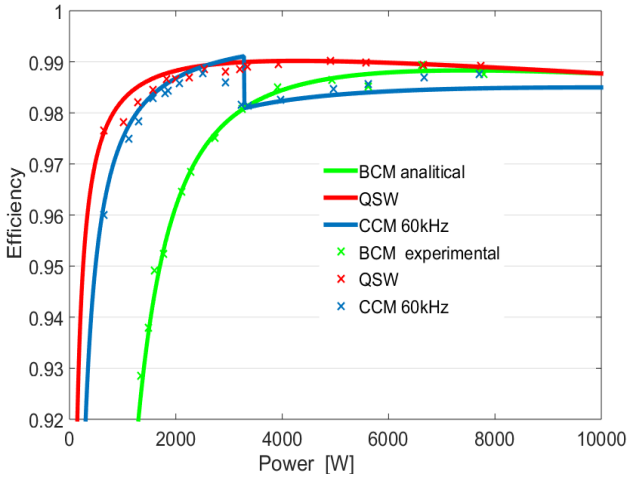


Fig. 3 Analytical and experimental efficiency comparison

II. Analysis of Different Conduction Modes

Different control strategies have been proposed for boost converter topology (Fig. 1a, green converter). A brief summary of the characteristics of the three analyzed continuous conduction modes (CCM) is presented and their key waveforms are shown in Fig. 2.

1) CCM hard switching (CCM-HS). Reduced current ripple (inductance current always positive) and constant switching frequency (f). Its key advantage is the low current ripple, performing low conduction losses. High switching losses are the main drawback. At light loads, this mode achieves ZVS (Triangular Conduction Mode (TCM)).

2) Boundary Conduction Mode with Zero Current Switching (BCM-ZCS). Large current ripple (inductance current is zero at the turn-on of S_1) and variable switching frequency. Switching losses are reduced but, conduction losses are increased [10], [11].

3) Quasi-Square Wave mode with Zero Voltage Switching (QSW-ZVS) [12]. Large current ripple (inductance current is negative at the turn-on of S_1) and variable switching frequency. Full ZVS can be achieved for certain relations of input and output voltages [12], reducing switching losses but also increasing conduction losses.

Analytical models for the estimation of the efficiency of a synchronous boost converter operating in the three specified conduction modes are developed and experimentally validated (Fig. 3) in a synchronous SiC-based boost converter going from 400V to 800V and maximum power rate of 10kW. The switching frequency is 60kHz for CCM-HS and varies from 20kHz to 200kHz [13] for BCM-ZCS and QSW-ZVS.

Among the different Wide Band Gap (WBG) semiconductors, SiC MOSFETs are chosen since they allow high efficiency operation of the power converter even under high switching frequencies and high voltage requirements [14]. The use of these SiC MOSFETs allows a wide variation of the switching frequency, providing high efficiency at low power, where high frequency is needed to maintain QSW-ZVS.

BCM is disregarded in the following sections of this work since it does not provide any improvement for any load range compared to the other two conduction modes, as can be seen in Fig. 3.

In order to obtain high performance in a synchronous boost converter, SiC MOSFETs are employed and a variable switching frequency control strategy is implemented. This technique is beneficial to provide ZVS, especially at light and medium load operating points. However, a high current ripple is the price to pay of the proposed operation mode, which increases conduction losses, especially at full load [15],[16]. To take advantage of the different conduction modes and to obtain a high performance of the converter in the full power range, a control strategy switching among modes is proposed

III. Implementation of the Digital Control Strategy

Many blocks are distinguished during the implementation of the whole system (Fig. 4), each one focused on a different task.

Firstly, the boost converter block itself, considering it as the hardware used: SiC power devices, driver, inductor and capacitors (which will be described in detail in Section IV). Gate signals (G_1, G_2) are given to the driver of the boost converter, so it is able to convert a certain DC input voltage value into another output voltage level (V_o) under certain load demands.

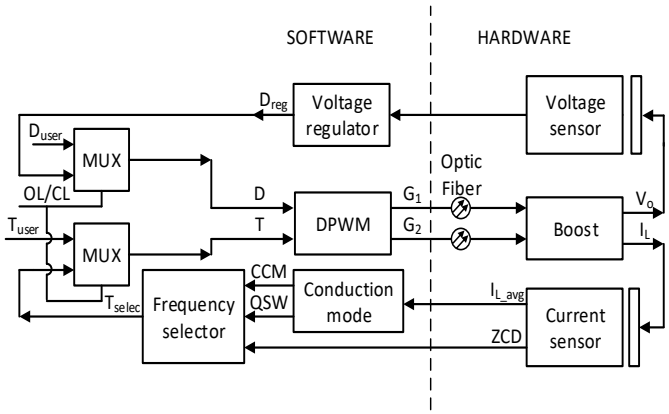


Fig. 4 Blocks schematic of the topology implemented

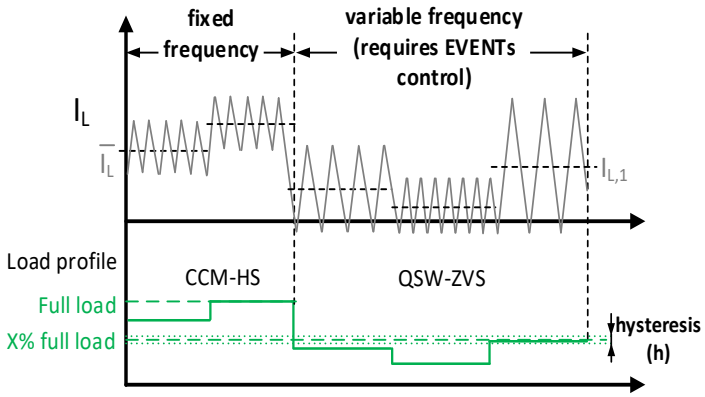


Fig. 5 Switching among modes depending on the load level

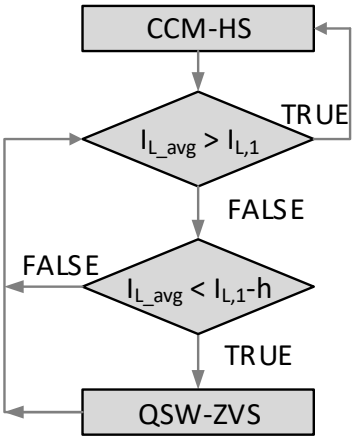


Fig. 6 Flow chart explaining switching between modes

The rest of the blocks are implemented through an FPGA, except the current and voltage sensors (which will be also described in Section IV).

The purpose of the DPWM is generating the proper gate signals required by the boost converter. For that, it needs the duty cycle (D) and the period (T) desired for each switching period. It also sets the mandatory deadtimes needed to avoid short-circuits or any other undesired behaviour.

The main object of MUX blocks is assuring complete control of the system during the failure procedure test. This means that when working in closed loop (CL) the MUXs provide the DPWM with the period or duty cycle calculated by the voltage regulator and the frequency selector (D_{reg} and T_{selec}, respectively). In contrast, during failure procedure tests (open loop, OL) the user can select any desired value (D_{user} and T_{user}) to analyse the performance of the topology under any load condition.

The blocks named voltage regulator, conduction mode and frequency selector are deeply explained in the following sections. They are the key to implement an event control strategy based on variable switching frequency able to adapt to changing load conditions without losing high performance.

It is worth to remark that the communication between the power stage (boost block) and the control stage (rest of blocks) is isolated providing more reliable working conditions of the system. The communication (gate and error signals provided by the driver) between the FPGA and the driver is done through optic fiber, while isolated sensors are used to obtain the output voltage and the inductor current.

A. *Changing among conduction modes to improve efficiency*

In order to optimize the performance for the whole power range, a control strategy based on switching among conduction modes for different load levels is applied (Fig. 5 and Fig. 6). The efficiency at high load for these conduction modes are similar for the analysed specifications (calculated using the efficiency models and experimentally validated, see Fig. 3). It allows a control strategy based on other factors, such as, current ripple or peak current level, which are beneficial strategies during the battery charging process, because during the initial stage of charge, currents are considerably higher, and allow a reduction of the current stress of the power devices.

Other conditioning factors to stablish a compromise could be considered, such as, ElectroMagnetic Interferance (EMI) due to frequency variation, but it is not the scope of this work.

The algorithm proposed concedes special attention to current level. To reduce the current ripple and the peak current level through the MOSFETs and inductor, CCM-HS is preferred for high loads. It also provides easier control since it works at a fixed frequency. When the power decreases and the peak current level of QSW-ZVS is similar to that of CCM-HS at full load (considering a certain hysteresis), QSW-ZVS is selected and maintained for lower loads to keep high efficiency. The average inductor current value associated to this peak current level is called $I_{L,1}$ in this paper (Fig. 5 and Fig. 6).

An example with the prototype specifications: if peak current level at 10kW is 33A for CCM-HS, the control will change to QSW-ZVS when the load level is below 5.4kW (which corresponds to $I_{L,1}$ = 13.5A and 33A of peak current level for QSW-ZVS). It is also worth to remark that below this power level the efficiency using QSW-ZVS is considerably higher than CCM-HS

This control strategy and the estimation of the proper value of $I_{L,1}$ can be carried out since all the information about the different conductions modes (switching frequencies, peak current values, efficiency, etc. for different loads) is given by the developed efficiency models[13] (briefly presented in Fig. 3).

In this application, the average current through the inductor (I_{L_avg}) is measured using a high bandwidth current sensor (CQ3200) twice every period at T/4 and 3·T/4 (see Fig. 7). Then, this value is compared with $I_{L,1}$ and a decision about the best conduction mode is taken. A hysteresis condition is contemplated in order to avoid loss of control for boundary situations (i.e. when I_{L_avg} is exactly $I_{L,1}$ any variation in load, noise or any other source of disturbance could make the control continually shift the frequency).

Consequently, the Conduction mode block discerns whether if CCM-HS or QSW-ZVS is the better option depending on the average current of the inductor (I_{L_avg}) given by the current sensor.

B. Event-based DPWM to operate in QSW-ZVS

A DPWM at constant frequency is easily implemented. Constant dead-times and the duty cycle given by the voltage closed loop control are used to generate the gate signals to operate in CCM-HS. However, to assure QSW-ZVS (variable frequency) a more careful design of the control is required (Figure 7).

In the Frequency selector block, a period is chosen depending on the conduction mode. There are no calculations needed when CCM is desired, but the block requires extra-information from the current sensor block if QSW is the mode selected.

S1 conduction time (t_{onS1}) is given by the voltage regulator, to ensure the desired output voltage. Nevertheless, S_2 conduction time (t_{onS2}) depends on zero current detection (ZCD) to assure QSW-ZVS operation. It is difficult to find an ADC fast enough to obtain an accurate digital detection of the ZCD. Therefore, the output of the current sensor used to measure (I_L) is analogically compared with a reference (LMV7219) providing an event to the FPGA. This event is detected by the FPGA within a certain delay that remains constant for any frequency (t_{det}). The value of the following switching period is determined by the exact moment where the FPGA detects this current event. After the ZCD a certain time (t_{QSW}) where the resonance takes place is set. This time is big enough to allow the energy stored in the inductance discharges the capacitor of the power device achieving ZVS. The delay between ZCD and the current event does not compromise the accuracy of this method, since this time delay is constant for different switching frequencies and is lower than t_{QSW}. Finally, after the deadtime finishes, S_1 is turned on, beginning a new period. Fixed dead-times to avoid shoot-through, t_{d1} and t_{d2} (included in t_{QSW}) are used.

IV. Experimental Results

Some experimental results to validate the proper operation of the proposed converter composed of the blocks showed in Fig. 4 are exposed.

The boost converter prototype developed (Fig. 8) consists of the MOSFET module CCS020M12CM2 from CREE® and the 3-channel driver CGD15FB45P1. The value of the inductor is 200µH (one inductor of 600µH per branch, 3 branches in parallel). The FPGA under current use is Nexys 4 DDR based on a ARTIX 7 from XILINX ®. Small capacitor values are used for this application: 4 µF for the input and 12 µF for the output.

Regarding the current sensor, it is especially interesting to show the current event detection in which this work is focused. To obtain this event, the current sensor CQ3200 and analog comparator LMV7219 are used. In Fig. 9 tests under 3.5kW are performed, with 800V as output voltage and 43kHz of switching frequency in order get QSW-ZVS. As it can be seen, t_{det} is shorter than the time needed to achieve ZVS t_{QSW}, so the event control method fits the requirements.

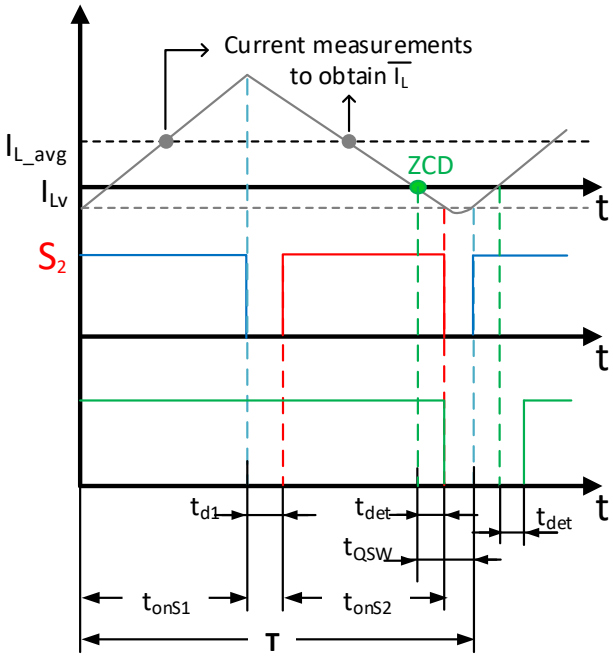


Fig. 7 Current through the inductor (in black), gate signals (S_1 in blue, S_2 in red) and current event detection signal (in green).

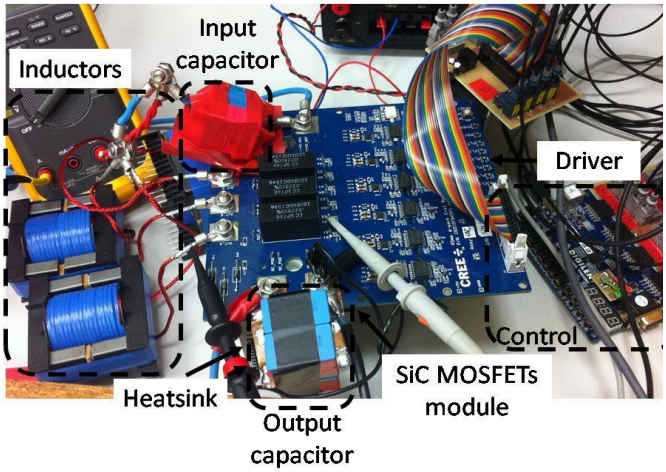


Fig. 8 Prototype: 200uH inductor, MOSFET CCS020M12CM2 and Driver CGD15FB45P1.

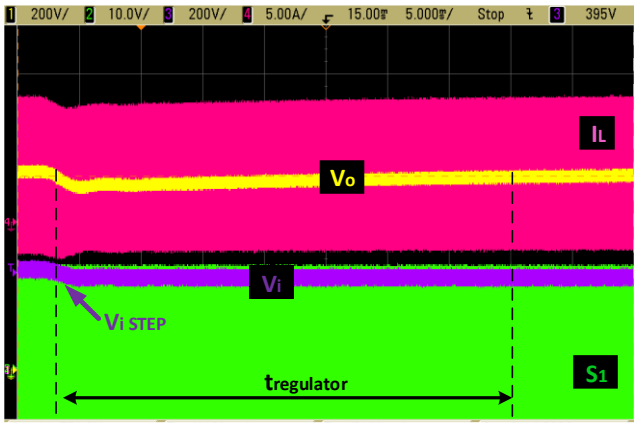


Fig. 9 Dynamic behavior of th PI regulator after a step in the input voltage. Input voltage (V_i, in purple), gate signal (S_1, in green), current through the inductor (I_L, in pink) and output voltage (Vo, in yellow)

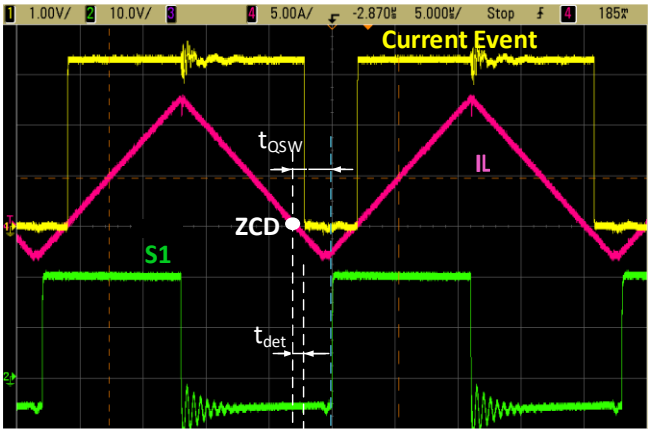
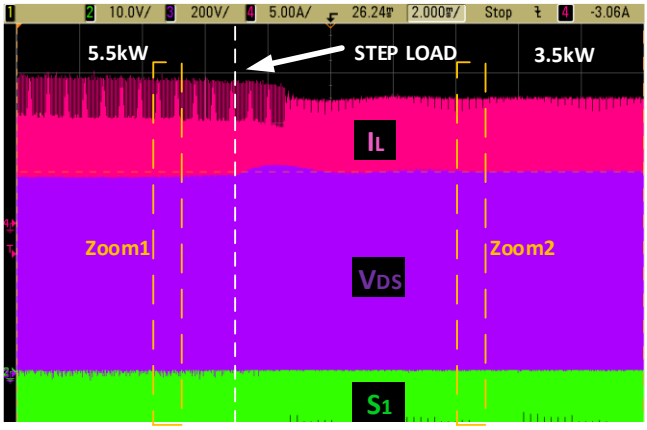


Fig. 10 Current event detection based on the current sensor and ZCD. Gate signal S_1 in green, current through the inductor in pink and current event signal in yellow.

In relation to the close loop voltage regulator, in Fig. 9 a step in the input voltage is shown to prove its dynamic behaviour, going from 400V to 350V, but keeping 800V in the output. A PI regulator is designed for this purpose with a slow time response (see $t_{regulator}$, which is around 35ms). In this application, fast transient is not required. In contrast, a slow and smooth recovering is desired, not to damage the system, since devices are withstanding high voltages and high currents might be circulating. The PI regulator is further tested under steps in the reference voltage and step loads fitting in all cases the expectations.

The current event detection is tested in Fig. 10. When the current through the inductor goes below 0A, the current event signal changes its edge. This event arrives to the control after a certain delay (t_{det}). At that moment the control saves the time that has passed from the beginning of the switching period to that instant, to stablish the following switching period. As can be seen, t_{det} is smaller than t_{QSW}, which, as seen before, is the period of time where the current goes negative and the output parasitic capacitance of the device is discharged.



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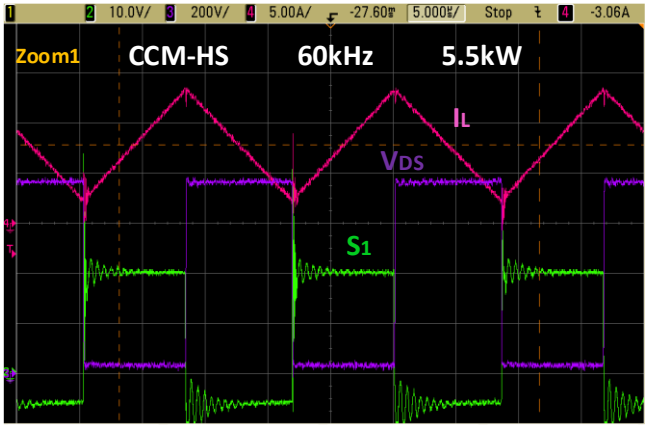

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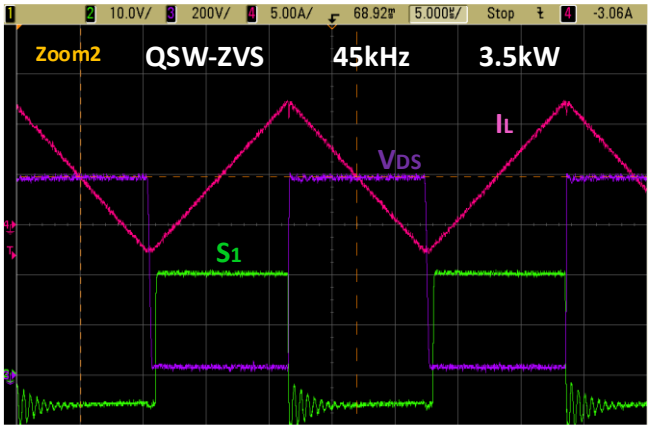


(c)

Fig. 11 Switching from CCM-HS conduction mode to QSW-ZVS conduction mode after a step load. by detecting $I_{Lavg\_} < I_{L,1}$ (a) general view, (b) zoom of the CCM-HS mode and (c) zoom of the QSW-ZVS mode.

In Fig. 11a, b and c a step load is performed in order to prove the two methodologies proposed and described in this paper.

On one side, changing between modes is tested. The control is able to detect the average value of the inductor current, I_{L_avg} and compare it with a certain value, $I_{L,1}$ +/- a certain hysteresis and set a certain switching frequency depending on it.

On the other side, when the control decides that QSW-ZVS is preferred, the control can stablish exactly the switching frequency needed for any load.

In Fig. 11a, a general view of the step load performed is shown, with an appreciable load change going from 5.5kW to 3.5kW. As it was explained in previous sections, the boundary average current in this application is set for $I_{L,1}$ =13A. When the load demand I_{L_avg} goes under/over this value the preferred mode changes.

In Fig. 11b, a zoom of the first stage of the step load is displayed. CCM-HS conduction modeat a fixed switching frequency of 60kHz is selected. It is seen that the current through the inductor is always positive and with reduced current ripple.

In Fig. 11c, a zoom of the second stage of the step load is presented. In this case QSW-ZVS conduction mode with an automatically selected switching frequency of 45kHz appears. It is appreciable how V_{DS} goes to zero just before the next switching period, avoiding hard switching, yet dealing with high current ripple.

In the same way, in Fig. 12a, b and c a step load is performed to prove how the control changes the switching frequency when operating always under the threshold $I_{L,1}$.

In Fig. 12a, a general view of the step load performed is shown, with a step load going from 3kW to 2.5kW. Since both power demands correspond to average currents lower than the threshold, the conduction mode preferred is QSW-ZVS.

In Fig. 12b, a zoom of the first stage of the step load is presented. In this case QSW-ZVS conduction mode with an automatically selected switching frequency of 54kHz appears.

In Fig. 12c, a zoom of the second stage of the step load is shown. In this case QSW-ZVS conduction mode with a switching frequency of 69kHz is automatically set.

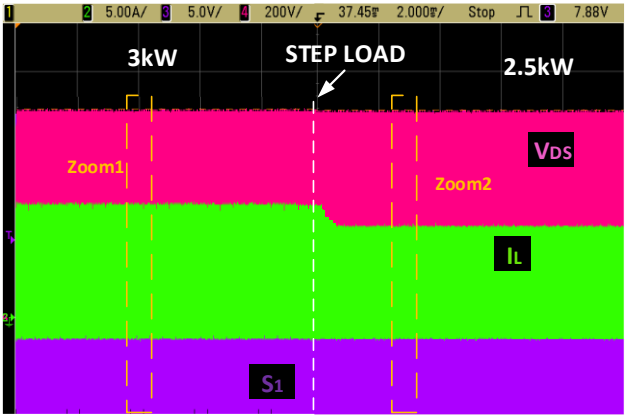
V. Conclusions

Three conduction modes in a SiC-based synchronous boost converter are analysed and compared in this work showing both theoretical and experimental efficiency results with good match between them.

The efficiency results given by the theoretical models of each conduction mode, allow the design of a control based on switching among different conduction modes depending on the load demand to keep the efficiency almost constant in a wide operation range, assuring good performance under certain current levels, which is beneficial for certain applications, i.e, battery charging.

Besides the control strategy, an event detection strategy followed to assure QSW-ZVS operation mode is developed in order to get a variable frequency, showing the expected results in the experimental tests.

CCM-HS mode provides low current ripple at the expense of hard-switching behaviour, while QSW-ZVS is able to keep efficiency for really low loads with soft switching at the cost of higher current ripples. To take advantage of both conduction modes a digital control is developed to select the better one depending on the inductor current.



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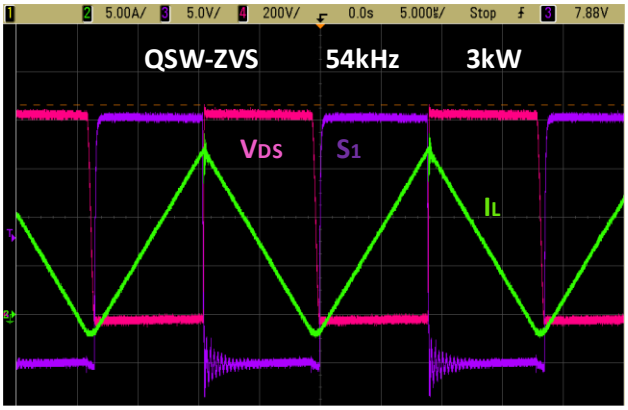

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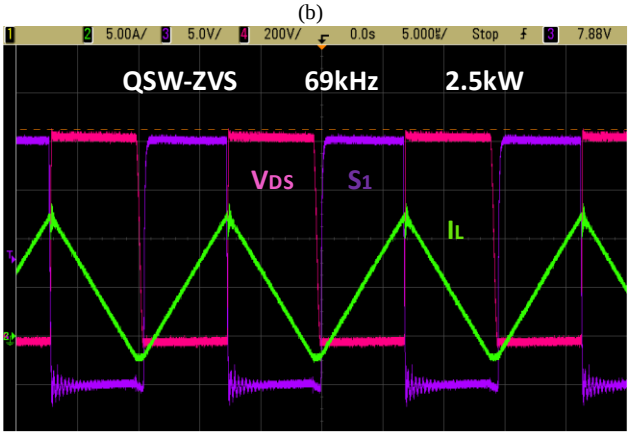

(c)

Fig. 12 Switching from QSW-ZVS conduction mode to QSW-ZVS conduction mode after a step load by detecting I_{Lavg}< $I_{L,1}$ (a) general view, (b) zoom of the QSW-ZVS mode at 54 kHz and (c) zoom of the QSW-ZVS mode at 69 kHz.

Acknowledgments

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