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Impact of Precisely Positioned Dopants on the Performance of an Ultimate Silicon Nanowire Transistor: A Full 3-D NEGF Simulation Study

Vihar P. Georgiev, Ewan A. Towie, Asen Asenov, *Senior Member, IEEE*

***Abstract*— In this paper, we report the first systematic study of quantum transport simulation of the impact of precisely positioned dopants on the performance of ultimately scaled gate-all-around silicon nanowire transistors (SNWT) designed for digital circuit applications. Due to strong inhomogeneity of the self-consistent electrostatic potential, a *full* 3-D *real-space* Non-Equilibrium Green's Function (NEGF) formalism is used. The simulations are carried out for an n-channel NWT with 2.2 x 2.2 nm^2 cross-section and 6 nm channel length, where the locations of the precisely arranged dopants in the source drain extensions and in the channel region have been varied. The individual dopants act as localized scatters and, hence, impact of the electron transport is directly correlated to the position of the single dopants. As a result, a large variation in the ON-current and modest variation of the subthreshold slope are observed in the I_D-V_G characteristics when comparing devices with microscopically different discrete dopant configuration. The variations of the current-voltage characteristics are analyzed with reference to the behaviour of the transmission coefficients.**

***Index Terms*— single-atom transistor, discrete dopants, nanowire transistor, non-equilibrium Green's function (NEGF), 3-D simulations, quantum transport.**

I. INTRODUCTION

SILICON TECHNOLOGY can deliver sub-10 nm devices where 'every atom counts'. Manipulation of atoms with high precision on such a scale, in principle, can lead to technological innovations, such as transistors with extremely short gate length [1], quantum computing components [2] and optoelectronic devices [3]. One possible strategy to create this next generation of devices is to precisely place individual discrete dopants (such as phosphorous atoms) in a nanoscale transistor [4]. The number and the spatial distribution of individual dopants within the transistor of modern silicon chips determine both their characteristics and their unwanted variability [5], [6]. Hence, it is crucial to establish a direct link between the position of individual dopants and the transistors' performance [7], [8]. At the physical limit of transistor scaling a single phosphorous atom embedded within epitaxial silicon environment, in principle, can be used to build a single-atom transistor [9]. Although such an idea looks spectacularly attractive, the side gate architecture as explained in reference [9] is not really fit for the purpose of digital applications. In order to be able to reliably switch on/off such nanometer-scale transistors the preferable transistor architecture needs to be in 3D with a gate wrapped around the conductive channel. Such structures include FinFETs, trigate, Π–gate, Ω–gate and gate-all-around (GAA) MOSFETs. In particular the gate-all-around nanowire transistors (NWT) with a very small cross-section are very promising due to their excellent electrostatic integrity and scalability down to sub-5 nm dimensions [10]. Indeed such SNWTs have not only been experimentally demonstrated but they have also been the Holy Grail of demonstrating the impact of a single dopant in the channel [11]-[15].

Importantly, at channel lengths of sub 10-nm, all of these devices exhibit both strong quantum confinement and significant source-to-drain tunnelling [16], [17]. As a result, drift-diffusion and Monte Carlo simulations methods are not sufficient to describe their behaviour and full-scale quantum transport (QT) simulations are required. A favourite algorithm for such full 3-D QT calculations is the Non-Equilibrium Green's Function formalism (NEGF) [18], [19]. An additional strength of the 3-D NEGF method is in the potential to include consistently noncoherent scattering [20]-[22], such as phonon interactions, through introduction of appropriate self-energy matrixes. The self-energies allow folding of the entire many-body quantum transport algorithm into the one-particle Green's function equation [23]-[25]. In our work we neglected all sources of incoherent scattering, such as phonon interaction. The main reason for this is the 6 nm channel length of our SNWT. We believe that the inclusion of phonon scattering would have little impact on our results for the following reasons: Experiments and simulations of NWTs with 20 nm channel length and above show a high degree of ballisticity [26],[27]. Therefore we expect that nanowires with a channel length of 6 nm will operate close to the ballistic limit. In the highly doped source and drain regions the scattering is dominated by impurity scattering, and phonons play a minor role. It has been shown experimentally that the access resistance of the source and drain regions dominates the experimentally measured characteristics of such devices.

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V. P. Georgiev and E. A. Towie are with the Device Modelling Group, School of Engineering, University of Glasgow, G12 8LT Glasgow, U.K. (phone: +44-141-330-4792; fax: +44-141-330-4907; e-mail: Vihar.Georgiev@glasgow.ac.uk).
A. Asenov is with the Device Modelling Group, School of Engineering, University of Glasgow, G12 8LT Glasgow, U.K., and also with Gold Standard Simulations Ltd., G12 8LT Glasgow, U.K.

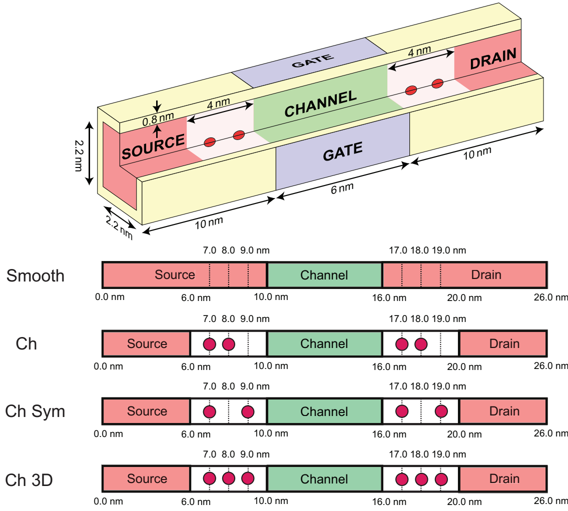


Fig. 1 Schematic view of the gate-all-around nanowires (Ch), showing the dimension of the transistor, and the shematic view for the Smooth, Ch, Ch Sym and Ch 3D devices used in the paper.

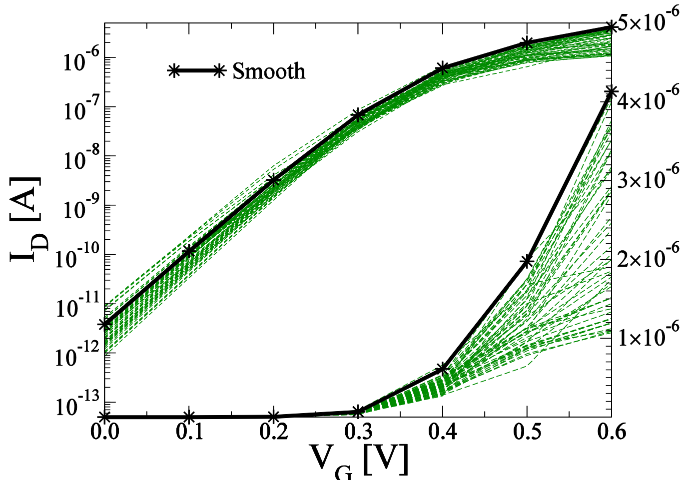


Fig. 2 I_D-V_G characteristics of 50 nanowire trasnsistors with discrete random dopants in the S/D region, a channel length 6 nm, and a cross-section of 2.2 x 2.2 nm^2, V_D = 50 mV.

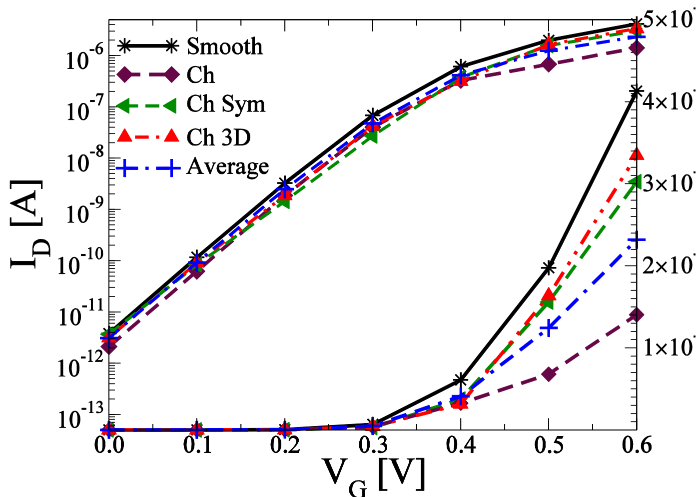


Fig. 3 I_D-V_G characteristics of a nanowire trasnsistor with discrete random dopants in the S/D region, a channel length 6nm, and a cross-section of 2.2 x 2.2 nm^2, V_D=50 mV. The violet line is the average value of the current obtained from Fig. 2.

In this paper, we begin with a brief description of the self-consistent NEGF/Poisson algorithm in Section II. Section III presents the results of the simulations, including the impact of precisely placed dopants in the access region in comparison with random doping (Subsection A). In Section III B we investigate the effect of a single channel dopant and its position along the channel on the device performance. Lastly, Section IV summarizes the main points and conclusions of this work.

II. Transport Model and Device Description

A. Simulation methodology

The simulations are carried out with the quantum transport module of the GSS TCAD simulator GARAND [28]. Quantum carrier transport is described using the full 3-D Nonequilibrum Green's Function simulation (NEGF) approach, which is a generalization of Landauer's formalism [29]-[32] used to treat many-body systems at room temperature in the context of one particle Green's function. The Hamiltonian used in the discretization of the NEGF equations is the effective-mass Hamiltonian that folds the full crystal interaction into the electron effective masses. The effective masses of the valleys are extracted from tight binding calculations that capture the dependence of the electron band structure on the nanowire cross-section. Due to the small cross-section of SNWT, only four of the six valleys of the silicon conduction band were included. The two valleys that were neglected have transversal masses (0.3m_e) in the direction perpendicular to the wire axes resulting in a larger ground-state-energy shift. As a result, the electron population in these valleys is negligible if compared to the other four valleys for the simulated nanowire orientation, diameter, temperature, and bias conditions. The correlation matrix, $G^<$, was calculated using a recursive algorithm [33]. Boundary conditions of the Green's function equations at the contacts, which are given throughout the contact self-energies, were defined by using the algorithm described in reference [34]. From the correlation matrix, the electron and current densities are calculated by the following equations:

$$n(E,x) = iG^<(E,x,x) \qquad (1)$$

$$J(E,x) = -i\frac{e\hbar}{2m}(\nabla - \nabla')G^<(E,x,x)\Big|_{x=x'} \qquad (2)$$

where $n(E,x)$ and $J(E,x)$ are the electron and current densities, respectively. The electron density is used to calculate, self-consistently, the electrostatic potential through the Poisson's equation. Adaptive damping is used after the solution of the Poisson equation to limit the change in the potential and improve the convergence. The obtained solutions of the NEGF and Poisson are iterated until density and current converge.

B. Simulated devices

The simulated devices are 6 nm channel length n-type SNWTs with a cross-section of 2.2 x 2.2 nm^2 illustrated in Fig 1. This type of device is expected by many researchers to mark the limit of the transistor scaling. The total length of

the simulated wire is (6 + 4 + 6 + 4 + 6) nm = 26 nm, where the five numbers represent the length of different regions into which the device is subdivided.

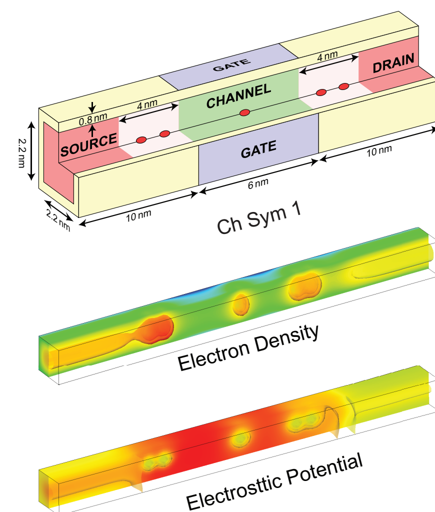
The 6 nm regions on the far left (source) and far right (drain) represent the S/D 'contact' regions of continuous doping, which provide smooth contact injection of self-energies and preserve the charge neutrality of the contacts. The electron transport in the nanowire occurs in the < 1 0 0 > direction. The donor concentration in the S/D contact regions is 10^{20} cm^{-3}. The oxide thickness is 0.8 nm and it is not included in the NEGF solution region but it is included in the electrostatic potential calculations. The dopants are introduced in a 4 nm-long extension regions between the S/D contacts and the gate region. For a doping concentration of 10^{20} cm^{-3}, there are only 2 dopants on average in the volume of 4 x 2.2 x 2.2 nm^3. All simulations were carried out at drain voltage (V_D) equal to 0.05 V in order to investigate the charge density around the impurities more easily and to provide consistent comparison with previously published results [35], [36], [37].

III. Performance Evaluation and Variability

A. Impact of the precise dopant placement on performance

As a first step in our study we carried out simulations on fifty devices with random dopants in the source and drain region reflecting the traditional way of introducing doping by using ion implementation and annealing. The current-voltage characteristics for all of these fifty microscopically different NWTs (with various impurity configurations) are presented in Fig. 2. The nanowire with continuous doping (labelled as "smooth" in the figure) is shown for comparison. Similarly to previously published results, [35]-[37], presence of the random dopants in the access regions leads to fluctuation of the threshold voltage and the OFF- and ON-current. Importantly, the existence of random dopants also results in a significant reduction of the average ON-current if compared to the smooth transistor. At $V_G < 0.3$, which marks the transition between the subthreshold slope and the linear region of the transistor, the device configuration with high concentration of discrete dopants close to the channel is lower than the gate barrier potential, leading to higher current than in the smooth case. At $V_G > 0.3$, the smooth device always delivers higher current than the nanowires with discrete dopants. This is directly correlated to introduction of ionised impurity scattering in the source/drain regions, which leads to increasing of the access resistance. Additionally, the random dopant configurations in the access regions also result in threshold voltage and subthreshold slope variations but these are relatively small.

Hence, it can be concluded that presence of random dopants in the access regions has significant influence over the main device characteristics. Furthermore, the average magnitude of the ON-current drops by 43% (violet line in Fig. 3) in comparison to the uniformly doped purely ballistic devices (smooth). More importantly, the standard deviation of the ON-current, for all fifty transistors, is extremely high (41%). This is beyond the variability level of tolerance for the present



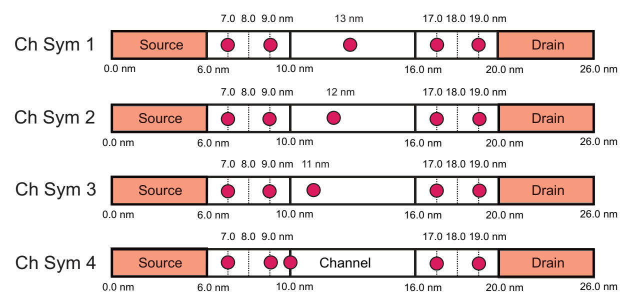


Fig. 4 3-D electrostatic potetnial and electron density for Ch Sym 1 device, the shematic view for Ch Sym 1, Ch Sym 2, Ch Sym 3 and Ch Sym 4 devices used in the paper.

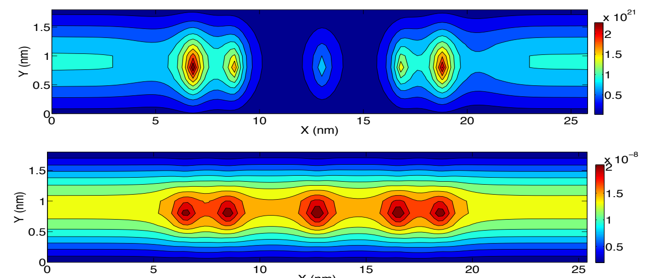


Fig. 5 Electron density (cm^{-3}) and J_X componet of the current (A) along the nanowire for the Ch Sym 1 configuration.

technology. In attempt to reduce the ON-current variability and to improve the transistor performance we created nanowire transistors with precisely placed discrete dopants in the S/D regions. The spatial distribution of the impurities is chosen to enhance the electron injection in the channel based on our previous work [35] and preliminary calculations.

We built our transistors with dopants positioned in the middle and aligned along the device – Ch, Ch Sym and Ch 3D, which are illustrated at the bottom of Fig. 1. Two of the devices presented in Fig. 1, Ch and Ch Sym, have four precisely placed dopants, which correspond closely to the average number of dopants in the access regions. The only difference between those two SNWTs is the position of two phosphorous atoms along the wire. From our previous work and the simulations presented earlier in this section, it is clear that the choice of the impurities can dramatically impact the ON-

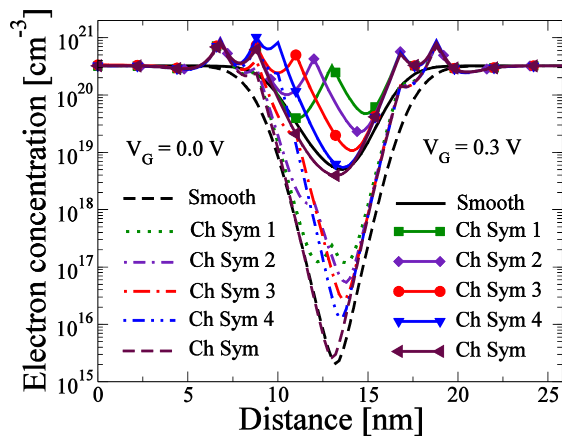


Fig. 6 Electron concentration, at two gate voltages, along the nanowire for all devices with a single channel dopant. The smooth device is also shown for comparison.

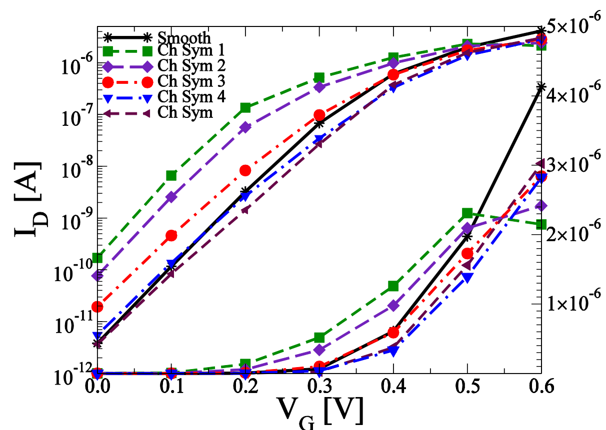


Fig. 8 I_D-V_G characteristics, on linear and logarithmic scales, for all calculated devices with a single channel dopant. The smooth device is also shown for comparison.

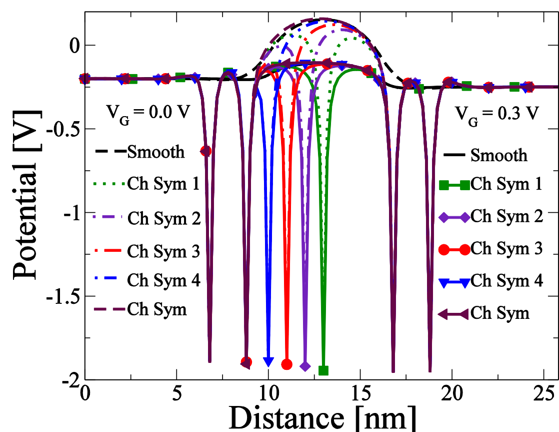


Fig. 7 Electron potential, at two different gate voltages, along the nanowire for all devices with a single channel dopant. The smooth device is also shown for comparison.

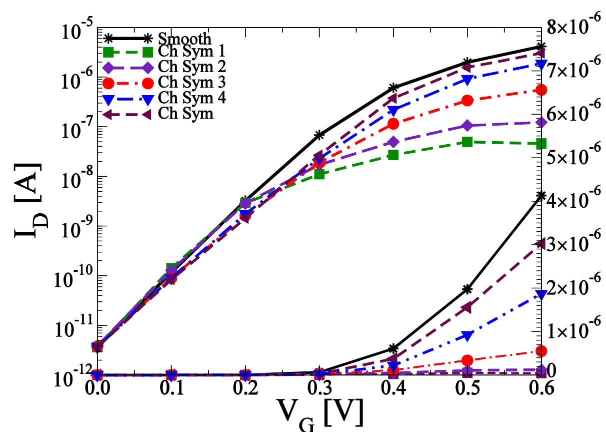


Fig. 9 Adjusted I_D-V_G characteristics to yield the same OFF-current, on linear and logarithmic scales, for all calculated devices.

current without affecting significantly the threshold voltage and the electrostatic integrity (subthreshold slope). For example, the symmetrically placed dopants, in the case of Ch Sym, result in high ON-current, which is above the average value obtained from the random dopant simulations. In the Ch Sym transistor, the ON-current is 71% of the maximum possible ballistic value (smooth device). Such a high level of ballisticity is unprecedented for devices with random dopants [38]. It is important to emphasise that in the case of random dopants the average ballisticity in this 6 nm channel length transistor is only 57%. Additionally, arranging the dopants asymmetrically in the S/D, Ch configuration, results in a dramatic reduction in the ON-current. In such a transistor the drive current has the lowest value among all transistors and the ballisticity coefficient drops to 33%.

Further improvement in the transistor performance can be achieved by increasing the number of precisely placed dopants in the access regions – Ch 3D. The 'highly doped structure' shows remarkably high level of balisticity, 81%. This is a 10% increase in the current if compared to the Ch Sym case.

However, the nanowire with the continuous doping still has high ON-current in comparison to all transistors with discrete dopants in the S/D. Again, in an attempt to improve even further the behaviour of the devices with discrete impurities we introduced a single phosphorous atom to the channel.

B. *Precisely placed single channel dopant*

There have been speculations that a single donor dopant in the channel can increase the ON-current by creating a 'sombrero' potential [35] and a resonant current path between the source and the drain. In this section, we investigate the effect of a single phosphorous atom in the channel region on the performance of the Si nanowire transistors. Four test devices are considered (Ch Sym 1, Ch Sym 2, Ch Sym 3 and Ch Sym 4) and they are schematically illustrated in Fig. 4. All four wires have symmetrically placed dopants in the S/D and one dopant in the channel. The obtained results are compared to the smooth and Ch Sym transistors. 3-D plots of the electrostatic potential and electron density for the Ch Sym 1 device are shown in Fig. 4 at V_G = 0.4V. Presence of an impurity in the middle of the wire, combined with the maximum of the cross-section wave function, enhances the electron concentration in the center of the transistor. The same is valid for the electrostatic potential which has a localized maximum in the middle of the wire and around the single phosphorous atoms.

The same conclusions can be obtained from Fig. 5 which shows the electron concentration and the current density in a

plane along the channel in the centre of the cross-section for the Ch Sym 1 configuration at V_G = 0.3V. Electron density profile reveals that the impurties, in the access regions (closer to the channel) are partially depleted by the gate potential. The J_X component of the current increases around the position of the discrete phosphorous atoms as if a funnel was created by the impurity potential. This derives from an increase in electron concentration in the middle of the wire.

More elaborate information about the electron density and the potential evolution along the channel at two different gate biases is shown in Fig. 6 and Fig. 7. The depletion of the electron density in the dopants close to the channel, presented in Fig. 5, is clearly visible in the 2-D plot in Fig. 6. The electron concentration at the vicinity of the same impurities and the channel dopant increases with increasing of the gate potential. This is determined by the 'sombrero' potential, which is a combination of the Coulomb potential of the ionized dopant and the potential associated with the electron screening charge (Fig. 7). The potential has a double barrier shape that is specific for quasi-bound states similar to those that appear in the resonant tunneling structure. Opposite to the electron density profile along the wire, at low gate bias (V_G = 0.0V), the potential barrier between the source and the channel is high because the gate potential keeps the electrons away from the channel. As a result, the electrons from the source cannot overcome the potential barrier or tunnel through and this results in a significantly lower electron concentration in the channel in comparison to the S/D contacts. At higher gate voltages (V_G = 0.3 V), the potential barrier between the contacts and the channel region decreases and, as a consequence, the electrons can travel above and tunnel through the potential barrier more easily. This results in an increase of the current at higher gate voltages in general.

The current-voltage characteristics of the simulated structures with a channel dopant, for the smooth and for Ch Sym, transistors are presented in Fig. 8. Fig. 9 shows the same I_D-V_G curves as Fig. 8 but adjusted to deliver the same OFF-current for all devices at V_G = 0.0 V. An analysis of Fig. 8 and Fig. 9 shows two important effects of the additional channel dopant over the device performance.

Firstly, there is a threshold voltage reduction associated with the lowering of the potential barrier between the source and the drain by the dopant atom. The effect is more dramatic when the dopant is placed at the maximum of the barrier (Ch Sym 1) and almost negligible when the dopant is close to the source extension (Ch Sym 4).

Secondly, the channel dopant increases the Coulomb scattering in the channel region, reducing the ON-current. For example, Fig. 9 shows clearly that for the same leakage current the drive current drops from around 25% in the Ch Sym case to a staggering almost 200% in the Ch Sym 1 structure if compared to the smooth case. A detailed explanation of this behaviour is based on an analysis of the corresponding transmission coefficients as a function of the energy. Fig. 10 shows the transmission spectra for Smooth, Ch Sym, and the two most extreme cases - Ch Sym 1 and Ch Sym 4 transistors at high and low gate voltages. At V_G=0.0V, the

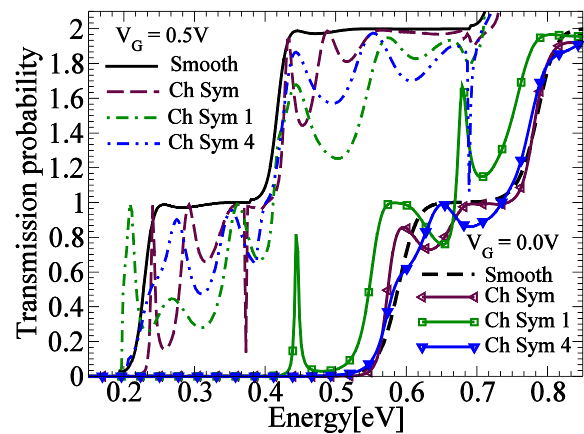


Fig. 10 Transmission probability at V_G = 0.0 V and V_G = 0.5 V for Smooth, Ch Sym, Ch Sym 1and Ch Sym 4 devices.

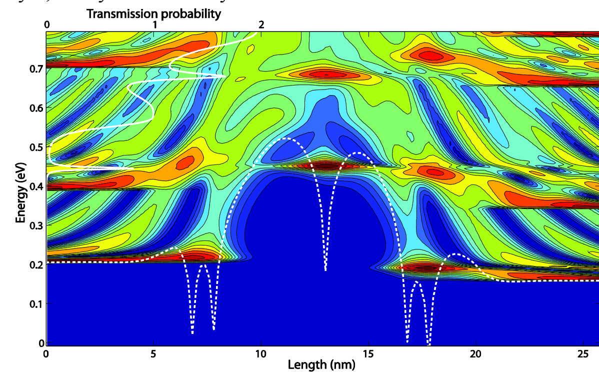


Fig. 11 The transmission probability (solid white line) and density of states along the wire for the Ch Sym 1 case for a gate voltages V_G = 0.0 V. The horizontal dashed white line is the electrostatic potential and it has been aligned to the first subband energy at the source.

discrete dopants lead to resonates peaks which are very well pronounced in the Ch Sym 1 device – peaks around 0.45 and 0.7 eV. The transmissions spectra for the transistor rise first and, hence, the devices has the highest leakage current at low gate biases. At V_G=0.5V, the curves are more jagged and translated to higher energies, due to increasing of scattering inside of the channel. For all transistors with discrete dopants the shape of the self-consistent potential around the impurities produces so called Fano-type resonances, which appear as asymmetric dips and peaks in the transmission [39]. The width, position and the number, of the resonant peaks and antiresonant dips depends of the position of the impurity in the SNWT. Note that the transmission for the smooth device has a stair-type characteristic as expected. Therefore, the irregular shape and peaks/dips in the transmission for the devices with discrete impurities can be interpreted as a fraction of carriers being reflected back. This feature is not visible at lower gate bias because of the dominant reflection of the carriers by the channel barrier potential [40], [41].

The resonances are clearly shown in the distribution of density of state (DOS) along the channel as presented in Fig. 12 for the Ch Sym 1 case. The electrostatic potential along the channel is plotted in a white dashed line, which is aligned to the first sub-band energy at the source. This gives an opportunity to compare the position of the quasi-bound states relative to the inverted sombrero shape of the potential. The

DOS is higher around the discrete dopants and the transmission function (plotted on the left-hand side of Fig. 12 with white solid line) has peaks where are the channel dopant energy levels.

IV. Conclusions

We have performed quantum transport simulations of the impact of discrete phosphorous atoms on the operation of an all-gate-around silicon nanowire transistor (SNWT) in order to assess its potential application in digital circuits and systems. The impact of the specific spatial configuration and of the number of discrete dopants in the transistor has been investigated in detail. The transistors that include only S/D dopants show almost negligible difference in the subthreshold slope and the threshold voltage. On a contrary, we have observed a general decrease and large variations in the drive current associated with the position of the discrete dopants due to backscattering.

Additionally, introducing an individual phosphorous atom in the channel region of the transistor leads to an even stronger deterioration in the performance of nanowire transistors in comparison to the undoped channel wires, such as Ch Sym. The ON-current that is critical for the circuit performance is worse for all discrete dopant transistors considered in our study in comparison to the uniform doped devices. Presence of backscattering and resonances, including very localized zero-transmission resonances deriving from unscreened Coulomb wells, is a common trend in the transmission functions. Furthermore, despite the lower threshold voltage, which results in a high gate voltage overdrive, all transistors with a single dopant in the channel, have lower ON-current at the anticipated supply voltage of 0.6V. These results provide guidance to the development of the next generation components with sub 10 nm dimensions for the semiconductor industry.

References

[1] D. J. Frank, *et al*., "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE,* vol. 89, pp. 259-288, 2001.

[2] J. J. Morton, D. R. McCamey, M. A. Eriksson, S. A. Lyon, "Embracing the quantum limit in silicon computing," *Nature,* vol. 479, pp. 345-353, 2011.

[3] P. M. Koenraad, M.E. Flatte,"Single dopant is semiconductors," *Nature Mater*., vol .10, pp. 91-100, 2011.

[4] International Technology Roadmap of Semiconductors (ITCM). (Online). Available: http://public.itrs.net.

[5] S. Roy, A. Asenov, "Where do the dopants go?," *Science,* vol. 309, pp. 388-390, 2005.

[6] T. Shinada, S. Okamato, T. Kobayashi, I. Ohdomari, "Enhancing semiconductor device performance using ordered dopant arrays," *Nature,* vol. 437, pp.1128-1131, 2005.

[7] M. Pierre, *et al.,* "Single-donor ionization energies in a nanoscale CMOS channel," *Nature Nanotech.,* vol. 5, pp. 133-137, 2010.

[8] K. Y. Tan, *et al.,* "Transport spectroscopy of single phosphorous donors in a silicon nanoscale transistor," *Nano Lett.,* vol. 10, pp. 11-15, 2010.

[9] M. Fuechsle, *et al.,* "A single-atom transistor," *Nature Nanotech.,* vol. 7, pp. 242-246, 2012.

[10] N. Singh, *et al.,*"High-performance full depleted silicon nanowire (diameter ≤ 5nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.,* vol. 27, pp. 383-386, 2006.

[11] G. P. Lansbergen, *et al*., "Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET," *Nature Phys.,* vol. 4, pp. 656-661, 2008.

[12] B. C. Johnson, *et al.,* "Drain current modulation in a nanoscale field-effect-transistor channel by single dopant implantation," *Appl. Phys. Lett.,* vol. 96, pp. 264102, 2010.

[13] H. Sellier, G. P. Lansbergen, J. Caro, S. Rogge," Transport spectroscopy of a single dopant in a gated silicon nanowire," *Phys. Rev.Lett., vol* 97, pp. 206805, 2006.

[14] T. Shinada, T. Kurosawa, H. Nakayama, Y. Zhu, M. Hori, H. Ohdomari, "A reliable method for the counting and control of single ions for single-dopant controlled devices," *Nanotechnology,* vol. 19, pp. 345202, 2008.

[15] Y. Ono, *et al., "*Conductance modulation by individual acceptors in Si nanoscale field-effect transistors," *Appl. Phys. Lett.,* vol. 90, pp. 102106, 2007.

[16] N. Singh, *et al.,* "Ultra-narrow silicon nanowire gate-all-around CMOSdevices: Impact of diameter, channel-orientation and low temperature on device performance," in *IEDM Tech. Dig.,* pp 547-505, 2006.

[17] K. H. Cho, *et al.,* "Experimental evidence of ballistic transport in cylindrical all-gate-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.,* vol. 92, no. 5, pp. 052 102-1 – 052 102-3, 2008.

[18] A. Martinez, *et al.,* "A self-consistent 3D-full real space NEGF simulator for studying nonpertubative effect in nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2213-2222, 2007.

[19] M. Luiser, A. Shenk, and W. Fichter, "Three-dimensional full-band simulations of Si nanowire transistors," in *Proc. Int. Electron Devices Meetng Tech. Dig,* pp. 811-814*,* 2006.

[20] A.Svizhenko and M. P. Anantram, "The role of scattering in Nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp.1559-1466, 2003.

[21] S. Jim, Y.-J. Park, and H. S. Min, "A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interaction," *J. Appl. Phys.,* vol. 99, pp. 123719-1 – 123719-10, 2006.

[22] M. Aldegunde, A. Martinez, and A. Asenov, "Non-equilibrium Green's function analysis of cross section and channel length dependence of phonon scattering and its impact of the performance of Si nanowire field effect transistor," *J. Appl. Phys.,* vol. 110, pp. 094518, 2011.

[23] J. Schwinger, "Brown motion of a quantum oscillator," *J. Math. Phys.,* vol. 2, pp. 407-432, 1961.

[24] L. V. Keldysh, "Diagram technique for non-equilibrium processes," *Sov. Phys. –JEPT*, vol. 20, pp. 1018-1026, 1965.

[25] G. D. Mahan, "Quantum transport equations for electric and magnetic fields," *Phys. Rep.*, vol. 145, pp. 251-318, 1987.

[26] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Liebert, "One-dimensional hole gas in germanium/silicon nanowire herterostructures," *Proc. Nat. Acad. Sci. U.S.A.*, vol. 102, pp.10 046 – 10 051, 2005.

[27] K. H. Cho, "Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field effect transistor,"*Appl. Phys. Lett.,* vol. 92, no. 5, pp. 052 102, 2008

[28] http://www.goldstandardsimulations.com/products/garand/

[29] R. Landauer, "Electrical resistance of disordered one-dimensional lattices," *Philos. Mag.,* vol. 21, pp. 863-867, 1970.

[30] M. Buttiker, "Symmetry of electrical conduction," *IBM J. Res. Dev.,* vol. 32, pp. 317-334, 1981.

[31] H. L. Engquist and P. W. Anderson, "Definition and measurements of the electrical and thermal resistances," *Phys. Rev. B.,* vol. 24, pp. 1151-1154, 1981.

[32] Y. Imry and R. Landauer, "Conductance viewed as transmission," *Rev. Mod. Phys*., vol. 71, pp. 306-312, 1999.

[33] A. Svizhenko, M. P. Anatram, T. R. Govindan, B. Biegel, and R. Venugopal, “Two dimensional quantum mechanical modelling of nanotransistors,” *J. Appl. Phys.*, vol. 91, pp. 2343-2354, 2002.
[34] R. Venugopal, Z. Ren, S. Datta, D. Jovanovic and M. S. Lundstrom, “Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches.,” *J. Appl. Phys.,* vol. 92, pp. 3730-3739, 2002.
[35] A. Martinez, *et al.*, “3-D nonequilibrium Green’s function simulation of nonperturbative scattering from discrete dopants in the source and drain of a silicon nanowire transistor,” *IEEE Trans. Nanotechnol.,* vol. 8, pp. 603-610, 2009.
[36] N. Seoane, *et al. ,*“Current variability is Si nanowire MOSFETs due to random dopants in the source/drain region: A full 3D NEGF study,” *IEEE Electron Devices, vol.* 56, no. 7, pp. 603-610, 2009.
[37] A. Martinez, *et al.*, “Quantum transport study on the impact of channel length and cross section on variability induced by random discrete dopants in narrow GAA Si nanowire transistor,” *IEEE Electron Devices, vol.* 58, no. 8, pp. 2209-2217, 2011.
[38] V. Barral, *et al.*, “Experimental investigation on the quasi-ballistic transport: Part II – Backscattering coefficient extraction and link with the mobility,” *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 420-430, 2009.
[39] M. P. Persson, et al., “Charged impurity scattering and mobility in gated silicon nanowires”, *Phys. Rev. B.*, vol. 82, pp. 115318, 2010.
[40] M. Bescond, M. Lannoo, L. Raymond, F. Michelini, “Single donor induced negative differential resistance in silicon n-type nanowire metal-oxide-semiconductor transistrors,” *J. Appl. Phys*., vol. 107, pp. 093703, 2010.
[41] Bescond, M. Lannoo, F. Michelini, L. Raymond, M. G. Pala, “3D real-space quantum transport simulation of nanowire MOS transistors: Infuence of the ionized doping impurity,” *Microelectron. J*., vol. 40, pp. 756, 2009.

Vihar P. Georgiev received the BSc in Chemistry, MSc in Computational Chemistry from Sofia University, Sofia, Bulgaria, in 2004 and 2006 correspondingly and a Ph.D. degree from University of Oxford, Oxford, UK in 2011. He is currently a member of the Device Modelling Group, Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow, UK .

Ewan Towie received the BEng in Electronics and Software Engineering, and a PhD degree from University of Glasgow, Glasgow, UK in 2004 and 2009 correspondingly. He is currently a member of the Device Modelling Group, School of Engineering, University of Glasgow, Glasgow, UK

Asen Asenov (M’96–SM’05–F’11) received the M.Sc. degree in solid-state physics from Sofia University, Sofia, Bulgaria, in 1979 and the Ph.D. degree in physics from the Bulgarian Academy of Sciences, Sofia, Bulgaria, in 1989.
He is currently with the University of Glasgow, Glasgow, UK. He is also a Cofounder, CEO, and Director of Gold Standard Simulations Ltd.