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Yearlong 500 °C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits

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Abstract

This work describes recent progress in the design, processing, and testing of significantly up-scaled 500 °C durable 4H-SiC junction field effect transistor (JFET) integrated circuit (IC) technology with two-level interconnect undergoing development at NASA Glenn Research Center. For the first time, stable electrical operation of semiconductor ICs for over one year at 500 °C in air atmosphere is reported. These groundbreaking durability results were attained on two-level interconnect JFET demonstration ICs with 175 or more transistors on each chip. This corresponds to a more than 7-fold increase in 500 °C-durable circuit complexity from the 24 transistor ring oscillator ICs reported at HiTEC 2016 [1]. These results advance the technology foundation for realizing long-term durable 500 °C ICs with increased functional capability for combustion engine sensing and control, planetary exploration, deep-well drilling monitoring, and other harsh-environment applications.

Keywords: SiC, JFET, Integrated Circuit

I. Introduction

Significant improvements to aerospace, automotive, energy production, and other industrial systems are expected from extension of the operating temperature envelope of transistor integrated circuits (ICs) well above the effective 300 °C limit of silicon-on-insulator technology [2,3]. Wide bandgap semiconductors have enabled T ≥ 500 °C IC demonstrations [1,4-17]. However, most envisioned applications require stable IC operation over time periods exceeding one thousand hours at extreme temperature in addition to circuitry complex enough to perform desired electronic functions in the harsh environment.

To date, work demonstrating over 1000 hours of stable IC operation at T ≥ 500 °C has only been reported using high-temperature packaged ICs comprised of interconnected SiC n-channel junction field effect transistors (JFETs) and resistors [1,11-17]. Likewise, 4H-SiC JFET IC's are the only electronics that have demonstrated prolonged operation unprotected from the 460 °C, 9.4 MPa super-critical CO_2 Venus surface environment [18]. Prior to the fabrication and testing of the ICs described in this HiTEC 2018 paper and [17] (an earlier and far less-comprehensive preliminary report), the most complicated semiconductor IC chip to function for more than 1000 hours at 500 °C was a 24-transistor ring oscillator IC that we reported on at HiTEC 2016 [1]. This paper reports the detailed design, fabrication and year-long 500 °C operational testing of significantly (> 7-fold) more complicated 4H-SiC JFET IC chips. In particular, the demonstrated year-long 500 °C operational durability of these more complex ICs has exceeded the 258 day longest observed 500 °C operating time from the previous (simpler) generation of ICs. Furthermore, excellent output signal stability during this year-long 500 °C testing has also been demonstrated. These results therefore represent an important advancement to the technology foundation for realizing 500 °C durable ICs for combustion engine sensing and control, planetary exploration, deep-well drilling monitoring, and other harsh-environment applications.

II. Experimental

A. Circuit Design

A variety of basic digital logic and analog amplifier demonstration circuits were prototyped alongside the increased complexity ICs that are focus of this report. The basic logic gate approach, based on integrated normally-on n-channel 4H-SiC JFETs and resistors powered by $+V_{DD}$ (around +25 V), GND, and $-V_{SS}$ (around -25 V) supplies, has been previously described [12,13,19]. In this approach, the logic high V_H is around 0 V, while logic low V_L is approximately -10 V, largely dictated by the negative threshold voltage of the normally-on JFET. Fundamental logic functions (NOT, NAND, NOR etc.) are synthesized in an inverting amplifier stage that feeds positive voltages to a level-shift stage that translates the output back to the negative voltage needed to drive subsequent logic gates of the same type. More complex logic can also be combined in the inverting amplifier stage as illustrated by the combination logic function gate schematic of Figure 1. This approach has experimentally demonstrated successful logic functionality from 25 °C to more than 800 °C without any changes to power supply and input signal voltages [20].

Two digital logic technology demonstrator ICs, each with more than 100 transistors per chip, were implemented based upon this core logic gate approach. The first demonstrator IC was a 195-transistor 16-bit random access memory (RAM) configured in a 4x4 array of 6-transistor memory cells with supporting address/read/write drive/sense circuitry. Figure 2 illustrates the overall circuit architecture including 4x4 array of 16 RAM cells (center), address decoder (left) driving row/word access lines, column bit line pairs with write drive (top) and read sense amplifiers and output buffer gates (bottom). Data IN lines D0-D3 IN are used to input data for memory write operations, while read memory contents are output via Data OUT lines D0-D3 OUT lines.

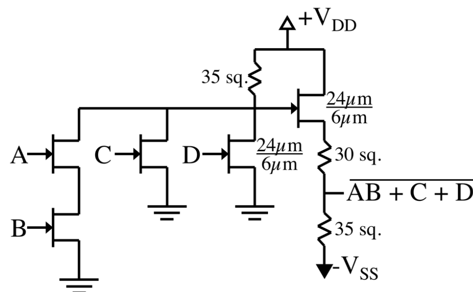

Figure 1. Schematic diagram of 500 °C durable SiC JFET combination logic gate.

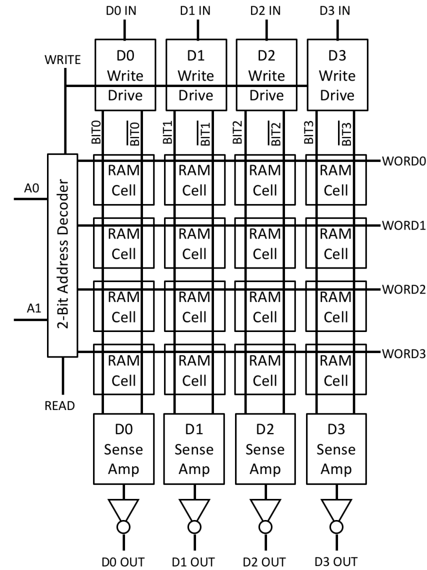

Figure 2. Circuit architecture of the prototyped 500 °C durable SiC JFET RAM chip.

Figure 3 shows the schematic diagram of the 6-transistor RAM cell. At first glance the RAM cell follows the traditional RAM cell configuration of a central latch of cross-coupled NOT gates connected to the bit line pair though access transistors. However, in order to achieve isolation of the cell from the bit lines using access transistors that are normally on (i.e., conducting current at gate to source bias V_{GS} = 0 V), the column bit lines must be operated at positively shifted logic voltages compared to the NOT gate logic voltages. Therefore, the access transistors connect to the NOT gate inverting amplifier stage outputs (that are positive voltages), and the bit lines are also operated at positive voltages. This biasing scheme enables the access JFETs to sufficiently isolate the

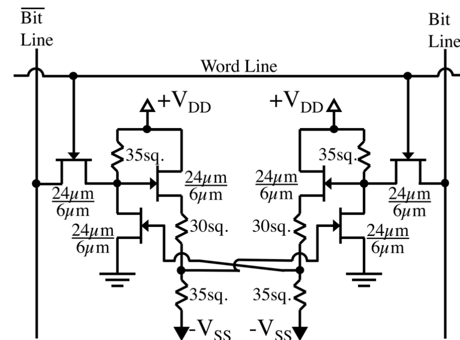

Figure 3. Schematic diagram of the prototyped 500 °C durable SiC JFET RAM cell. The bit lines are operated at positively shifted voltages and coupled to inverting amplifier nodes to enable normally-on JFETs to function as memory cell access transistors.

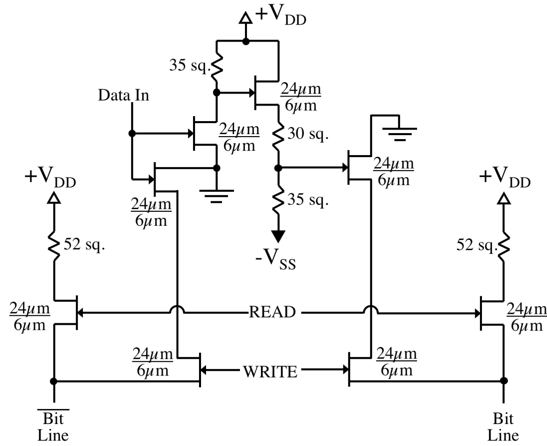

Figure 4. Bit line write driver circuit employed in the prototyped 500 °C durable RAM chip.

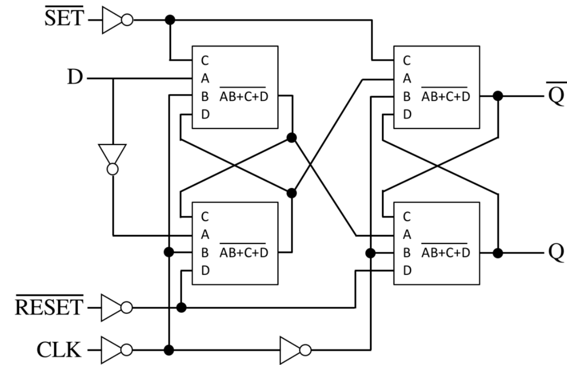

Figure 5. Circuit schematic of 500 °C durable SiC JFET D-type flip flop. See Figure 1 for the schematic detail of the 4 combined-function logic blocks.

latch from the bit lines when the word line is low (around -10 V), yet sufficiently connect to bit lines for reading and writing the cell when the word line is high (around 0 V).

Figure 4 shows the bit line pair write drive circuit. During read operations (i.e., when READ is high and WRITE is low), the pass transistors gated by the READ signal enable equal positive pull-up voltages on both bit lines of the pair prior, which the contents of the addressed memory cell pull off of equipotential for the sense amplifiers detect. The output sense amplifier consists of a fully differential amplifier and level shifters. The sense amplifier circuit has identical topology, but with slightly different component ratios, as shown in Figure 7 of [1]. The output signal of the differential sense amplifier is buffered through an "MF" design NOT gate (detailed in [14]) to the data output bond pad. During write operations (i.e., WRITE is high and READ is low) the Fig. 4 circuit drives bit lines to different (positively shifted) voltages to impose data onto an addressed memory cell.

The second demonstration IC is a 175-transistor clock signal generator with electronically selectable frequency divide by 2 or 4 output (÷2/÷4 Clock). The master (base) clock on this chip is a 21-stage ring oscillator of "LF" design NOT gates (detailed in [14]), the oscillation frequency of which exhibits strong temperature dependence (~ 4X decrease from 25 °C to 500 °C [13]). The frequency division of this base clock signal is carried out using D-type flip flops with some signal propagation control logic gates. Figure 5 details the schematic for the 500 °C durable SiC JFET D-type flip flop sub-circuit. When SELECT chip input signal is low (~ -10 V), the chip outputs ½ the base clock frequency. When SELECT input signal is high (~ 0 V), the chip outputs ¼ the base clock frequency. The chip has output pads for both the base clock signal and the selectable frequency divided clock signal.

B. IC Fabrication

The overriding design criteria of the NASA Glenn SiC JFET IC process is attainment of durable and stable extreme-environment electrical IC operation. Figure 6 illustrates the cross-section of the 4H-SiC devices that were fabricated towards this end under the wafer designation "IC Version 10.1". The

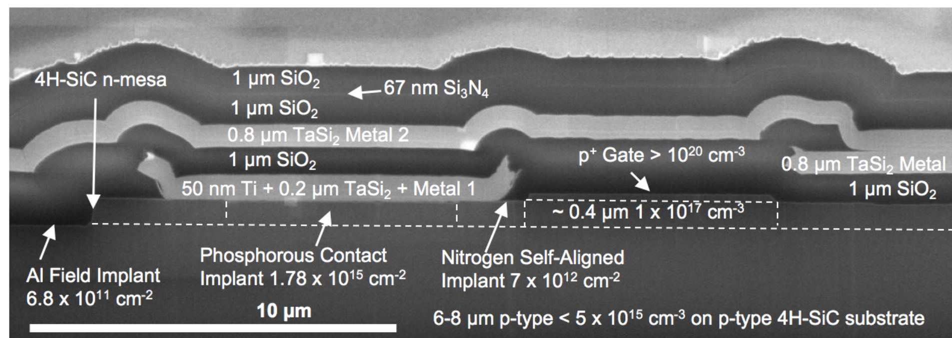

Figure 6. Scanning electron micrograph cross-section of source and gate region of an as-fabricated 500 °C durable 4H-SiC JFET with two levels of interconnect.

process used patterned mesa etching and ion implantations to implement 4H-SiC SiC n-channel JFETs (with p^+ doped epilayer gates) and resistors with 6 μm lateral minimum feature size [14]. The "self-aligned" (SA) nitrogen implant reduces parasitic source/drain spacing resistance, while the Al field implant between devices inhibits parasitic inversion channel n-MOSFETs from forming electrical leakage paths beneath interconnect traces over field regions. The heavily-doped phosphorous contact implant promotes ohmic source/drain contact formation. Following the patterned mesa etches and ion implantations, the wafer was capped with 1 μm of SiO_2 deposited at 720 °C by low-pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) precursor before an activation anneal at 1360 °C in N_2 for 100 hours. The activation cap was then stripped and two short sacrificial thermal oxidations of the wafer were performed and stripped with 6:1 buffered oxide etchant (BOE) to condition the wafer surface for device-quality oxide formation.

A third thermal oxide was grown 30 nm thick [21] and then coated with 1 μm TEOS LPCVD SiO_2 for the first dielectric layer. Photoresist-patterned vias through the first dielectric layer were dry etched through most of the 1 μm SiO_2 and then finished with a brief wet etch (6:1 BOE, with ultrasonic agitation) in order to achieve desired via aspect ratio with sloped sidewall and pristine SiC surface for contact deposition. The sample was loaded immediately following post-BOE DI H_2O rinse and N_2 blow dry for pump down and sputter deposition of around 50 nm titanium contact metal capped with roughly 0.2 μm of $TaSi_2$ deposited without substrate heating at target-to-substrate distance of ~ 51 mm in a custom multiple-gun sputter deposition system. The photoresist mask that defined both the via etch and the metal contact area was then stripped using acetone and dry O_2 plasma leaving behind a liftoff-patterned Ti/$TaSi_2$ contact metal plug. The contact plugs were then over-coated by 1 μm thick $TaSi_2$ "Metal 1" layer (Figure 6). Both Metal 1 and Metal 2 $TaSi_2$ interconnect layers were blanket sputter deposited following a 1 hour 300 °C bake-out followed by ~ 1-hour cooldown to approximately 100 °C substrate temperature with the custom sputter deposition system at a target to substrate spacing of 21 mm in order to minimize void formation over topologic features. Dry etching using photoresist masks formed the interconnect patterns. A 1 μm thick TEOS LPCVD SiO_2 layer resides between the Metal 1 and Metal 2 interconnects.

The wafer was passivated by top layers of 1 μm TEOS LPCVD SiO_2, 67 nm stoichiometric Si_3N_4, and 1 μm TEOS LPCVD SiO_2. Photoresist-patterned dry and wet etching was used to strip all dielectric layers from bond pad regions. Multi-layer bond pads of $TaSi_2$/Pt/Ir/Pt were deposited (onto exposed SiC in bond pad regions) [22] and patterned via dry etching defined with photoresist masking. Likewise, dielectric layers were stripped from the wafer backside and the same $TaSi_2$/Pt/Ir/Pt layers deposited there to form electrical contact to the entire wafer backside. Bond pads were then capped by liftoff-patterned 1 μm thick electron-beam deposited Au film. The same (1 μm thick Au but without patterning) film was deposited on the backside and the process concluded with a 10 hour anneal in 96% N_2:4%H_2 forming gas at 500 °C.

Figure 7 shows annotated optical images of the as-fabricated chips after dicing, prior to high temperature packaging. The three largest metal traces running vertically through the middle of the chips are the main $+V_{DD}$, GND, and $-V_{SS}$ power supply busses. The locations of key sub-circuits on these chips are denoted by annotations on the images. The inactive D flip-flop on the clock chip was intended to provide different circuit functionality, but a layout error excluded this feature from being realized.

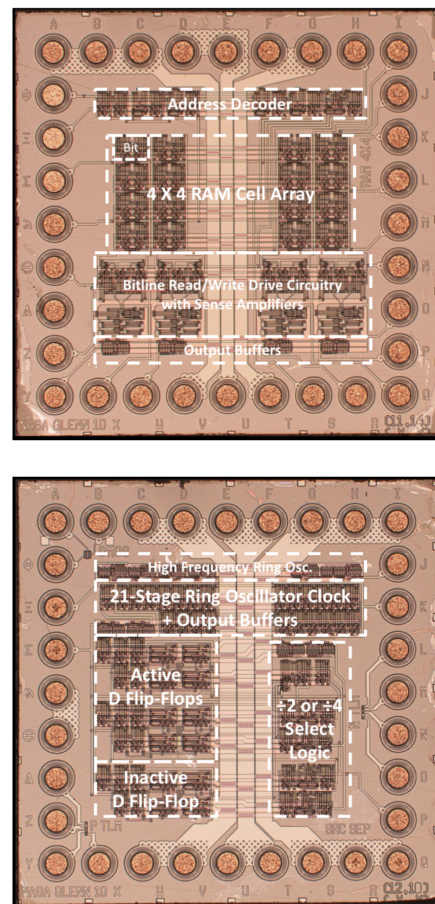

Figure 7. Annotated optical images of 3mm x 3mm 500 °C durable demonstration ICs prior to packaging. Top: RAM IC with 195 4H-SiC JFETs. Bottom: Clock IC with 175 4H-SiC JFETs. After [17] © Trans Tech Publications Ltd.

III. Results and Discussion

A. Room Temperature Wafer Probing

All devices and circuits were probe-tested on-wafer at 25 °C prior to dicing and packaging. Due to epilayer non-uniformity, JFET threshold voltage (V_T) varied as a function of radial distance ***r*** from the 76 mm diameter wafer center (from -7.9 V at wafer center to -13.8 V at wafer edge for substrate bias V_S = -15 V). Within experimental error, the V_T behavior of this "IC Version 10.1" wafer quantitatively matched the radial position V_T dependence plotted for "Wafer 9.1" in Reference [23] that was produced during the same commercially purchased multi-wafer epilayer growth run. For wafer regions where V_T fell within circuit-design limits (***r*** < 25 mm), wafer probe yields for all circuits exceeded 70% [17].

B. Prolonged 500 °C Electrical Testing

Seven 3 mm x 3 mm SiC IC chips (two RAM chips and 5 clock chips) from radial wafer positions between 6.7 mm ≤ ***r*** ≤ 24.2 mm were bonded into custom 32-input/output (I/O) high temperature co-fired ceramic composite (HTCC) packages [25] and wired for prolonged operational 500 °C testing in room-air ovens. The oven testing setup is not practically suited for low noise or high frequency AC measurements due to large wiring/cabling capacitances and substantial electromagnetic coupling of oven heating element power to unshielded gold wires inside the oven [12]. All waveforms were measured using a digitizing oscilloscope with 10 MΩ passive probes connected to the chip package via setup with varying cabling lengths up to a couple of meters and unshielded oven wiring. Therefore, all recorded waveforms are impacted to varying degrees by non-trivial resistive-capacitive loading effects. Oven heating/cooling ramp rates were restricted to ≤ 3 °C/minute, and testing started on different dates for each chip/oven.

Table I summarizes the prolonged 500 °C room-air oven testing results to date. RAM #1 chip was tested as a 12-bit memory due to damage/failure of one row/word line that occurred between on-wafer probing and conclusion of high temperature packaging. The RAM #1 chip test was suspended after 1525 hours of 500 °C operation to facilitate use of the same oven and instrumentation to start RAM #2 chip 500 °C testing. Clock chips 3A, 3B, and 3C were packaged "multi-chip" into the same 32-I/O high temperature package. Data from a 20-hour thermal cycle to room temperature due to an accidental laboratory power outage is excluded, but otherwise the 500 °C testing has been continuous. As shown in Table I, testing of RAM #2 and three of the five ÷2/÷4 clock chips is continuing approaching or beyond 10,000 hours at 500 °C as of this writing.

Table I. 500 °C JFET IC Test Summary

Packaged IC Sample	***r*** (mm)	500 °C Time	Test Status
RAM #1	13.4	1525 h	Suspended
RAM #2	6.7	10100 h	Running
Clock #1	24.2	470 h	Failed
Clock #2	15.3	10500 h	Running
Clock #3A	12.4	9677 h	Running
Clock #3B	12.4	9677 h	Running
Clock #3C	13.4	2090 h	Failed

1) Prolonged 500 °C RAM Chip Test Results

Figures 8 and 9 plot RAM #2 measured waveforms recorded at 10,100 hours (421 days) of 500 °C chip testing under continuous operational electrical bias. During the first 100 hours of 500 °C operational burn-in, input voltages were adjusted some and finalized to V_{DD} = +25V and V_{SS} = -25 V for the power supplies and V_{INL} = -9 V and V_{INH} = -1 V for data input and control signals. The Figure 8 500 °C measured waveforms demonstrate successful writing, storage, and reading of a data test sequence as follows: A pattern of all 0's is written to the array in ascending address order, then successfully read back in ascending address order. A pattern of all 1's is likewise written and successfully read back. Finally, a more complicated pattern of 1's and 0's is stored in the array, then read back twice, once in ascending address order and then a second time in descending (reversed) address order. Note that data out traces D0-D3 only provide valid 0 or 1 output data signal voltages when READ is asserted high.

The Figure 9 500 °C measured waveforms plot internal RAM chip diagnostic voltages (i.e., signals that would not be used in an actual memory application) resulting from the same input test pattern. Word line waveforms output by the address decoder circuitry WORD0 – WORD3 are shown along with BIT3 and BITBAR3 bit line voltages waveforms for data column 3 (the only column that was connected for direct measurement to chip output pads). The BIT3 and BITBAR3 traces show the measured positive voltages on the bit lines for reading and writing of 1's and 0's consistent with Section II.A design discussion. Write operations are accomplished with around 6 V measured potential difference imposed between the bit lines by the write driver circuit of Figure 4, while reads are successfully captured by the sense amplifiers with less than 4 V potential difference imposed between the bit line pair by the addressed memory cell.

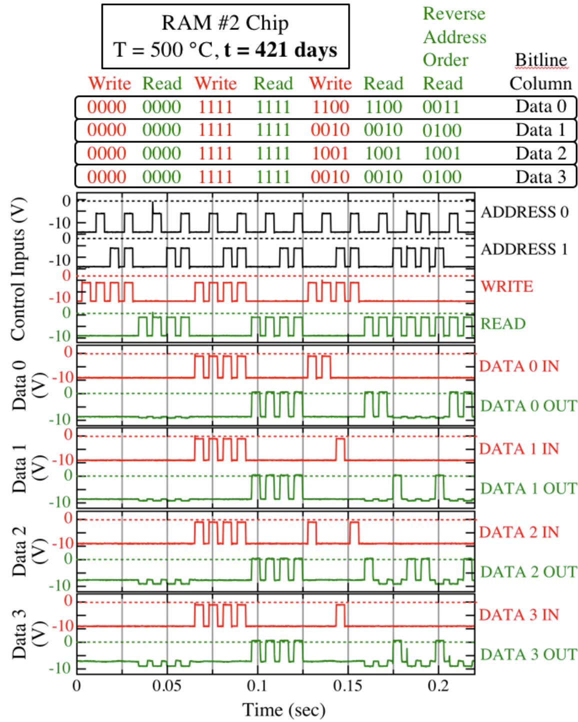

Figure 8. RAM Chip #2 input/output waveforms recorded at 421 days of 500 °C testing.

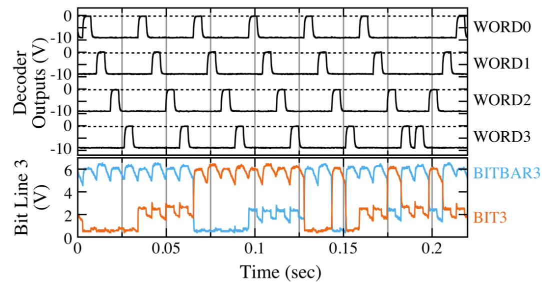

Figure 9. RAM Chip #2 internal (diagnostic) voltage waveforms recorded from the 500 °C test shown in Figure 8. The positive voltages of bit line (column) 3 operation are evident in the lower graph, with correspondence to Data 3 traces shown in the bottom-most graph of Figure 8.

Figure 10 plots the measured RAM chip output signal voltages (for D0-D3 outputs) as a function of 500 °C testing time. Following the initial burn-in period, all measured output signal voltages exhibit negligible change. *Report of such prolonged 500 °C operational durability and stability is unprecedented for any integrated circuit chip implemented in any semiconductor*. The power consumption of the entire RAM chip under these 500 °C test conditions was 194 mW. 116 mW (4.64 mA) was drawn from the V_{DD} supply while 78 mW (3.10 mA) came from the V_{SS} supply.

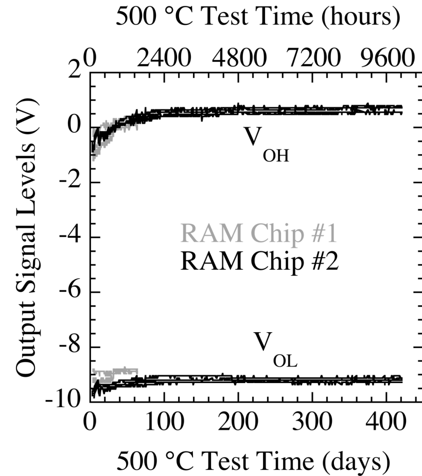

Figure 10. SiC JFET RAM IC output high (V_{OH}) and output low (V_{OL}) signal voltage levels (D0-D3 outputs) measured as a function of 500 °C test time.

2) Prolonged 500 °C ÷2/÷4 Clock Chip Test Results

Unprecedented 500 °C operational durability and stability was also measured for three of the five oven-tested ÷2/÷4 clock chips. Figure 11 plots ÷2/÷4 Clock #2 chip output waveforms recorded at 437.5 days of 500 °C testing. The circuit functionality described in Section II.A is realized in that the chip outputs ½ the base clock frequency when SELECT input signal is low (~ -10 V), whereas ¼ the base clock frequency is output when the SELECT input signal is high (~ 0 V). It is important to note that the waveforms are non-square to varying degree due to capacitive-resistive loading effects arising from the combination of the setup cabling, oven wiring and oscilloscope probes. As expected, the lower-frequency ÷4 measured waveform more closely approximates square-wave output shape than the higher-frequency ÷2 and base clock output signals.

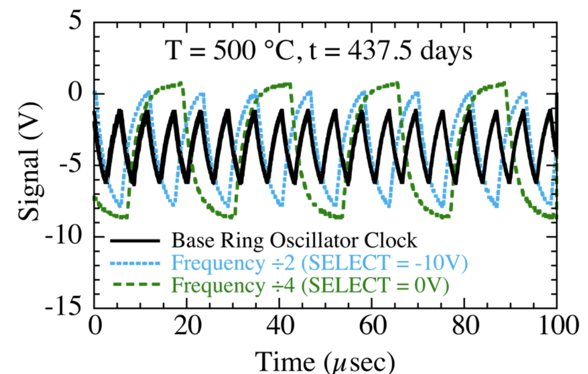

Figure 11. SiC JFET ÷2/÷4 Clock #2 IC waveforms recorded at 437.5 days of 500 °C testing.

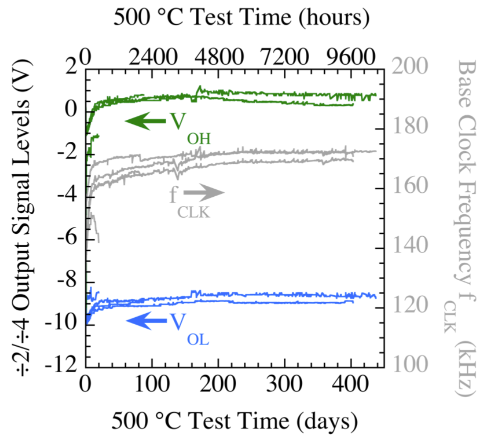

Figure 12. SiC JFET Clock IC ÷4 output low (V_{OL}) and high (V_{OH}) signal voltage levels and base clock frequency (f_{CLK}) measured as a function of 500 °C test time. Data from all clock chips tested (listed in Table I) is plotted.

Figure 12 plots the measured base clock frequency (f_{CLK}) and output low (V_{OL}) and high (V_{OH}) signal voltage levels of the ÷4 output signal as a function of 500 °C testing time for all the ÷2/÷4 clock chips that were oven-tested (Table I). Similar to the behavior of simpler ICs in our prior reports [1,15], the clock chip output values stabilize after ~100-200 hours of operation at 500 °C. After the initial burn-in, measured clock output parameters change less than 5% for the remainder of 500 °C testing prior to circuit failure. The measured 500 °C average power consumption of Clock #2 chip is 298 mW, 185 mW (7.42 mA) of which is drawn from V_{DD} while 113 mW (4.51 mA) comes from V_{SS}.

Clock #1 was the only chip that failed prior to 1000 hours of operation at 500 °C. The observed electrical failure mode was the 21-stage ring oscillator base clock sub-circuit ceased functioning. Post-test optical microscope inspection of this failed chip revealed the presence of abundant dielectric cracks and discolored metal traces localized to the 21-stage ring oscillator, including those denoted by arrows in Figure 13. The observations of dielectric cracks and discolored metal traces are consistent with our prior studies of long-term 500 °C SiC JFET IC failure [1,16]. In particular, failure occurs where overlying dielectric films become cracked, enabling oxygen transport and localized oxidization of $TaSi_2$ metal beneath the cracks that eventually disrupts electrical conduction through metal interconnect traces. The further understanding and mitigation or elimination of this failure mechanism remains a goal of on-going research.

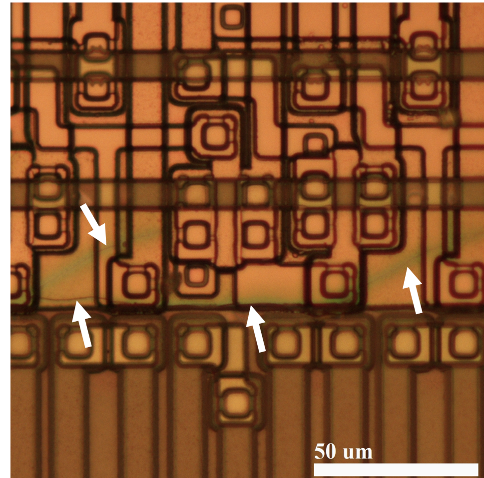

Figure 13. Post-test optical micrograph of portion of the Clock #1 chip ring oscillator sub-circuit that failed. White arrows denote examples of dielectric cracks and metal trace discoloration, symptoms of the primary 500 °C IC failure mechanism.

IV. Conclusion

This work has demonstrated the longest duration of 500 °C electrical operation ever reported for a semiconductor integrated circuit. Such unprecedented durability, demonstrated on circuits of increased complexity (≥ 175 transistors/chip) compared to prior 500 °C-durable circuits, validates 4H-SiC JFETs as a leading technology for placing beneficial electronics into much harsher environments for combustion engine, planetary, deep-well drilling, and other extreme-environment applications. Beyond the initial feasibility demonstrations conducted to date, considerable optimization, up-scaling, and verification of this integrated approach remains to be accomplished.

Acknowledgements

The authors wish to gratefully acknowledge the assistance of D. Lukco, K. Moses, J. Gonzalez, A. Avishai, M. Mrdenovich, G. Hunter, R. Buttler, F. Miranda, L. Matus, and R. Okojie. This work was conducted by The NASA John H. Glenn Research Center in Cleveland, OH USA under joint funding from NASA Science Mission Directorate (High Operating Temperature Technology, Planetary Instrument Concepts for the Advancement of Solar System Observations, and Long-Lived In-Situ Solar System Explorer projects) and NASA Aeronautics Directorate (Transformative Tools and Technologies project).

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