Double Data Rate (DDR) Memory Devices

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Lentech, Inc. in support of NEPP

Acknowledgment:
This work was sponsored by:
NASA Electronic Parts and Packaging (NEPP)

Acronyms

Acronym	Definition
1MB	1 Megabit
3D	Three Dimensional
3DIC	Three Dimensional Integrated Circuits
ACE	Absolute Contacting Encoder
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AF	Air Force
AFRL	Air Force Research Laboratory
AFSMC	Air Force Space and Missile Systems Center
AMS	Agile Mixed Signal
ARM	ARM Holdings Public Limited Company
BGA	Ball Grid Array
BOK	Body of Knowledge
CAN	Controller Area Network
CBRAM	Conductive Bridging Random Access Memory
CCI	Correct Coding Initiative
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CRÈME	Cosmic Ray Effects on Micro Electronics
CRÈME MC	Cosmic Ray Effects on Micro Electronics Monte Carlo
CSE	Crypto Security Engin
CU	Control Unit
D-Cache	defered cache
DCU	Distributed Control Unit
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DLA	Defense Logistics Agency
DMA	Direct Memory Access
DMEA	Defense MicroElectronics Activity
DoD	Department of Defense
DOE	Department of Energy
DSP	Digital Signal Processing
dSPI	Dynamic Signal Processing Instrument
Dual Ch.	Dual Channel
ECC	Error-Correcting Code
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
EMIB	Multi-die Interconnect Bridge
ESA	European Space Agency
eTimers	Event Timers
ETW	Electronics Technology Workshop
FCCU	Fluidized Catalytic Cracking Unit
FeRAM	Ferroelectric Random Access Memory
FinFET	Fin Field Effect Transistor (the conducting channel is wrapped by a thin silicon "fin")
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FY	Fiscal Year
GaN	Gallium Nitride
GAN GIT	Panasonic GaN GIT Eng Prototype Sample
GAN SIT	Gallium Nitride GIT Eng Prototype Sample
Gb	Gigabyte
GCR	Galactic Cosmic Ray
GIC	Global Industry Classification

Acronym	Definition
Gov't	Government
GPU	Graphics Processing Unit
GRC	NASA Glenn Research Center
GSFC	Goddard Space Flight Center
GSN	Goal Structured Notation
GTH/GTY	Transceiver Type
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HMC	Hybrid Memory Cube
HP Labs	Hewlett-Packard Laboratories
HPIO	High Performance Input/Output
HPS	High Pressure Sodium
HUPTI	Hampton University Proton Therapy Institute
I/F	interface
I/O	input/output
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IC	Integrated Circuit
IC	Integrated Circuit
I-Cache	independent cache
IUCF	Indiana University Cyclotron Facility
JFAC	Joint Federated Assurance Center
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (FPGAs use JTAG to provide access to their programming debug/emulation functions)
KB	Kilobyte
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
LANL	Los Alamos National Laboratories
LANSCE	Los Alamos Neutron Science Center
LLUMC	Loma Linda University Medical Center
L-mem	Long-Memory
LP	Low Power
LVDS	Low-Voltage Differential Signaling
LW HPS	Lightwatt High Pressure Sodium
M/L BIST	Memory/Logic Built-In Self-Test
MBMA	Model-Based Missions Assurance
MGH	Massachusetts General Hospital
Mil/Aero	Military/Aerospace
MIPI	Mobile Industry Processor Interface
MMC	MultiMediaCard
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	Microprocessor
MP	Multiport
MPFE	Multiport Front-End
MPU	Microprocessor Unit
Msg	message
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NASA STMD	NASA's Space Technology Mission Directorate
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPP	NASA Electronic Parts and Packaging
NGSP	Next Generation Space Processor
NOR	Not OR logic gate

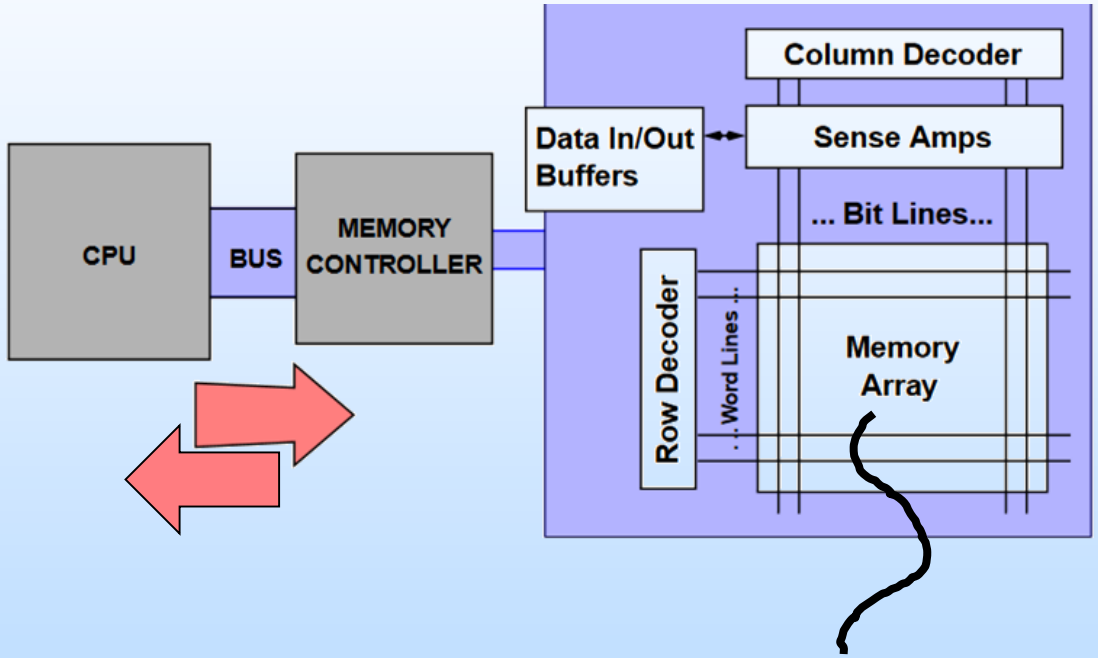
Acronym	Definition
NRL	Naval Research Laboratory
NRO	United States Navy National Reconnaissance Office
NSWC Crane	Naval Surface Warfare Center, Crane Division
OCM	On-chip RAM
PBGA	Plastic Ball Grid Array
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
PLL	Phase Locked Loop
POL	point of load
PoP	Package on Package
PPAP	Production Part Approval Process
Proc.	Processing
PS-GTR	High Speed Bus Interface
QDR	quad data rate
QFN	Quad Flat Pack No Lead
QSPI	Serial Quad Input/Output
R&D	Research and Development
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
SATA	Serial Advanced Technology Attachment
SCU	Secondary Control Unit
SD	Secure Digital
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDM	Spatial-Division-Multiplexing
SEE	Single Event Effect
SESI	secondary electrospray ionization
Si	Silicon
SiC	Silicon Carbide
SK Hynix	SK Hynix Semiconductor Company
SLU	Saint Louis University
SMDs	Selected Item Descriptions
SMMU	System Memory Management Unit
SNL	Sandia National Laboratories
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
STT	Spin Transfer Torque
TBD	To Be Determined
Temp	Temperature
THD+N	Total Harmonic Distortion Plus Noise
TRIUMF	Tri-University Meson Facility
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
U MD	University of Maryland
UART	Universal Asynchronous Receiver/Transmitter
UFHPTI	University of Florida Proton Health Therapy Institute
UltraRAM	Ultra Random Access Memory
USB	Universal Serial Bus
VNAND	Vertical NAND
WDT	Watchdog Timer

Outline

- What the technology is (and isn't)
- Our tasks and their purpose
- Roadmap
- Partners
- Test Readiness
- Plans
- Comments

Technology

- **Double Data Rate (DDR) Memories**
  - **Memory transfer upon rising and falling edges of the clock signal**
    - **permits *double the transfer rate* without increasing the frequency of the clock signal**
  - **Advanced error correction features can be employed**
  - **Cell disturbance via Rowhammer has manifested in DDR3 & DDR4 due to feature scaling**
  - **Typical software model:**
    - **Flight computers boot from ROM, but tend to run from RAM**
    - **RAM permits *larger* data sets to be processed concurrently**



- Memory array does not have to be DRAM
- We are focusing on a DDR interface

FY18-19: DDR Testing

Description:

- This is a task over all device topologies and process.
- The intent is to determine inherent radiation tolerance and sensitivities,
- Identify challenges for future radiation hardening efforts,
- Investigate new failure modes and effects
- Testing includes total dose, single event (proton) and reliability. Test vehicles will include a variety of volatile memory devices as available

FY18-19 Plans:

- Prove out DDR4 test capability
- Probable test structures for TID and SEE:
  - Micron
  - Samsung
  - Hynix
  - Nanya
  - Intelligent Memory
- Tests:
  - characterization pre and post-rad

Schedule:

Microelectronics T&E	FY18				FY19							
	M	J	J	A	S	O	N	D	J	F	M	A
On-going discussions for test samples	■	■	■	■	■	■	■	◇				
DDR4 Tester Development	■	◇	■	■								
TID Testing									◇	■	■	
SEE Testing									◇	■	■	
Analysis and Comparison				■					■	■	■	◇

Lead Center/PI: GSFC/Lentech/Wyrwas

Deliverables:

- Test reports and quarterly reports
- Expected submissions for publications

NASA and Non-NASA Organizations/Procurements:

- Source procurements: TID (GSFC), Proton (MGH, Cincy, NWMCPC, Mayo, Provision)

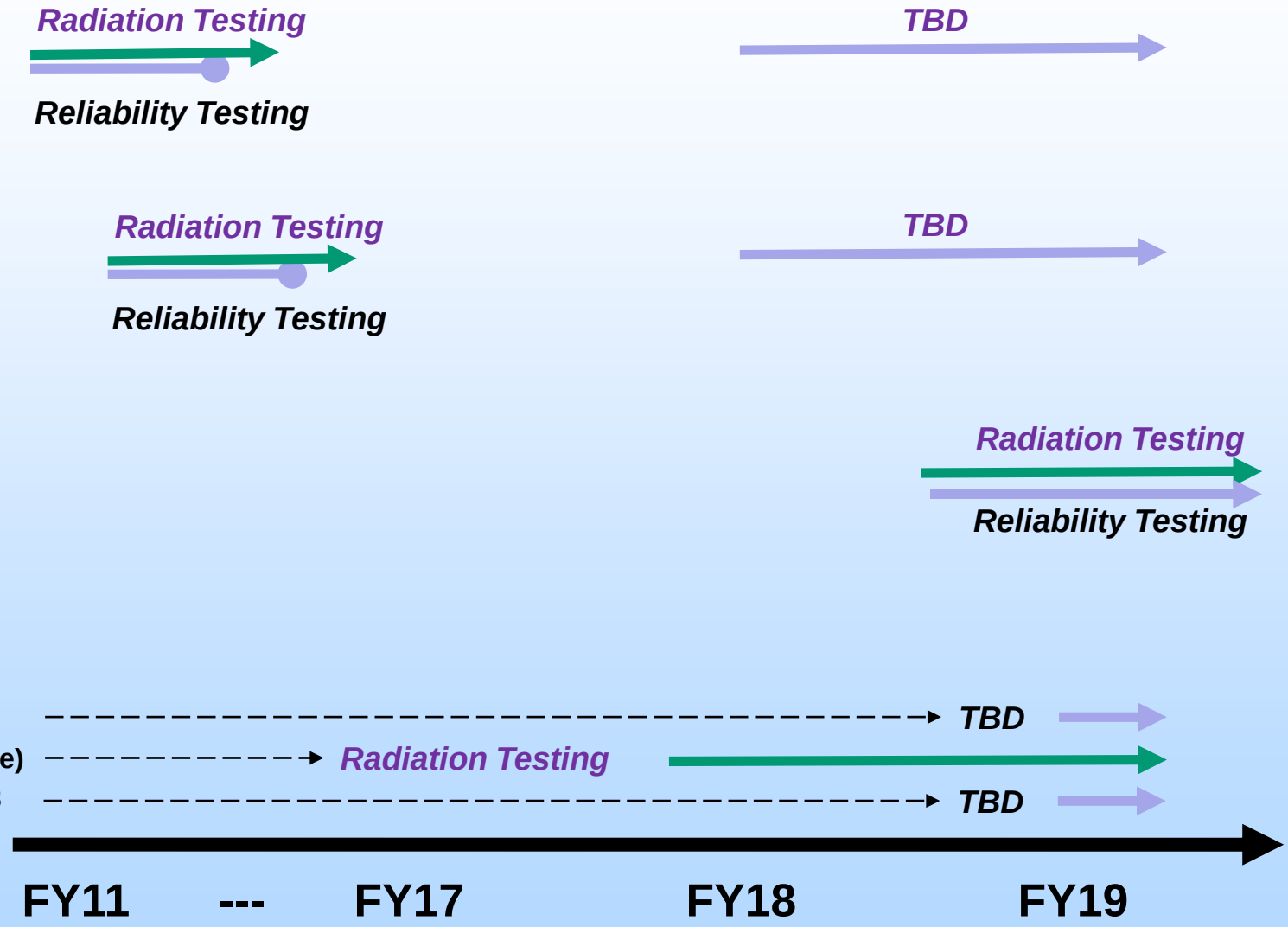
DDR Roadmap

DDR2
- ISSI
- Hynix
- Samsung
- Micron

DDR3
- Intelligent Memories
- Hynix
- Samsung
- Micron 16nm

DDR4
- Samsung
- Micron
- Hynix
- Nanya
- Intelligent Memories

DDR-like & 3D Memories
- DiRAM (Tezzaron)
- 3D Xpoint (Intel Optane)
- Everspin MRAM DDR3



Test Readiness

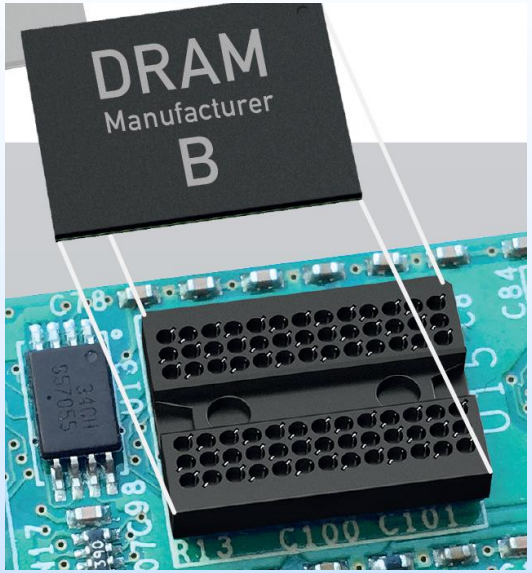
- Collaboration with Kozio has yielded a straightforward economic approach to testing multiple DDR4 types and speed grades
  - Single and Dual Rank DIMMs
  - Single and multiple chip select (CS)
  - ECC and non-ECC
- Based on a low cost reference design board (RDB) from NXP/Freescale
  - LS1046A-RDB containing four (4) 64-bit ARM Cortex-A72 microprocessors
  - DRAM Controller is 32 \ 64-bit DDR4
  - Software is loaded over the JTAG port using USB 2.0, but run from the microprocessor
- Software permits a comprehensive test suite to produce and apply payload patterns to the DRAM
  - During benchmarking we are able to do 0s, 1s, checkerboard, inverted-checkerboard, ‘walking 1s’ and ‘walking 0s’ patterns with read, write, verify (RWV) in under 60 seconds
  - Software loads custom firmware for DDR4 controller during hardware initialization
- We have established a relationship with a supplier to build socketed DDR4 DIMMs
  - for each available type of memory (both FBGA78 and FBGA96 chip components)
  - across our five (5) semiconductor vendors
  - Same configuration can be utilized with DDR3 memory

Plans Moving Forward

- We will be procuring DIMMs:
  - UDIMM, single-sided, 7 Chips plus 1 socket, all x8 in FBGA78
  - UDIMM, double-sided, 15 Chips plus 1 socket, all x8 in FBGA78
  - ECC UDIMM, single-sided, 8 Chips plus 1 socket, all x8 in FBGA78
  - ECC UDIMM, double-sided, 17 Chips plus 1 socket, all x8 in FBGA78
  - UDIMM, single-side, 3 Chips plus 1 socket, all x16 in FBGA96

- The DIMMs will be assembled using DDR4 components from:
  - Samsung
  - Micron
  - Hynix
  - Nanya
  - Intelligent Memories

- The NXP LS1046A-RDB will receive an interposer to extend the DIMM above the circuit board to permit better alignment to radiation sources



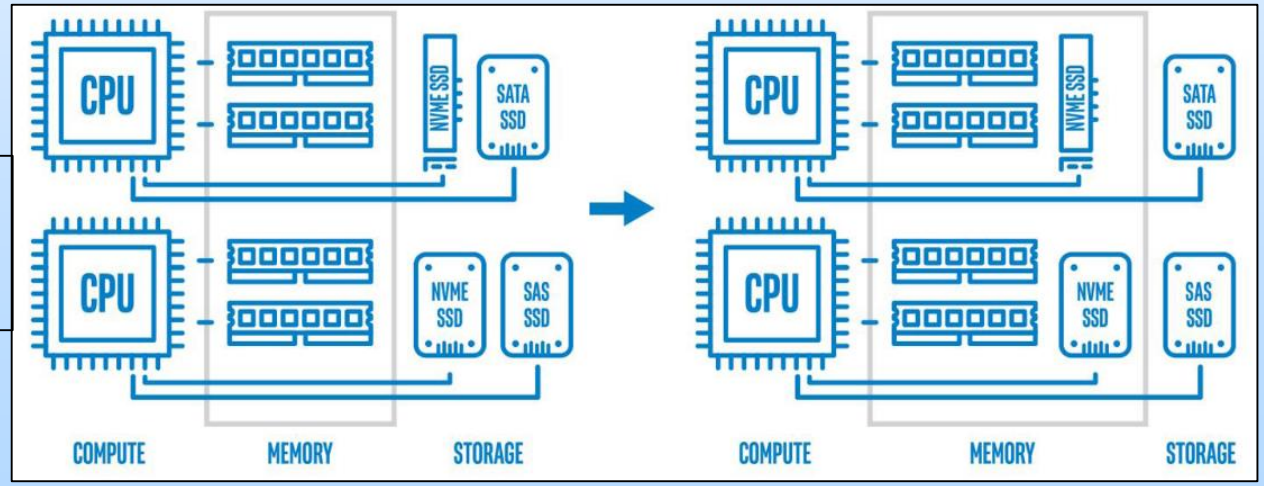
Comments

- Sad News:
  - Kozio is leaving the DDR calibration and testing business
  - … But we have an arrangement to continue to use their code library to continue the development of our platform

- We have ongoing collaboration with JPL, Kozio, Cubic Aerospace, Everspin (MRAM), and others
  - Please contact Ed if you have any interest in DDR memory devices

- Emerging non-volatile memory (NVM) technologies are beginning to infiltrate the computing regime as storage-class memory (SCM)
  - SCM uses NVM as the storage and DRAM as a cache for active data
  - Some NVM technologies can be tested as DDR

Paradigm Shift



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