Development of an Optical Slice for an RF and Optical Software Defined Radio

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ABSTRACT

A key component in the Integrated Radio and Optical Communications project at the National Aeronautics and Space Administration's (NASA) Glenn Research Center (GRC) is the radio frequency (RF) and optical software defined radio (SDR). A NASA RF SDR might consist of a general purpose processor to run the Space Telecommunications Radio System (STRS) Architecture for radio command and control, a reconfigurable signal processing device such as a field programmable gate array (FPGA) which houses the waveform, and a digital to analog converter for (DAC) transmitting data. Prior to development, SDR architecture trades on how to combine the RF and optical elements were studied. A modular architecture with physically separate RF and optical hardware slices was chosen and the optical slice of an SDR was designed and developed. The Harris AppSTAR™ platform, which consists of an FPGA processing platform with a mezzanine card targeted for RF communications, was used as the base platform in prototyping the optical slice. A serially concatenated pulse position modulation (SCPPM) optical waveform was developed. The waveform follows the standard described in the Consultative Committee for Space Data Systems (CCSDS) Optical Communions Coding and Synchronization Red Book. A custom optical mezzanine printed circuit board card was developed at NASA GRC for optical transmission. The optical mezzanine card replaces the DAC, which is used in the transmission of RF signals. This paper describes RF and optical SDR architecture trades, the Harris AppSTAR™ platform, the design of the SCPPM waveform, and the development of the optical mezzanine card.

Keywords: Optical communications, software defined radio, pulse position modulation, waveform

1. INTRODUCTION

NASA communication systems are being upgraded in order to accommodate the increased data return requirements of future NASA missions. In the past, X-band or S-band links were capable of meeting the mission requirements for telemetry, tracking, and command (TT&C) as well as data return. Therefore, only one communications system was necessary. In the future, missions will need a high data return communications link, combined with a more reliable link for TT&C. Integration of these multi-band systems will be necessary in order to save mass and power, and also optimize re-usability across different NASA missions. One part of the communication system which can be integrated is the software defined radio.

This paper describes an architecture design and implementation of an integrated RF and optical reconfigurable software defined radio. Relevant background information is described Section 2. A description of architecture trades is given in Section 3. Section 4 includes the design and implementation of the optical slice for the RF and optical SDR.

2. BACKGROUND INFORMATION

2.1 The Space Telecommunications Radio System

The Space Telecommunications Radio System (STRS)[1] is an open architecture for NASA software defined radios (SDRs). It provides a common framework which abstracts the application software, including the waveform, from the radio platform. This enables waveform portability across different SDR platforms. The STRS Architecture separates the radio hardware into three functional modules – the general-purpose processing module (GPM), signal processing module (SPM), and the radio frequency (RF) module (RFM). The GPM receives commands from the avionics and provides control signals to the waveform running in the field programmable gate array (FPGA). The SPM, which typically consists of FPGAs, contains the waveform application. The RFM consists of analog to digital converters (ADCs) and digital to analog converters (DACs) which are used to receive and send an intermediate frequency to and from the FPGA. A diagram of an

STRS SDR is shown in Figure 1. An optical module (OM) is included in the standard as a placeholder for future development. The architecture standard does not specify a specific physical implementation of each module or the interfaces to each module, but does advocate for a modular hardware architecture.

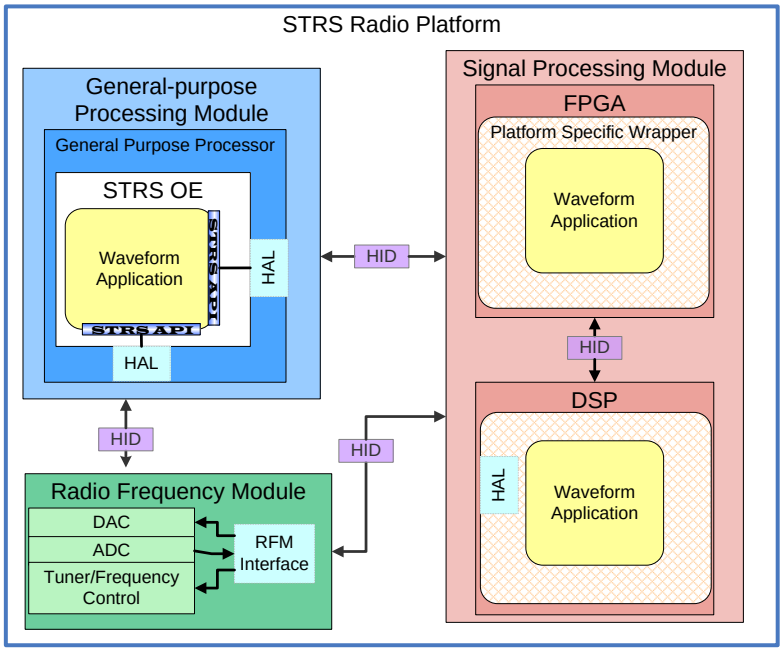

Figure 1: Notional STRS SDR platform block diagram.

2.2 CCSDS Optical Communications Standards

NASA is taking part in the development of Consultative Committee for Space Data Systems (CCSDS) standards for the channel coding, synchronization, and physical layer of optical communications. One of the CCSDS standards is for high photon efficiency optical communications systems, which send and receive signals in photon starved links through the atmosphere. The standard is based on serially concatenated pulse position modulation (SCPPM)[2], which was used on the Lunar Laser Communications Demonstration. It is geared towards missions for deep space or other missions requiring a high photon efficiency. It consists of pulse position modulation (PPM) orders M=4, 8, 16, 32, 64, 128, and 256. The code rates are 1/3, 1/2, and 2/3. The PPM slot clock is 0.125 ns, 0.25 ns, 0.5 ns, 1 ns, 2 ns, 4 ns, 8 ns, or 512 ns. PPM symbols can be repeated up to a factor of 32 in order to achieve a slower effective slot rate. It also contains a convolutional interleaver for channel fades.

2.3 Harris AppSTAR™ Platform

The second generation Harris AppSTAR™ platform is comprised of a suite of components which can be configured to fit a particular mission. Of interest to this project is the combination Reconfigurable Space Processor (RSP) and Mezzanine circuit cards. The RSP is a general purpose FPGA card. The Mezzanine is a high performance DAC/ADC for transmitting and receiving data. The Mezzanine is connected directly to the RSP via a high density, impedance controlled connector. This interface is defined with the VITA 57.1 standard. When attached, the RSP and Mezzanine interface to a Space VPX backplane, occupying a single card slot.

The RSP is an FPGA host card which contains two Xilinx Virtex 7 FPGA's, a digital signal processor (DSP), and supplemental memory. The RSP also contains a radiation tolerant Xilinx Virtex 5 FPGA. The Virtex 5 is used to route SpaceWire and JTAG data from the backplane to the rest of the card.

The Mezzanine card is the analog portion of the system. It contains a phase locked loop (PLL), DAC and ADC. This card is designed to receive and transmit intermediate frequencies. This card was not used in the development of the Optical Mezzanine (OM) and therefore will not be discussed in detail here.

3. RF AND OPTICAL SDR ARCHITECTURE STUDY

Future NASA missions will include several different communications systems, which will be used for different purposes. For example, the Mars Reconnaissance Orbiter launched in 2005 includes an X-band system for TT&C with a Ka-band system for data return. Future deep space mission communications systems will also include an optical system for data return. A goal of the Integrated Radio and Optical Communications (iROC) project is to study different ways of effectively integrating the RF radio with the optical radio in order to save size, mass and power. Additionally, it is important to consider other factors such as cost, modularity, and re-usability across NASA missions. Integration of RF and optical can be performed to different degrees, as is shown in Table 1.

The bottom row of the table shows the least integration, with two separate radios integrated together and managed by a common processor. This could be the easiest to implement as no hardware integration is done and each radio can be completely designed and built independently. If the radios are SDRs, they could offer the flexibility to change the waveform after deployment. However, this method does not save mass and power as there is no integration performed.

The top row of the table shows a high level of integration, a custom application specific integrated circuit (ASIC). This is the most mass and power efficient but it is also complicated to develop. However, an ASIC can be costly when the non-recurring engineering development is only spread across a few missions. It is not an SDR and therefore cannot be changed after deployment.

The middle two rows in the table are of interest because they can be realized as an SDR. An SDR enables new waveforms to be loaded and used after the radio has been deployed in space. The case of having multiple processing devices co-located on a single card can be realized as an SDR and saves mass compared to two separate systems. However, it is complicated to design and could have a higher cost than a modular slice architecture. It is also not as modular compared to a slice architecture where the RF and optical would have individual cards in a common chassis or slices in a stacked configuration.

Table 1. SDR architecture integration levels.

Integration Option	Architecture description	Mass/ Power	Modification after deployment	Level of Integration	Modularity	Cost
Chip-level	Custom ASIC	Low/ Low	Only within initial design	High	Low	High
RF and Optical processing co-located on a single circuit card	Integration of RF and optical waveform on same FPGA or on different FPGA but same circuit card	Medium/ Medium	Can change by loading new waveforms	Medium	Low	High
Modular slice architecture	Individual cards for RF and Optical with a shared GPP, packaging, power	Medium/ Medium-High	Can change by loading new waveforms	Medium	High	Low
None	Separate radios	High/High	Can change by loading new waveforms	Low	High	Low

The modular slice architecture can be implemented as an SDR with individual cards for RF and optical integrated through packaging. It can be designed as a stacked architecture or as separate RF and optical cards located in a common chassis. The stacked architecture is shown in Figure 2 and the separate cards located in a common chassis is depicted in Figure 3. This modular slice architecture gives NASA the flexibility to customize the SDR for each mission because the RF and optical cards are separate. Therefore, NASA could utilize one or both of the cards depending on the communications systems selected for a particular mission. The Jet Propulsion Laboratory has implemented a stacked architecture in the Universal Space Transponder (UST) SDR[3].

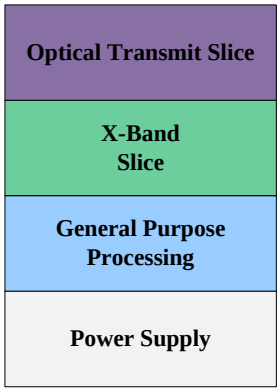

Figure 2. Modular slice architecture in a stacked configuration.

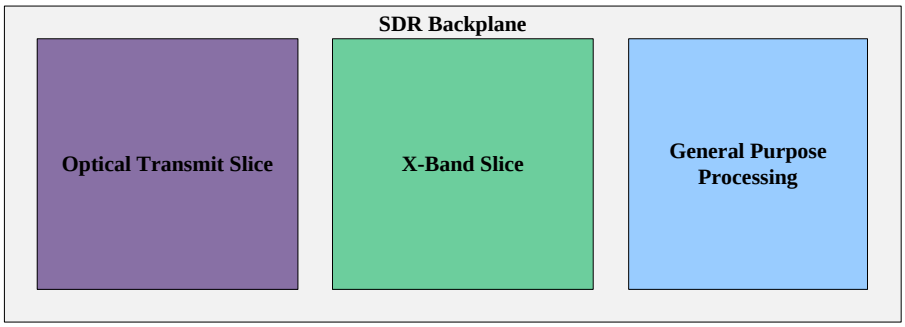

Figure 3. Modular slice architecture implemented as cards in a common backplane.

A standardized modular hardware architecture would give NASA the ability to re-use hardware modules and the flexibility to easily customize the SDR for a particular mission. Standardized hardware interfaces between key modules would be necessary. For example, the module containing the FPGA or other waveform processing device should have a standardized interface to a module which contains the DAC, ADC, or parallel to serial conversion. This module would be a mezzanine card on the waveform processing card or a separate physical slice. This architecture, shown in Figure 4, depicts the optical transmit slice and X-band slice each having the same waveform processing card with customized mezzanine cards. The common interface between the waveform processing card and the mezzanine, shown in blue, allows the FPGA module to be re-used across missions and the SDR to be customized for a particular mission. There should also be an interface to a GPM for command and control of the radio. Additionally, a standardized physical form factor should be considered, such as Space VPX (VITA 78). This would allow NASA the flexibility to purchase different modules from different companies.

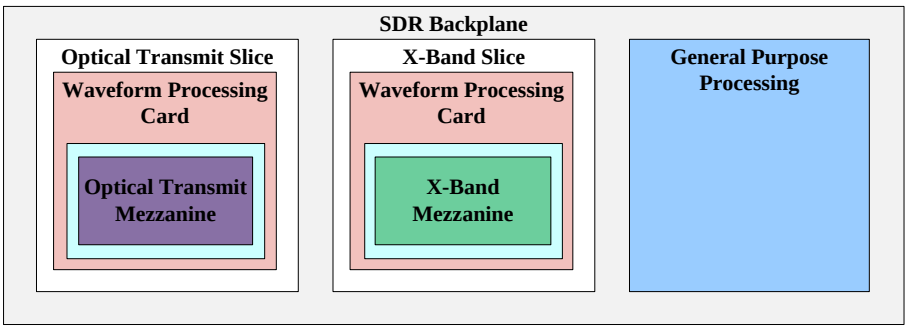

Figure 4. Modular slice architecture showing common interfaces between the waveform processing card and the mission specific mezzanine card.

4. DESIGN AND IMPLMENTATION OF THE OPTICAL SLICE

A laboratory implementation[4] of the optical slice architecture design was implemented using a Xilinx FPGA development platform. Next, the Harris AppSTAR™ platform, in combination with a custom optical mezzanine card, was used to implement the optical slice. The CCSDS Optical Communications high photon efficiency waveform was implemented on the FPGA. The waveform command and control was implemented on a computer for laboratory testing purposes. The implementation is shown in Figure 5. A description of the platform and waveform design follows.

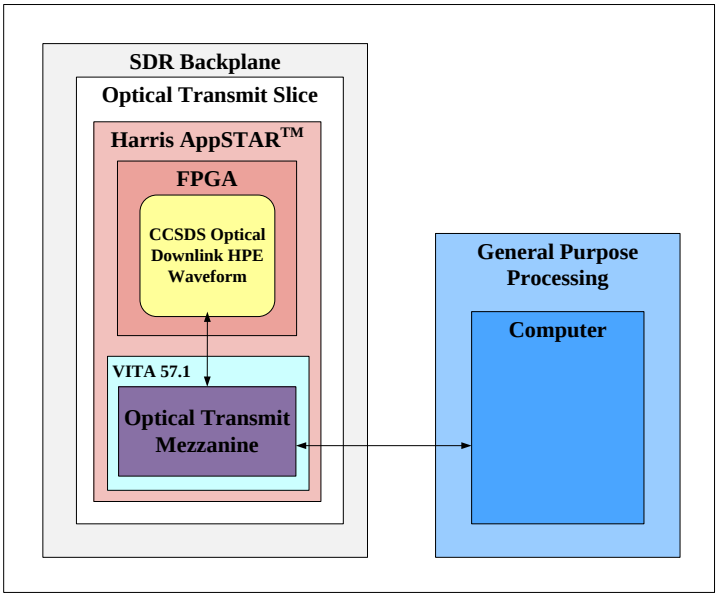

Figure 5. GRC implementation of the optical slice.

4.1 Optical Mezzanine Card Architecture

The main goal of the Optical Mezzanine (OM) development was to design the interface between the FPGA and the electro-optic subsystem using high reliability components. As such, significant development time was avoided by selecting an existing FPGA development platform. The Harris AppSTAR™ platform was selected due to its ease of re-configurability and heritage on the Space Communications and Navigation (SCaN) Testbed[5]. The RF mezzanine was removed and replaced with a custom OM card. The architecture of the OM can be seen in Figure 6.

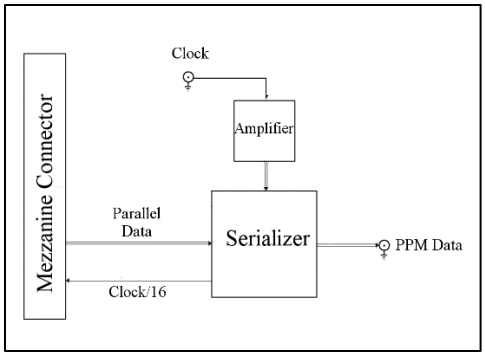

Figure 6. Optical mezzanine card architecture.

The main function of the OM is to perform serialization on the parallel data generated in the FPGA. The user has the capability to input a variable clock. It allows the user to test the system using any desired input clock and not be limited by a PLL frequency range and resolution. The large clock bandwidth requires all downstream components to also accept a large bandwidth, therefore introducing jitter.

The clock signal is then fed into an LVDS limiting amplifier. This amplifier converts the unbalanced input signal to the balanced LVDS signal required downstream. The input sine wave is amplified and then limited to the rails of the system, approximating a square wave clock signal.

The heart of the serialization section is the parallel to serial interface which is built from a high bandwidth multiplexer. Modulated data from the FPGA is applied to the multiplexer through 16 parallel input lines and output serially at the applied clock speed. The multiplexer provides an output clock at a rate 16 times less than the input clock. This signal is fed back to the FPGA for data synchronization. The hardware multiplexer allows the FPGA to run at a lower clock speed, offering much more flexibility to the waveform developer.

4.2 Extinction Ratio Results

To analyze the extinction ratio (ER) potential of the system, a time domain measurement was taken and imported into MATLAB for analysis. The system was set to generate a periodic function with every sixteenth bit set high and the rest set to low. This produced the measured waveform seen in Figure 7.

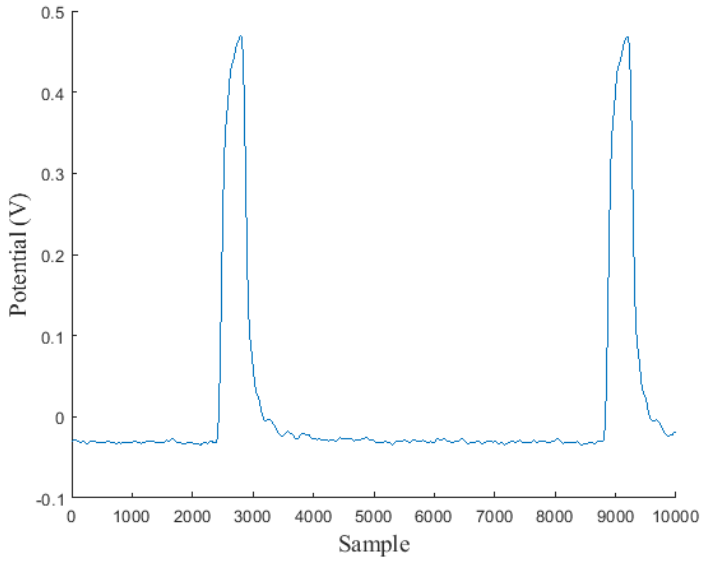

Figure 7. Raw waveform with 0.5 ns slot clock.

A properly biased and normalized signal is represented by PPM(t) where S(t) represents the measured waveform.

$$PPM(t) = \frac{\left(S(t) - \frac{\int_{\pi}^{2\pi} S(t)dt}{\pi}\right)}{\frac{\int_{0}^{\pi} S(t)dt}{\pi}} \quad (1)$$

In this case an interferometer is used to modulate the continuous wave laser. The output light intensity can be obtained with the following transfer function.

$$I(t) = \sin\left(\frac{\pi}{2}.\frac{PPM(t)}{V_{\pi}}\right)^2 \quad (2)$$

Where I(t) is the output intensity as a portion of the input intensity and V_{π} is half the period of the modulator. The non-linearity of the interferometer can be used to increase ER if the input signal has peak to peak amplitude V_{π} and is DC biased such that the logic levels fall on the minimum and maximums of the interferometer transfer function.

The resulting waveform I(t) was then parsed into 16 slots, each with a length equal to the slot width. This gives a dataset of slots from which an ER estimation cab be calculated for a range of different modulation orders. For PPM orders with greater than 16 slots, the most stable slot (15) was repeated. The assumption is such that all transients have converged to a stable state by slot 15 and therefore slot 15 is a valid estimation of any later slot before the next pulse. For PPM orders with less slots than 16 slots, the unused slots were trimmed from the dataset.

$$ER = 10\log_{10}\left(\frac{\int I(t_1)dt}{\int I(t_2)dt / N_{slots}}\right) \quad (3)$$

Where t_1 it the duration of the pulse slot, t_2 is the duration of the slots with no pulses, and N_{slots} is the number of PPM slots per symbol not containing a pulse.

Table 2 shows the resulting ER for a set of different clock speeds and modulation orders. An interesting result is that ER increases with modulation order without the need for increased pulse quality. This is driven by the N_{slots} term that appears in the denominator of the ER calculation.

Table 2. Extinction ratio results for slot widths from 0.25 ns to 8 ns.

Slot Width (ns)	**PPM-4 (dB)**	**PPM-8 (dB)**	**PPM-16 (dB)**	**PPM-32 (dB)**	**PPM-64 (dB)**	**PPM-128 (dB)**	**PPM-256 (dB)**	**PPM-512 (dB)**
8	21	25	28	32	34	37	40	43
4	21	24	28	31	34	37	40	43
2	18	22	26	29	32	35	38	41
1	17	21	25	28	31	34	37	40
0.5	17	20	24	27	30	33	36	39
0.25	8	12	15	18	21	25	28	31

4.3 Jitter Results

In order to define the requirement for the maximum timing jitter of the transmitter clock, the jitter of the receiver must be considered. Jitter introduced in the receiver will have the same impact on bit error rate (BER) as jitter introduced in the transmitter; therefore, it is possible to define a requirement based on an acceptable increase in the largest known source of jitter in the system. The main source of jitter in the system is the single photon counting detector which has typical jitter values between 25ps and 915ps[6]. Under the assumption that the phase noise distribution approaches a Gaussian random variable, the total system jitter can be obtained via root sum of squares.

$$\sigma_{\text{total}}{}^2 = \sigma_{\text{Rx}}{}^2 + \sigma_{\text{Tx}}{}^2 \tag{4}$$

A coefficient c is defined to represent an acceptable increase in total system jitter with reference to receiver jitter. A c value of one would represent a zero percent increase in total system jitter, while a c value of 1.02 would represent a two percent increase in total system jitter with respect to receiver jitter.

$$\sigma_{\text{Total}} = c\sigma_{\text{Rx}}; c \in [1, +\infty) \tag{5}$$

Combining the above equations reveals the following requirement model for transmitter jitter. Figure 8 shows this result for a selection of common single photon detectors.

$$\sigma_{\text{Tx}} \leq \sigma_{\text{Rx}}\sqrt{(c^2 - 1)} \tag{6}$$

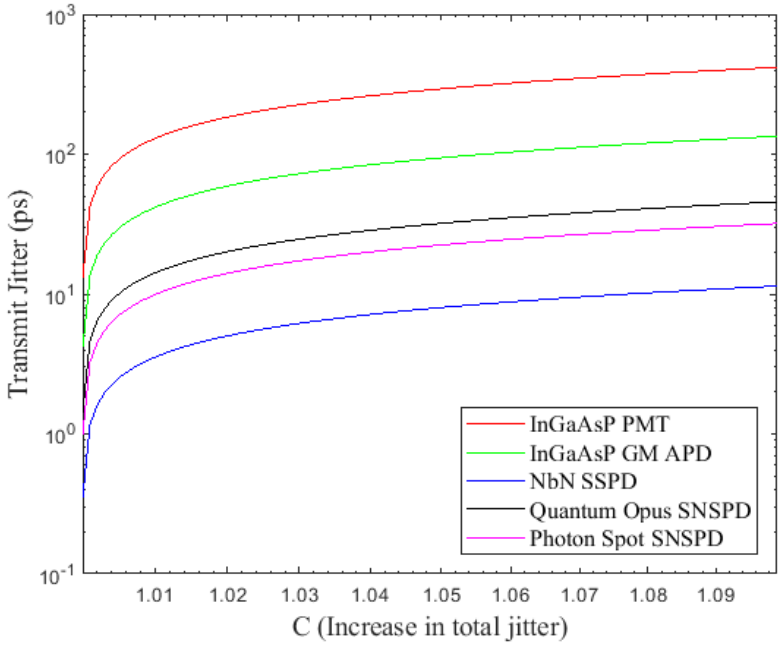

Figure 8. Impact of transmitter jitter on total system jitter[6, 7].

For the lowest jitter single photon counting detector, a 3.6ps transmitter jitter value results in a one percent increase in total jitter. In this case, a design requirement was set to a ten percent increase in total jitter which corresponds to an 11.4ps jitter requirement.

Transmitter jitter was measured with an oscilloscope set to measure a statistical distribution of the zero crossing of the output waveform. The standard deviation of this distribution is a good approximation of the system jitter. The system showed a jitter of 5.4ps, which is well within the requirement.

4.4 Optical Waveform Architecture

The CCSDS optical communications high photon efficiency waveform was implemented and tested on an FPGA. The waveform consists of the modules shown in Figure 9. All modulation orders (M=4, 8, 16, 32, 64, 128, 256) and code rates (1/3, 1/2, 2/3) are re-configurable in real time. The convolutional channel interleaver has been implemented and tested on the FPGA with small values for N (number of rows) and B (shift register length parameter), which are modifiable at compile time. The Verilog code for the channel interleaver was generated using a MATLAB script, which allows the interleaver values for N and B to be modified before the code is generated. All of the reconfigurable parameters in the waveform are listed in Table 3.

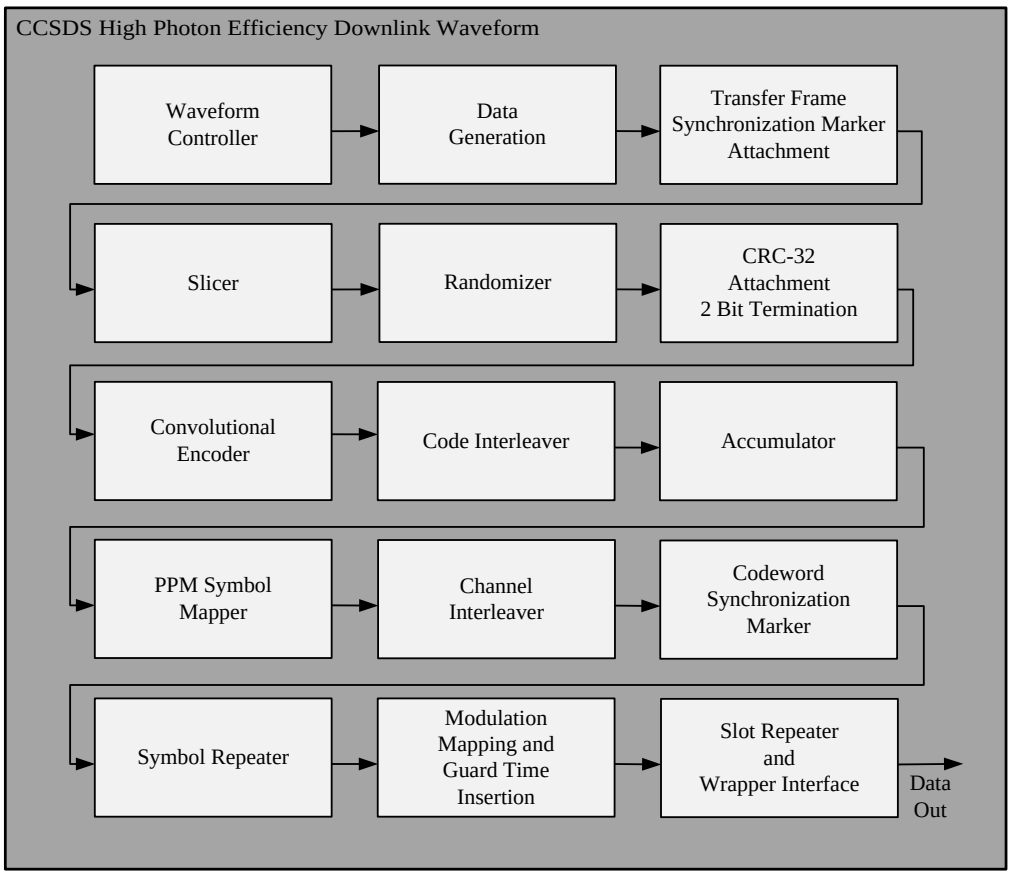

Figure 9. Block diagram of the optical waveform.

Table 3. Reconfigurable parameters in the optical waveform.

Module Name	**Reconfigurable Parameters**	
Data Generation	Data Source: PRBS 2^{23}-1, Constant, Counting Up	
Transfer Frame Synchronization Marker	-	
Slicer	-	
Randomizer	-	
CRC-32 Attachment / 2 Bit Termination	-	
Convolutional Encoder	Code Rate: 1/3, 1/2, 2/3	
Accumulator	-	
PPM Symbol Mapper	-	
Channel Interleaver	Number of Rows: N Shift Register: B	Note: Reconfigurable at compile time only
Codeword Synchronization Marker	-	
Symbol Repeater	Number of Symbol Repeats: 1, 2, 3, 4, 8, 16, 32	
Modulation Mapping and Guard Time Insertion	M: 4, 8, 16, 32, 64, 128, 256	
Slot Repeater and Wrapper Interface	Number of Slot Repeats: 1, 2, 4, 8, 16, 1024	

The waveform is clocked off of a single input clock, which is 125 MHz when the slot clock is set at 2 GHz. The slot repeater module repeats each slot in order to achieve the 1 ns, 2 ns, 4 ns, 8 ns, and 512 ns slot widths. The waveform is capable of effective data rates as high as 528 Mbps with a 2 GHz (0.5 ns) slot clock. Higher rates could be achieved by increasing the slot clock.

The waveform has a modular design with common input and output interfaces on each block. The data input and data output are paired with data enable lines to indicate when the data is valid. First in first outs (FIFOs) are inserted in blocks in which there is a rate transition. The waveform has an 8 bit parallel bus in between each block, which enables the waveform to operate at the full rate of 528 Mbps when M=4. The data is treated as a serial stream of bits up through the accumulator. The PPM bit to symbol mapper performs a mapping of the bits to PPM symbols. After this block, the data is processed as PPM symbols. This design allows any modulation order to be paired with any code rate.

The waveform has been implemented on a Xilinx ML605 development platform which contains a Virtex 6 FPGA and the Harris AppSTAR™ platform which contains a Virtex 7 FPGA. Utilization metrics without the channel interleaver are listed in Table 4 for the Virtex 6 and the Virtex 7 FPGA.

Table 4. FPGA utilization metrics for the optical waveform without the channel interleaver.

	Virtex 6 FPGA		**Virtex 7 FPGA**	
	Number	**Utilization**	**Number**	**Utilization**
Slice Registers	5,192	1 %	6,043	1.5 %
Slice LUTs	7,098	4 %	4,514	2.2 %
Occupied Slices	2,235	6 %	2,003	3.9 %
LUT FF Pairs Used	7,349	-	6,631	3.3 %
RAMB36	19	4 %	19	2.5 %
RAMB18	9	1 %	9	0.6%

5. CONCLUSIONS

Multiple communications systems within a single NASA mission present new integration design considerations. An architecture for the design of an optical slice in an RF and optical SDR was presented. This architecture was implemented in the Harris AppSTAR™ platform. A custom optical mezzanine card was developed and performance metrics were discussed. The CCSDS Optical Communications high photon efficiency downlink transmit waveform was implemented and tested on Harris AppSTAR™ platform and on the Xilinx Virtex 6 development platform. Implementation metrics were given. The next steps in this project include development of a CCSDS Optical Communications high photon efficiency real-time receiver system.

6. ACKNOWLEDGEMENTS

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