SPIE.

Development of an Optical Slice for an RF and Optical Software Defined Radio

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INTRODUCTION

In the future, NASA missions will need a high data return communications link, combined with a more reliable link for TT&C. Integration of these multi-band systems will be necessary in order to save mass and power, and also optimize re-usability across different NASA missions. One part of the communication system which can be integrated is the software defined radio.

BACKGROUND INFORMATION

Space Telecommunications Radio System

The Space Telecommunications Radio System (STRS)[1] is an open architecture for NASA software defined radios. It provides a common framework which abstracts the application software, including the waveform, from the radio platform.

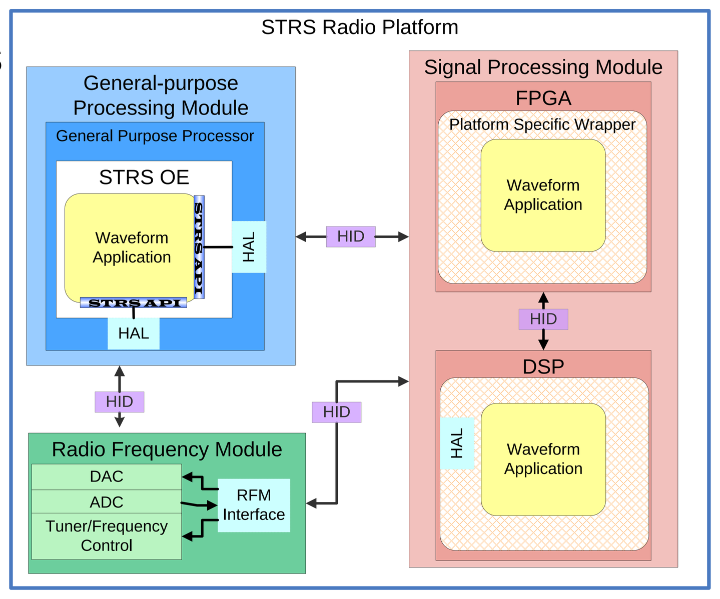

Fig. 1. Notional STRS platform block diagram.

CCSDS Optical Communications Standards

NASA is taking part in the development of Consultative Committee for Space Data Systems (CCSDS) standards for the channel coding, synchronization, and physical layer of optical communications, including a high photon efficiency standard for deep space.

RF AND OPTICAL SDR ARCHITECTURE

A modular slice architecture is advantageous when integrating RF and Optical in an SDR.

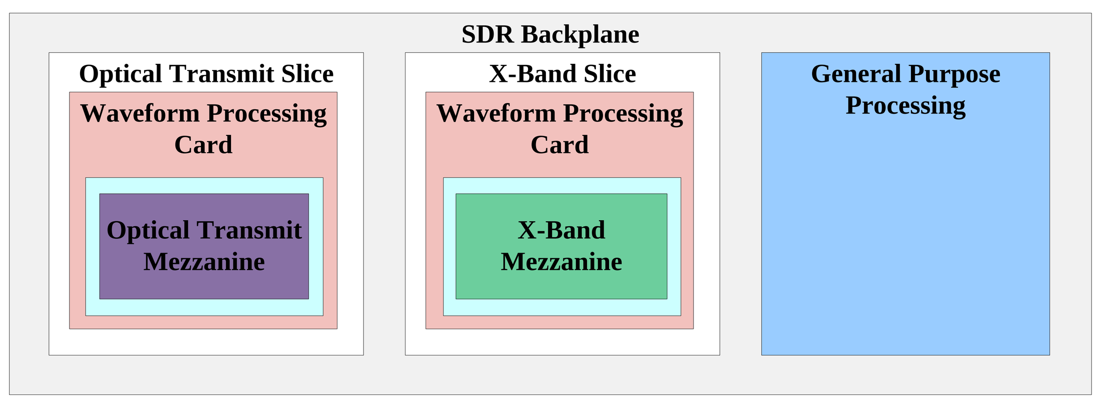

Fig. 2. Modular slice architecture showing common interfaces between the waveform processing card and the mezzanine card. A standardized hardware architecture would allow re-use of the waveform processing card and the flexibility to customize the SDR with a mission specific mezzanine card.

OPTICAL SLICE IMPLEMENTATION

The optical slice was implemented on the Harris AppSTAR™ platform. It includes an optical mezzanine card and the CCSDS Optical Downlink High Photon Efficiency Waveform.

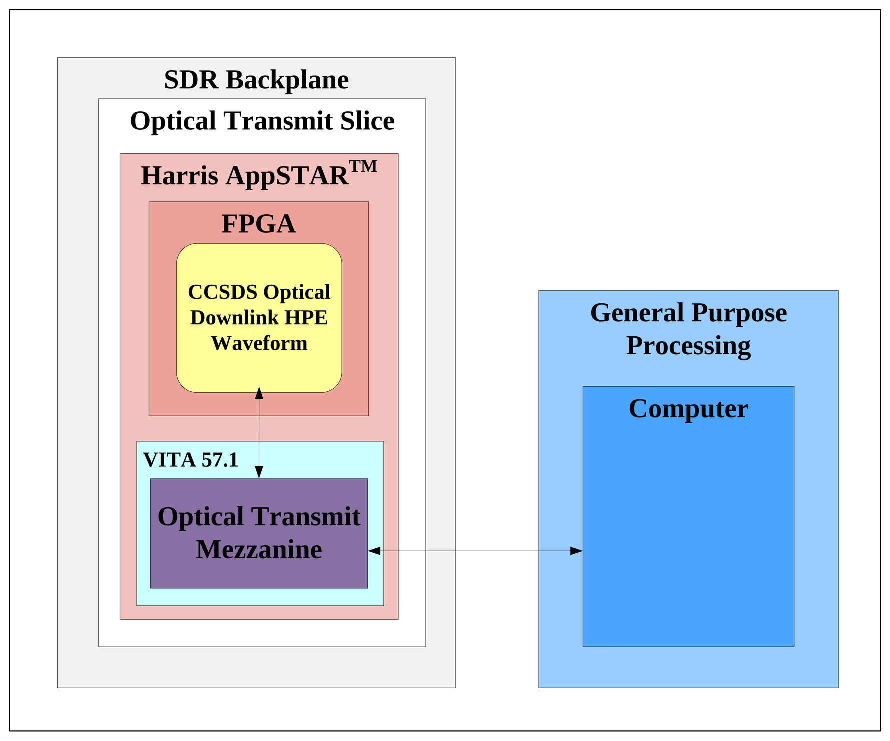

Fig. 3. NASA implementation of the optical slice utilizing the Harris AppSTAR™ platform.

Optical Mezzanine Card

The main function of the optical mezzanine card is serialization of the parallel data generated on the FPGA.

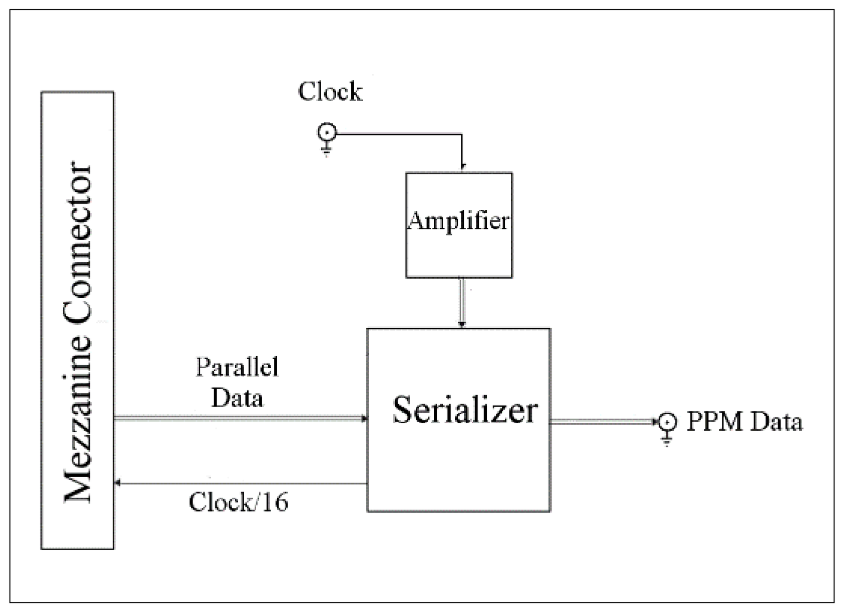

Fig. 4. Optical mezzanine card architecture.

Optical Waveform

The optical waveform implements the CCSDS optical communications standard for high photon efficiency, which is based on the serially concatenated pulse position modulation.[2]

Table 1. Waveform module list with reconfigurable parameters.

Module Name	Reconfigurable Parameters
Data Generation	Data Source: PRBS 2^{23}-1, Constant, Counting Up
Transfer Frame Synchronization Marker	-
Slicer	-
Randomizer	-
CRC-32 Attachment / 2 Bit Termination	-
Convolutional Encoder	Code Rate: 1/3, 1/2, 2/3
Accumulator	-
PPM Symbol Mapper	-
Channel Interleaver	Number of Rows: N Shift Register: B Note: Reconfigurable at compile time only
Codeword Synchronization Marker	-
Symbol Repeater	Number of Symbol Repeats: 1, 2, 3, 4, 8, 16, 32
Modulation Mapping and Guard Time Insertion	M: 4, 8, 16, 32, 64, 128, 256
Slot Repeater and Wrapper Interface	Number of Slot Repeats: 1, 2, 4, 8, 16, 1024

RESULTS

Optical Mezzanine Card Extinction Ratio

The extinction ratio for different modulation orders and slot widths was calculated from a 1/16 duty cycle waveform.

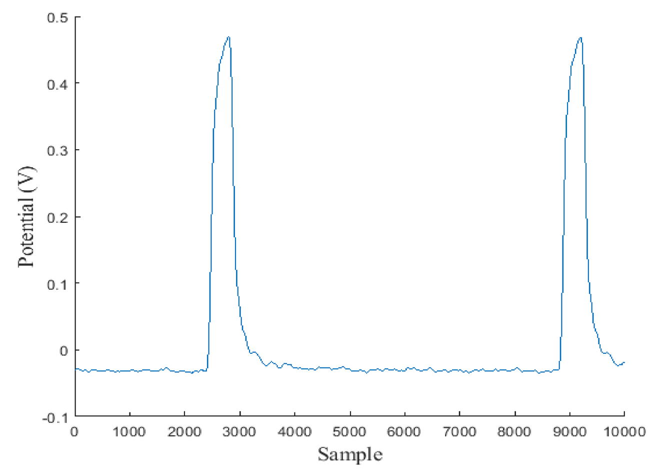

Fig. 5. Waveform used to calculate extinction ratio.

Table 2. Extinction ratio results for slot widths from 0.25 to 8 ns.

Slot Width (ns)	PPM-4 (dB)	PPM-8 (dB)	PPM-16 (dB)	PPM-32 (dB)	PPM-64 (dB)	PPM-128 (dB)	PPM-256 (dB)	PPM-512 (dB)
8	21	25	28	32	34	37	40	43
4	21	24	28	31	34	37	40	43
2	18	22	26	29	32	35	38	41
1	17	21	25	28	31	34	37	40
0.5	17	20	24	27	30	33	36	39
0.25	8	12	15	18	21	25	28	31

Optical Mezzanine Card Jitter Results

The optical mezzanine card has a jitter of 5.4 ps.

FPGA Utilization

FPGA utilization metrics are given for the Virtex 6 FPGA and the Virtex 7 FPGA. The metrics do not include the channel interleaver, as the implementation will vary depending on the mission.

	Virtex 6 FPGA		Virtex 7 FPGA	
	Number	Utilization	Number	Utilization
Slice Registers	5,192	1 %	6,043	1.5 %
Slice LUTs	7,098	4 %	4,514	2.2 %
Occupied Slices	2,235	6 %	2,003	3.9 %
LUT FF Pairs Used	7,349	-	6,631	3.3 %
RAMB36	19	4 %	19	2.5 %
RAMB18	9	1 %	9	0.6%

Table 3. FPGA utilization metrics without the channel interleaver.

FUTURE DEVELOPMENT

The next steps in this project include development of the optical communications high photon efficiency real-time receiver system.

REFERENCES

1. "Space Telecommunications Radio System (STRS) Architecture Standard Release 1.02.1" (2012).
2. Moison, B. and Hamkins, J., "Coded Modulation for the Deep-Space Optical Channel: Serially Concatenated Pulse Position Modulation," The Interplanetary Network Progress Report 42(161) (2005).