Low power signal processing electronics for wearable medical devices

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Abstract— **Custom designed microchips, known as Application Specific Integrated Circuits (ASICs), offer the lowest possible power consumption electronics. However, this comes at the cost of a longer, more complex and more costly design process compared to one using generic, off-the-shelf components. Nevertheless, their use is essential in future truly wearable medical devices that must operate for long periods of time from physically small, energy limited batteries. This presentation will demonstrate the state-of-the-art in ASIC technology for providing online signal processing for use in these wearable medical devices.**

I. INTRODUCTION

Miniaturised medical devices, such as electrocardiogram (ECG) and electroencephalogram (EEG) recorders, are of interest in a large number of fields. Miniaturisation is important for user acceptance, but this implies that only small, energy limited batteries are available for use. Thus for prolonged monitoring the average power consumption must be very low. [1] quantifies this well. If the overall device is assumed to have a volume of 1 cm^3, a common aim for such systems, and half of this space is reserved for a custom made battery of energy density 200 Wh/L, 100 mWh of energy is stored. For operation over 30 days the average power consumption must be less than 140 μW.

This is a challenging power budget to meet. Fig. 1 shows a block diagram of a typical physiological sensor. Key to realising future wearable medical devices is the implementation of the online signal processing stage. This stage provides either real-time data reduction, or real-time analysis of the physiological data such that much less information needs to be transmitted from the medical device. Given a high power wireless transmitter, transmitting less data can significantly reduce the average system power consumption, provided that the online signal processing itself consumes very little power [2].

This presentation will overview state-of-the-art electronics for providing the required signal processing in dedicated electronic circuits. We will overview ASIC technologies, methodologies and the state-of-the-art in terms of performance.

II. LOW POWER SIGNAL PROCESSING HARDWARE

For implementing the online signal processing many design choices are available. For example, should the algorithm be implementation in software or hardware; or using off-the-shelf components or custom microchips? What circuit topologies are the most suitable for use?

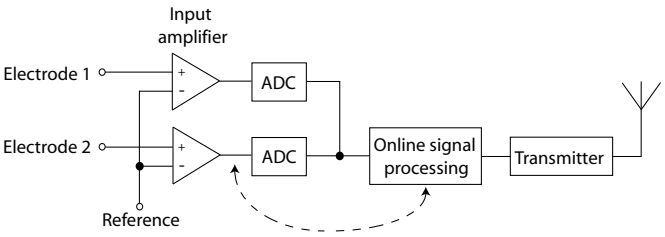

Fig. 1. A block diagram of a two-channel wireless physiological monitor consisting of: an input amplifier; an Analogue-to-Digital Converter (ADC); online signal processing; and a wireless transmitter. The online signal processing block could be implemented in either the analogue or digital domain, before or after the ADC.

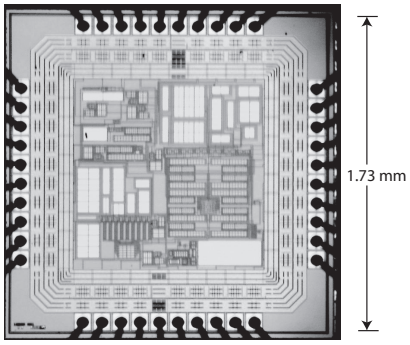

Fig. 2. A micro-photograph of an Application Specific Integrated Circuit (ASIC). Fully custom circuit design can result in the lowest possible device power consumption.

In general, hardware implementations using custom microchips, known as an Application Specific Integrated Circuits (ASICs), offer the lowest power consumption for implementing a given function. An example ASIC is illustrated in Fig. 2. The superior power performance is because in a custom device every aspect of the electronic circuit can be tailored for the wanted operation. However, this comes at the cost of a more complex and time consuming design, which is also more expensive.

Successful ASIC design will rely on having a highly integrated design flow. Beginning at the application level, robust and well verified algorithms are required. These must also have a low computational complexity for low power implementation. The algorithm complexity then sets the circuit topologies and approaches that are suitable for use. Some circuit topologies are more suitable than others due to their intrinsic robustness or power requirements. Only once

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all of these factors have been considered is the transistor level design possible.

Using the requirements of wearable EEG as an example we will demonstrate how ultra-low power signal processing circuits can be designed and verified. We will discuss the full range of ASIC design ranging from system architectures [2], [3] to the transistor level design [4], [5].

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