Multiplexing single electron transistors for application in scalable solid-state quantum computing

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Single electron transistors (SETs) are nanoscale electrometers of unprecedented sensitivity, and as such have been proposed as readout devices in a number of quantum computer architectures. The authors show that the functionality of a standard SET can be multiplexed so as to operate as both readout device and control gate for solid-state qubit systems based on charge localization and spin-charge transduction. Such multiplexing offers new possibilities for gate density reduction in nanoscale devices, and may therefore play a role in scalable quantum computer architectures.
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The single electron transistor[1] (SET) is a device that can act as an exquisitely sensitive electrometer. This sensitivity derives from precise control of the absolute charge state of a small metallic island, coupled via tunnel junctions to macroscopic leads. Since Fulton and Dolan's[2] initial experiments, SETs have been suggested for a diverse range of applications, from elements for classical logic[3] to single-photon detectors.[4] SETs are commonly suggested as readout mechanisms for quantum scale devices such as cellular automata[5] and quantum computers (QCs),[6] either via direct sensing of charge qubits[7–9] or of spin qubits after an initial spin to charge transduction process,[10–14] and this sensitivity has been routinely proven, e.g., Refs. 15 and 16.

Merely showing that SETs have the required sensitivity for qubit readout is not, however, sufficient for the development of a scalable quantum computer architecture. Of principle concern in this letter is the requirement for minimal gate density in the surface metal layer.[17] Standard designs for SETs usually have a relatively large footprint [e.g., $\gtrsim 10^4$ nm^2 (Ref. 18) such as in Fig. 1(a)], which with attendant control gates may be problematic in terms of spacing in the original Kane one-dimensional[10] and the scalable two-dimensional[19] QC architectures. Antenna structures[18,20,21] and further miniaturization may be of some assistance in packing in all the required elements, however, as the number of readout elements are increased from proof of principle devices to fully operational QCs, a degree of multiplexed functionality may be advantageous.

In this letter we show that any SET can be used for both qubit control and readout, reducing the number of electrodes required for the operation of the QC. Multiplexing in this manner suggests structures such as Fig. 1(b), where the placement of the SET gate above the source, island and drain minimizes the footprint of the device on the surface of the silicon substrate. Such "strip" SET designs, combined with multiplexed functionality, will benefit scalable QC design by allowing each SET to be used for both control and qubit readout. The particular miniaturized SET design shown represents a limit of the multiplexing idea in terms of fabrication and current detection. Beyond this illustrative example, it is the multiplexed functionality of SET design, in general, that we wish to focus on in this letter, leaving specifics of the scalable quantum computer design for a time when the required atomic precision of the qubits is achievable.

Although we explicitly consider a charge-based double quantum dot (QD) qubit system in our model, the results are applicable to spin qubits in that the process of spin-charge transduction requires a similar gate control and a charge localized readout. The qubit states correspond to the localization of a shared electron between one of two QDs. The circuit model for this SET-2QD system is shown in Fig. 1(c).

We work in the steady state regime where the current through the SET is modeled via energy minimization arguments of the entire system, following the orthodox theory of

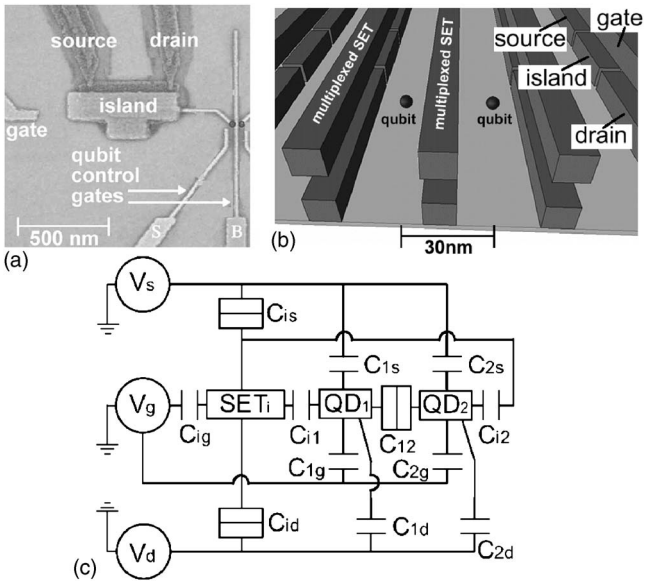

FIG. 1. (a) Example of conventional single electron transistor (SET) design. The large footprint will present difficulties in a scalable quantum computer. (Image taken from Ref. 18.) (b) Schematic of multiplexed SETs designed for minimizing gate density in a scalable quantum computer. (c) Circuit diagram for the SET coupled to two quantum dot (SET-2QD) system. The SET consists of three continuously variable voltage sources (source, drain, and gate), coupled to an isolated island. The source and drain are connected to the island by tunnel junctions, allowing for current flow through the SET. Isolated regions in which effects due to electron occupation number are critical have been indicated with boxes.

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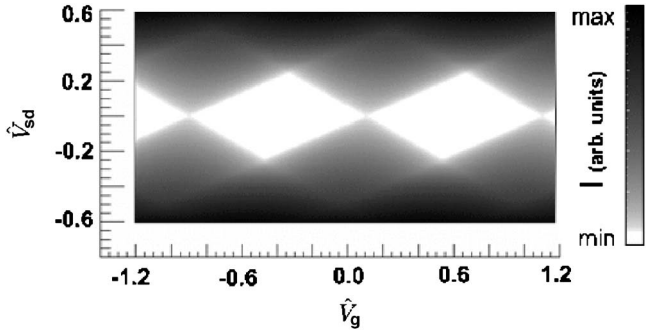

FIG. 2. SET current vs dimensionless gate voltage ($\hat{V}_g = V_g C_{ig}/e$) and source-drain potential difference ($\hat{V}_{sd} = V_{sd}(C_{is}+C_{id})/e$). Maxima occur when there is degeneracy in the energy of neighboring charge occupations on the island. In between these maxima the device is "blockaded" and sequential charge tunneling is suppressed. The diamond shapes produced by sweeping the voltage parameter space of the electrodes are indicative of SET behavior. Since the voltages on the electrodes do not uniquely determine the current, the SET can be multiplexed for both readout and control of qubits.

single electron tunneling.[1] SET readout consists of inferring the state of the qubit by the current through the SET. The current depends on the state of the qubit, and also on the potential differences between the SET island and any other electrodes capacitively coupled to it. In Fig. 2 we sweep the voltages on the SET electrodes in our circuit model, to produce the familiar Coulomb diamonds, indicative of SET behavior. In the interests of generality we have normalized the input voltages: $\hat{V}_g = V_g C_{ig}/e$, $\hat{V}_{sd} = V_{sd}(C_{is}+C_{id})/e$, where e is the magnitude of the electronic charge. Figure 2 shows that the SET current is not uniquely determined by the electrode voltages. Therefore, there is some freedom to choose the potentials on the SET source, drain, and gate electrodes to obtain a particular SET current, or alternatively to vary the SET current without affecting the rest of the circuit: this is the essence of the multiplexed functionality.

The behavior of mesoscopic circuitry is dependent on the interplay between the continuous variable given by the definition of capacitance, $C \equiv Q/V$, and the actual number of excess electrons on an isolated region of the circuit (SET island and QDs). We refer to the continuous variable as the virtual charge. The virtual charge induced on any isolated region is $\tilde{Q}_\alpha = \Sigma_\beta C_{\alpha\beta} V_\beta$. The full vector $\tilde{\mathbf{Q}}$ describing the virtual charge induced on each isolated region of the system is then $\tilde{\mathbf{Q}} = C_c \mathbf{V}$, where C_c is the correlation capacitance matrix describing capacitive coupling between the electrodes and quantized charge regions and $\mathbf{V}$ is the vector of electrode potentials. Labeling each QD with a numeric subscript we write

$$C_c = \begin{bmatrix} C_{is} & C_{id} & C_{ig} \\ C_{1s} & C_{1d} & C_{1g} \\ C_{2s} & C_{2d} & C_{2g} \end{bmatrix}, \quad \mathbf{V} = \begin{bmatrix} V_s \\ V_d \\ V_g \end{bmatrix}. \tag{1}$$

The total energy of the full system is

$$E = \frac{1}{2}\mathbf{Q}^T C_E^{-1} \mathbf{Q}, \tag{2}$$

where $\mathbf{Q}$ is a vector containing the virtual and actual charge on all isolated sections of the circuit (i.e. the island and QDs) and C_E is the "energy" capacitance matrix (defined below). The total charge is expressed as $\mathbf{Q} = \tilde{\mathbf{Q}} - \mathbf{n}q_e$, where $\mathbf{n}$ is a vector containing the excess electrons on each isolated region. C_E describes the cross capacitances of the QDs and the island and is given by

$$C_E = \begin{bmatrix} C_{i\Sigma} & -C_{i1} & -C_{i2} \\ -C_{1i} & C_{1\Sigma} & -C_{12} \\ -C_{21} & -C_{2i} & C_{2\Sigma} \end{bmatrix}, \tag{3}$$

where $C_{\alpha\Sigma}$ is the total capacitance of the α isolated region to all other objects in the system ($C_{\alpha\Sigma} = \Sigma_{m\neq\alpha} C_{\alpha m}$). The above relations allow the determination of the current through the SET for the full SET-2QD system for any voltage on the electrodes. We calculate the current based on a standard master equation approach and the materials and geometry of the SET design.[21]

The present limit to detectable SET currents is in the femtoampere regime.[22] We choose to scale the geometry of a SET in Fig. 1(b) to produce a minimal footprint such that the electrodes' height and width are 10 nm, and the tunnel junction barriers are 3 nm thick, while remaining above this limit. Such a scaling is conducive to current estimates of the size and spacing required for atomic-scale solid-state qubits in silicon, indicating that the structure of Fig. 1(b) is compatible with future scalable quantum computers. Reducing the resistance of the SET tunnel junctions will provide a commensurate increase in current without affecting the conclusions of this letter, for example, by using devices fabricated with overlapping junctions obtained by standard shadow mask evaporation techniques. Furthermore, an alternative fabrication method based on the use of scanning tunneling microscopes[23] indicates that structures of this scale are achievable.

The capacitive coupling between the leads of the SET (e.g., source and gate) may be problematic in this structure due to the slowing of the rise time ($t=RC$) of the voltages on the leads for qubit control. Our finite element modeling of the scaled geometry of Fig. 1(b) determines these cross-lead capacitances to be of the order of 10 aF. The operation speed for qubit control can therefore be maintained at an acceptable picosecond rise time for the voltages on the leads, so long as the resistance in the leads is of the order of kilohms. For the SET to perform readout of the qubit, the operation will need to be performed such that the variation in the current through the SET for the qubit being in each of its two states is a maximum. For control, the SET will need to be operated in regions where there is no current passing through the SET. We therefore sweep the parameter space of the SET electrode voltages, calculating the current through the SET for an electron being located on QD1, then QD2 in Fig. 1(c). We then take the magnitude of the difference in the current for each of these states ($|\Delta I_{12}|$), allowing us to determine the regions of the parameter space suitable for qubit readout, and those suitable for qubit control. Figure 3 displays this magnitude of the current variation as a function of the the normalized gate voltage ($\hat{V}_g$) and the normalized average of the potentials on the source and drain $\hat{V}_{\text{ave}} = (V_s+V_d)(C_{is}+C_{id})/2e$ (maintaining a constant source-drain bias).

The lines A, B, and C in Fig. 3 (and all lines parallel to them) are lines of constant inter-QD potential difference, with corresponding potential well diagrams shown. The paths were calculated using Eq. (2), noting that constant po-

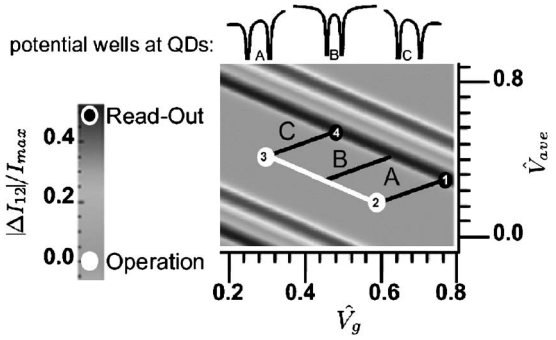

FIG. 3. Magnitude of the difference in current through SET for a single electron occupying QD1 or QD2 ($|\Delta I_{12}|$) in Fig. 1(c), normailzed to the maximum current through the device. Units are dimensionless: $\hat{V}_g = V_g C_{ig}/e$, $\hat{V}_{\text{ave}} = (V_s + V_d)(C_{is} + C_{id})/2e$. Following the path 1-2-3-4, the SET can be used to both readout and control the state of the qubit.

tential difference between the QDs is equivalent to a constant difference in induced charge. We term this axis the readout axis, as varying the control gates along this direction alters the readout sensitivity without changing the qubits. Conversely, we see that moving from point 2 to point 3 (or lines parallel) will alter the relative potential on the quantum dots, without affecting the SET readout signal. We refer to this axis as the control axis, as we can use this to control the double-dot potential without affecting the readout. These two axes are in some sense orthogonal, and the freedom to choose either constitutes the desired multiplexed functionality. In particular, note that moving along A, would result in measurement of the electron in the left-hand dot with high probability, and along path C, to measurement of the electron in the right-hand dot with high probability. Movement along path B would keep the electron in a superposition of left and right dots, and so in the quantum limit, the measurement outcome would be expected to show coherent tunneling oscillations. We have therefore the ability to control the logical state of the qubit with the SET itself.

We have shown that a full exploration of the parameter space for SET operation allows a SET to be operated as either a readout device or control gate independently. Such multiplexed functionality allows for a significant reduction in overall gate density, which we believe to be necessary for practical quantum computing. We have also presented a strip design SET at the limit of current detection, to further reduce gate densities, in anticipation of scalable solid-state quantum computing.

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