Barium Strontium Titanate Thin Films for Tunable Microwave Applications

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Declaration

I certify that except where due acknowledgement has been made, the work is that of the author alone; the work has not been submitted previously, in whole or in part, to qualify for any other academic award; the content of the thesis is the result of work which has been carried out since the official commencement date of the approved research program; and, any editorial work, paid or unpaid, carried out by a third party is acknowledged.

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Abstract

There has been unprecedented growth in wireless technologies in recent years; wireless devices such as cellular telephones and wireless local area network (WLAN) transceivers are becoming ubiquitous. It is now common for a single hardware device, such as a cellular telephone, to be capable of multi-band operation. Implementing a dedicated radio frequency (RF) front-end for each frequency band increases the component count and therefore the cost of the device. Consequently, there is now a requirement to design RF and microwave circuits that can be reconfigured to operate at different frequency bands, as opposed to switching between several fixed-frequency circuits.

Barium strontium titanate (BST) thin films show great promise for application in reconfigurable microwave circuits. The material has a high dielectric constant which can be controlled by the application of a quasi-static electric field, combined with relatively low losses at microwave frequencies. Tunable microwave components based on BST-thin films have the potential to replace several fixed components, thereby achieving useful size and cost reductions.

This thesis is concerned with the growth and microwave circuit applications of BST thin films on *c*- and *r*-plane sapphire substrates. Sapphire is an ideal substrate for microwave integrated circuit fabrication due to its low cost and low loss. Electronically tunable capacitors (varactors) were fabricated by patterning interdigital electrode structures on top of the BST films. High capacitance tunabilities of 56% and 64% were achieved for the films grown on *c*-plane and *r*-plane sapphire, respectively, at 40 V bias.

A novel electronically tunable 3 dB quadrature hybrid circuit was also developed. Prototypes of this circuit were initially implemented using commercial varactor diodes, in order to validate the design. An integrated version of the coupler was then fabricated using BST varactors on *c*-plane sapphire. The results achieved demonstrate the potential of sapphire-based BST thin films in practical microwave circuits.

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Glossary

ADS	Advanced Design System (Agilent)
AFM	Atomic Force Microscope
BPF	Bandpass Filter
BST	Barium Strontium Titanate
CCD	Charge Coupled Device
CSD	Chemical Solution Deposition
CMOS	Complementary Metal Oxide Semiconductor
CPW	Coplanar Waveguide
DC	Direct Current
DI	De-Ionised (Water)
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
FWHM	Full Width Half Maximum
GPS	Global Positioning System
GSG	Ground-Signal-Ground
HEMT	High Electron Mobility Transistor
IDC	Interdigital Capacitor
IP3	Third Order Intercept Point
IPA	Isopropyl Alcohol
ISM	International Scientific and Medical
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MEMS	Micro Electro Mechanical Systems
MMTC	Microelectronics and Materials Technology Centre

MOCVD	Metalorganic Chemical Vapour Deposition
OIP3	Output Third Order Intercept Point
PDMS	Polydimethylsiloxane
PLD	Pulsed Laser Deposition
PLZT	Lead Lanthanum Zirconate Titanate
PVD	Physical Vapour Deposition
RBS	Rutherford Backscattering
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMIT	Royal Melbourne Institute of Technology
SEM	Scanning Electron Microscope
SoS	Silicon on Sapphire
TEC	Thermal Expansion Coefficient
TMP	Turbomolecular Pump
UV	Ultraviolet
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integrated
VNA	Vector Network Analyser
WLAN	Wireless Local Area Network
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

Chapter 1

Introduction

1.1 Thesis Outline

This thesis is concerned with the deposition and integration of barium strontium titanate (BST) thin films for electronically tunable microwave circuits. The core objectives are to realise BST thin films with high dielectric tunability and low loss on single crystal c- and r-plane sapphire substrates, and to demonstrate these films in a microwave integrated circuit. Therefore, this thesis is somewhat multidisciplinary; the two major areas of investigation are in the fields of materials science and microwave engineering.

Chapter 2 provides an overview of the existing body of knowledge regarding BST thin films. The potential applications of BST thin films are surveyed, and problems which have so far limited the large scale commercialisation of BST are discussed. Important properties for BST microwave varactors are outlined, and these microwave parameters are correlated with the material properties of the films from which the varactors are realised.

The next two Chapters of the thesis concern the growth of high tunability BST films on single crystal sapphire substrates. In Chapter 3, a process developed at Royal Melbourne Institute of Technology (RMIT) University for $Ba_{0.5}Sr_{0.5}TiO_3$ growth on c-plane sapphire is presented. The process uses radio frequency (RF) magnetron sputtering for the film deposition, and post-deposition annealing is employed to achieve strain relieved films with high tunability. The influence of processing parameters (such as sputtering gas pressure and substrate temperature) during deposition on the materials properties of the films is investigated. Microwave variable capacitors, or varactors, are formed by electroplating low loss gold electrodes on the surface of the BST film. Single port reflection measurements on a vector network analyser (VNA) are then used to extract the microwave properties of the

varactors, including dielectric tunability and Q-factor. From these results, a mapping between the materials and microwave properties of the films is established, in order to achieve predictable microwave performance by controlling the processing conditions.

Chapter 4 presents the results of a collaboration with the Electroceramics Research Group at Rutgers University, New Jersey, USA. In this study, thin films of $Ba_{0.6}Sr_{0.4}TiO_3$ were grown on r-plane sapphire by pulsed laser deposition (PLD). The commercial silicon-on-sapphire (SoS) semiconductor process employs r-plane sapphire substrates. Therefore, there is the potential to integrate BST-based tunable microwave circuits with very large scale integrated (VLSI) digital baseband circuitry to realise a single-chip reconfigurable transceiver.

Microwave characterisation of the BST films on r-plane sapphire was then performed using the interdigital capacitor method introduced in Chapter 3. In a series of films with thickness ranging from 25 to 400 nm, the highest capacitance tunability of $\sim$64% was achieved with a 200 nm film. These results suggest that BST thin films could be integrated into the SoS process for tunable RF or mixed signal RF/digital integrated circuits.

The microwave circuit applications of BST thin films are considered in Chapter 5. A method for lowering the tuning voltage of BST varactors by decreasing the gap between the interdigital fingers is presented, and the nonlinear properties of the varactors are investigated. A novel, frequency agile 90° hybrid coupler design is also introduced. Prototypes were initially built using commercially available varactor diodes to validate the design. An integrated version of the tunable hybrid coupler was then realised using BST varactors and spiral inductors on a c-plane sapphire substrate. The end-to-end process, including BST deposition, lithography and packaging, was performed at RMIT University.

Chapter 6 provides a summary of the results achieved in this thesis. Opportunities for further work based on these outcomes are also presented.

1.2 Publications

1.2.1 Peer Reviewed Journal Publications

1. **E.A. Fardin**, A.S. Holland, and K. Ghorbani, "Electronically tunable lumped element 90° hybrid coupler," *IEE Electronics Letters*, vol. 42, no. 6, pp. 353-355, 2006.

2. **E.A. Fardin**, A.S. Holland, P. Reichart, and K. Ghorbani, "Enhanced tunability of magnetron sputtered $Ba_{0.5}Sr_{0.5}TiO_3$ thin films on *c*-plane sapphire substrates," *Applied Physics Letters*, vol. 89, no. 2, pp. 022901, 2006.

3. **E.A. Fardin**, E.K. Akdogan, W.K. Simon, A.S. Holland, J.Y. Wang, A. Safari, and K. Ghorbani, "Polycrystalline $Ba_{0.6}Sr_{0.4}TiO_3$ thin films on *r*-plane sapphire: Effect of film thickness on strain and dielectric properties," *Applied Physics Letters*, vol. 89, no. 18, pp. 182907, 2006.

4. G. Kostovski, A. Mitchell, A.S. Holland, **E.A. Fardin**, and M. Austin, "Nanolithography by elastomeric scattering mask: An application of photolithographic standing waves," *Applied Physics Letters*, vol. 88, no. 13, pp. 133128, 2006.

1.2.2 Peer Reviewed Conference Publications

1. **E.A. Fardin**, A.S. Holland and K. Ghorbani, "Low cost interdigital BST varactors for tunable microwave applications" in *Proc. IEEE TenCon*, Melbourne, Australia, Nov., 2005.

2. **E.A. Fardin**, A.S. Holland and K. Ghorbani, "A varactor tuned branch-line hybrid coupler," in *Proc. APMC*, vol. 3, Suzhou, China, Dec., 2005 pp. 1408-1411.

3. **E.A. Fardin**, A.S. Holland, K. Ghorbani, and B.F. Usher, "Structural and microwave characterization of magnetron sputtered $Ba_{0.5}Sr_{0.5}TiO_3$ films on *c*-plane sapphire substrates," in *Proc. Mater. Res. Soc. Symp.*, vol. 928, San Francisco, CA, Apr., 2006.

4. **E.A. Fardin**, A.S. Holland and K. Ghorbani, "Barium strontium titanate thin film varactors on r-plane sapphire," in *Proc. APMC*, Yokohama, Japan, Dec., 2006.

5. **E.A. Fardin**, A.S. Holland and K. Ghorbani, "Frequency agile 90° hybrid coupler using barium strontium titanate varactors," accepted for presentation, *IEEE MTT-S*, Honolulu, U.S.A., Jun., 2007.

1.3 Original Contributions

This thesis has resulted in a number of original contributions to the body of knowledge regarding BST thin films for microwave applications. A summary of these

contributions is provided below:

1. The structural properties of $Ba_{0.5}Sr_{0.5}TiO_3$ thin films grown on *c*-plane sapphire by RF magnetron sputtering were established. Processing conditions to achieve high dielectric tunability were also identified.

2. The thickness dependent dielectric and microwave properties of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown on *r*-plane sapphire by PLD were established. These results demonstrate the possibility of incorporating BST into the commercial SoS semiconductor process.

3. A novel frequency agile 90° hybrid coupler design was proposed and implemented using commercial semiconductor varactor diodes. An integrated version of this circuit was then implemented on *c*-plane sapphire, using BST varactors and on-chip inductors.

Chapter 2

Literature Review

2.1 Introduction and Motivation

During the last 10 to 15 years, there has been extraordinary growth in wireless technologies for the consumer market. Cellular phones, global positioning system (GPS) terminals and wireless local area network (WLAN) modems, for example, now sell in very high volumes to worldwide markets. Recent years have seen a trend of increasing integration. It is now relatively common for cellular handsets to be capable of operating at several different frequency bands, and for laptop computers to provide both Bluetooth and WLAN connectivity. This multi-band or multi-mode functionality means that several wireless transceivers are often required in a single hardware device.

Due to competition among suppliers, it is important to minimise the manufacturing costs of these devices, in order to maintain profit margins. Implementing several separate transceiver circuits in a single hardware device increases the component count and hence the overall cost [1]. Therefore, in terms of the RF front end circuitry, a significant cost savings can be achieved by using electronically tunable components. In this scenario, a single, tunable component is employed to replace several fixed components. For example, a bandpass filter (BPF) with a tunable passband could replace several fixed filters, or a tunable delay line could replace a set of fixed delay lines in the beamforming network of a phased array antenna. In a production line environment, electronically tunable matching networks could also be combined with an automated calibration system to reduce labour costs.

Electronically tunable capacitors, also called varactors, can be used to fabricate reconfigurable components for RF and microwave applications. Barium strontium titanate is of particular interest for tunable microwave devices, since it has a high dielectric constant that can be tuned by applying an electric field, and relatively low

loss at microwave frequencies. The high dielectric constant is useful for minimising the size of components fabricated from BST, leading to higher integration. Another useful property of BST is that the microwave dielectric properties can be tailored for specific applications by controlling the ratio of barium to strontium, according to the formula $Ba_xSr_{1-x}TiO_3$.

The established technology for microwave varactors is based on semiconductors, typically employing GaAs or silicon substrates. It is interesting to note a historical reference to the development of varactors in [2]: "At one time it seemed as if the voltage change of dielectric constant [in ferroelectric materials] would find application in voltage-tunable capacitors, but varactor diodes won the race." Therefore, varactor diodes are now a proven technology. Another advantage of varactor diodes fabricated on silicon substrates is that they are easily incorporated in the standard complementary metal oxide semiconductor (CMOS) integrated circuit process. However, BST varactors have some important advantages over semiconductor varactors, including higher power handling and lower cost [3]. It has also been shown that BST varactors have lower device losses than silicon-based varactors at frequencies above 10 GHz [4].

Micro Electro Mechanical Systems (MEMS) technology can also be used to fabricate varactors. The advantages of MEMS varactors include high power handling and low intermodulation distortion [5]. However, MEMS devices require careful packaging [6], and reliability is an issue due to the mechanical moving parts. Furthermore, MEMS devices have a lower tuning speed than both BST and semiconductor varactors [5].

It is also worth noting that BST thin films have been investigated for application in dynamic random access memories [7]. The high dielectric constant of BST can be used to reduce the size of dynamic random access memory (DRAM) storage cells, an important requirement for maintaining the current rate of increase in storage density into the future. This size reduction is also useful in microwave circuits, where the dimensions of on-chip direct current (DC) blocking capacitors could be significantly reduced by employing BST as the dielectric instead of conventional SiO_2 or Si_3N_4 dielectric films.

The two parameters that need to be optimised in BST thin films for microwave applications are the capacitance tunability and the Q-factor (the reciprocal of the loss tangent, $Q = 1/\tan\delta$), which should both be as high as possible. Many factors related to the device fabrication, including the substrate material, the substrate temperature during deposition, and residual strain in the BST film, among many others, affect the microwave properties of BST varactors. Therefore, it is very important to

understand the relationship between the material and microwave properties of the devices, in order to optimise the performance of BST-based microwave components.

This Chapter provides a review of BST thin films for microwave applications. An overview of the physical properties of BST bulk materials and thin films is presented, followed by a survey of the various deposition techniques which can be used to grow BST thin films. Next, a review of the existing research into BST thin films for microwave circuit applications is presented. Also, the structural properties of single crystal sapphire are introduced, since the BST films prepared as part of this thesis work were deposited on c- and r-plane sapphire substrates. Finally, based on the existing work, opportunities for further investigation are identified.

2.2 BST Material Properties

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BST is essentially a solid solution of $BaTiO_3$ and $SrTiO_3$. $BaTiO_3$ is in the ferroelectic (polar) phase at room temperature, and has a ferroelectric to paraelectric transition temperature (Curie point) of 130°C , while $SrTiO_3$ is paraelectric (non-polar) down to absolute zero [8]. In the BST solid solution, substitution of Sr atoms in the place of Ba atoms causes the Curie point to decrease linearly. Data by Jaffe, Cook and Jaffe [8] suggests that the Curie point of BST drops to 0°C with ∼34% Sr content, corresponding to a decrease of 3.8°C per molar percent Sr.

Both $BaTiO_3$ and $SrTiO_3$ have the perovskite crystal structure, shown in Fig. 2.1 for $BaTiO_3$. Therefore, as expected, BST is also a perovskite. In general, perovskites have the chemical formula ABO_3, where A is usually an alkaline earth or a larger lanthanide, and B is usually a transition metal or a smaller lanthanide [9]. In the case of BST, Ba and Sr atoms occupy the A site, while Ti atoms occupy the B site.

The dielectric constant of BST is tuned by applying a quasi-static electric field to the material. Under an applied field, the central Ti atom in the BST unit cell is displaced from its zero field position in the central TiO_6 octahedron [10]. This displacement decreases the dielectric constant. The amount of displacement (and therefore the tunability) is affected by many factors, including temperature, Ba/Sr ratio, and residual strain in the BST film.

A high dielectric permittivity of roughly 100-20000 can be obtained with BST material [4]. In bulk materials (single crystals or ceramic powder samples), the dielectric constant is strongly temperature dependent, with a sharp peak at the Curie point. Thin films generally have a lower, less temperature dependent permittivity than bulk materials, as illustrated in Fig. 2.2. The smaller temperature dependence

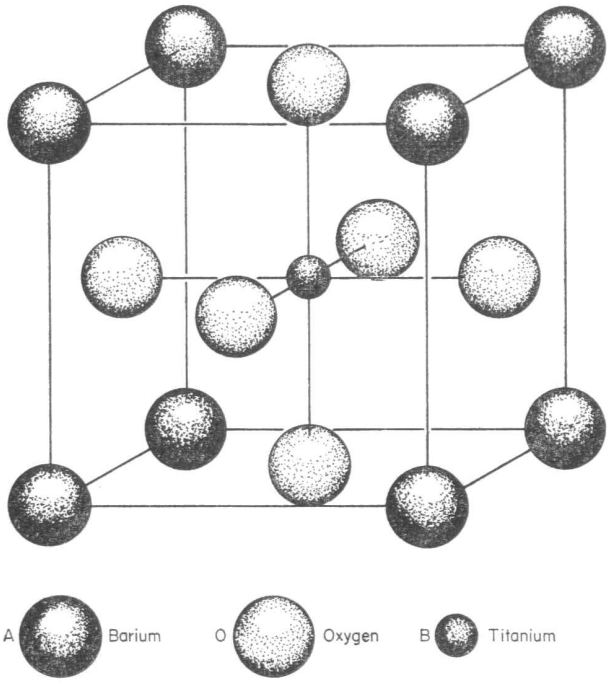


Figure 2.1: Perovskite structure of $BaTiO_3$ [8].

of permittivity in thin films is desirable, because it means that electronic components fabricated from these films are more likely to maintain their performance over a wide operating temperature range. The lower permittivity in thin films can be attributed to small grain size, interfacial capacitance, and residual stress [11]

For microwave applications, it is generally suggested that BST thin films should be in the paraelectric phase at room temperature. In the paraelectric phase, BST has simultaneously high tunability and relatively low dielectric loss at microwave frequencies [12]. At room temperature the paraelectric phase can be achieved by adjusting the chemical composition so that $x \leq 0.7$ in $Ba_xSr_{1-x}TiO_3$. In the ferroelectric polar phase, BST is also piezoelectric, and dielectric losses are associated with mechanical damping caused by domain wall motion [8]. This results in high dielectric loss at microwave frequencies.

However, the paraelectric phase of the dielectric may not always be required for tunable microwave devices [13]. In [13], measurements of the high frequency tunability and Q-factor of piezoelectric $Na_{0.5}K_{0.5}NbO_3$ film were presented. It was found that the domain wall movements do not contribute strongly to microwave losses at millimetre wave frequencies. At 40 GHz, a high Q-factor (for this frequency) of $\sim$20 was achieved; however, at 2 GHz, $Q \ll 10$. Therefore, for this material, the Q-factor increases with frequency, while $Q \propto 1/f$ in semiconductor varactors. Based

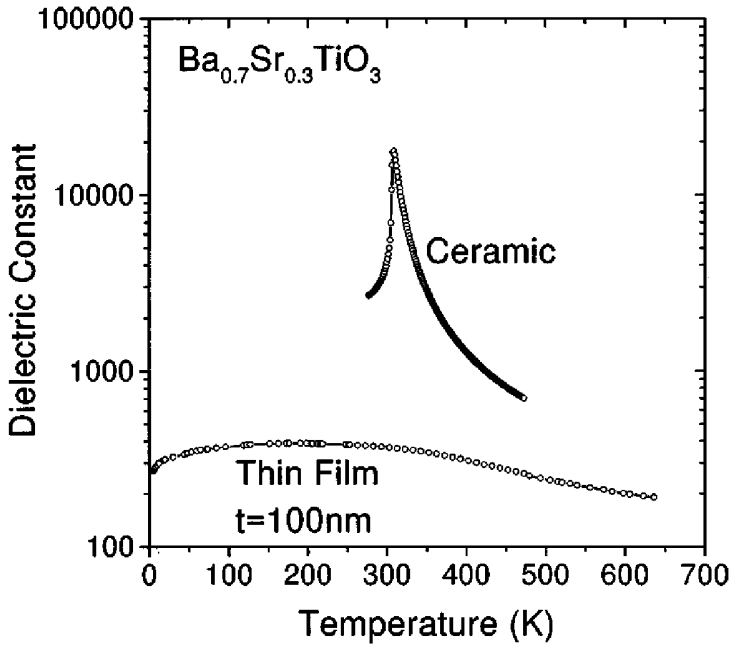


Figure 2.2: $Ba_{0.7}Sr_{0.3}TiO_3$ bulk and thin film dielectric constant as a function of temperature [11].

on these results, it appears that the paraelectric phase of BST should be used for microwave devices operating below 10 GHz, while the ferroelectric phase should be considered at higher frequencies.

There are a number of factors which contribute to the dielectric loss of BST films at microwave frequencies. The total loss is composed of contributions from intrinsic (present in a perfect BST crystal) and extrinsic (associated with defects) mechanisms [14]. There are three main intrinsic loss mechanisms in BST, namely, the three quantum, four quantum and quasi-Debye mechanisms [12]. The extrinsic losses are derived from charged defects, the universal relaxation law mechanism and a quasi-Debye mechanism associated with material defects [12].

Many reports on the microwave properties of BST thin films, for example [13, 15–17], show a trend of decreasing loss tangent ($\tan\delta$) with increasing DC bias field. The opposite situation has been observed in paraelectric single crystals, where the dielectric loss increases under an applied bias field [18]. There are some exceptions to the trend observed in thin films; for example, in a $Ba_{0.25}Sr_{0.75}TiO_3$ thin film, $\tan\delta$ increased between 0 and 10 GHz and decreased between 10 and 45 GHz at 700 kV/cm bias, relative to the zero-bias value [14]. The authors attributed this behaviour to the launching of acoustic waves within the device.

In general, microwave dielectric losses are higher in BST thin films than in the

equivalent bulk materials. This is illustrated in Fig. 2.3 for a $Ba_{0.25}Sr_{0.75}TiO_3$ thin film and a BST single crystal of virtually the same composition. Since the loss is much lower in the single crystal, the loss mechanisms in the thin film must arise from the extrinsic mechanisms discussed above. It is suggested that the dielectric loss of BST films at microwave frequencies can be reduced by minimising the density of oxygen vacancies in the film [14].

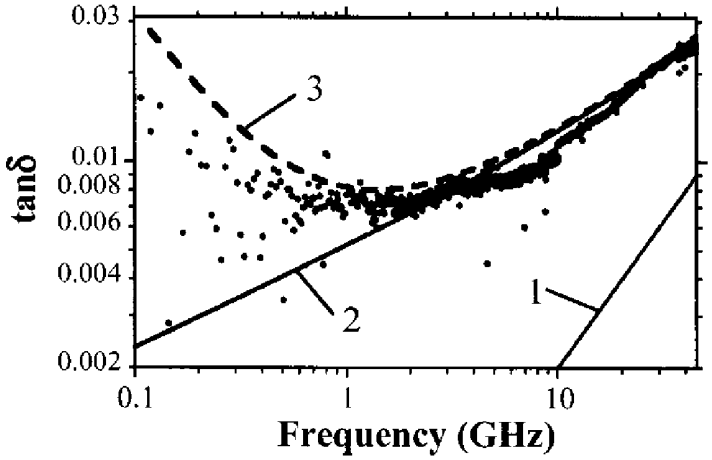


Figure 2.3: Frequency dependent loss tangent of $Ba_{0.25}Sr_{0.75}TiO_3$ thin film varactor at 0 V bias. The loss tangents of a $Ba_{0.23}Sr_{0.77}TiO_3$ single crystal – 1, BST film with charged defects – 2, and BST film with charged defects and Si substrate loss – 3 are also shown [14].

Strain can greatly alter the physical properties of a thin film from those observed in the equivalent single crystal material. Recently, for example, it was shown that tensile in-plane induced in a $SrTiO_3$ thin film by epitaxial growth on a $DyScO_3$ substrate resulted in ferroelectric behaviour at room temperature [19]. As noted above, bulk $SrTiO_3$ normally remains paraelectric down to 0 K. Therefore, strain can be used to control the ferroelectric-paraelectric transition temperature in BST films, and therefore also the microwave properties of the film.

The relationship between the physical properties and strain in ferroelectric films is explained by the Landau-Devonshire phenomenological theory [20]. A paper by Pertsev et al. [21] presents the phase diagrams of $BaTiO_3$ and $PbTiO_3$ epitaxial thin films as a function of temperature and misfit strain. The misfit strain arises from the lattice mismatch between the film and the substrate, and is defined as $u_m = (b - a_o)/b$, where b and a_o are the substrate and film lattice parameters, respectively. These theoretical results demonstrate that the strain imposed by the substrate leads

to the appearance of phases (polarisation states) in the thin film which are not present in the bulk material. Ban and Alpay [20, 22] extended these results to BST thin films, and demonstrated a link between misfit strain and tunability. It was also shown that the film thickness affects the misfit strain, and therefore the tunability [20, 22].

There are a number of factors contributing to residual strain in BST thin films. These include lattice mismatch between the BST material and the substrate on deposition, thermal mismatch that occurs when cooling the sample from the deposition to room temperature, and film contraction resulting from the compensation of oxygen vacancies in the film during annealing [23]. X-ray diffraction (XRD) provides a convenient, non-destructive means to measure the stress/strain in thin films [24]. Raman spectroscopy is also a useful tool for observing strain-induced shifts of phase transitions in BST thin films [25].

2.3 BST Thin Film Deposition

Several techniques are available for the deposition of BST thin films. These include physical vapour deposition (PVD), chemical vapour deposition (CVD) and sol-gel processing. A brief outline and some references to existing work are provided below, followed by a summary of the advantages and disadvantages of each approach.

There are numerous reports in the literature of BST films prepared by sputtering [10,25–38] and PLD [39–50]. Both of these techniques are part of the PVD family of methods. The key characteristics of the PVD process relevant to sputtering and PLD include: [51]

1. Reliance on solid source material (target).
2. Physical mechanisms (collision impact in the case of sputtering and laser excitation in the case of PLD) by which source atoms enter the gas phase.
3. A vacuum atmosphere through which the gaseous species are transported.

Sputtering and PLD are the most common deposition methods employed by research groups investigating BST thin films.

Substantial work has also been done with BST films prepared by metalorganic chemical vapour deposition (MOCVD) [7, 52–56]. In the MOCVD process, liquid phase metalorganic precursors containing Ba, Sr and Ti are mixed and delivered to a reactor via a temperature controlled flash vapouriser [54]. Since all of the constituents are in the vapour phase, gas flow rates and partial pressures can be

precisely adjusted using mass flow controllers [51]. Other related CVD methods, including liquid-delivery-source CVD [57] and combustion CVD [58] have also been successfully employed for BST film growth.

Growth Method	Advantages	Limitations
Solution		
Sol-Gel and Chemical Solution Deposition (CSD)	• Inexpensive • Rapid turnaround and sampling	• Phase control • Composition Control • Morphology • Reproducibility • Scalability
Energetic		
Sputtering	• Uniformity • Scalability • Low thermal budget	• Point defect concentrations • Limited compositional control • High residual stresses • Poor conformality
Pulsed Laser Deposition (PLD)	• Rapid sampling • Quickly produce new materials	• Morphology (bouldering) • Point defect concentration • Scalability • Uniformity • High residual stresses
Vapour		
Metal Organic Chemical Vapour Deposition (MOCVD)	• Uniformity • Morphology • Composition control • Low thermal budget • Scalability • High conformality	• Expensive • Precursor availability • Precursor stability • *Still a relatively immature technology*

Table 2.1: Comparison of different techniques for BST thin film deposition [59].

Sol-gel processing has also been used to prepare BST thin films [60–62]. The first steps in the sol-gel process are to prepare an appropriate solution containing the constituent elements of BST, and then to polymerise the solution to form a gel [61]. Thin films are then prepared by spin coating the solution onto a substrate, drying, thermal decomposition, and in some cases, annealing [63].

Regardless of the deposition method, a high substrate temperature (typically

650 to 800°C) is required to form the perovskite phase of BST. This means that the deposition system must be equipped with a high temperature substrate heater and temperature controller. Sol-gel processing is an exception, since crystallisation of the BST film can be achieved by annealing the spin coated film [61]. The high temperature processing is a challenge, since the BST layer must be grown before depositing any layers of material with a melting point below the BST deposition temperature.

The advantages and disadvantages of the main BST thin film growth techniques are compared in Table 2.1 [59]. While MOCVD offers many advantages, it is an expensive and relatively new technique that is not widely available in university research labs. Sputtering and PLD systems are lower in cost, and have been successfully employed by research groups around the world to produce high quality BST films. Residual strain in BST films produced by these techniques can be controlled by varying the film thickness [64] and by post-deposition annealing [23].

2.4 BST Thin Films for Microwave Circuit Applications

Tunable microwave components based on BST thin films typically rely on varactors as the tunable circuit element. To fabricate varactors from BST films, a set of electrodes is required, both to connect the component to the external circuit, and to apply a quasi-static bias field to control the dielectric constant of the BST material. In most cases, a single set of electrodes serves both purposes simultaneously. The two most common approaches are to locate the BST film between parallel plate top and bottom electrodes, and to fabricate a set of interdigital electrodes on top of the BST film. This Section contains a description of the interdigital and parallel plate varactor implementations. A summary of the existing work with BST for microwave circuit applications is also provided.

2.4.1 Interdigital Varactor Implementation

An interdigital BST varactor is shown schematically in Fig. 2.4. In this device architecture, the BST film is normally deposited directly on a low loss substrate, and the electrode metallisation is patterned on top of the BST film. With interdigital varactors, the minimum gap between the electrodes is limited to approximately 1 to 2 μm, using standard photolithographic tools available in most university laboratories. Note that this is a fabrication limitation, rather than a functional require-

ment of the devices. The dielectric constant of the BST film is tuned by applying a DC bias between the interdigital electrodes. In these devices, the capacitance tunability $T_C(V) = [C(0) - C(V)]/C(0)$ is smaller than the dielectric tunability $T_\epsilon(V) = [\epsilon(0) - \epsilon(V)]/\epsilon(0)$ since part of the electric field is in air [13].

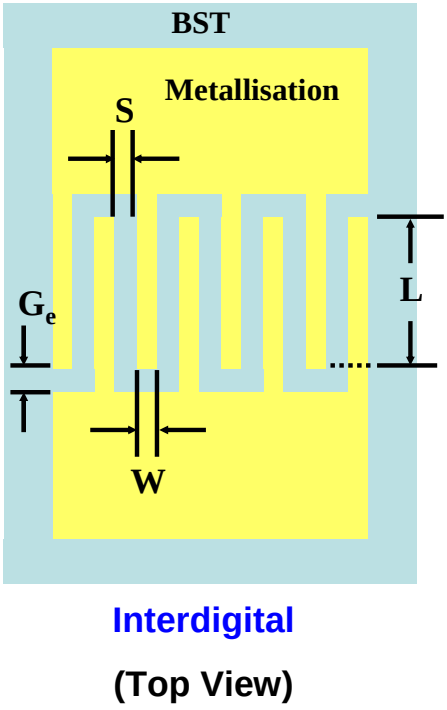


Figure 2.4: Schematic diagram of an interdigital BST varactor.

To minimise the conductor losses, the interdigital electrodes should be made from a highly conductive metal, such as Cu or Au, and the thickness of the metal should be more than one skin depth at the desired frequency of operation. The discussion of the losses in BST films in Section 2.2 did not take into account the effect of the metal electrodes. For a BST-based microwave varactor, the total device loss includes contributions from both the BST film and from the electrode metallisation.

The Naval Research Laboratory in the United States was one of the first groups to investigate BST thin films for microwave applications [23, 43, 46, 60]. This work is based on interdigital varactors and cubic, single crystal substrates. Since, for interdigital varactors, the BST film is deposited directly on the substrate, epitaxial growth is possible by choosing a lattice-matched substrate. Table 2.2 [23] gives the material data for MgO and $LaAlO_3$ substrates and $Ba_{0.5}Sr_{0.5}TiO_3$ bulk material. As can be seen from the a values in the Table, BST is well lattice matched to MgO

	MgO	**$LaAlO_3$**	**Bulk BST** ($x = 0.5$)
a [Å]	4.213	3.787	3.947
$\alpha[10^{-6}/^{\circ}C]$	13.8	10.0	10.5

Table 2.2: Lattice parameters and thermal expansion coefficient (TEC) data for MgO, $LaAlO_3$ and $Ba_{0.5}Sr_{0.5}TiO_3$ [23].

and $LaAlO_3$. Therefore heteroepitaxial BST films can be grown on these substrates, and there are many studies of the properties of <100> oriented BST films grown on <100> oriented MgO and $LaAlO_3$ [29, 42–48]. Heteroepitaxial <110> BST films have also been successfully grown on <100> $NdGaO_3$ substrates [40].

Many factors contribute to residual strain in BST films, as discussed in Section 2.2. The lattice misfit results in tensile strain in the case of MgO substrates (due to the larger lattice parameter of MgO than BST) and compressive strain with $LaAlO_3$ (since $LaAlO_3$ has a smaller lattice parameter than BST) [44]. Since BST has a smaller thermal expansion coefficient (TEC) than MgO (Table 2.2), cooling to room temperature after deposition compresses the BST film [23]. Therefore, the choice of substrate can affect the strain state, and therefore the tunability of epitaxial BST thin films [22].

2.4.2 Parallel Plate Varactor Implementation

A schematic diagram of a parallel plate BST varactor is shown in Fig. 2.5. The bias field is applied across the thickness of the film (approximately 50 to 500 nm), resulting in a lower bias voltage requirement for a given capacitance tunability in parallel plate devices compared to interdigital devices. For parallel plate varactors, the dielectric tunability $T_\epsilon(V)$ is similar to the capacitance tunability $T_C(V)$ [13].

An advantage of the parallel plate approach is that a cheap Si wafer can be used (instead of the more expensive $LaAlO_3$ or MgO substrates). Because the lattice constants of Pt and BST are very similar, and Pt has low reactivity, Pt electrodes are often used in parallel plate BST varactors [65]. Parallel plate devices on Si with good performance have been demonstrated at Chalmers University of Technology, Sweden [4, 14, 66]. Varactors with a capacitance tunability of 40 % and Q-factor of 40 at 45 GHz were reported by the group [66]. In this work, an oxidised high resistivity (ρ = 5 kΩcm) Si substrate was employed to minimise substrate losses. A $Ba_{0.25}Sr_{0.75}TiO_3$ film was grown by PLD on a Pt(50 nm)/Au(500 nm)/Pt(100 nm)/TiO_2(15 nm) bottom electrode stack, where

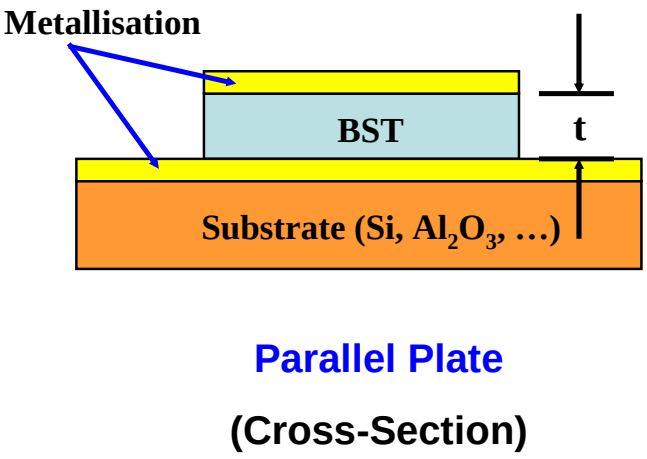


Figure 2.5: Schematic diagram of a parallel plate BST varactor.

the purpose of the thick gold layer was to minimise conductor losses. Top electrodes were formed by depositing Au(500 nm)/Pt(50 nm) on top of the BST layer.

There are some difficulties with building BST devices on a Pt/Si substrate, mainly due to the high temperature requirement for BST deposition. It has been shown that hillocks can form in Pt layers on Si during high temperature processing, due to the different TECs of Pt ($9\times10^{-6}/°$C) and Si ($2.5\times10^{-6}/°$C) [67]. This can lead to shorted devices [5], lowering the yield of working devices per wafer. Also, compared to interdigital devices, fabrication is more complicated, since the BST film needs to be etched to expose the bottom electrode in the parallel plate architecture. The bottom electrode may also need to be pre-patterned before deposition of the BST film.

High performance parallel plate BST varactors on *c*-plane sapphire substrates have been developed by the University of California at Santa Barbara [5, 68–70]. Sapphire has a TEC of $6.0\times10^{-6}/°C$, which provides a better match with Pt and lowers the possibility of hillock formation [59]. Sapphire also has a very high resistivity compared to standard silicon, which means that low loss microwave transmission lines can be realised. The device layout of the University of California varactors is shown in Fig. 2.6 [5]. The base electrode is fabricated from Pt(100 nm)/Au(100 nm)/Ti(50 $\AA$). Next, the BST film (∼200 to 300 nm) is deposited, followed by thin metal layers Au(500 nm)/Pt(100 nm). An upper thick metal layer of Au(1.2 μm)/Ti(10 nm) helps to minimise conductor losses. These devices had a Q-factor of ∼ 25 at 10 GHz and a capacitance tunability of 60%.

Several other groups have investigated parallel plate BST varactors for microwave

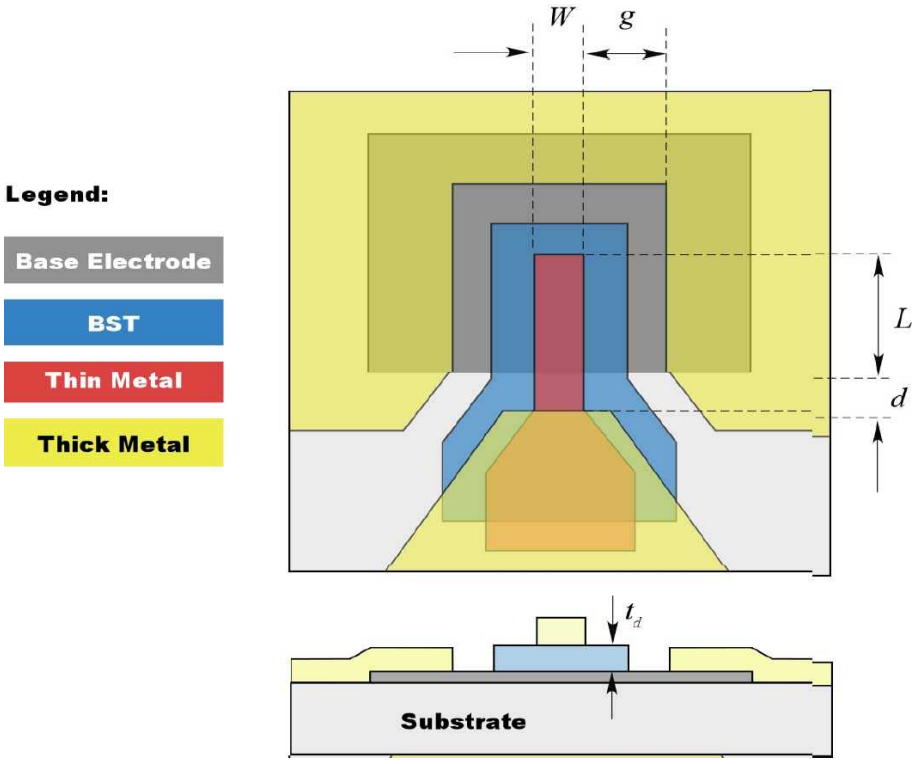


Figure 2.6: Layout of parallel plate varactor with pre-patterned bottom electrode [5].

applications [30, 34, 49, 50, 52]. A limitation of parallel plate devices is that the electrode metallisation contributes more to the device losses than in the case of interdigital varactors [12]. This problem is compounded by the high deposition temperature, which means that refractory metals (such at Pt) with limited conductivity are required for the base electrode [71].

2.4.3 Microwave Circuit Applications

There are several reports of the application of both interdigital and parallel plate BST varactors in electronically tunable microwave circuits. Potential applications include phase shifters, filters, matching networks and voltage controlled oscillators (VCOs) [6]. The results that have been achieved so far demonstrate the potential of employing BST thin films in microwave integrated circuits.

Phase shifters can be realised by periodically loading a transmission line with varactors, as shown in Fig. 2.7. A coplanar waveguide is often used, with the varactors placed between the centre conductor and the ground planes on either side. Very good performance was achieved in a phase shifter employing the parallel plate BST varactors developed at the University of California [5]. The phase shifting range was 0° to 250° at 10 GHz with an applied bias of 0 to 17.5 V, as shown in

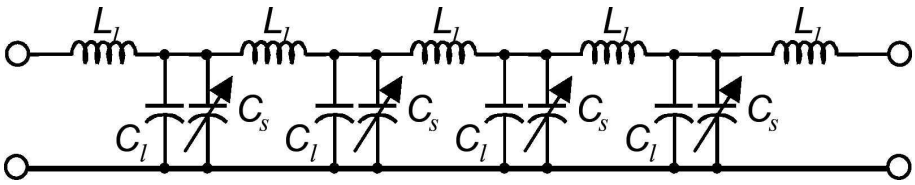


Figure 2.7: Equivalent circuit model of a varactor loaded transmission line phase shifter [71].

Fig. 2.8. The maximum insertion loss was 3.1 dB at 10 GHz and 0 V bias.

Coplanar waveguide phase shifters using interdigital varactors on (100) MgO substrates have been developed at the Electronics and Telecommunications Research Institute in Korea [72, 73]. An X-band phase shifter showed a phase shifting range of 153° at 10 GHz with an applied bias of 0 to 40 V; the maximum insertion loss was 11.6 dB [72]. A K-band phase shifter demonstrated a phase shift of 179° at 20 GHz and 200 V bias; in this case, the maximum insertion loss was 5.6 dB [73]. Similar results were achieved at Chalmers University in Sweden with a BST film deposited on a high resistivity Si substrate [74].

An alternative to the varactor loaded transmission line phase shifter is the reflection type phase shifter. A BST-based prototype was developed at the Georgia Institute of Technology in the United States [3]. In this circuit, shown in Fig. 2.9, a phase shift is achieved via tunable reflective terminations on a quadrature hybrid coupler. The measured results are shown in Fig. 2.10. A phase shifting range of

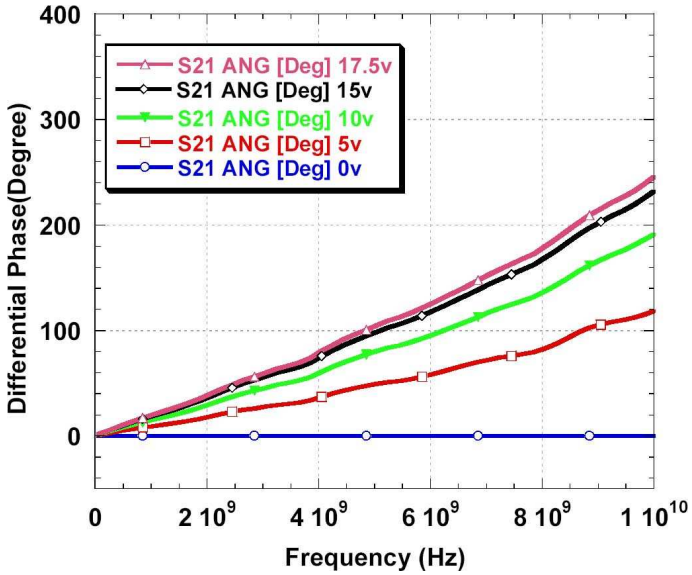


Figure 2.8: Bias voltage dependent phase shift of a BST varactor loaded coplanar waveguide phase shifter [5].

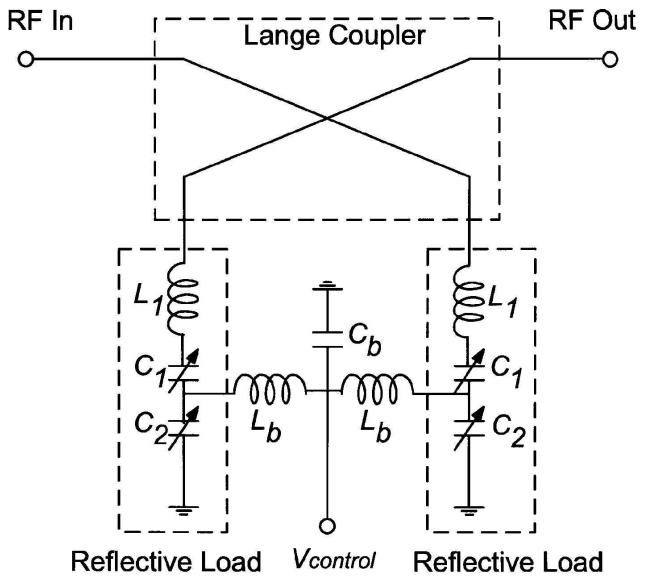


Figure 2.9: Schematic diagram of a reflection-type phase shifter [3].

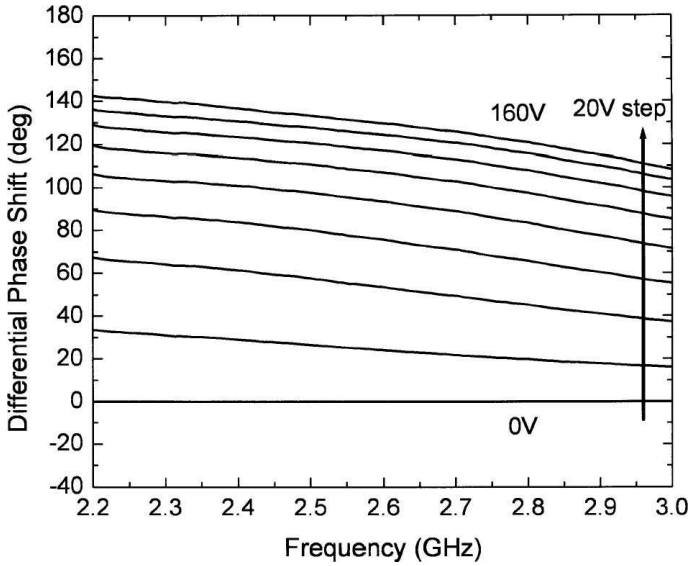


Figure 2.10: Measured differential phase shift of a reflection-type phase shifter with folded-type Lange coupler [3].

130° at 2.5 GHz was achieved with 160 V bias; the insertion loss better than 2.3 dB.

Several other BST-based phase shifters have been proposed and/or demonstrated. These include phase shifters using BST thick films [75, 76], a digital-analog phase shifter [77] and phase shifters with a SiO_2 layer between the coplanar waveguide metallisation and the BST film to reduce dielectric losses [78, 79]. BST phase shifters have also been employed to provide adaptive nulling of interfering tones in

a cellular band duplexer [80].

Electronically tunable filters have been implemented using BST varactors. Bandpass filters operating in the 4 to 5 GHz range were demonstrated in [81], while lowpass and bandpass filters operating in the 100 to 300 MHz range were demonstrated in [6]. A drawback of these tunable filters is the low third order intercept (IP3), +19 dBm in [6]. This would limit use of the filters to low power receive applications.

BST thin films have also been employed to realise reduced size DC blocking capacitors in a C-band oscillator circuit [82]. Tunable impedance matching networks were proposed for single-ended [83] and balanced [84] amplifier designs. Integrated tunable matching networks have also been demonstrated in [5, 85]. Therefore, while there are many examples of phase shifters using BST varactors, there are several other potential applications for BST thin films in microwave circuits.

2.5 Sapphire Single-Crystal Substrates

Sapphire has very low dielectric loss at microwave frequencies ($\tan \delta = 1\times10^{-4}$ at 10 GHz) [86] and a high dielectric constant, which helps to reduce the dimensions of distributed microwave components, including transmission lines, capacitors and inductors. Also, sapphire does not suffer from surface deliquescence as does MgO [87], whereby the surface finish is damaged by exposure to moisture during processing. These properties, combined with the relatively low cost of sapphire compared to MgO and $LaAlO_3$ [5] make it an ideal substrate for microwave integrated circuits.

The BST films grown for this thesis were deposited directly on single crystal sapphire substrates. Sapphire was chosen not only because of its excellent physical properties, but also because there are few reports of BST thin films grown on sapphire. Research into BST thin films at the University of California employed sapphire substrates, but was largely based on parallel plate varactors, with the BST film deposited on a Pt bottom electrode [5, 69, 70]. There was also limited investigation of BST thin films deposited directly on sapphire by the University of California research group [68, 88]; however, these devices had a relatively low capacitance tunability of ∼43% with a high bias field of 900 kV/cm [88]. BST thin films deposited directly on sapphire were also investigated at the Georgia Institute of Technology [3, 16, 89–92]. Using a proprietary combustion chemical vapour deposition process [58], an improved tunability of 64% at 350 kV/cm was achieved with interdigital varactors fabricated from these films [90]. However, there was little investigation of the material properties of these films, such as crystal structure and residual strain, and their influence on the microwave properties of the films.

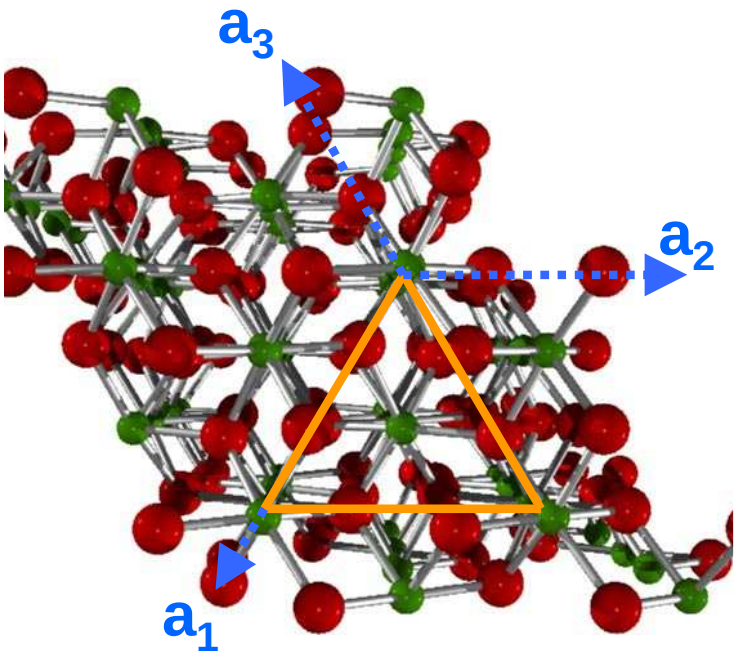


Figure 2.11: Ball and stick model of a sapphire crystal, viewed along the c-axis [93]. One-sixth of the basal plane of the hexagonal unit cell is highlighted in orange; $\mathbf{a}_i$ are the basal vectors of the unit cell.

Therefore, further investigation of the microwave properties of BST films deposited on sapphire substrates is warranted.

Sapphire belongs to the $R\bar{3}3$ crystal space group, and can be described by a hexagonal structural unit cell [94]. A ball and stick model of the sapphire crystal lattice is shown in Fig. 2.11. The green balls represent aluminium (Al) atoms, and the red balls represent oxygen (O) atoms. In Fig. 2.11, one-sixth of the top face of a hexagonal unit cell is highlighted in orange.

Two of the most widely available sapphire substrate orientations are c-plane and r-plane, where c and r denote the orientation of the substrate surface with respect to the hexagonal unit cell. The three-index Miller system of the form (hkl) is followed throughout this thesis to describe BST and sapphire crystal structure. A four-index Miller-Bravais indices of the form $(hkil)$ can also be used to describe the hexagonal structure of sapphire, where i is determined by h and k according to [95]

$$h + k = -i \tag{2.1}$$

The Miller indices for the c and r crystallographic planes are (001) and (102), respectively. Figure 2.12 shows the orientation of these crystallographic planes in the hexagonal unit cell. In the case of c-plane sapphire, the (001) plane is the growth surface for BST, while, for r-plane sapphire, the (102) plane is the growth surface.

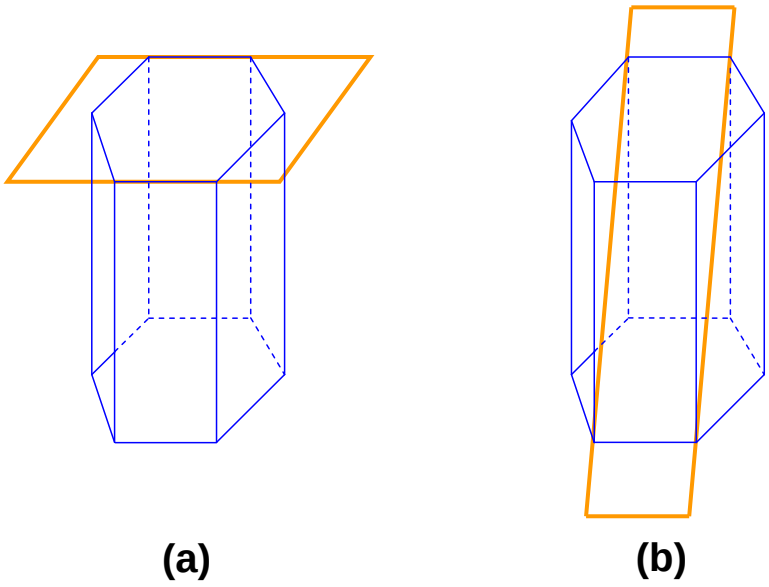


Figure 2.12: Orientation of (a) c-plane and (b) r-plane in the sapphire hexagonal unit cell.

2.6 Conclusions

There have been a significant efforts by several research groups to develop tunable microwave components employing BST thin films. The potential for employing BST in tunable microwave components has been recognised for many years; for example, a phase shifter using bulk BST was developed over 40 years ago [96]. Research in the past decade or so has focussed on developing BST thin films, rather than bulk materials, since thin films are more suitable for microwave integrated circuit applications. Thin films of BST have physical properties which are significantly different to those of bulk, single crystal BST. In particular, a lower dielectric constant and higher dielectric losses are observed in thin films compared to the bulk material. These differences need to be taken into account when designing microwave components employing BST thin films.

There are several techniques available for the deposition of BST thin films. Sputtering and PLD are the two most popular methods, due to the wide availability of these systems in university research labs. The sol-gel method has also been used for BST thin film preparation, with the main advantage being that a vacuum system is not required. However, there are problems with the composition control and reproducibility which make this approach less attractive. MOCVD can also be used to deposit high quality BST thin films; however, the equipment required is expensive

and is not widely available in university research labs.

Tunable microwave circuits based on BST thin films generally employ either interdigital or parallel plate varactors. In either case, a DC electric field controls the permittivity of the BST layer, and therefore the capacitance of the device. Varactors based on BST thin films require a high dielectric (and therefore capacitance) tunability; low dielectric losses at microwave frequencies are also important. Optimisation of these parameters can be achieved by understanding the relationship between the materials and microwave properties of the films.

Several research groups have demonstrated tunable microwave circuits employing BST thin films. There are many reports of coplanar waveguide and reflection-type phase shifters. Tunable filters, matching networks and VCOs with integrated BST films have also been reported. These results demonstrate the great potential of BST thin films in phased array antennas and in microwave integrated circuits for consumer applications such as WLAN transceivers and cellular handsets. The study of BST thin films for tunable microwave circuit applications remains an active research topic.

Residual strain in BST films has a strong influence on the tunability, with maximum tunability achieved at zero strain. Strain in the film can be minimised by depositing the BST film on a lattice-matched substrate. Films grown on MgO, $LaAlO_3$ and Pt, which provide a good lattice match to BST, have been thoroughly investigated. The relationship between the materials and microwave properties of BST grown on sapphire substrates has not been studied in detail. This, combined with the excellent microwave properties and low cost of sapphire substrates, presents an opportunity for further investigation.

An important focus of this thesis is on understanding the relationship between the material and microwave properties of BST thin films on single crystal sapphire substrates. BST films are grown on both c- and r-plane sapphire, as these substrate orientations are readily available from commercial suppliers. The influence of the deposition conditions on the crystal structure and the residual strain in the BST film is investigated. From this knowledge, a set of deposition conditions which provide low residual strain and therefore high tunability can be determined. Establishing these conditions is important, since the relationship between the deposition conditions and the microwave properties of BST thin films grown directly on sapphire has not been systematically studied.

Dielectric losses are also an important consideration in BST films for microwave applications. The capacitance tunability and dielectric loss of the BST films is measured by patterning interdigital electrodes on top of the BST layer. On-wafer

calibration standards are also included, in order to facilitate accurate measurement of losses associated with the BST layer. This allows a link to be established between the deposition conditions and the device losses.

A further objective of this work is to demonstrate the potential of BST films grown on sapphire substrates for use in tunable microwave integrated circuits. Several BST-based circuits, most notably phase shifters, have been demonstrated by other research groups. A novel frequency agile hybrid coupler is developed in this thesis, initially with surface mount semiconductor varactors. An integrated tunable hybrid chip with planar spiral inductors and BST varactors is then successfully demonstrated.

Chapter 3

BST Thin Films on *c*-plane Sapphire

3.1 Introduction

As discussed in Chapter 2, many studies of BST thin films for RF / microwave applications have employed (100) cubic substrates such as MgO and $LaAlO_3$ [23, 28, 42–46, 72]. Another common approach has been to deposit BST onto Pt coated Si substrates [4, 14, 31]. There have been comparatively few reports of BST films grown directly on *c*-plane sapphire, despite the excellent microwave properties of this material.

The microwave properties of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown directly on single-crystal sapphire using CCVD have been investigated by Kim et al. [3, 16, 89, 90]. A capacitance tunability of ∼50% at 200 kV/cm bias was achieved in this work [16]. Magnetron sputtered $Ba_{0.5}Sr_{0.5}TiO_3$ films on *c*- and *r*-plane sapphire were reported by Bhakdisongkhram et al. [87], however no capacitance tunability data was presented. Importantly, the relationship between the deposition conditions and the material and microwave properties of BST films grown on *c*-plane sapphire has not previously been investigated.

Although *c*-plane sapphire is not widely used as a substrate material in commercial semiconductor processes, there are some niche applications for microwave devices. In particular, *c*-plane sapphire is a suitable substrate for the growth of GaN films used in RF high electron mobility transistors (HEMTs) [97, 98]. GaN-based devices show great promise for RF power amplifiers due to their high breakdown voltage and the spontaneous and piezoelectric induction of a high mobility two-dimensional electron gas (2-DEG) [99]. Therefore, it is possible to integrate BST-based tunable devices on *c*-plane sapphire with microwave circuits employing

GaN HEMTs. The integration of parallel plate BST varactors with GaN HEMT circuits has recently been investigated by Xu et al. [82, 100–102].

This Chapter presents a study of the materials and microwave properties of BST thin films on (001) c-plane sapphire. Thin films of BST were deposited on c-plane sapphire by RF magnetron sputtering using the facilities in the Microelectronics and Materials Technology Centre (MMTC) at RMIT University. The material properties of these films were investigated by several different analytical techniques, including Rutherford backscattering spectroscopy (RBS), x-ray photoelectron spectroscopy (XPS), x-ray diffraction (XRD) and atomic force microscopy (AFM). Following the material characterisation, electrodes were patterned on the surface of the films by Au plating, forming an array of interdigital capacitors (IDCs). Microwave measurements of these devices using a network analyser and wafer probe station were used to determine the capacitance tunability and Q-factor of the IDCs. A high capacitance tunability of $\sim$56% at a bias field of 200 kV/cm was achieved by depositing the BST film at 700°C and post-deposition annealing at 900°C .

3.2 RF Magnetron Sputtering of BST Thin Films

Preparation of BST thin films by RF magnetron sputtering has been undertaken by several research groups. The deposition conditions described in their reports, for example [31, 33, 54], served as a starting point for the development of a BST sputtering process at RMIT. In the sputter deposition of thin films, parameters such as substrate temperature, process gas mixture, process gas pressure, substrate to target distance and RF forward power influence the material properties of the sputtered film. Therefore, the optimisation of sputtering conditions for the best electrical properties in the deposited film can be a time consuming process.

An early decision was made to use a mixture of 90% Ar and 10% O_2 as the sputtering gas, since a gas mixture at or near this value has been used by other research groups [26, 30, 33] working with BST thin films. The total pressure of the process gas (Ar+O_2) during sputtering affects the stoichiometry of perovskite oxide films of the form ABO_3. For BST films, Ba and Sr atoms occupy the A site, and Ti atoms are located at the B site. Control of the A to B site ratio, expressed as (Ba+Sr)/Ti, is important for achieving favourable electrical properties [34], in particular high tunability and Q-factor in the case of BST. Before describing the specific details of the sputtering process used to prepare BST films at RMIT, some background on sputter deposition is provided below.

3.2.1 Introduction to Sputter Deposition

Sputter deposition is a common technique for the preparation of thin films, and is part of the PVD group of methods, which also includes PLD and electron beam evaporation. There are several different sputtering methods, including DC sputtering, RF sputtering, and DC/RF magnetron sputtering. DC sputtering is used for conducting materials, while insulating materials require an RF power supply.

Regardless of the specific method of sputtering employed, the sputtering target and substrate on which the film is to be deposited are both placed inside a vacuum chamber. The target is normally a highly pure (>99%) material source, and the objective is to deposit a thin, uniform layer of the target material on the substrate, replicating the composition of the target material as closely as possible. An exception to this case is reactive sputtering, where the sputtering gas reacts with atoms deposited from the target. For example, a N_2 sputtering gas atmosphere combined with an Al target yields an AlN film [103].

At the start of a sputtering run, the sputtering chamber is evacuated to a high vacuum, to remove atmospheric gases. This is normally a two stage process - a short pump cycle with a high pumping rate, low vacuum roughing pump, followed by a changeover to a high vacuum pump and a longer pumping time to high vacuum. During the high vacuum pumping cycle, the roughing pump serves as a backing pump for the high vacuum pump. A base pressure in the range of 10^{-6} to 10^{-8} Torr is achieved on most sputtering systems.

Once the desired base pressure is achieved, highly pure sputtering gas is admitted to the vacuum chamber, and the sputtering pressure is controlled by a combination of throttling the high vacuum pump and regulating the process gas flow. It should be noted that the high vacuum pump is not completely throttled during while sputtering; a steady gas flow through the chamber is maintained during deposition. Inert gases, such as Ar, are normally used for sputtering. In the case of oxide target materials, including BST, an Ar/O_2 gas mixture is used [10,30,33,34]. The O_2 in the gas mixture compensates for O_2 ions scattered during the sputtering process. Without O_2 in the sputtering gas mixture, the deposited film would contain a large number of oxygen vacancies [35].

Deposition of the film is initiated by establishing a plasma inside the vacuum chamber. A DC diode, with the anode and cathode under vacuum, is the simplest sputtering configuration. Using a DC power supply, a high voltage is established between the anode and cathode. With the correct vacuum, the sputtering gas will break down into a plasma discharge [104]. Argon ions are accelerated towards the sputtering target, where they dislodge atoms of the target material. A percentage

of these dislodged atoms will impinge on the substrate, and nucleation of target species on the substrate establishes film growth.

To maintain the plasma with an insulating target material such as BST, an RF power supply is required, since a prohibitively high voltage would be required for DC sputtering to occur [51]. This power supply typically operates in the 13.56 MHz international scientific and medical (ISM) band, and is capable of >100 W output power. A matching network is also required to match the 50 Ω output impedance of the RF source to the input impedance of the RF magnetron assembly. Once the RF plasma is established, the matching network is adjusted to minimise the reflected power.

A magnetron can be employed in both DC and RF sputtering configurations to enhance the deposition rate. Magnetrons are based on a static magnetic field at the cathode, which may be established by an array of magnets behind the sputtering target. Secondary electrons emitted at the cathode due to ion bombardment can be constrained to move in a current loop parallel to the cathode surface if the magnetic field is set up correctly [104]. In the magnetron configuration, electrons in the plasma are subject to forces from both the electric field **E** and the magnetic field **B** according to [51]

$$\mathbf{F} = m\frac{dv}{dt} = -q(\mathbf{E} + \mathbf{v} \times \mathbf{B}) \tag{3.1}$$

where q, m and v are the charge, mass and velocity of electrons, respectively. The magnetic field **B** is configured so that electrons move in a circular path, according to the cross product $\mathbf{v} \times \mathbf{B}$ in Equation 3.1. This helps to confine electrons within the plasma and close to the target, leading to a higher ionisation rate of the Ar gas and hence a higher deposition rate than do simple diode sputtering configurations [51].

3.2.2 RMIT Sputtering System

The MMTC sputtering system is based around a Materials Research Corporation vacuum chamber and a vacuum tube RF power supply. An Advanced Energy MDX-1.5K DC power supply is also available for sputtering conductive materials. A photograph of the chamber and the associated RF matching network is shown in Fig. 3.1. The two large knobs on the front panel of the matching network are adjusted to minimise the reflected RF power once a plasma is established.

Figure 3.2 shows a schematic diagram of the RF magnetron sputtering system located in the MMTC Vacuum Laboratory. The chamber is equipped with a single circular magnetron located in the centre of the chamber at the top; sputtering is therefore on-axis in the sputter-down configuration. The magnetron is designed for

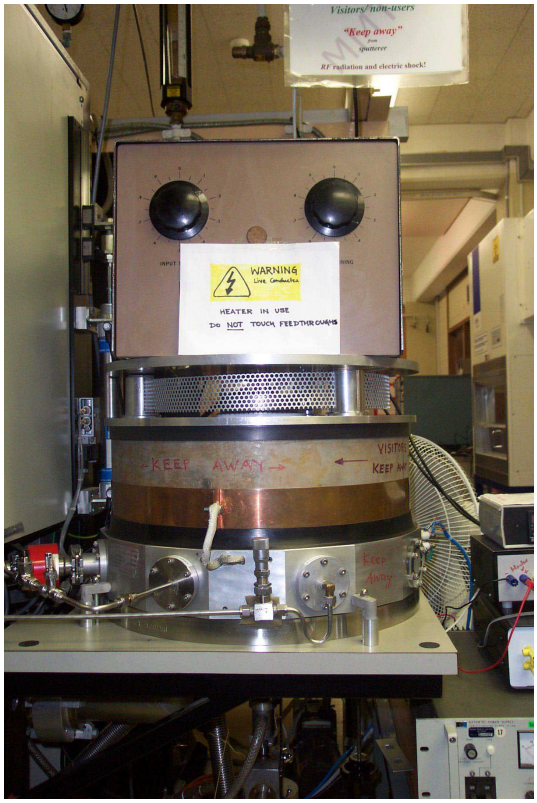


Figure 3.1: View of the vacuum chamber and RF matching box on the RF magnetron sputterer used for BST deposition in the RMIT Vacuum Laboratory.

100 mm diameter circular targets; sputtering targets are secured to the magnetron with a stainless steel circular clamp. A graphite disc is placed between the target backing plate and the magnetron when mounting the target, to ensure good thermal contact between the target and the magnetron. A water cooling system maintains the magnetron temperature at ∼10°C during deposition.

The vacuum system is based around a turbomolecular high vacuum pump and a rotary vane roughing pump. After loading a sample into the deposition chamber, the roughing valve is opened and the roughing pump is used to bring the chamber pressure down to ∼20 mTorr. At this point, the roughing valve is closed, the foreline valve is opened, and the gate valve is opened. A turbomolecular pump (TMP) is used both to pump the chamber to high vacuum and to maintain vacuum during film deposition. There are three vacuum gauges on the system; a thermocouple gauge for low vacuum (used during roughing and venting of the chamber), an ionisation gauge for high vacuum (used to check the base pressure prior to admitting the sputtering gas) and a capacitance manometer gauge which provides feedback to the mass flow controller system during sputtering.

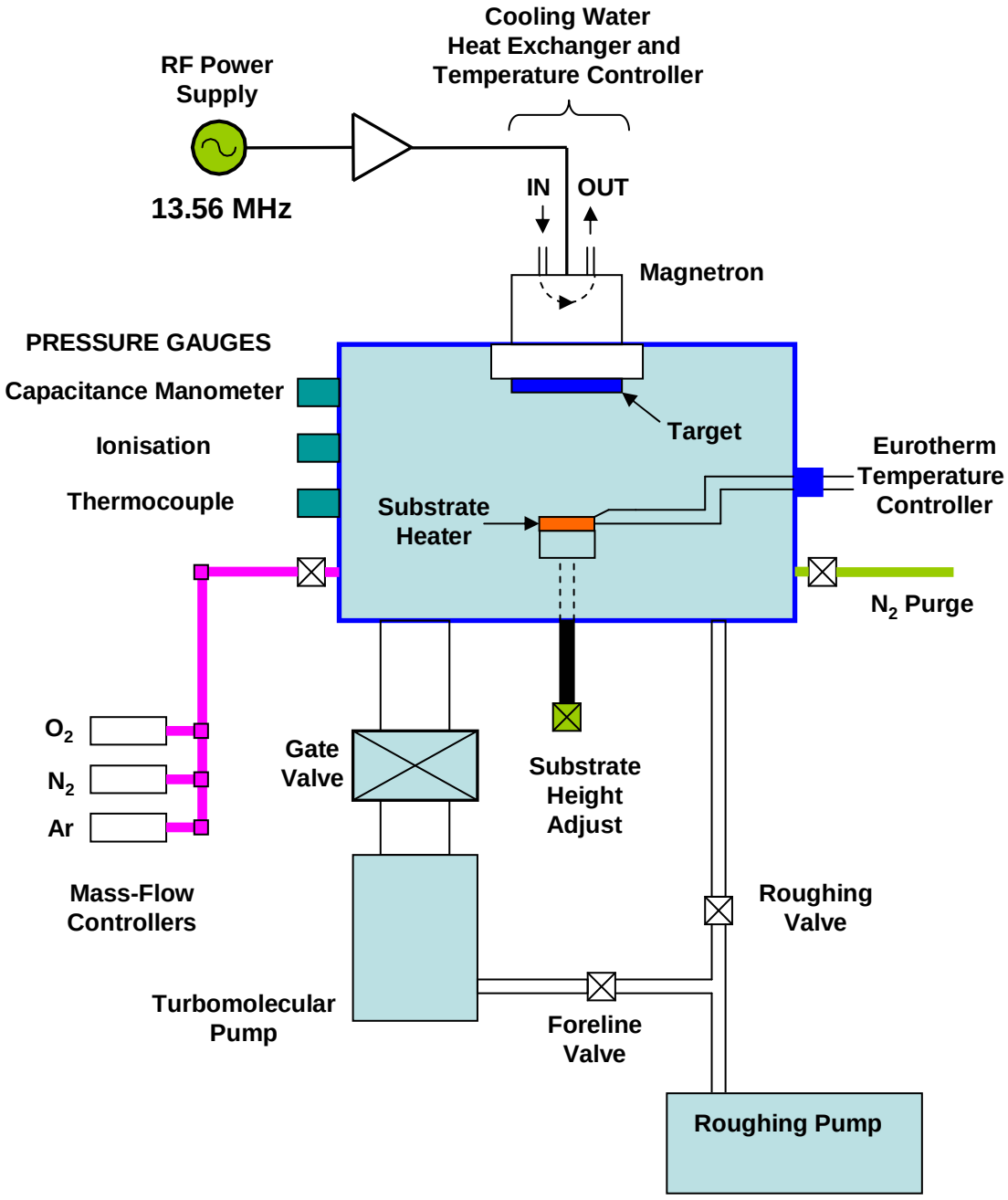


Figure 3.2: Schematic diagram of the sputtering system located in the RMIT Vacuum Laboratory.

3.2.3 Deposition of BST Thin Films

All of the sputter depositions described in this Chapter were from a stoichiometric 100 mm diameter $Ba_{0.5}Sr_{0.5}TiO_3$ target purchased from Williams Advanced Materials. The target to substrate distance was set to 60 mm; this target to substrate distance had previously been used for the deposition of perovskite lead lanthanum zirconate titanate (PLZT) thin films in the same sputtering system [105]. After reaching base pressure by pumping the vacuum chamber with the TMP, sputtering gas (a mixture of 90% Ar and 10% O_2) was admitted to the chamber via mass-flow controllers, raising the chamber pressure to 10 mTorr. The target was pre-sputtered without any sample in the chamber for 8 hours to remove any surface contamination.

After pre-conditioning the sputtering target, BST films were sputtered on single crystal *c*-plane sapphire substrates (Techno Chemics, Ichikawa City, Japan) with dimensions $10\times10\times0.5$ mm^3. Before loading the sapphire substrates into the sputterer for BST film deposition, the substrates were rinsed in acetone, isopropyl alcohol and de-ionised water and then baked at 110°C for 20 minutes to remove any residual moisture. To ensure good thermal contact with the substrate heater, the substrates were fixed to the heater block using silver paste. The substrate temperature was measured by an S-type thermocouple inserted into the heater block.

Initial depositions were performed at 5, 10, 20, 30 and 40 mTorr, in order to determine the effect of the process gas pressure on the material properties of the films. For these depositions, the RF forward power was 90 W, the deposition temperature 625°C and the deposition time was 30 minutes. Although time consuming, the sputtering experiments at different process gas pressure were required, since BST films had not previously been deposited at RMIT. The objective of these experiments was to establish the process gas pressure which provided the best replication of the BST target stoichiometry.

As discussed later in Section 3.3.3, the crystal structure of the BST films on *c*-plane sapphire was improved by increasing the substrate temperature to 700°C during deposition. A pre-deposition heat treatment [64] also influenced the crystal structure of the BST films, and was found to be beneficial in improving the microwave properties of the films. The steps for performing the heat treatment were as follows:

- Ramp the substrate temperature to 700°C at 10°C / min, after reaching the desired base pressure.
- Admit pure oxygen to the deposition chamber, raising the pressure to 20 mTorr, while continuing to pump the chamber with the TMP. These condi-

tions should result in the combustion of any organic contaminants remaining on the sapphire substrate.

- Maintain these conditions for 1 hour before switching to the process gas mixture of Ar/O_2 9:1 and starting deposition.

After deposition of the BST film, all samples were cooled back to room temperature at a maximum rate of 10°C / min before removing them from the deposition chamber.

Some of the BST samples deposited at 700°C were also post deposition annealed in air at 900°C in a ceramic tube furnace. To perform the annealing step, BST samples were loaded into a quartz boat. After the furnace reached the desired 900°C operating temperature, the quartz boat was placed at the mouth of the furnace, and the boat was slowly moved to the centre of the furnace using a glass push-rod. The samples were then annealed for two hours, before slowly removing them from the furnace, in order to avoid possible cracking of the sapphire substrate due to rapid cooling.

3.3 Materials Analysis

Several different analytical techniques were employed to examine the material properties of the sputtered BST films. Rutherford backscattering was used to determine the stoichiometry and thickness of the initial series of films deposited at 625°C. X-ray photoelectron spectroscopy provided information about the chemical bonds present near the surface of the 625°C series of BST films. An important objective of the RBS and XPS experiments was to establish that the composition of the sputtered films was close to that of the $Ba_{0.5}Sr_{0.5}TiO_3$ target. The crystal structure of the films deposited at 625°C and 700°C was studied by XRD, using both a powder diffactometer and a high resolution diffractometer equipped with a Eularian cradle. Note that the substrate temperature was increased from 625°C to 700°C to investigate the effect of the substrate temperature on the crystal structure of the BST film. The RBS measurements were not repeated for the films deposited at 700°C, since previous work has shown that increasing the substrate temperature from 600°C to 700°C has little effect on the film composition [29]. Characterisation of the surface morphology and grain size of the films was performed by AFM measurements. The results of these analyses are provided below; in each case, a brief introduction to the technique is also given.

3.3.1 Rutherford Backscattering Spectroscopy

In Rutherford backscattering, a target material is bombarded by high energy, low mass (generally H or He) ions, which travel hundreds of nanometres or even microns into the target. The scattering processes which the ions undergo are influenced by the constituent atoms in the target. This allows the composition of the target to be determined by measuring the energy of the backscattered ions. In the case of thin film targets, such as BST films on sapphire substrates, the thickness of the film can also be extracted from the RBS data.

A proportion of the incident ions punch through the electron cloud surrounding a target atom and are scattered by close interaction with the nucleus of the target atom, which is also positively charged [51]. The fundamental equation which describes the scattering process is [51]

$$E_1 = \left\{ \frac{M^2 - M_0^2 \sin^2\theta + M_o \cos\theta}{M_o + M} \right\}^2 E_o \tag{3.2}$$

where E_1 is the ejected ion energy, E_o is the incident ion energy, M is the atomic mass of the ejected ion, M_o is the atomic mass of the incident ion and θ is the scattering angle. A kinematic factor is calculated according to

$$K_m = \frac{E_1}{E_o} \tag{3.3}$$

Since $M_o = 4$ for He, E_o is determined by the accelerator, and E_1 is measured by the detector, K_m is simply determined by the mass of the target atoms.

The thickness and composition of each of the series of BST films deposited at 625°C was determined by RBS measurements using 2 MeV $^4He^{2+}$ ions at the Melbourne 5 MV Pelletron accelerator, located at The University of Melbourne, Australia. A schematic representation of the system is shown in Fig. 3.3. In this diagram, θ is the scattering angle; that is, the obtuse angle between the incident ion beam and the backscattered ion detector. The entire beam line, including the focussing lens and the RBS analysis chamber, is evacuated to high vacuum.

A particular advantage of the Melbourne Pelletron system is that the incident beam is focussed to a very small spot size (of the order of 1 μm). In the case of the BST films, the advantage of the small beam diameter was that only a small area of the film was exposed to the ion beam. Although RBS is a non-destructive technique, the high energy of the ion beam is likely to affect the crystal structure of the irradiated region of the film. This could affect the electrical performance of devices fabricated on the same film. However, since the ion damage was confined to a small area of the BST films on *c*-plane sapphire, the same films could be further processed to realise BST varactors.

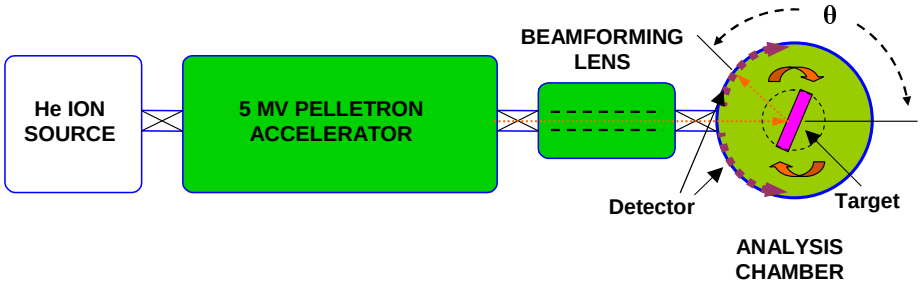


Figure 3.3: Schematic diagram of the Melbourne 5 MV Pelletron accelerator and associated RBS analysis chamber.

In our RBS experiments, the surface normal of the sapphire substrate was parallel to the incident $^4He^{2+}$ ion beam, and the scattering angle θ was set to 135°. The data obtained from the RBS experiments were analysed using SIMNRA software [106], with the detector resolution set to 15 keV in the SIMNRA simulation. The measured and fitted RBS spectra are shown in Fig. 3.4. For the Ba, Sr and Ti atoms in the BST film, the fit between the measured and calculated data is very good. However, the fit for the substrate constituent atoms (Al and oxygen) is not as good, particularly in Fig.3.4(a) and (d). This may be attributed to channelling, where incident ions penetrate down crystallographic directions in the lattice of a single crystal material [51], resulting in a lower backscattered yield. Since the substrates were mounted in the RBS system with the surface plane of the *c*-plane sapphire substrate normal to the incident ion beam, incident ions may travel along the [001] direction in the substrate, resulting in a lower than anticipated backscattered yield. Where better agreement is achieved for the substrate constituents aluminium (Al) and oxygen (O), it is likely that the samples were slightly misaligned relative to the incident beam. This problem could have been avoided by mounting the samples in the RBS chamber with the surface normal of the substrates oriented at a small angle ($\sim$5°) relative to the incident beam.

Figure 3.5 provides a summary of the BST film thickness and stoichiometry information determined by SIMNRA. A lower deposition rate was observed at higher process gas pressures, as shown in Fig. 3.5(a). This is expected, since a higher process pressure increases the probability of a scattering collision between ions sputtered from the BST target and atoms of the sputtering gas. Figure 3.5 also shows the vari-

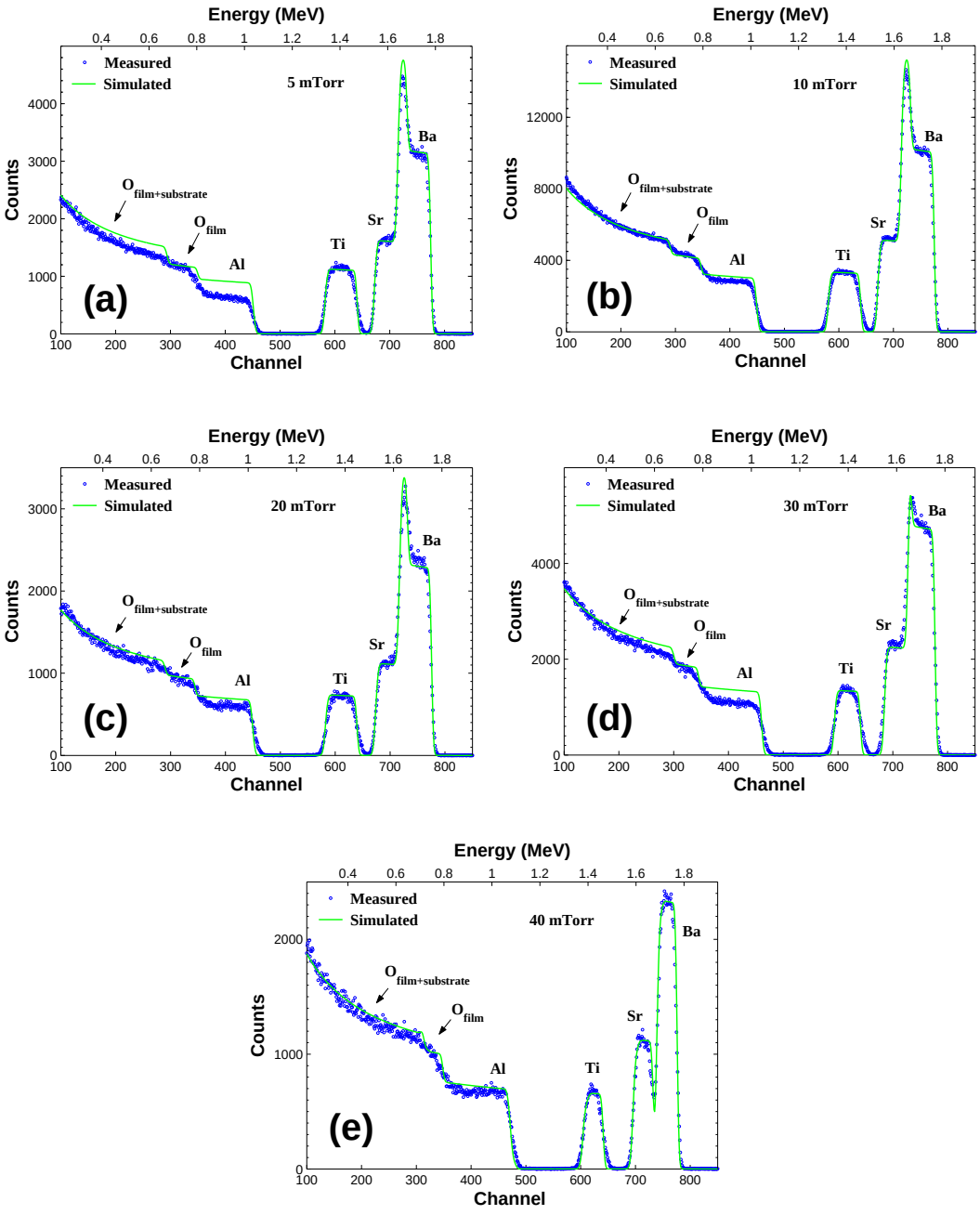


Figure 3.4: Measured and simulated RBS (He^{2+}) data for BST films deposited from a $Ba_{0.5}Sr_{0.5}TiO_3$ target at 5 to 40 mTorr process gas pressure and 625°C substrate temperature.

ation in film composition with deposition pressure. Note that the ideal composition of $Ba_{0.5}Sr_{0.5}TiO_3$ is 10 at.% Ba/Sr, 20 at.% Ti and 60 at.% oxygen. Importantly, films deposited at 5 to 30 mTorr are found to be significantly oxygen deficient. Oxygen vacancies are undesirable, because they increase the microwave dielectric loss of the BST film [14]. In general, BST thin films with a (Ba+Sr)/Ti ratio close to 1.0 have shown the highest permittivity and tunability [33,34]. As discussed in Section 2.2, the Ba/Sr ratio influences the Curie point of the film. Although the film sputtered at 40 mTorr is slightly Ti deficient, with 22.4 at.% Ba+Sr and 19.7 at.% Ti, this was accompanied by higher oxygen incorporation. The films sputtered at lower pressures were more than 5 at.% oxygen deficient. Close replication of the target stoichiometry is achieved with a 40 mTorr process gas pressure, although the film is slightly Ti and oxygen deficient.

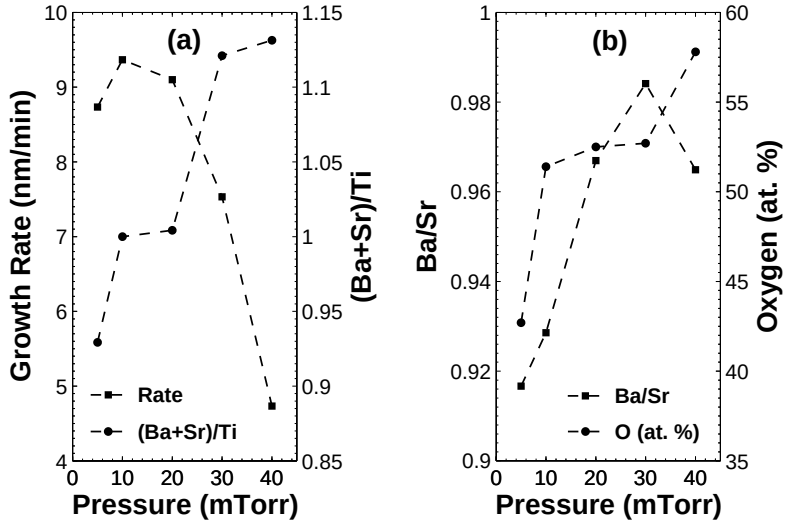


Figure 3.5: (a) BST film growth rate and (Ba+Sr)/Ti ratio and (b) Ba/Sr ratio and oxygen incorporation as a function of total process gas pressure ($Ar+O_2$).

3.3.2 X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy provides information about the chemical bonding and valence states in a thin surface layer ($\sim$15 $\AA$) of a target material [51]. In these experiments, a monochromated beam of incident x-ray photons ejects a valence or core electron from an atom in the sample material; photoelectrons are ejected at a takeoff angle θ from the surface plane of the sample. The kinetic energy of the electrons is equal to the difference between the incident photon energy and the binding energy of the electron in the target [107]. Unlike RBS, XPS does not provide accurate compositional information without the use of appropriate reference

standards. The measurements described in this Section were performed at RMIT on a MicroLab 310-F instrument with Al K_α radiation (1486.6 eV) and a takeoff angle of $\theta = 90°$.

For each of the series of films sputtered at 625°C, a complete spectrum of data for ejected photoelectrons with energies in the range 0 to 1400 eV was gathered, with a 2 eV step size. Refined spectra with a 100 meV step size were also gathered for the constituent elements in BST; a Sr $3d$ spectrum from ∼130 to 138 eV, a Ti $2p$ spectrum from ∼447 to 467 eV, an O $1s$ spectrum from ∼526 to 534 eV and a Ba $3d$ spectrum from ∼775 to 784 eV. A similar set of spectra was also gathered for a powder sample taken from the sputtering target. Compensation for sample charging was performed by comparison of the C $1s$ peak in each of the wide spectra with the known value (284.6 eV) of the adventitious C $1s$ peak.

The spectra associated with the Ba $3d$ energy range showed significant differences between the samples sputtered at different pressures. Figure 3.6 shows the Ba $3d_{5/2}$ XPS peaks for each film and also for a powder sample taken from the BST target. A fit to the measured data was performed using three separate peaks centred at 780.5 eV (Ba1), 779 eV (Ba2) and 777.9 eV (Ba3). The decomposition of the Ba $3d_{5/2}$ level into two peaks centred at 780.5 eV and 779 eV has previously been reported by Craciun and Singh [108]. In the work of Craciun and Singh, the Ba2 peak is attributed to the perovskite phase of BST, while the higher energy Ba1 peak is related to a thin decomposed surface layer that forms when the film is exposed to atmosphere. To obtain an accurate fit to the measured data for the BST films sputtered at RMIT, an additional peak at 777.9 eV (Ba3) was required. This lower energy Ba3 peak could be caused by weaker Ba-O bonds related to oxygen deficiency [108]. When correlated with the RBS data in Fig. 3.5(b), a strong Ba3 peak at ∼778 eV is indicative of oxygen deficiency in the film. The low intensity of the Ba1 peak, compared to other published results [108, 109] may be due to the 90° takeoff angle in the experiments performed at RMIT, which lowers the contribution of the sample surface to the XPS signal.

Confirmation of the presence of the perovskite phase of BST in all of the 625°C films was a useful result from the XPS investigation. As discussed in Chapter 2, the perovskite structure is the desired atomic arrangement for the fabrication of electronically tunable microwave devices. Further confirmation of the perovskite structure in the BST films was achieved by XRD experiments.

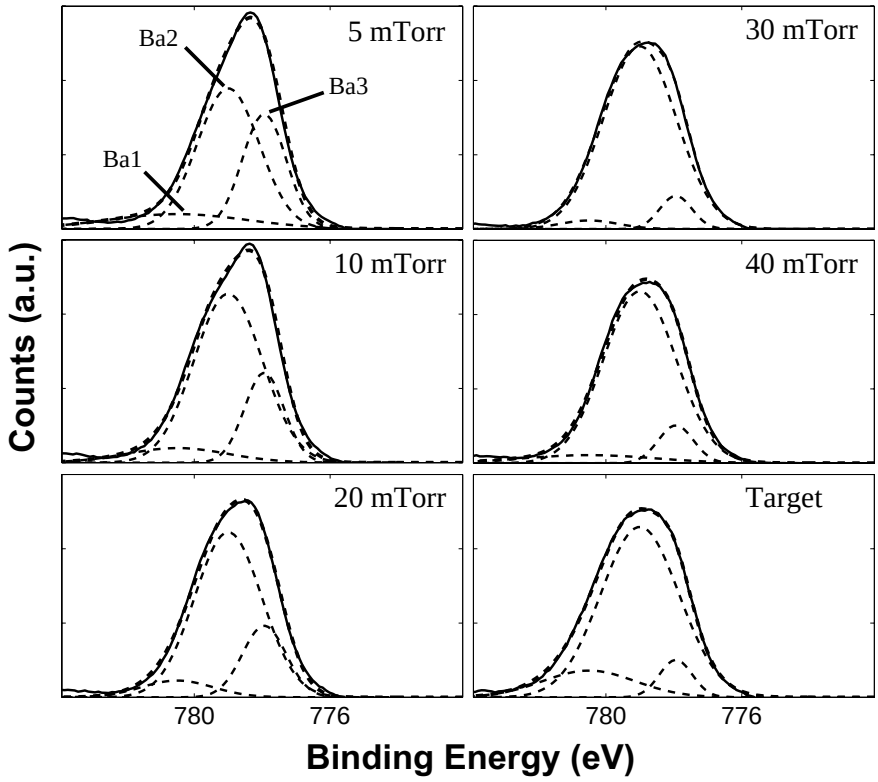


Figure 3.6: Measured (solid lines) and fitted (dashed lines) XPS spectra for the Ba $3d_{5/2}$ energy level, as a function of the process gas pressure ($Ar+O_2$), for 625°C substrate temperature. The XPS spectrum of a powder sample taken from the $Ba_{0.5}Sr_{0.5}TiO_3$ sputtering target is also shown.

3.3.3 X-Ray Diffraction

X-ray diffraction is a well-known technique for characterising the crystal structure of materials. Radiation from an x-ray source has a wavelength of the order of Angstroms (10^{-10} m), which is comparable to the interatomic spacing in solid materials. Therefore, when a material with a regular, repeating arrangement of atoms is illuminated by an x-ray source, a diffraction pattern can be observed. This diffraction pattern is directly related to the crystal structure of the material under observation.

The diffraction of x-rays by a crystalline material is illustrated in Fig. 3.7. A parallel beam of x-rays of wavelength λ is incident on the sample at an angle θ to the surface. Constructive interference between the diffracted beams $1'$ and $2'$ occurs when the path difference between the diffracted beams is equal to a whole number of wavelengths. This diffraction condition, known as the Bragg Law, can be expressed

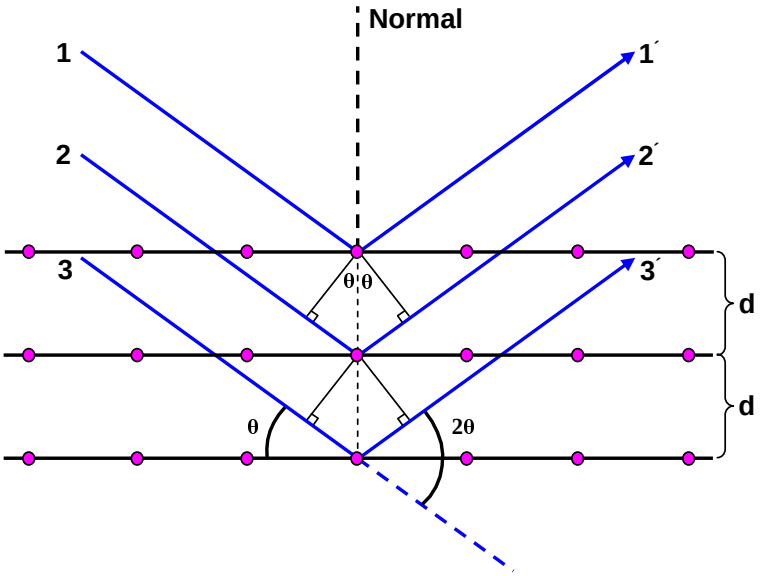


Figure 3.7: X-ray diffraction in a crystalline material, based on [95].

as

$$n\lambda \;=\; 2d\sin\theta \tag{3.4}$$

Therefore, given the wavelength λ of the x-ray source and the measured angular position θ of a diffraction peak, the interplanar spacing d of a set of crystallographic planes in a crystalline material can be determined.

Conventional $\theta - 2\theta$ XRD scans of the BST films were performed using a Bruker D8 Discovery powder diffractometer at the RMIT Chemistry Department. This instrument is equipped with Soller slits in the incident and diffracted beam paths, which collimate both the x-ray beam incident from the Cu K_α ($\lambda \;=\; 1.5406$ $\mathring{A}$) line source and the beam diffracted from the sample in one dimension. A fixed 1.0 mm slit in the incident beam path limits the divergence of x-rays normal to the plane of the Soller slits. The instrument is also equipped with a Ni filter to attenuate Cu K_β radiation from the x-ray source. In order to further increase the resolution of the measurements, a 0.1 mm slit was placed in the diffracted beam path between the Soller slits and the x-ray detector.

XRD $\theta - 2\theta$ scans in the Bruker system were performed by rotating the x-ray source and detector at an equal rate to preserve the surface symmetric configuration illustrated in Fig. 3.7. The BST samples were mounted in a sample changer at the centre of the diffractometer, and remained stationary during the scans. XRD results for the samples deposited at 625°C confirmed that the BST films were single phase,

that is, free of any other compounds, such as $BaSrTiO_4$ or $Ba_{0.5}Sr_{0.5}Ti_3O_7$, that could form from the constituent elements of the $Ba_{0.5}Sr_{0.5}TiO_3$ sputtering target. In other words, only peaks corresponding to the perovskite structure of $Ba_{0.5}Sr_{0.5}TiO_3$ were observed, which also confirms the XPS results.

Since XRD peaks corresponding to different crystallographic planes, including (100), (110) and (111) were observed in the XRD patterns, it was concluded that the BST films were polycrystalline. Therefore, individual grains constituting the BST film were randomly oriented with respect to the single crystal substrate. The (110) BST reflection was stronger than other BST peaks in the diffraction pattern, as shown in Fig. 3.8(a) for the 40 mTorr sample. This <110> preferred orientation was observed for all process gas pressures. As the process gas pressure increases, the BST peaks shifted to a slightly higher angle, indicating a trend of decreasing lattice spacing according to Equation 3.4. This is likely due to higher oxygen incorporation in the film [23], which is also in agreement with the results obtained by RBS and XPS.

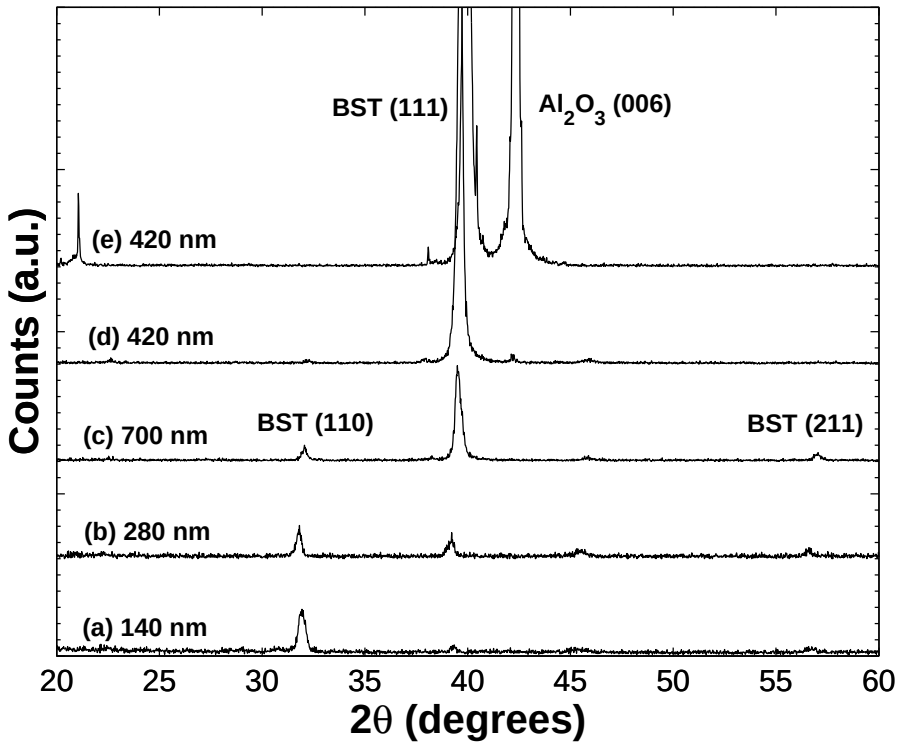


Figure 3.8: XRD patterns of BST thin films deposited at 40 mTorr with substrate temperature (a) 625°C and (b)-(e) 700°C. Film thickness is also indicated. The sample shown at (d) was heat treated at 700°C in Ar/O_2 1:9 inside the deposition chamber for 60 minutes prior to sputtering the film. After a 2 hour post-deposition anneal of sample (d) in air at 900°C, the XRD pattern (e) was obtained.

In order to investigate the effect of substrate temperature on the growth of the BST films, further depositions were performed at 700°C . For these depositions, the process gas pressure was set to 40 mTorr, in order to minimise oxygen deficiency in the BST films. Stronger <111> orientation is observed in thicker films deposited at 700°C , as shown in Figs. 3.8(b) and 3.8(c). Pre-deposition heat treatment of the substrate according to the procedure outlined in Section 3.2 was found to strongly increase the <111> orientation of the subsequently deposited film. The effect the heat treatment on the crystal structure of the BST film can be seen in Fig. 3.8(d). Fig. 3.8(e) shows XRD data for the same film as Fig 3.8(d) after 2 hour post-deposition annealing in air at 900°C . Highly <111> oriented films have previously been observed in $Ba_{0.1}Sr_{0.9}TiO_3$ films grown by MOCVD on c-plane sapphire substrates [56].

Because the films deposited at 700°C with a pre-deposition heat treatment and post-deposition annealing were very strongly <111> oriented, it is interesting to consider whether growth of the BST film is heteroepitaxial. If this were the case, a fixed relationship between crystallographic planes in the substrate and in the BST film would be expected, with $(111)_{BST}\|(001)_{SUB}$. In order to investigate the orientation of the BST film with respect to the c-plane sapphire substrate, a high resolution XRD system was required. This is because the orientation of the substrate relative to the x-ray source and detector cannot be precisely controlled in a powder diffractometer. A PANalytical X'Pert diffractometer located at LaTrobe University, Australia was used for the high resolution XRD measurements. The instrument is equipped with a PW3050/65 goniometer and a Eularian cradle with three independent axes of rotation for the sample stage. These axes, ϕ, ψ and ω, are illustrated in Fig. 3.9. Before commencing the measurements, the [006] direction of the substrate was aligned parallel to the diffraction vector of the diffractometer. Ideally (if the c-plane sapphire substrate were perfectly cut) the sapphire (006) reflection would be surface symmetric, or parallel to the surface normal of the substrate. However, the specifications from the substrate supplier indicated that the cut was accurate only to within $\pm 0.5°$. Therefore, it is helpful to align the sample so that the (006) reflection satisfies the diffraction condition at the $\psi = \phi = 0°$ position of the diffractometer, in order to account for any substrate miss-cut.

After aligning the sample, a series of rocking curves were taken for the BST (111) reflection at four different in-plane rotations (ϕ = 0°, 90°, 180°, 270°) as shown in Fig. 3.10(a). These measurements are also called ω-scans, since the sample is scanned in ω (rocked) while keeping the x-ray source and detector fixed. Essentially, the rocking curves measure the degree of tilt of (111) planes the BST film relative to the surface plane of the sapphire substrate. For a post-deposition annealed sample,

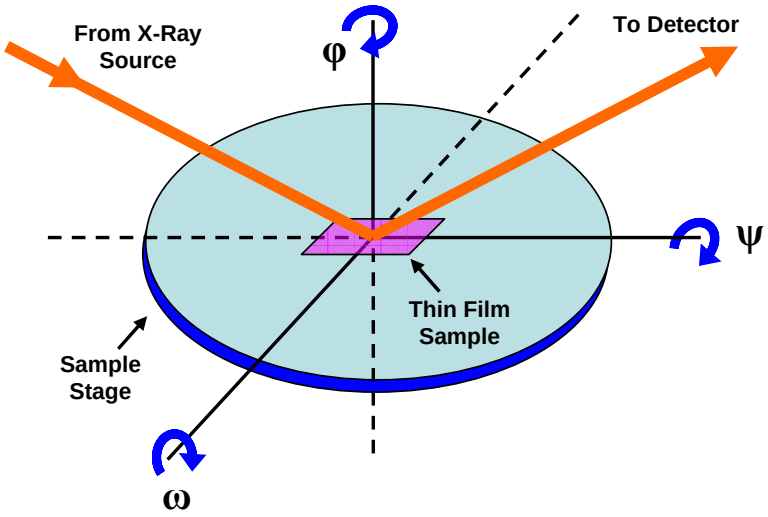


Figure 3.9: Axes of sample rotation ϕ, ψ and ω in a high-resolution XRD system.

the full width half maximum (FWHM) of the rocking curves was ~4.9° in all four ϕ settings, which suggests a uniform distribution of crystallites about the surface normal. Note that most single crystals have a rocking curve width of 0.03° to 0.3° [95]. For another sample deposited with the same sputtering conditions, but not post-deposition annealed, the FWHM was ~7.7°. From these results, it can be concluded that the BST film is not precisely aligned to the substrate. However, post deposition annealing does improve the orientation significantly.

In an earlier report [87], a (111) rocking curve for $Ba_{0.5}Sr_{0.5}TiO_3$ sputtered on *c*-plane sapphire at 600°C had a FWHM of 13.5°. The high level of tilt of (111) planes in the BST layer, both in [87] and in this thesis, may be caused by nucleation of <100> and <110> oriented grains in the initial stages of film growth, since weak (100) and (110) reflections are observed in θ-2θ scans of un-annealed films deposited at 700°C (Fig. 3.8(d)). In contrast, thin films of $SrTiO_3$ and $BaTiO_3$ deposited on *c*-plane sapphire by MOCVD at 800°C had FWHM values of 0.25° and 0.35°, respectively [55]. It is unclear whether this improved epitaxy, relative to the sputtered films, is due to the deposition method, or to the increased substrate temperature.

The in-plane arrangement of BST crystallites with respect to the substrate was examined by XRD ϕ-scans. To bring the <012> substrate reflections into the diffraction plane, the sample tilt ψ was set to 57.61°, the angle between (006) and (012)

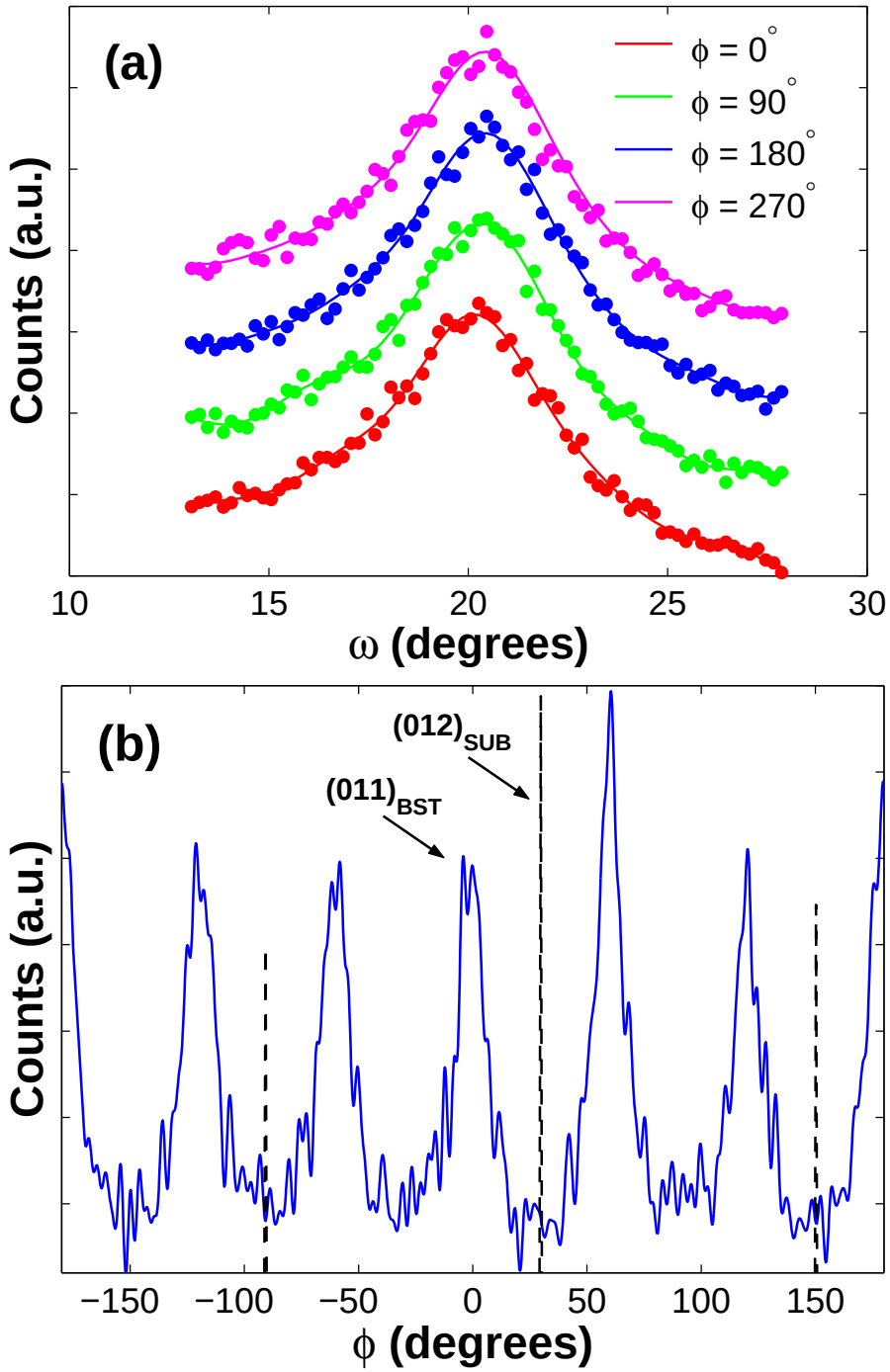


Figure 3.10: (a) Rocking curve data for surface symmetric BST (111) reflection and (b) ϕ-scans of BST <011> and sapphire <012> reflections. Data is for a 700 nm film deposited at 700°C and post-deposition annealed.

in the sapphire hexagonal unit cell. As shown in Fig. 3.10(b), three substrate peaks were observed, corresponding to the (012), ($\bar{1}$02) and (1$\bar{1}$2) planes. The substrate peaks shown in Fig. 3.10 occur at 'corrected' ϕ values of -90°, 30° and 150°. The correction was necessary to account for misalignment of the substrate edge cuts. Correspondence with the substrate manufacturer indicated that two edges of the square substrate are roughly parallel to [110], although an exact tolerance was not provided. Therefore, an offset was applied to the measured data to remove the offset associated with misalignment of the substrate edge cuts.

By changing the sample tilt ψ to 35.26°, the angle between (111) and (110) in the cubic BST unit cell, the <011> BST reflections were observed. The BST <011> ϕ-scan of a post-deposition annealed sample is superimposed on the substrate <012> ϕ-scan in Fig. 3.10. For a given family of crystallites with $(111)_{BST}\|(001)_{SUB}$, three BST <011> peaks mutually separated by 120° would be expected in the ϕ-scan. However, six BST <011> peaks were observed, as shown in Fig. 3.10. The three extra BST peaks are due to an additional set of crystallites which grow at an in-plane rotation of 60° relative to the original set, as observed in [56]. The ϕ scan results show a crystallographic relationship of the form $(1\bar{1}0)_{BST}\|(100)_{SUB}$ in the plane of the BST film. However, since the FWHM of the BST <011> peaks is ∼15°, the coherence between the film and substrate is poor. Note that the in-plane relationship observed here is identical to one recently reported for perovskite $Pb_{0.3}Sr_{0.7}TiO_3$ thin films grown on *c*-plane sapphire [110].

Having established the in-plane and out of plane relationships of the BST film with respect to the sapphire substrate, the arrangement of BST atoms on *c*-plane sapphire can now be considered. A possible epitaxial relationship between the sapphire substrate and the film is shown in Fig. 3.11. The interatomic distances in the substrate can be established from studies of the crystal structure of sapphire [94, 111–113]. In the arrangement shown in Fig. 3.11, the sapphire substrate is terminated by an uppermost layer of Al atoms, which form one corner of the BST cubic unit cell. This substrate-film relationship is based upon earlier work by Rafaja et al. [56], but the BST unit cell is rotated in-plane by 30° with respect to the model proposed by Rafaja. A possible reason for this difference is that the depositions in [56] were performed at 800°C, 100°C higher than the films prepared at RMIT. A different mutual orientation between the film and substrate may be favoured at this higher temperature [114].

Although the sapphire substrate did impose a definite order on the growth of the BST film, it is not strictly correct to call the growth epitaxial, due to the large FWHM of the ω and ϕ scans. To confirm that epitaxial growth of BST was possible

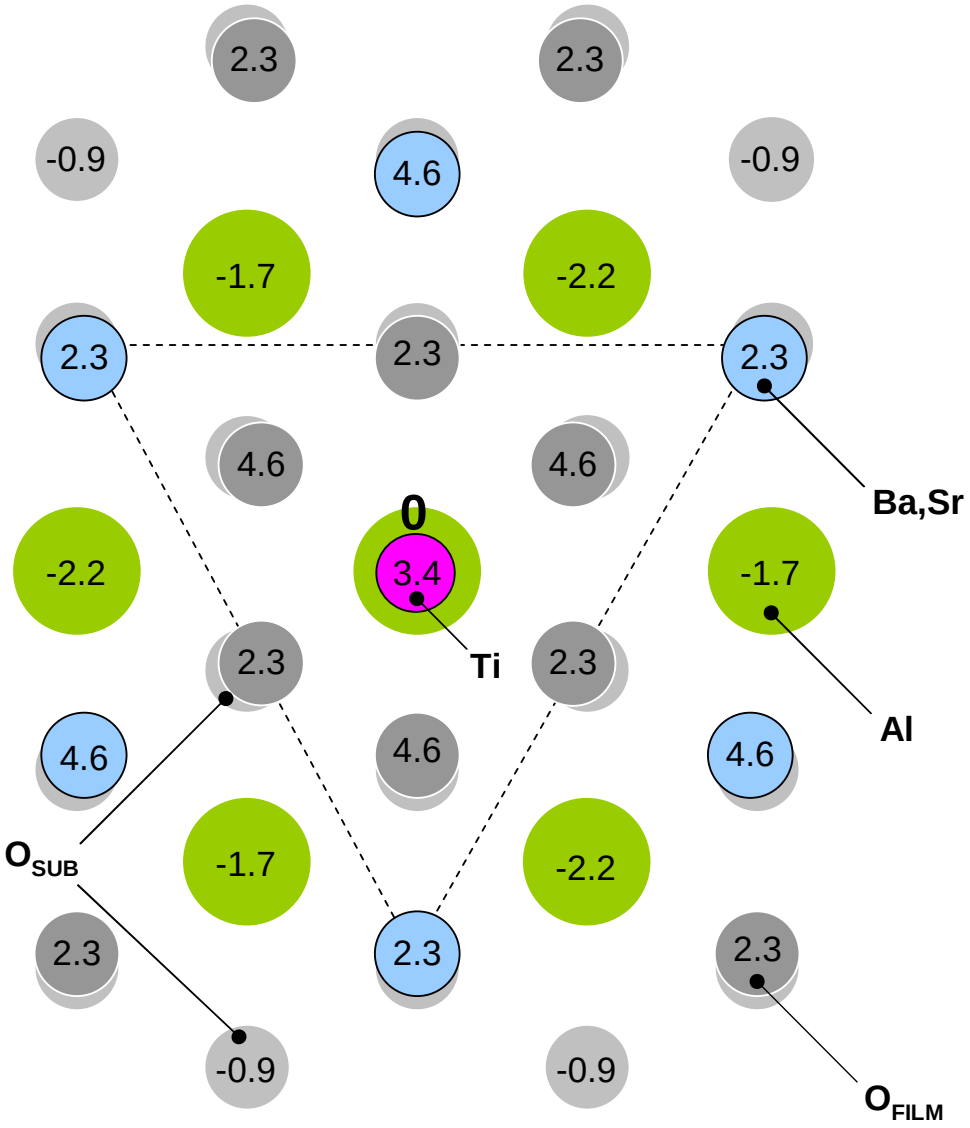


Figure 3.11: Schematic diagram of the hypothetical epitaxial relation between BST and c-plane sapphire. Numbers denote the distance ($\AA$) in the (001) or z direction, referred to the film-substrate interface. The central Al atom lies at the $z = 0$ position.

using the MMTC sputtering system, a $Ba_{0.5}Sr_{0.5}TiO_3$ film was grown on a (100) $LaAlO_3$ substrate. The deposition conditions were identical to the BST films grown on *c*-plane sapphire at 700°C . A PANalytical high resolution XRD system was used to analyse the crystal structure of the BST film. As shown in Fig. 3.12, growth of the BST layer is epitaxial, since only (100) and (200) BST reflections were observed in the $\theta - 2\theta$ scan. A BST (200) rocking curve had a FWHM of $\sim$0.03°, indicating a high degree of epitaxy. Therefore, epitaxial growth of BST films is possible in the MMTC sputtering system.

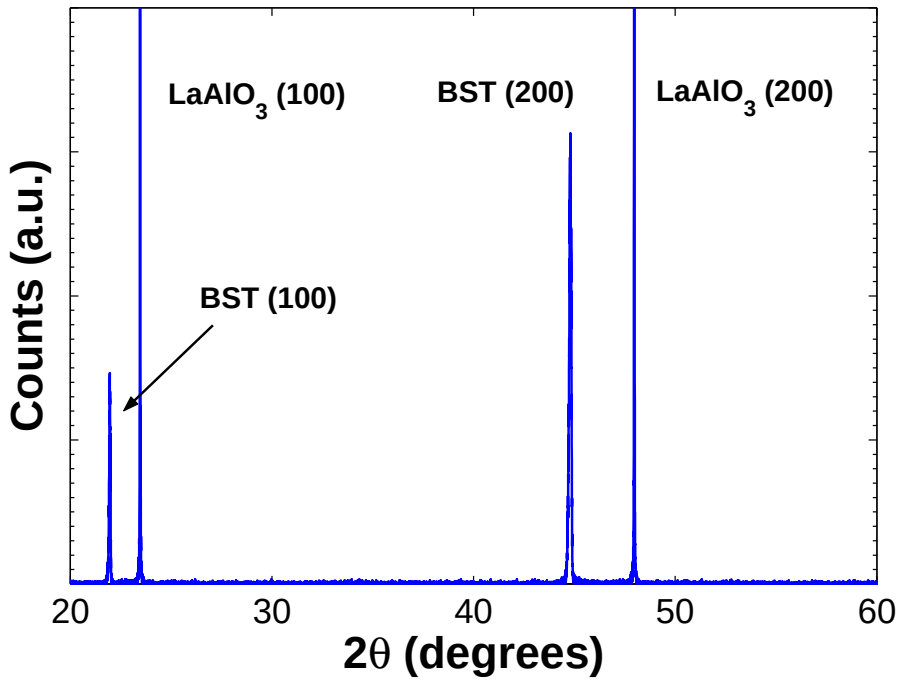


Figure 3.12: XRD pattern of a $Ba_{0.5}Sr_{0.5}TiO_3$ film prepared by RF magnetron sputtering on $LaAlO_3$ substrate at RMIT.

3.3.4 BST Film Strain Measurement X-Ray Diffraction

Several publications have demonstrated a correlation between strain and dielectric tunability in BST thin films [20, 22, 23, 39]. The focus of this earlier work was on epitaxial BST thin films grown on cubic or orthorhombic substrates. In [20,22,23,39], the highest dielectric tunability was achieved when residual strain in the BST film was minimum. In this Section, the strain in <111> textured BST films deposited on *c*-plane sapphire is investigated.

X-ray diffraction provides a convenient means of measuring strain in thin films; the technique is non-destructive and no special sample preparation is required [95].

Essentially, strain in a thin film is determined by observing the distortion of the unit cell caused by the strain. For example, a compressive strain in the plane of the film causes the in-plane lattice spacing to decrease relative to the strain-free state, while the out of plane lattice spacings increase [115]. In the $\sin^2\psi$ method for stress measurement, the lattice spacing d is measured at several different sample tilts ψ, where ψ is defined in Fig. 3.9. The stress is then determined from the slope of the d–$\sin^2\psi$ characteristic [95]. High angle reflections (XRD peaks that occur at large 2θ values in θ–2θ scans) are needed for strain measurements [116]; these reflections provide more accurate d-spacing values because they are less sensitive to goniometer misalignment.

The $\sin^2\psi$ method [24, 95, 116] was employed to determine the effect of post-deposition annealing on the in-plane strain of the <111> textured BST films on c-plane sapphire. For the films on which strain measurements were performed, the deposition temperature was 700°C and a pre-deposition heat treatment was employed. A series of measurements was performed on the BST (222) peak, which occurs at $2\theta \simeq 85°$. Sample tilts ψ of 0°, ±18.43°, ±26.57° and ±33.21°, corresponding to $\sin^2\psi$=0, 0.1, 0.2 and 0.3, respectively, were introduced in the scan configuration.

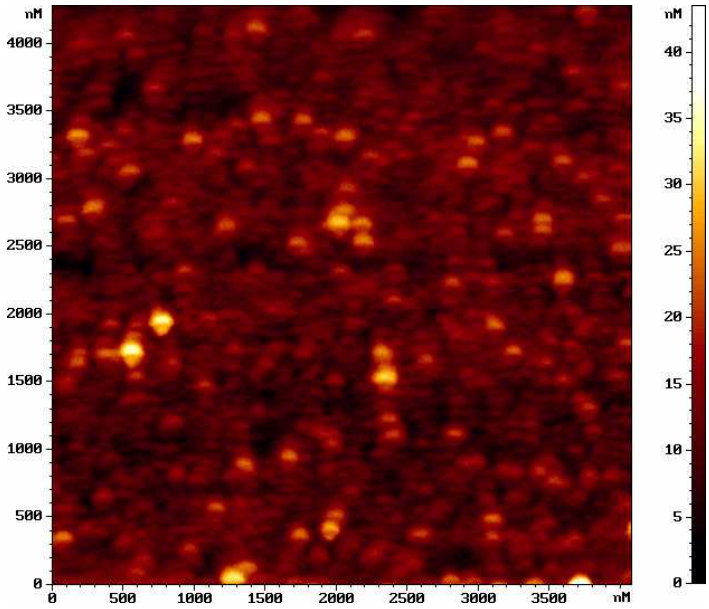
For <111> oriented films, the strain at an angle ψ to the surface normal is [24]

$$\varepsilon_{\psi}^{[111]} = \frac{d_{\psi} - d_o}{d_o} \tag{3.5}$$

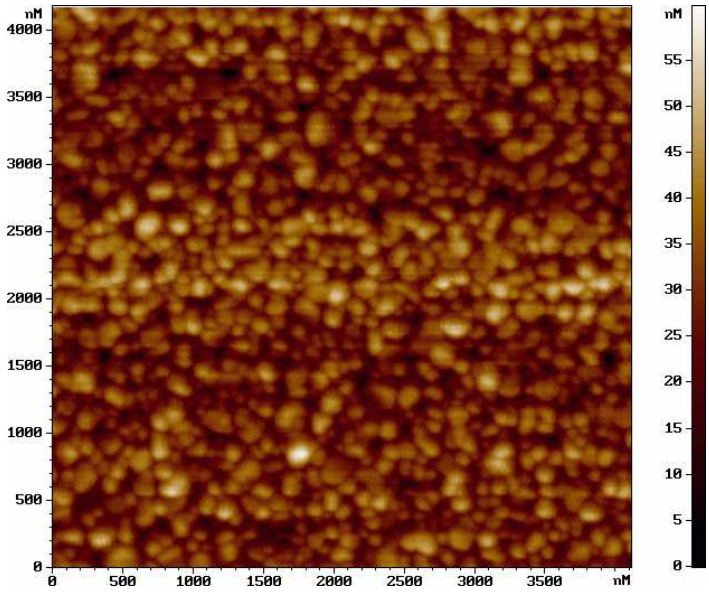
$$= \sigma\left(\frac{2s_{11} + 4s_{12} - s_{44}}{3} + \frac{s_{44}}{2}\sin^2\psi\right) \tag{3.6}$$

where d_{ψ} is the d-spacing for a set of planes with normals at an angle ψ to the surface normal, d_o is the unstrained plane spacing, s_{ij} are elastic compliances, and σ is the stress. The elastic data for $Ba_{0.5}Sr_{0.5}TiO_3$ in [22] was used for strain calculations. Strain-free lattice parameters d_o, calculated from Equation 3.6, were 3.984 $\mathring{A}$ (as deposited) and 3.941 $\mathring{A}$ (annealed). From these values, a tensile in-plane strain of 0.94% for the as-deposited film and a compressive in-plane strain of -0.38% for the annealed film, were calculated.

It is difficult to isolate a single cause for the reduced strain observed following post deposition annealing. The stress field in the BST film is affected by the lattice and thermal coefficient mismatch between the film and substrate, and by film contraction on annealing due to oxygen incorporation [23]. It is possible that all of these factors simultaneously contribute to the strain reduction upon annealing.



(a)



(b)

Figure 3.13: AFM images (∼4×4 μm^2) of 700 nm $Ba_{0.5}Sr_{0.5}TiO_3$ thin films deposited on *c*-plane sapphire (a) before and (b) after post-deposition annealing at 900°C in air for 2 hours.

3.3.5 Atomic Force Microscopy

An AFM measures the surface topography of a sample by scanning a cantilever with an atomically sharp tip across the sample surface. A laser beam is focussed on to the Au coated cantilever, and then reflected via a mirror to a photodetector [64]. Vertical motion of the cantilever, corresponding to the surface topography of the sample, is measured by laser interferometry.

The effect of annealing on the film grain size and surface roughness was investigated with an AFM (NT-MDT Solver LS) at Swinburne University, Australia. The instrument was operated in high resolution semicontact mode. AFM images, shown in Fig. 3.13 reveal an average grain size of < 100 nm (as deposited) and 100 to 150 nm (annealed). The annealing process also resulted in an increase in the average surface roughness R_a from 2.7 nm to 5.9 nm. An increased grain size and surface roughness after annealing has previously been reported by Cole et al. [117].

3.4 Microwave Characterisation

Microwave properties of $Ba_{0.5}Sr_{0.5}TiO_3$ films on c-plane sapphire were measured via an array of interdigital electrode structures patterned on top of the BST film. By measuring the microwave properties of films deposited under different conditions, including substrate temperature and process gas pressure, it is possible to establish the effect of the processing conditions on the microwave properties of the films. The objective was to optimise the processing conditions in order to achieve the desirable microwave properties of high tunability and low dielectric loss.

Interdigital capacitors were fabricated on the BST films in a multi-step process shown schematically in Fig. 3.14. An outline of the processing steps is provided below; full details are provided in Appendix B.

1. The metal seed layer pattern for electroplating the IDCs was defined in AZ5206E photoresist spin coated onto the BST/sapphire sample.

2. A seed layer composed of 20 nm Ti, 30 nm Ni and 50 nm Au was deposited by electron-beam evaporation onto the AZ5206E/BST/sapphire sample. In this process, electrons emitted from a filament are focussed electromagnetically onto a crucible containing the source material [51]. The high energy density causes the source material to evaporate, whereby it adsorbs on the substrate.

3. After the seed layer deposition, a seed pattern was formed by liftoff, where the metal on top of the photoresist is lifted off by placing the sample in an

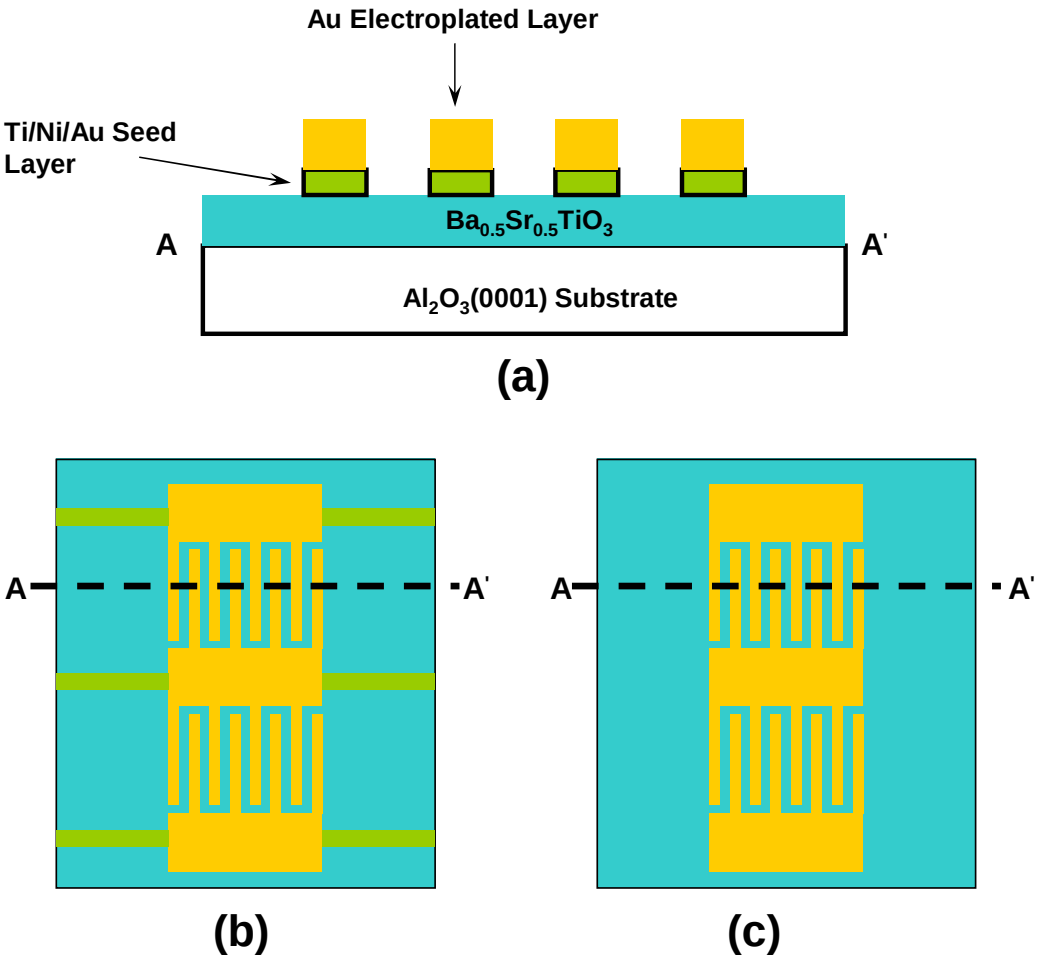


Figure 3.14: Illustration of the fabrication process for interdigital BST varactors: (a) Device cross-section, (b) top view before non-plated seed layer removal, and (c) top view after non-plated seed layer removal.

ultrasonic bath containing acetone.

4. A 2.5 μm Au layer was electroplated, using thick AZP4620 photoresist to define the plated regions of the seed layer. Note that the non-plated parts of the seed layer are necessary for electrical continuity.

5. Finally, the non-plated seed layer was removed by wet etching. The plated IDCs were masked off during this process to prevent damage to the devices during etching.

A series of IDCs with different electrode dimensions was realized, wherein the gap between the interdigital fingers ranged from 2 to 8 μm and the finger length from 90 to 130 μm; the finger width was fixed at 5 μm. Each IDC had two sets of interdigital electrodes, and was designed for probing in a 200 μm pitch ground-signal-ground (GSG) configuration. An array of fabricated BST varactors with adjacent open and short circuit calibration standards is shown in Fig. 3.15. The purpose of these on-wafer calibration standards is outlined later in this Section.

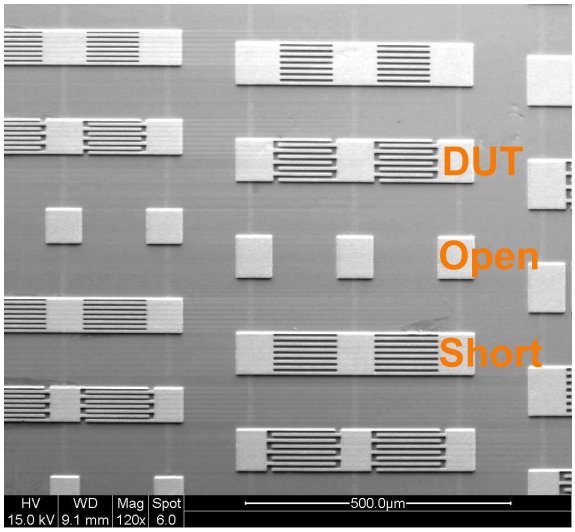


Figure 3.15: An array of interdigital capacitors with adjacent open and short circuit calibration standards.

Microwave measurements were performed on an Anritsu 37369A VNA connected to a wafer probe station. The experimental setup is shown in Fig. 3.16. A charge coupled device (CCD) camera and microscope were mounted above the sample so that manual adjustments could be viewed on a monitor adjacent to the VNA. Microwave wafer probes (40A-GSG-200-Q from GGB Industries) were mounted on Newport x-y-z micropositioners. Before calibrating the VNA, the wafer probes were

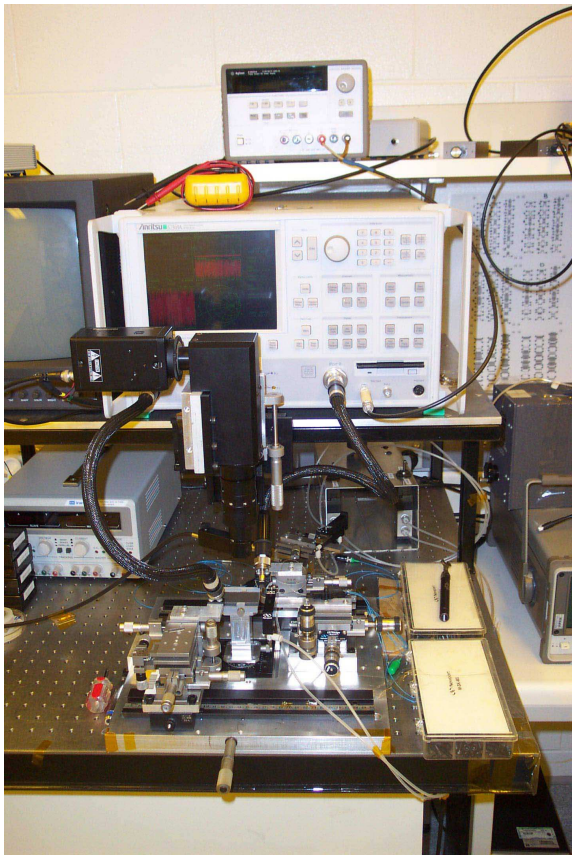


Figure 3.16: RMIT 40 GHz VNA and wafer probe station.

levelled by landing them on a Au plated dummy sample. The roll adjustment on the micropositioner was set so that all three pins on the GSG probe made an equal impression in the Au sample.

After levelling the wafer probes, calibration was performed using a CS-5 calibration substrate, also from GGB Industries. The alumina substrate contained an array of Au-plated open, short and 50 Ω load calibration standards, along with several different lengths of coplanar waveguide 50 Ω thru-lines. Both the SOLT and LRL/LRM calibration techniques were used to calibrate the VNA from 1 to 20 GHz. There was negligible difference between measured S-parameter results from the two calibration methods over this frequency range. Microwave S-parameters of the BST varactors were then obtained by landing one GSG probe on the IDC and saving the S_{11} data. DC bias was supplied to the IDCs via the internal bias tee on the VNA, and was therefore limited to ±40 V.

Initially, the IDCs were modelled by a series RC equivalent circuit. Using Agilent Advanced Design System (ADS), an optimisation routine was set up to fit the R and C values in the equivalent circuit to the measured S_{11} data. The ADS schematic

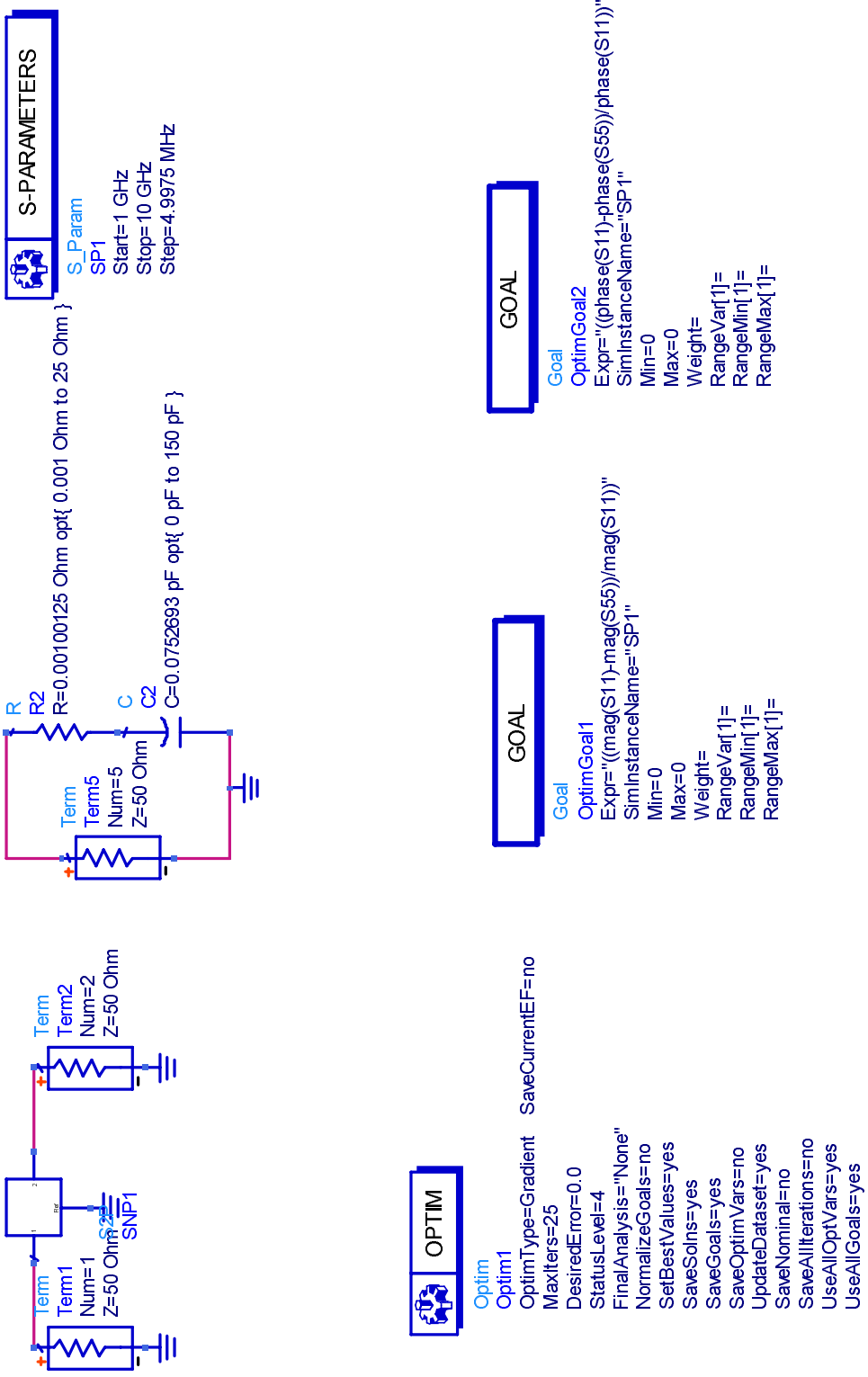


Figure 3.17: Series RC equivalent circuit model of the BST varactor implemented in Avanced Design System for extraction of varactor parameters from measured S-parameter data.

employed for the data extraction is shown in Fig. 3.17. From the extracted component values, the tunability and Q-factor of the varactors were calculated using Equations 3.7 and 3.8,

$$Tun = \frac{C_0 - C_{40}}{C_0} \times 100\% \tag{3.7}$$

$$Q = \frac{1}{\omega R_{BST} C_{BST}} \tag{3.8}$$

where C_0 and C_{40} are the extracted capacitance at zero and 40 V bias, respectively, ω is the radian frequency, and R_{BST} and C_{BST} are the extracted resistance and capacitance of the BST varactor at a given bias voltage. Although this approach works well over a relatively narrow frequency range (a few GHz), the optimisation in ADS did not converge well when fitting R_{BST} and C_{BST} over the entire 1–20 GHz frequency range. Another difficulty with using ADS for the data extraction is that frequency dependent component values are not easily handled by the software. For example, it should in principle be possible to obtain a better optimisation fit by allowing R_{BST} and C_{BST} to vary with frequency.

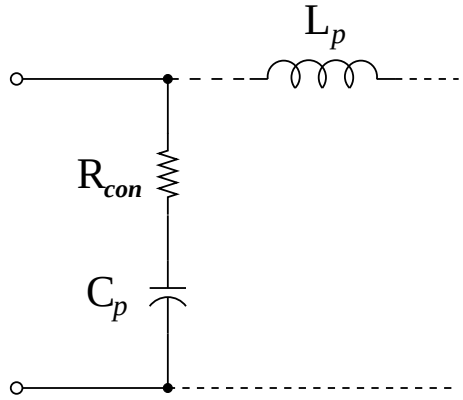


Figure 3.18: Equivalent circuit model of an open circuit BST varactor including pad parasitic components C_p and R_{con}.

In order to characterise the microwave properties of the varactors more accurately, it was necessary to de-embed the parasitic inductance, capacitance and resistance associated with the interdigital electrodes from the measured data, following the method described in [5, 118]. For this purpose, a set of open and short circuit calibration standards was patterned on the BST/sapphire sample adjacent to each IDC. The first step in the on-wafer calibration was to measure the S_{11} data of the open circuit standard. An equivalent circuit model for this standard is shown in Fig. 3.18, where C_p represents the parasitic capacitance associated with the IDC contact pads. In a slight modification to the Acikel model [5], R_{con} was added to the equivalent circuit model to account for the contact resistance. The complex input

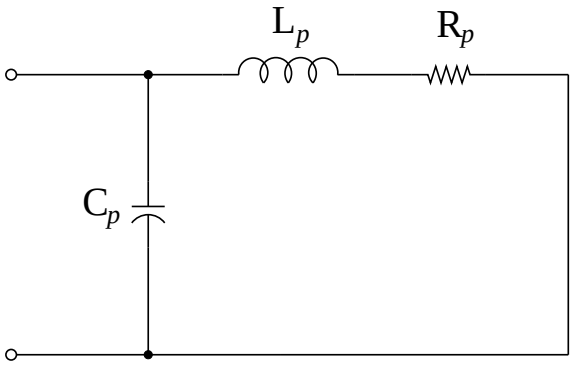


Figure 3.19: Equivalent circuit model of a short circuit BST varactor including pad parasitic components L$_p$, C$_p$ and R$_p$.

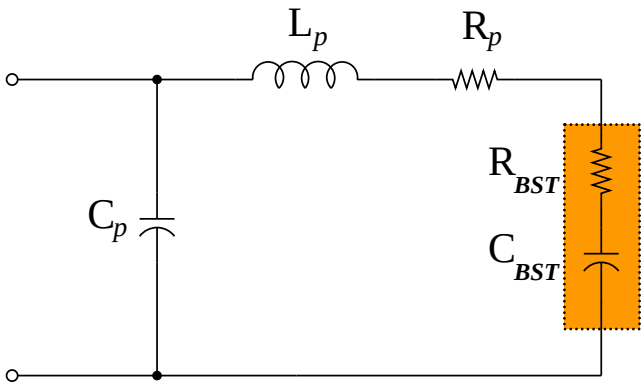


Figure 3.20: Equivalent circuit model of a BST varactor including pad parasitic components L$_p$, C$_p$ and R$_p$.

impedance of the equivalent circuit is

$$Z_L = R_{con} + \frac{1}{j\omega C_p} \tag{3.9}$$

An algorithm for fitting the equivalent circuit component values to measured S_{11} data was implemented in Matlab. The $fsolve$ routine, based on the nonlinear least squares method [119], was used to perform the optimisation. The Matlab code for this procedure (and also for the short circuit calibration standard and varactor device under test) can be found in Appendix A. The output of the optimisation routine was a vector containing the frequency dependent values of C$_p$.

The equivalent circuit model for the short circuit standard is shown in Fig. 3.19, where L$_p$ is the parasitic inductance of the interdigital electrodes and R$_p$ accounts for conductor loss associated with the electrodes. For the short circuit standard, the input impedance is

$$Z_L = \frac{R_p - j\omega R_p^2 C_p + j\omega L_p - j\omega^3 L_p^2 C_p}{(1-\omega^2 L_p C_p)^2 + (\omega R_p C_p)^2} \tag{3.10}$$

where the value for C_p is known from measuring the open circuit standard.

Having determined the values of R_p, C_p and L_p, the capacitance R_{BST} and resistance C_{BST} were determined by fitting the BST device under test (DUT) S_{11} reflection data to an equivalent circuit model which included the pad parasitics, shown in Fig. 3.20. For the DUT, the input impedance is given by

$$Z_L = \left\{ j\omega C_p + \frac{1}{j\omega L_p + R_p + R_{BST} + \frac{1}{j\omega C_{BST}}} \right\}^{-1} \tag{3.11}$$

Without modelling the contributions of R_p, C_p and L_p, significant variation in the extracted capacitance C_{BST} is observed over a broad frequency range. This is due in particular to the pad inductance L_p, which would cause self resonance of the varactor if the measurement frequency is high enough, or the capacitance C_{BST} is large enough to bring the self resonant frequency in to the 1 to 20 GHz band. Figure 3.21 illustrates the effect of including the electrode equivalent circuit model elements in the process of extracting the varactor capacitance C_{BST}. The apparent variation in C_{BST} with frequency that occurs when R_p, C_p and L_p are not modelled may be incorrectly attributed to dielectric dispersion, or variation in the BST film dielectric constant with frequency. Therefore, it is important to model the pad parasitics before drawing any conclusions regarding dispersion. From the results presented in

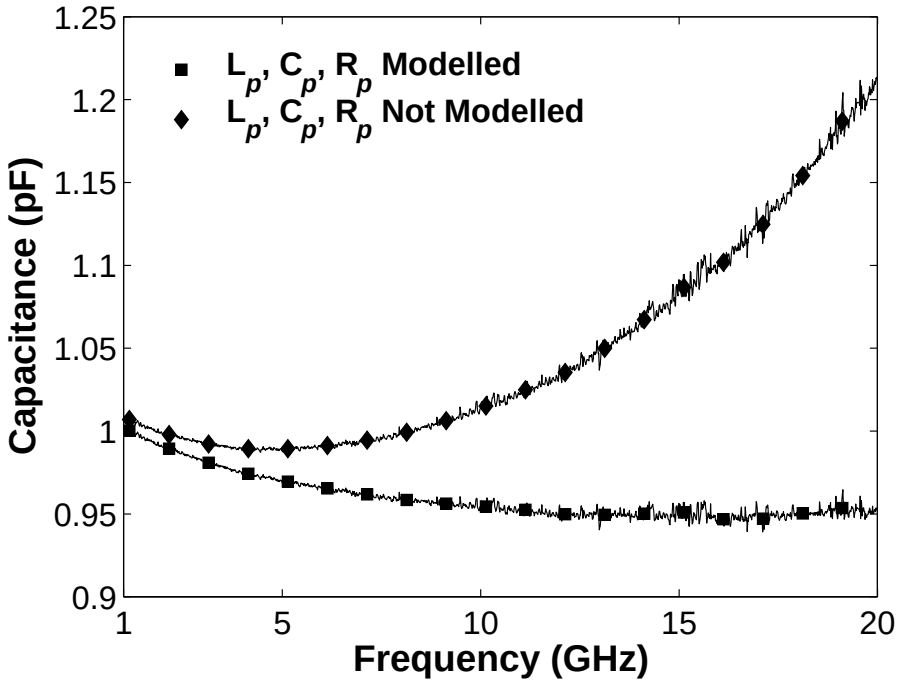


Figure 3.21: Extracted BST varactor capacitance (C_{BST}) with and without modelling the pad parasitics L_p, C_p and R_p.

Fig. 3.21, it may be concluded that the variation in the BST film dielectric constant from 1 to 20 GHz is around 5%. Due to the thick metal electrodes, the conductor losses were found to be negligible compared to the losses associated with the BST film.

Using the procedure outlined above, the microwave performance of the BST varactors was measured from 1 to 20 GHz. The initial series of samples deposited at 625°C showed limited capacitance tunability, as defined in Equation 3.7 of less than 2%. A rapid thermal anneal in air at ∼800°C for 60 sec improved the tunability to 5%. Increasing the deposition temperature to 700°C and employing a pre-deposition heat treatment of the substrate led to an improved capacitance tunability of ∼38%. This higher tunability can be attributed to the strongly (111) textured film growth, shown in Fig. 3.8(d).

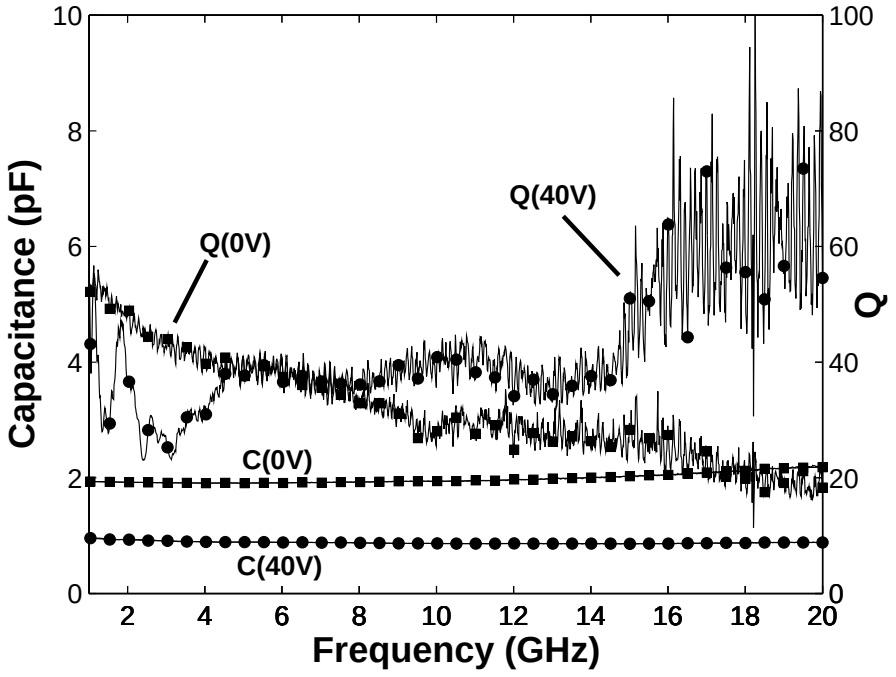


Figure 3.22: Extracted capacitance and Q-factor from 1 to 20 GHz at 0 and 40 V bias for 2 μm gap interdigital varactors. A pre-deposition heat treatment and 2 hour post-deposition anneal of the BST film were performed to increase the tunability.

Further improvement in tunability was achieved following a 2 hour post deposition anneal in air at 900°C. These results, presented in Fig. 3.22, show a capacitance tunability of ∼56% and Q_{min} of 25 at 10 GHz, for a bias field of 200 kV/cm. These results suggest that the increased grain size and strain relaxation observed following the post-deposition annealing procedure contribute to the improved tunability.

In a previously published result for a 100 nm $Ba_{0.7}Sr_{0.3}TiO_3$ thin film on c-plane sapphire, [88] the tunability reported was 16% at 200 kV/cm bias.

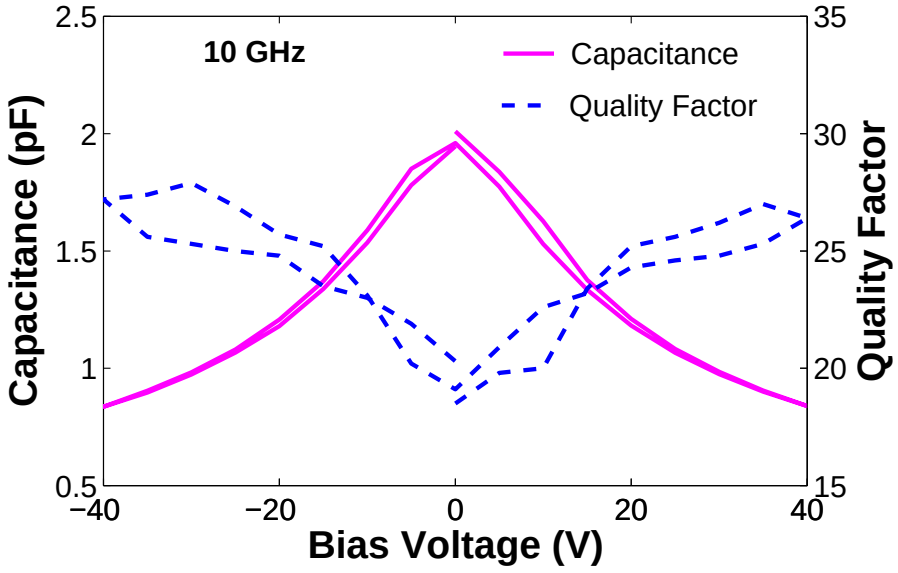


Figure 3.23: Capacitance and Q-factor versus applied voltage, measured at 10 GHz.

Figure 3.23 shows the field-dependent capacitance and Q-factor at 10 GHz for a BST varactor with 130 μm finger length and 2 μm gap. In this case, the measurement was performed by sweeping the bias voltage from 0 to +40 V, from +40 to -40 V and then back to 0 V, and recording S-parameter values at 5 V increments. A high tunability of ∼56% was observed with an applied field of 200 kV/cm. The Q-factor is better than ∼18 across the bias voltage range. Note that these measurements were for a different device than the one whose results are presented in Fig. 3.22. Some memory is apparent in both the capacitance and Q-factor variation as the bias voltage is swept. A possible cause is charge storage in a depletion layer at the electrode–BST interface [7].

3.5 Relative Permittivity of BST Film

In order to accurately design microwave circuits containing BST thin films, it is useful to determine the dielectric constant of a film prepared by a given set of processing conditions. A high dielectric constant in the BST film helps to reduce the size of varactors fabricated from the film. Also, BST films with high dielectric constant often have higher tunability than similar films with a lower dielectric constant [64].

There are several techniques available for microwave dielectric constant evaluation. In a non-destructive approach, a BST film can be placed on a microstrip

resonator [120, 121], where the dielectric constant of the film is determined by measuring the resonant frequency. Other non-destructive techniques include placing the sample in a waveguide [122], or between two dielectric resonators [123]. While these methods are useful for measuring the zero-bias dielectric constant of BST films, it is difficult to apply a large enough electric field to achieve significant dielectric tunability. An alternative approach is to incorporate BST films into parallel plate or interdigital capacitors. Large bias fields can be applied using this approach, and another advantage is that the devices can be employed in microwave circuits.

Determination of the BST film dielectric constant is straightforward in the case of a parallel plate varactor. The device capacitance is given by

$$C_{BST} = \varepsilon_o \varepsilon_r \frac{A}{d} \tag{3.12}$$

where C_{BST} is the varactor capacitance extracted from measured S-parameter data, A is the capacitor plate area and d is the BST film thickness, determined by profilometer measurements. The dielectric constant of the BST film, ε_r, is easily calculated from the measured capacitance using Equation 3.12. An alternative model proposed by Cramer et al. [65, 124] is also suitable for modelling parallel plate BST varactors.

The process for permittivity extraction from interdigital varactors is more complicated. A conformal mapping approach introduced by Gevorgian et al, [125, 126] is suitable for this purpose. The technique builds on earlier work, including papers by Alley [127], where a groundplane under the IDC is assumed, and Ghione and Naldi [128], where conformal mapping is used to analyse coplanar waveguides. The analysis steps outlined below follow directly from [126], unless otherwise stated.

A schematic diagram of an IDC with $n = 8$ fingers is shown in Fig. 3.24. In order to accurately model the IDC, three contributions to the total device capacitance are considered. These are C_n, the capacitance arising from the periodic $n - 3$ finger section; C_3, a capacitance contribution from the three outermost fingers (1.5 fingers on either side of the IDC); and C_{end}, a capacitance associated with the fringing fields at the ends of the interdigital fingers. Therefore, the total device capacitance is given by

$$C_{IDC} = C_3 + C_n + C_{end} \tag{3.13}$$

Given three dielectric layers (ε_1 - substrate, ε_2 - superstrate and ε_3 - capping layer), the contributions to the periodic section capacitance are (setting $\varepsilon_3 = 1$)

$$C_n = (n-3)\varepsilon_o \varepsilon_{en} \frac{K(k_o)}{K(k_o')} l \tag{3.14}$$

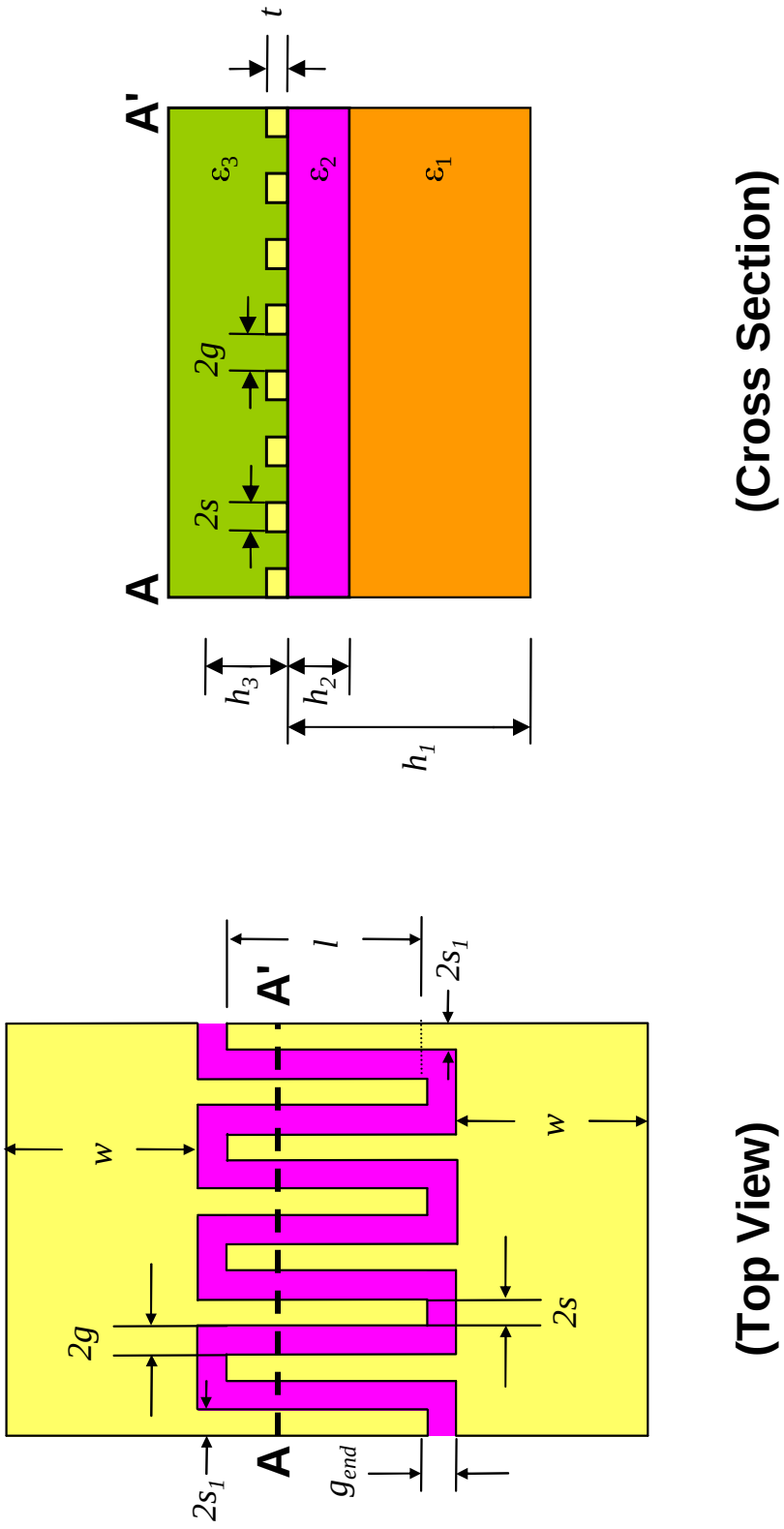


Figure 3.24: Schematic diagram of interdigital varactor structure with several dielectric layers - substrate (ε_1), BST film (ε_2) and capping layer (ε_3), based on [125].

where

$$\varepsilon_{en} = 1 + q_{1n}\frac{\varepsilon_1 - 1}{2} + q_{2n}\frac{\varepsilon_2 - \varepsilon_1}{2} \tag{3.15}$$

$$q_{in} = \frac{K(k_{in})}{K(k'_{in})}\frac{K(k'_o)}{K(k_o)} \tag{3.16}$$

$$k_0 = \frac{s}{s+g} \tag{3.17}$$

$$k'_0 = \sqrt{1 - k_0^2} \tag{3.18}$$

$$k_{in} = \frac{\sinh(\frac{\pi s}{2h_i})}{\sinh(\frac{\pi(s+g)}{2h_i})}\sqrt{\frac{\cosh^2(\frac{\pi(s+g)}{2h_i}) + \sinh^2(\frac{\pi(s+g)}{2h_i})}{\cosh^2(\frac{\pi(s)}{2h_i}) + \sinh^2(\frac{\pi(s+g)}{2h_i})}} \tag{3.19}$$

i = 1,2, $2s$ is the finger width, $2g$ is the finger spacing, h_i are the layer thicknesses, and l is the finger length, as shown in Fig. 3.24. Furthermore, $k'_{in} = \sqrt{1 - k_i^2}$ and $K(k)$ and $K(k')$ are elliptic integrals of the first kind.

For the three finger section, the capacitance is given by

$$C_3 = 4\varepsilon_o\varepsilon_{e3}\frac{K(k_{03})}{K(k'_{03})}l \tag{3.20}$$

where

$$\varepsilon_{e3} = 1 + q_{13}\frac{\varepsilon_1 - 1}{2} + q_{23}\frac{\varepsilon_2 - \varepsilon_1}{2} \tag{3.21}$$

$$q_{i3} = \frac{K(k_{i3})}{K(k'_{i3})}\frac{K(k'_{03})}{K(k_{03})} \tag{3.22}$$

$$k_{03} = \frac{s}{s+2g}\sqrt{\frac{1 - (\frac{s+2g}{3s+2g})^2}{1 - (\frac{s}{3s+2g})^2}} \tag{3.23}$$

$$k_{i3} = \frac{\sinh(\frac{\pi s}{2h_i})}{\sinh(\frac{\pi(s+2g)}{2h_i})}\sqrt{\frac{1 - \frac{\sinh^2(\frac{\pi(s+2g)}{2h_i})}{\sinh^2(\frac{\pi(3s+2g)}{2h_i})}}{1 - \frac{\sinh^2(\frac{\pi(s)}{2h_i})}{\sinh^2(\frac{\pi(3s+2g)}{2h_i})}}} \tag{3.24}$$

i = 1,2, and provided the widths of the external and periodic section fingers are the same. It is worth noting that the form of Equation 3.20 is different to that provided in [125, 126]. There is a small error in Equation (7) of [126] and Equation (15) of [125], where the prime symbol ($'$) appears in the argument of the numerator of the elliptic integral. This is inconsistent with earlier definitions (Equation (2) of [126] and Equation (10) of [125]) and most likely results from a direct application of equations contained in earlier work by Veyres and Hanna [129], where the arguments of the elliptic integral are defined differently. Although the influence of this error is negligible in IDCs with a large number of fingers, the effect is more significant

in IDCs with a small number of fingers, where the contribution of C_3 to the total capacitance C_{IDC} is larger. It is also worth pointing out that this error has been carried over into Equation (7.13) of Bahl's textbook [86], which references the work of Gevorgian et al. [125].

Finally, the capacitance associated with the finger ends can be calculated using

$$C_{end\infty} = 4s[n(2+\pi) - \pi]\varepsilon_o \varepsilon_{e,end\infty} \frac{K(k_{0e,end\infty})}{K(k'_{0e,end\infty})} \tag{3.25}$$

where

$$\varepsilon_{e,end\infty} = 1 + q_{1end\infty}\frac{\varepsilon_1 - 1}{2} + q_{2end\infty}\frac{\varepsilon_2 - \varepsilon_1}{2} \tag{3.26}$$

$$q_{iend\infty} = \frac{K(k_{iend\infty})}{K(k'_{iend\infty})}\frac{K(k'_{0end\infty})}{K(k_{0end\infty})} \tag{3.27}$$

$$k_{0end\infty} = \frac{x}{x + 2g_{end}} \tag{3.28}$$

$$k_{iend\infty} = \frac{\sinh(\frac{\pi x}{2h_i})}{\sinh(\frac{\pi(x+2g_{end})}{2h_i})} \tag{3.29}$$

i = 1,2, and infinite terminal width ($w \to \infty$) is assumed, since $w \gg 2g_{end}$. Equation 3.25 is slightly modified from the version supplied in [125], which is

$$C_{end\infty} = 4sn(2+\pi)\varepsilon_o \varepsilon_{e,end\infty} \frac{K(k_{0e,end\infty})}{K(k'_{0e,end\infty})} \tag{3.30}$$

The modification was made to reflect the fact that the fringing capacitance associated with the corners of the finger ends is smaller on the two outer fingers, since there is no adjacent electrode. This fact is not accounted for in the model of Gevorgian et al.

An algorithm for calculating the IDC capacitance C_{IDC}, was implemented in Matlab, based on code supplied as an Appendix in [64]. A complete listing of the Matlab code is provided in Appendix A of this thesis. In order to check the calculations, an array of IDCs was fabricated on a blank c-plane sapphire substrate (without depositing a BST film). Using the known dielectric constant of c-plane sapphire ($\varepsilon_r = 10.2$), the capacitance of an IDC with dimensions $t = 2.2$ μm, $2s = 2s_1 = 5$ μm, $2g = 2$ μm, $l = 100$ μm, $n = 8$, and $h_1 = 500$ μm, was calculated. The parameter x was set to 0.5, as suggested in [125]. The S-parameters of the same IDC were measured, and the capacitance was extracted using the procedure presented in Section 3.4. The measured value was 0.127 pF, while the calculated value with infinite width terminals was 0.120 pF. Therefore, it can be concluded that the analytical model is accurate to within 6 %.

Having verified the analytical model, it was now possible to extract the dielectric constant ε_r of the BST film from the measured capacitance values. This was done by modifying the value of ε_r in the Matlab code until good agreement with the measured capacitance was achieved. For a 700 nm thick BST film on c-plane sapphire, the zero-bias dielectric constant ε_r, increased from 280 (as-deposited) to 520 (post-deposition annealed), as determined by the conformal mapping technique.

3.6 Conclusions

This Chapter has presented a study of the material and microwave properties of sputtered $Ba_{0.5}Sr_{0.5}TiO_3$ films on c-plane sapphire substrates. Several different materials analysis techniques, including RBS, XPS and XRD were employed to characterise the composition and structural properties of the films. Interdigital electrodes were then patterned on the film surface to allow wafer-probed microwave measurements of the samples. Using an equivalent circuit model, the capacitance and Q-factor of the devices were extracted. Finally, the dielectric constant of the BST films was determined by a conformal mapping technique.

In order to optimise the composition of the films, a series of BST films were sputtered at 625°C with different process gas pressures in the range 5 to 40 mTorr. RBS measurements demonstrated that the stoichiometry of films sputtered at 40 mTorr was close to that of the $Ba_{0.5}Sr_{0.5}TiO_3$ sputtering target. This process gas pressure was therefore chosen for further experiments.

XRD measurements showed that films deposited at 625° were polycrystalline. Increasing the substrate temperature to 700°C and performing a pre-deposition heat treatment of the substrate resulted in highly <111> textured films. The structural relationship between the BST film and the sapphire substrate was examined by high resolution XRD measurements. Although the substrate imposed definite order on the BST films, the growth was not epitaxial. XRD measurements also showed reduced strain in the films following post-deposition annealing.

Microwave measurements of interdigital BST varactors fabricated on the films demonstrated high capacitance tunability (56% at 200 kV/cm bias field) and low loss ($Q > 15$ up to 20 GHz) for films deposited at 700°C with a pre-deposition heat treatment and post-deposition anneal. When correlated with the materials measurements, the increased tunability can be attributed to strain relaxation and larger grain size observed in the film after post-deposition annealing. Extraction of the varactor capacitance also permitted extraction of the BST film dielectric constant. These results showed a significant increase in the zero-bias dielectric constant

from 280 (as-deposited) to 520 (post-deposition annealed) for films deposited at 700°C with a pre-deposition heat treatment.

In order for BST-based microwave varactors to achieve commercial success, integration issues need to be considered. BST varactors on *c*-plane sapphire could potentially be integrated with GaN microwave power transistors, which can also be fabricated on *c*-plane sapphire substrates. However, the scope of this application is fairly limited. On the other hand, *r*-plane sapphire is widely used for commercial silicon on sapphire device technologies. The materials and microwave properties of BST films on *r*-plane sapphire are investigated in the next Chapter.

Chapter 4

BST Thin Films on *r*-plane Sapphire

4.1 Introduction

One of the challenges faced in fabrication of BST tunable components for microwave applications is the poor compatibility of BST with conventional Si-based semiconductor processes. A significant problem is the high deposition temperatures (typically 650 to 800°C) required to form the paraelectric perovskite phase of BST. In the parallel-plate capacitor architecture, it has been shown that thermal coefficient mismatch between the platinum bottom electrode and the Si substrate causes hillock formation, leading to short circuit devices [67]. Furthermore, the low resistivity of silicon makes the realization of low loss microwave transmission lines and passive components on silicon challenging.

Silicon on sapphire technology presents a possible solution to the integration of BST with semiconductor devices. In the SoS process, a thin ($\sim$0.5 μm) heteroepitaxial layer of Si is deposited on an *r*-plane sapphire substrate. Although high tunability BST films grown on *c*-plane sapphire have been developed as described in Chapter 3, this substrate orientation is not suitable for the growth of silicon on sapphire.

The main advantage of SoS over traditional bulk Si integrated circuits is high isolation between devices, which allows higher operating speed and lower power dissipation, and also minimizes the formation of parasitic semiconductor junctions [130]. Sapphire has excellent microwave properties compared to silicon, with a very high resistivity ($\rho = 10^{14}$ Ωcm [131]) leading to low substrate loss. This allows the formation of improved Q-factor on-chip inductors, thus overcoming a significant problem in bulk Si-based RF integrated circuits (RFICs). By depositing a BST layer on

sapphire early in the SoS process (before the contact metallization), the high substrate temperature can be tolerated without affecting the Si epilayer. Therefore, the advantages of SoS and tunable BST-based components can be combined to realize high performance RFICs.

Li et al. have demonstrated high tunability $Ba_{0.5}Sr_{0.5}TiO_3$ thin films on SiO_2 on r-plane sapphire [132]. The BST film was grown on Si/Al_2O_3 , and the underlying Si layer was converted to amorphous SiO_2 by annealing at 1000°C for 48 hours in an oxygen atmosphere. The microwave properties of $Ba_{0.65}Sr_{0.35}TiO_3$ films grown on r-plane sapphire with a $SrTiO_3$ buffer layer have also been reported by Hollman et al. [133]. Recently, the properties of a 1 μm thick $Ba_{0.5}Sr_{0.5}TiO_3$ film deposited by RF magnetron sputtering on r-plane sapphire were investigated and compared to identical films on MgO, Si and c-plane sapphire substrates [87]. However, there has been no comprehensive investigation into the thickness dependent properties of BST films grown directly on r-plane sapphire.

This Chapter investigates the microwave properties of $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown by PLD on r-plane sapphire. The work was done in collaboration with the Electroceramics Research Group at Rutgers University, New Jersey, USA. Deposition of the BST films and XRD measurements were performed at Rutgers, while the interdigital electrode metallisation and microwave measurements were performed at RMIT. Raman measurements were also performed on the films at Trinity College, Dublin, Ireland, to investigate the lattice vibrational modes of the BST films.

4.2 Pulsed Laser Deposition of BST Thin Films

There are many reports on the preparation of BST thin films by PLD [41,42,44,108, 134]. PLD, like sputtering, is performed inside a vacuum chamber. Instead of using a DC/RF power supply to ionise the process gas, resulting in ion bombardment of the target, PLD employs a high power laser to ablate the target material. A general introduction to the PLD process is provided below, followed by a description of the Rutgers PLD system, and the process used to deposit $Ba_{0.6}Sr_{0.4}TiO_3$ thin films on r-plane sapphire.

4.2.1 Introduction to Pulsed Laser Deposition

Pulsed laser deposition, like sputtering, is part of the PVD group of processes. PLD targets are somewhat smaller and therefore cheaper than sputtering targets. This means that new target compositions are easily fabricated and fitted into the

deposition system, resulting in low cost and fast turnaround time for trialling new thin film compositions.

The factors that affect film growth by PLD include the process gas pressure, the substrate to target distance, the laser fluence or energy density, the laser pulse repetition rate, and the laser spot size [64]. Because of the existing work on BST thin films prepared by PLD, the deposition conditions reported by other research groups [41,42,44,108,134] serve as a good reference for establishing a set of processing parameters that results in stoichiometric, single phase BST films.

In the PLD system, both the target and the substrate are located inside a vacuum chamber. Laser light enters the deposition chamber through a transparent window, and is focussed on to the target material. During a laser pulse, the energy density at the target is sufficiently high to eject atoms from the target. The ablated atoms then travel to the substrate inside a vapour plume. Some of this vapour condenses on the substrate, due to the free energy difference between the solid and vapour phase of the ablated target material [135]. Successive laser pulses lead to the formation of a thin film. A particular advantage of PLD is that the composition of the vapour plume is identical to that of the target material, regardless of the vapour pressures of the constituent atoms [135], which facilitates stoichiometric film growth. For ceramic oxides, such as BST, an O_2 process gas is used to minimise oxygen vacancies in the deposited thin film. Unlike sputtering, PLD does not rely on ion bombardment to eject target atoms; therefore, a 100 % O_2 process gas is used, rather than an Ar/O_2 gas mixture.

4.2.2 Rutgers Pulsed Laser Deposition System

A schematic diagram of the Rutgers Electroceramics Research Group PLD system is shown in Fig. 4.1. In this system, a KrF ultraviolet (UV) excimer laser ($\lambda = 248$nm) with 2 J/cm^2 fluence and 2 Hz repetition rate was used for the experiments. Figure 4.2(a) shows the deposition chamber and some of the ancillary equipment. The Rutgers PLD system had previously been used to grow epitaxial $Ba_{0.6}Sr_{0.4}TiO_3$ films on cubic MgO and $LaAlO_3$ [44, 136] and orthorhombic $NdGaO_3$ [39, 40, 137] substrates. During the initial characterisation of the system, the stoichiometry of the $Ba_{0.6}Sr_{0.4}TiO_3$ films was verified by RBS [64].

The vacuum system employed a TMP backed by a rotary vane pump, which was used to evacuate the PLD system to high vacuum. A separate, stand-alone rotary pump was used to evacuate the system to low vacuum before starting the TMP, and also to maintain the O_2 process gas pressure during deposition.

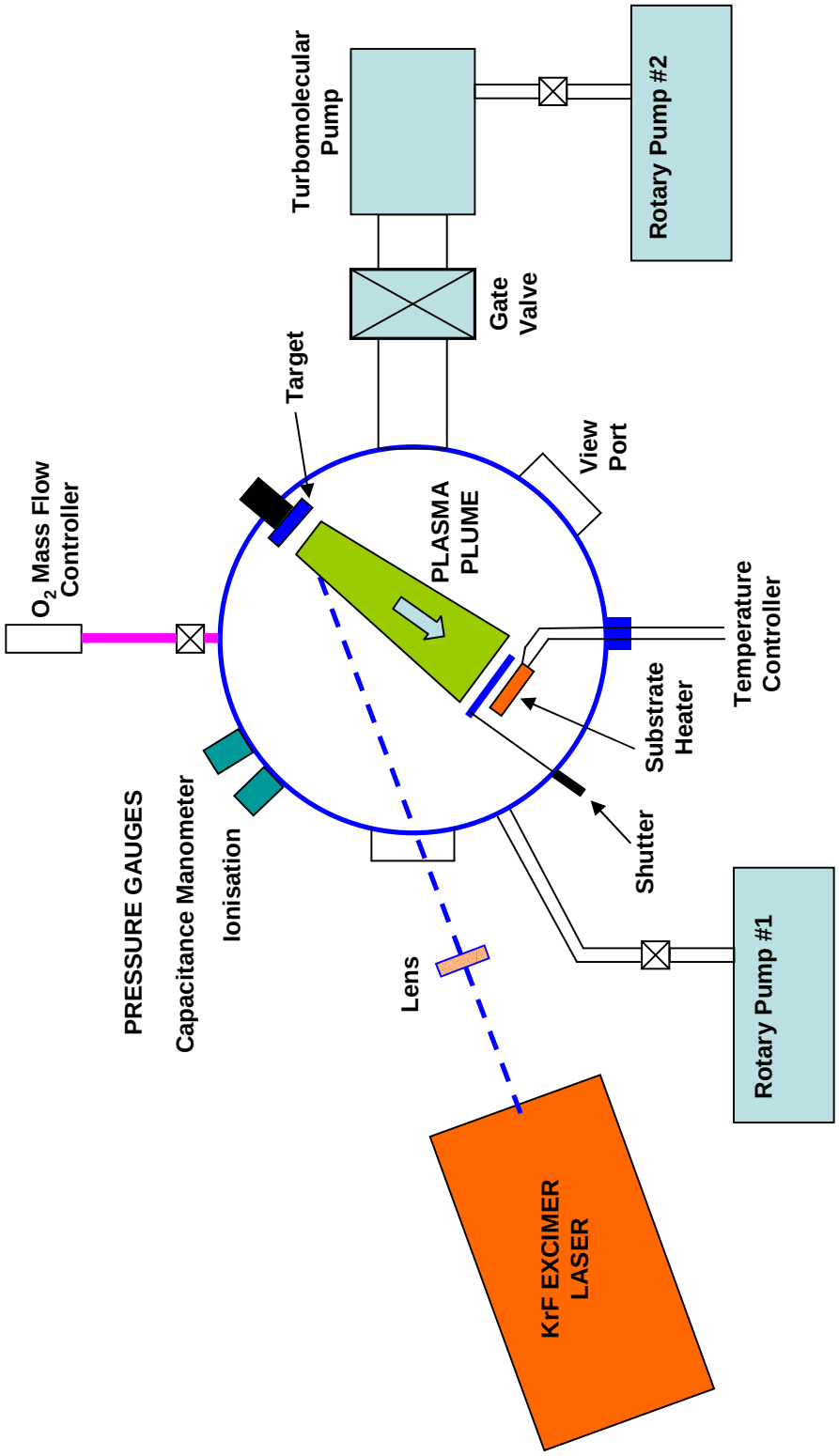
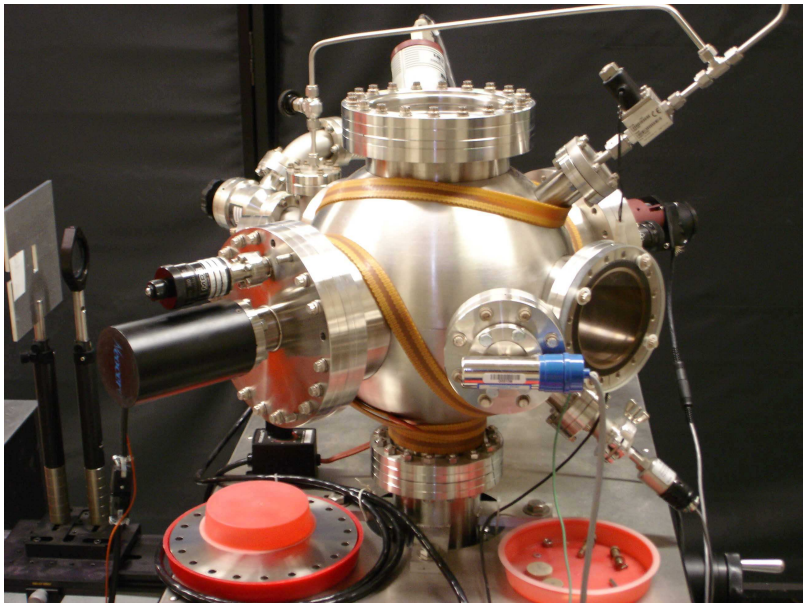
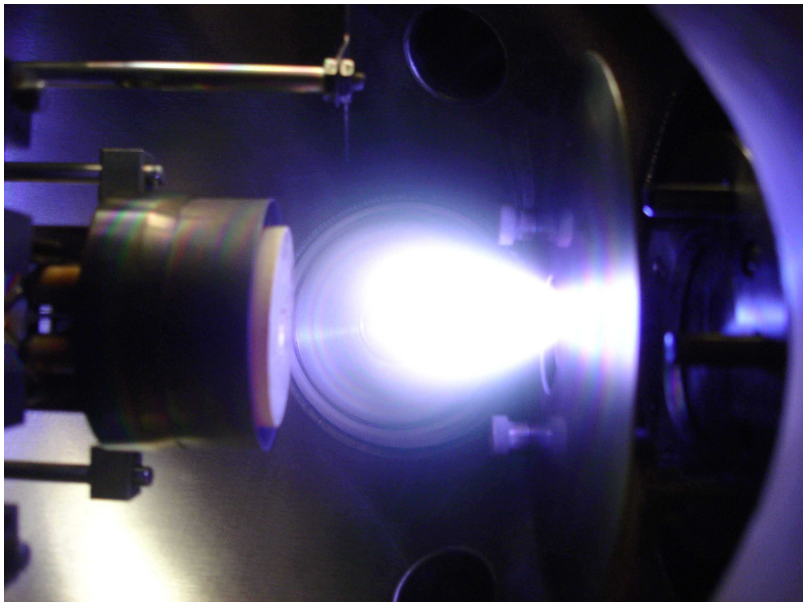


Figure 4.1: Schematic diagram of the Rutgers PLD system.



(a)



(b)

Figure 4.2: Photographs of the PLD system at Rutgers University - (a) vacuum chamber and ancillary equipment and (b) plasma plume incident on the substrate heater during a KrF laser pulse.

4.2.3 Deposition of BST Thin Films on *r*-plane Sapphire

All depositions were performed from a stoichiometric, one inch diameter $Ba_{0.6}Sr_{0.4}TiO_3$ circular target. The target was mounted on a rotating chuck, in order to ablate the target material uniformly from a circular track (rather than from a single point on the target).

The sapphire substrate dimensions were 10 × 10 × 0.5 mm^3; these were purchased from Techno Chemics. Before mounting the substrates in the deposition chamber, each sample was cleaned with acetone, methanol and de-ionised water. Samples were then attached to the heater block using silver paste to ensure good thermal contact. At this point, the vacuum chamber was sealed, and the pump-down sequence was initiated. A base pressure of 5 to 8×10^{-6} mTorr was achieved after 90 minutes of pumping with the TMP.

After reaching base pressure, the gate valve between the deposition chamber and the TMP was closed, and a 100 mTorr O_2 atmosphere was established in the chamber using a mass flow controller and the second rotary pump. Prior to deposition, the substrates were in-situ annealed in 100 mTorr flowing oxygen for 60 minutes at 700°C , in order to remove organic contaminants from the film surface [64].

At this point, the KrF excimer laser was switched on, and allowed to warm up for at least 5 minutes. A laser power meter was placed in the beam path to confirm the desired 2 J/cm^2 fluence. The BST target was then ablated for ∼5 minutes with the shutter closed to remove any surface contamination on the target. Deposition of the BST film was then initiated by opening the shutter between the target and the substrate. The substrate temperature and oxygen pressure in the chamber were maintained at 700°C and 100 mTorr, respectively, during deposition. Films of thickness 25, 50, 100, 200 and 400 nm were deposited in separate runs. All of the samples were post-deposition annealed inside the chamber at 700°C under 1 atm. oxygen pressure for 6 hours before cooling to room temperature.

4.3 Materials Analysis

Following the deposition of the BST films, a series of measurements relating to the materials properties of the films were performed. Since the stoichiometry of $Ba_{0.6}Sr_{0.4}TiO_3$ films deposited by PLD at Rutgers had been established in earlier work [64], there was no need to perform RBS or XPS measurements. However, an important objective was to characterise the structural properties of BST films grown on *r*-plane sapphire, and to measure the strain variation in the films as a function

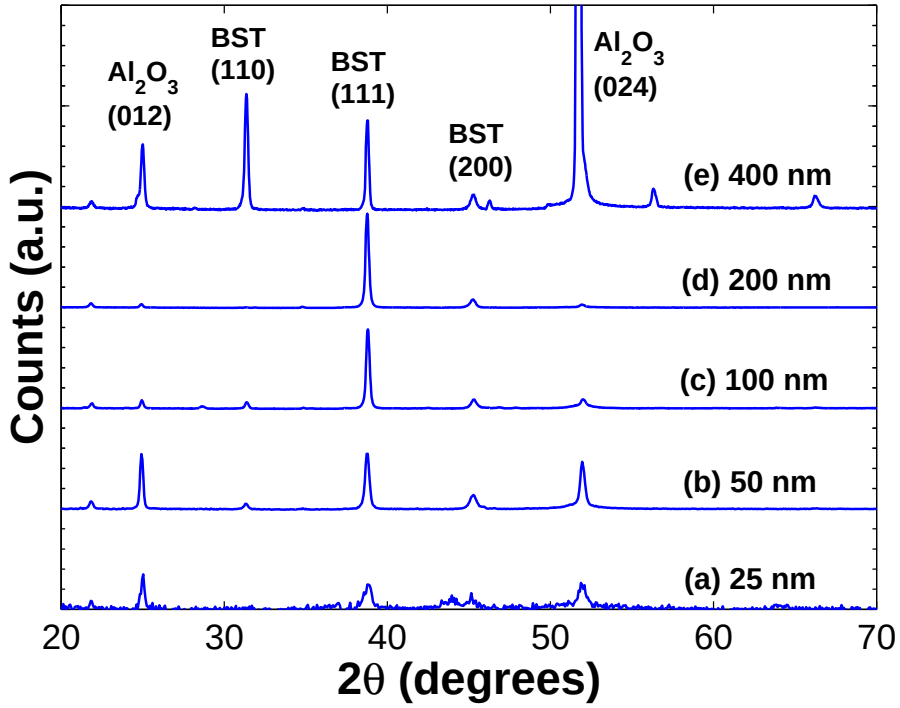


Figure 4.3: XRD patterns for polycrystalline BST thin films of thickness 25 to 400 nm on r-plane sapphire.

of film thickness. The crystal structure and residual strain were measured by XRD. Following the XRD measurements, an AFM was employed to measure the surface morphology of the films. Finally, the vibrational modes of the BST lattice were measured by Raman spectroscopy, confirming the single phase perovskite nature of the films.

4.3.1 X-Ray Diffraction

An XRD θ–2θ scan was performed on each of the samples, using a Siemens D500 diffractometer with a Cu K_α line source. As shown in Fig. 4.3, these scans indicate that films of all thicknesses were single phase and polycrystalline. Epitaxial film growth is precluded since the r-plane sapphire does not provide a lattice-matched growth surface for BST. Furthermore, it was found that the films are increasingly <111> oriented by monitoring the intensity of the (111) reflection as the thickness increases from 25 to 200 nm as shown in Fig. 4.3 (a)-(d). However, in Fig. 4.3 (e), a strong <110> BST peak is evident for the 400 nm film, indicating that the texture becomes bi-modal at higher thicknesses in such polycrystalline BST films.

Many reports have demonstrated a link between tunability and strain in BST

thin films, both experimentally [39, 40, 137] and theoretically [22]. High tunability is typically achieved when the residual stress in the film is vastly relaxed as the film thickness is increased [39, 40, 137]. The XRD $\sin^2\psi$ technique introduced in Section 3.3.4 was employed to determine the effect of the film thickness on the in-plane strain. Scans performed in two mutually perpendicular in-plane directions ($\phi = 0, 90°$) revealed no significant difference in the slope of the d–$\sin^2\psi$ characteristic traces. Therefore, both the in-plane and perpendicular shear stress components were inferred to be zero, resulting in an equal biaxial state of stress in the 50 to 200 nm films [24]. Using the linear theory of elasticity in conjunction with elasticity data [20] for BST 60/40, the in-plane strains were computed as depicted in Fig. 4.4. For the series of films, the strain was calculated according to Equation 3.6. The tensile residual misfit strain varies from 2.0% at 50 nm film thickness to ∼0.5% at 100 nm, followed by a decrease to ∼0% at 200 nm. Films greater than 200 nm in thickness are under a compressive state of strain, which reaches a magnitude of -0.6% at 400 nm. No strain data for the 25 nm film is presented due to the lack of a sufficiently strong high-angle diffraction peak suitable for stress measurement.

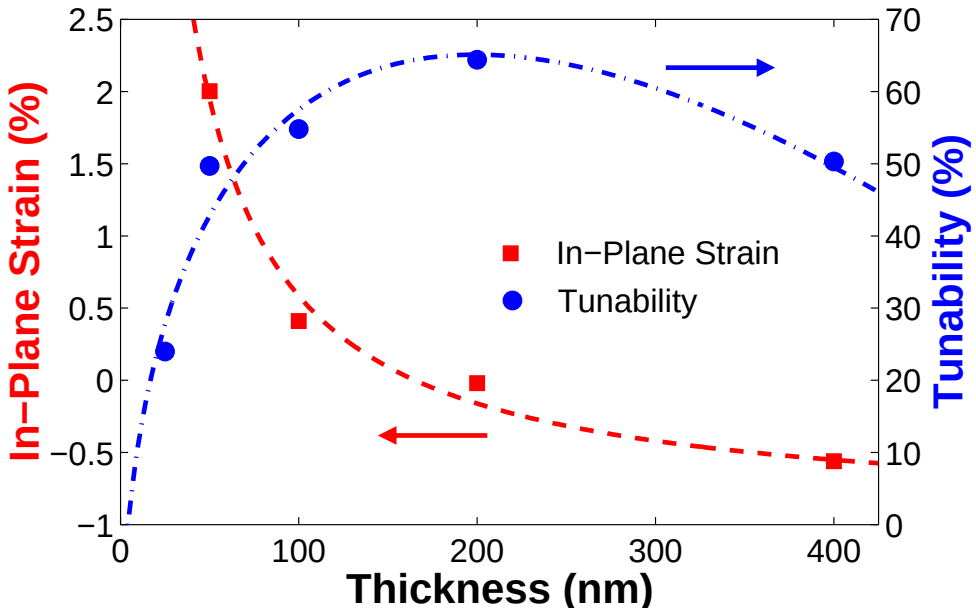


Figure 4.4: In-plane strain and capacitance tunability as a function of film thickness. The measured values and trend lines are represented by points and dashed lines, respectively.

This switch from tensile to compressive stress with increasing film thickness is attributed to the TEC mismatch between the substrate and the film. Noting that the dislocation slip system is $\{101\}\ <10\bar{1}>$ in perovskites [138], the development of

strong <110> texturing in the 400 nm film should in principle be due to the TEC mismatch-induced loss of crystallographic coherence arising from shear stresses on {110} planes and in <110> directions.

4.3.2 Atomic Force Microscopy

Measurements of the surface roughness and grain size of the films were obtained using a Solver AFM at Swinburne University, Australia. The average roughness parameter (R_a) varied from 2.2 nm for the thinnest (25 nm) film to 8.2 nm for the thickest (400 nm) film, which are consistent with epitaxial BST films deposited on MgO, $LaAlO_3$ and $NdGaO_3$ substrates using the same deposition system and similar PLD deposition parameters [39, 44, 136]. It was found that the grain size increased with film thickness, from ∼50 nm in the 25 nm film to ∼100 nm in the 400 nm film.

It has been suggested that small grain size, which leads to greater grain boundary area, and the associated interfacial capacitance is a major contributing factor to the lower permittivity observed in BST thin films relative to bulk ceramics of the same composition [11]. The larger grain size observed in the thickest BST/sapphire films is indicative of an island (Volmer–Weber) growth mechanism, where grain coalescence and therefore larger grain size is expected as the film thickness increases [51].

4.3.3 Raman Spectroscopy

Raman spectroscopy is an optical technique which is useful for measuring the lattice vibrational modes of a sample material. An incident photon, supplied by a laser, for example, undergoes an inelastic scattering collision with a crystal. In this process, a phonon, or lattice vibration is either created or destroyed [107]. Absorption of a phonon means that scattered photons have a higher energy than the incident photons. Photons scattered following the creation of a phonon will have a lower energy. Therefore, there are two separate regions in a Raman spectrum; the Stokes region is associated with the creation of a phonon, while the Anti-Stokes region is associated with the absorption of a phonon [107].

The experimental setup for Raman measurements generally consists of a laser excitation source coupled with a spectrometer and CCD detector to measure the scattered photon spectrum. The advantages of lasers, compared to arc lamp light sources, include monochromatic radiation, which simplifies the analysis of the spectrum, and high intensity of illumination, which provides a good signal to noise ratio [139].

Raman measurements of the PLD deposited $Ba_{0.6}Sr_{0.4}TiO_3$ films on r-plane

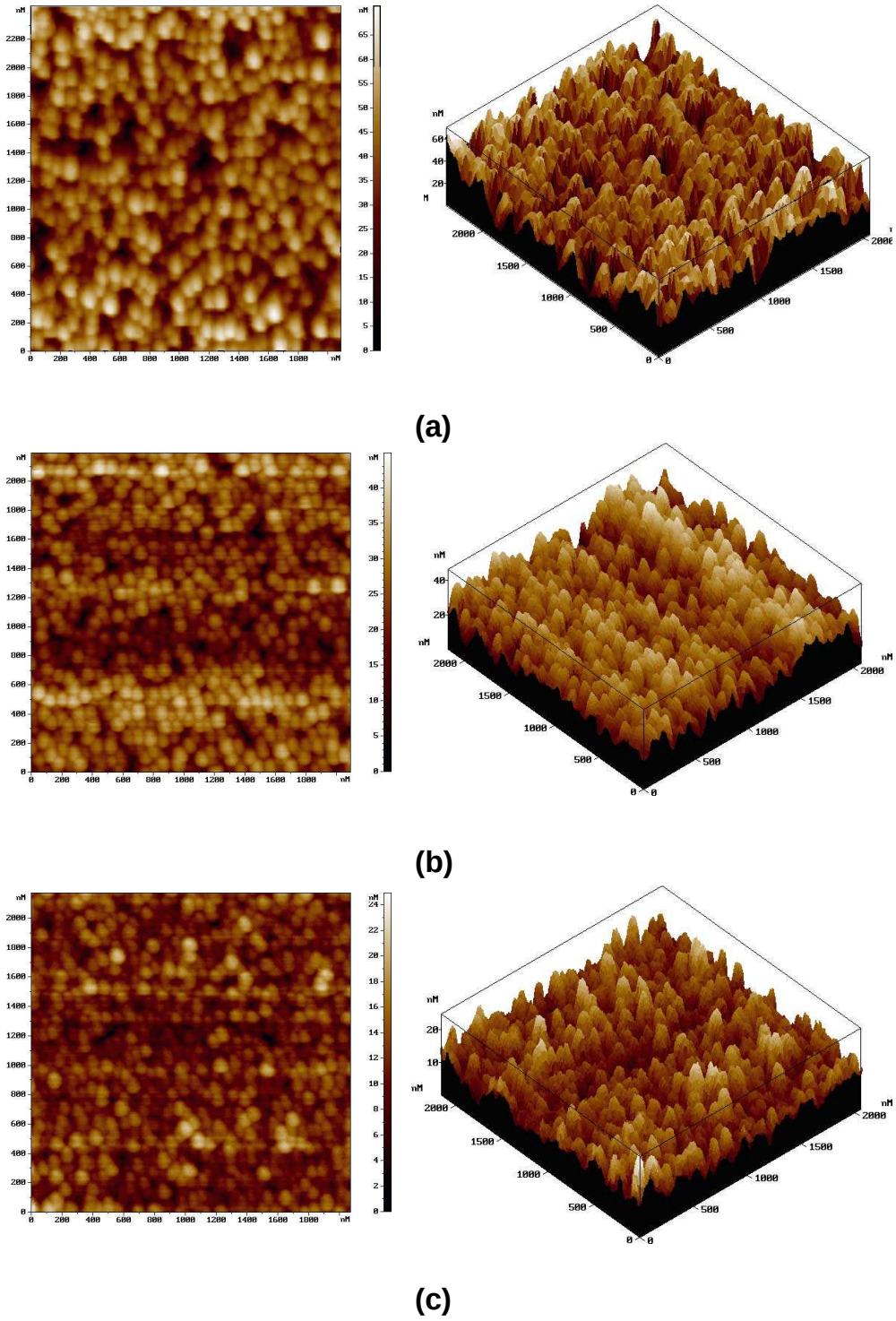
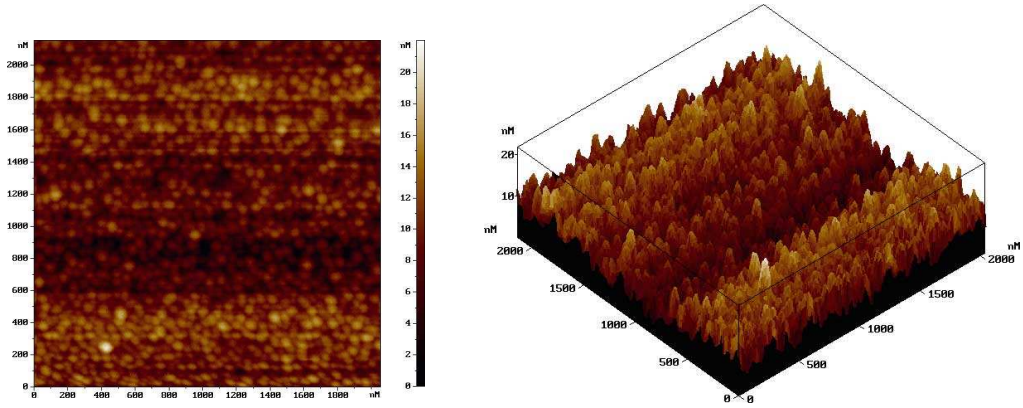
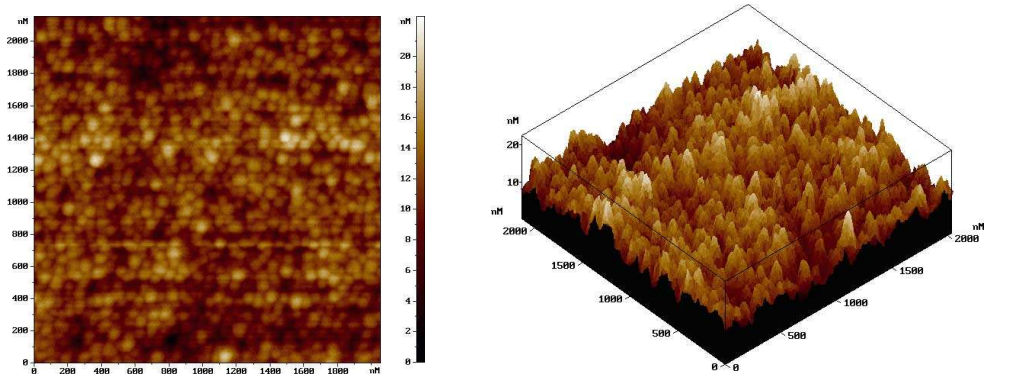


Figure 4.5: AFM images (∼2×2 μm^2) of (a) 400 nm, (b) 200 nm and (c) 100 nm $Ba_{0.6}Sr_{0.4}TiO_3$ thin films deposited on r-plane sapphire by PLD.



(d)



(e)

Figure 4.5 (continued) AFM images (~2×2 μm^2) of (d) 50 nm and (e) 25 nm $Ba_{0.6}Sr_{0.4}TiO_3$ thin films deposited on *r*-plane sapphire by PLD.

sapphire were carried out at Trinity College, University of Dublin, Ireland. The measurements were performed on a Renishaw 1000 micro-Raman system, with a 514.5 nm Ar^+ laser and a spectral resolution of $\sim$2.5 cm^{-1}. The spectra were recorded in the perpendicular polarisation configuration $z(x,y)\bar{z}$, where z is normal to the plane of the film [25]. Note that the measurements were performed after electrode metallisation on the samples. However, because the incident beam was focussed to a spot size of $\sim$3 μm, the measurements were easily taken by scanning between the electrodes of the 8 μm gap interdigital varactors. Therefore, the electrode metallisation did not interfere with the measurements.

Figure 4.6 shows the results of Raman measurements performed on the series of films at room temperature. The peaks near 220 cm^{-1} and 540 cm^{-1} are attributed to the TO_2 and TO_4 phonon modes in BST, respectively [25]. The remaining peaks in the spectrum can be attributed to modes associated with the sapphire substrate. This was confirmed by scanning a region where the BST film had been etched away; as shown in Fig. 4.7, no BST modes are present in this region.

Raman spectroscopy provides a means of identifying impurities in thin films [140], and is generally more sensitive to amorphous phases than XRD [141]. The absence

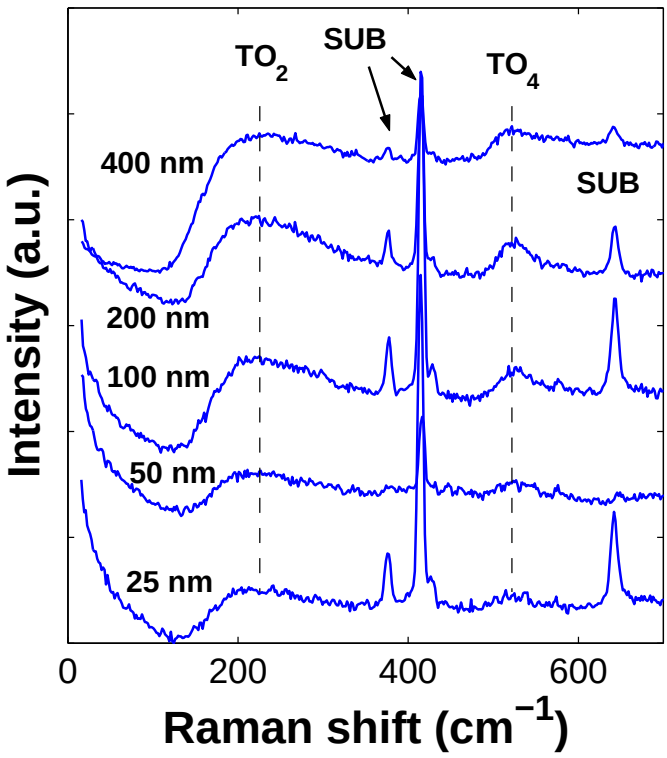


Figure 4.6: Raman spectra of $Ba_{0.6}Sr_{0.4}TiO_3$ films on r-plane sapphire at room temperature (298°C).

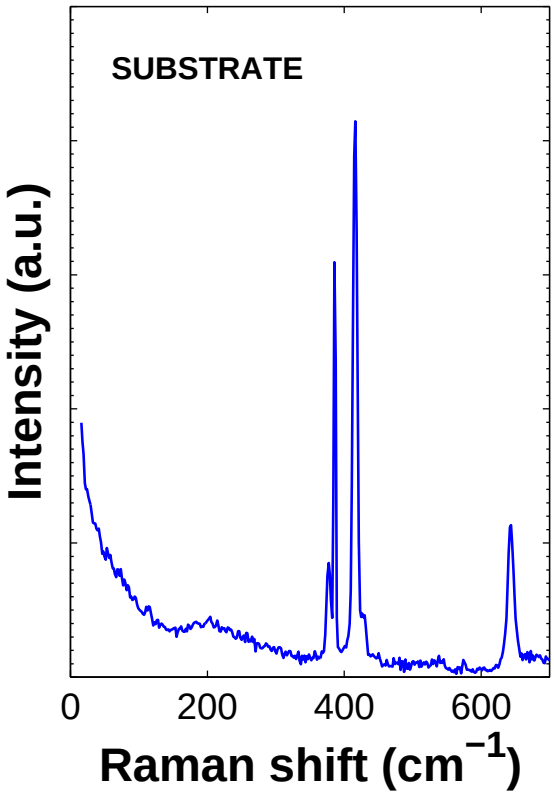


Figure 4.7: Room temperature Raman spectrum of r-plane sapphire substrate.

of any unexplained peaks in Fig. 4.6 shows that no impurities were introduced during film growth or subsequent processing. By comparing these results with other Raman measurements of BST thin films [25,140,142,143], the single phase perovskite nature of the films is confirmed. The large FWHM of the peaks associated with the BST film, relative to the substrate peaks, may be due to A-site cation (Ba/Sr) inhomogeneity and/or stress in the film [110].

4.4 Microwave Characterisation

Interdigital capacitors with adjacent open and short-circuit calibration standards were fabricated on the surface of the BST films by the method introduced in Chapter 3. The mask set used for BST varactors on r-plane sapphire was identical to the one used for the c-plane sapphire devices; the dimensions of the devices were therefore the same as those described in Section 3.4.

The experimental procedure for the microwave characterisation of the BST varactors on r-plane sapphire was identical to the c-plane sapphire devices. Full details of the procedure can be found in Section 3.4; the results presented here are for 2 μm gap

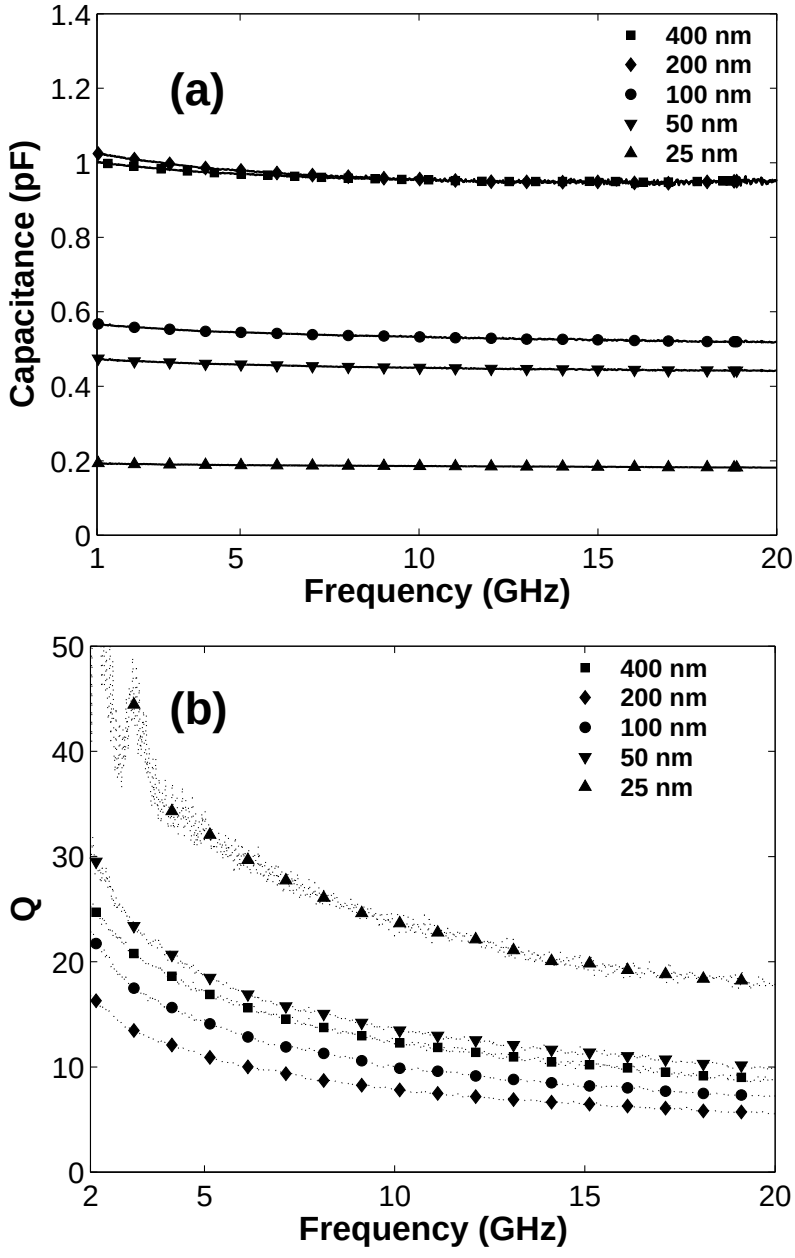


Figure 4.8: Measured zero bias performance of BST varactors as a function of film thickness: (a) capacitance C_{BST}, and (b) Q- factor.

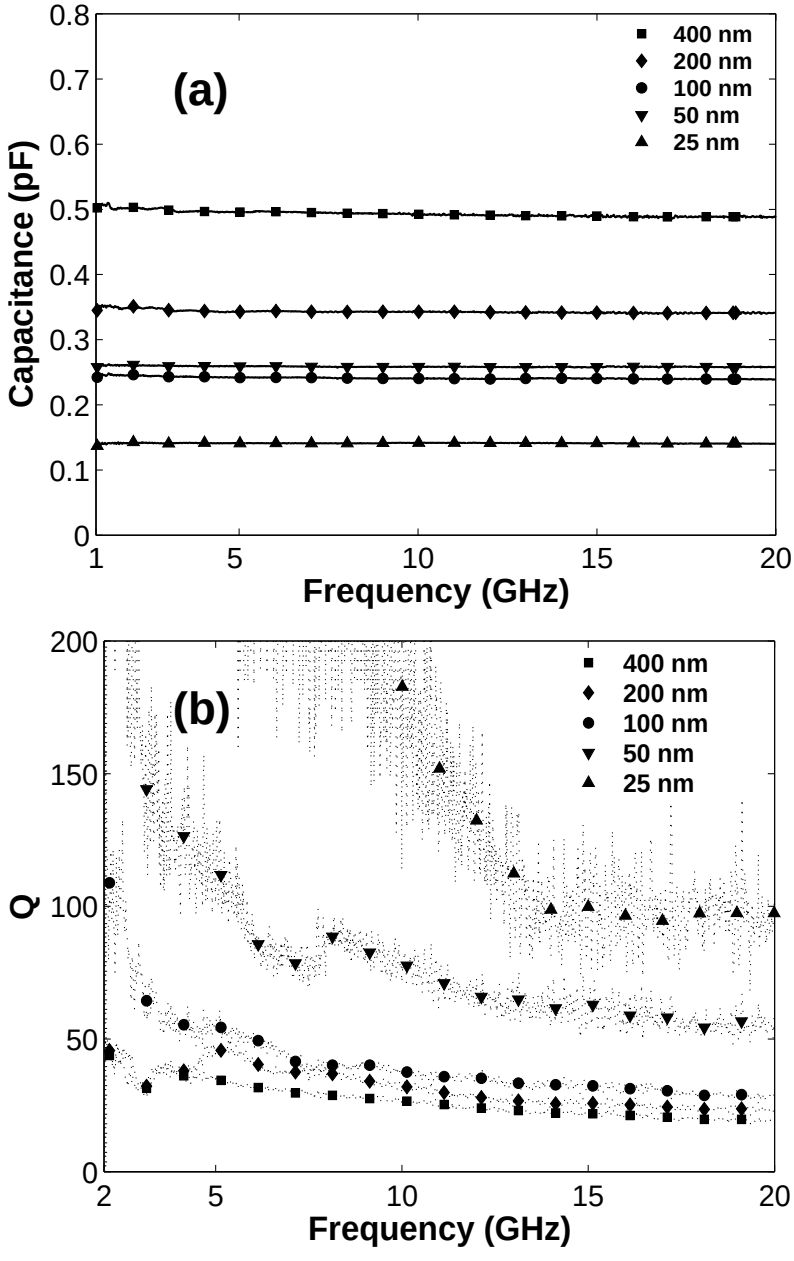


Figure 4.9: Measured 40 V bias performance of BST varactors as a function of film thickness: (a) capacitance C_{BST}, and (b) Q- factor.

devices. A high capacitance tunability of 64%, calculated as $[C(0) - C(40)]/C(0)$, was observed for the 200 nm film device. In the same device, a zero-bias Q-factor of ∼8 at 10 GHz was calculated using a series RC circuit to model the BST varactor [5]. The lowest tunability and best Q-factor of the series (24% and ∼23 at 10 GHz; respectively) were observed for the 25 nm film device. Figures 4.8 and 4.9 show the capacitance and Q-factor at 0 and 40 V, respectively. These results are summarised in Table 4.1.

Film Thickness (nm)	**C(0 V)** (pF)	**C(40 V)** (pF)	**Tun** (%)	Q**(0 V)**	Q**(40 V)**
25	0.19	0.14	24	22.9	180
50	0.45	0.26	43	13.4	78.3
100	0.53	0.24	55	9.90	37.8
200	0.96	0.34	64	7.80	32.2
400	0.99	0.49	50	11.8	26.9

Table 4.1: Summary of the microwave results for IDCs with $Ba_{0.6}Sr_{0.4}TiO_3$ thin films on r-plane sapphire.

Figure 4.10 shows the thickness dependence of the microwave properties of the devices. In Fig. 4.10(a), the strong dependence of the capacitance on film thickness can be seen. Figure 4.10(b) shows the dielectric permittivity, ε_r, and Q-factor variation with film thickness. The permittivity of the films was calculated by the conformal mapping technique introduced in Section 3.5. Note than an approximation for the elliptic integral argument (Equation (14) of [125]) was applied to avoid numerical problems in analysis of the ultra-thin 25 nm film. A significant decrease in the permittivity is observed between the 200 nm and 400 nm films, and is correlated with increasing compressive stress in the film and a larger grain size in the 400 nm film than the 200 nm film. The loss of crystallographic coherence in the 400 nm film may also contribute to the reduced permittivity. In the thinner films, ε_r decreases due higher tensile strain and reduced grain size.

Comparing the variation of tunability with the variation of residual misfit strain (Fig. 4.4), a trade off between strain and tunability is apparent. The observed behaviour parallels the one observed in epitaxial films [39, 40, 44, 136, 137], which indicates that the strain effect on tunability is in fact a universal phenomenon. Therefore, the polycrystalline (as opposed to epitaxial) nature of the films does not affect the overall strain dependence of tunability in paraelectric BST.

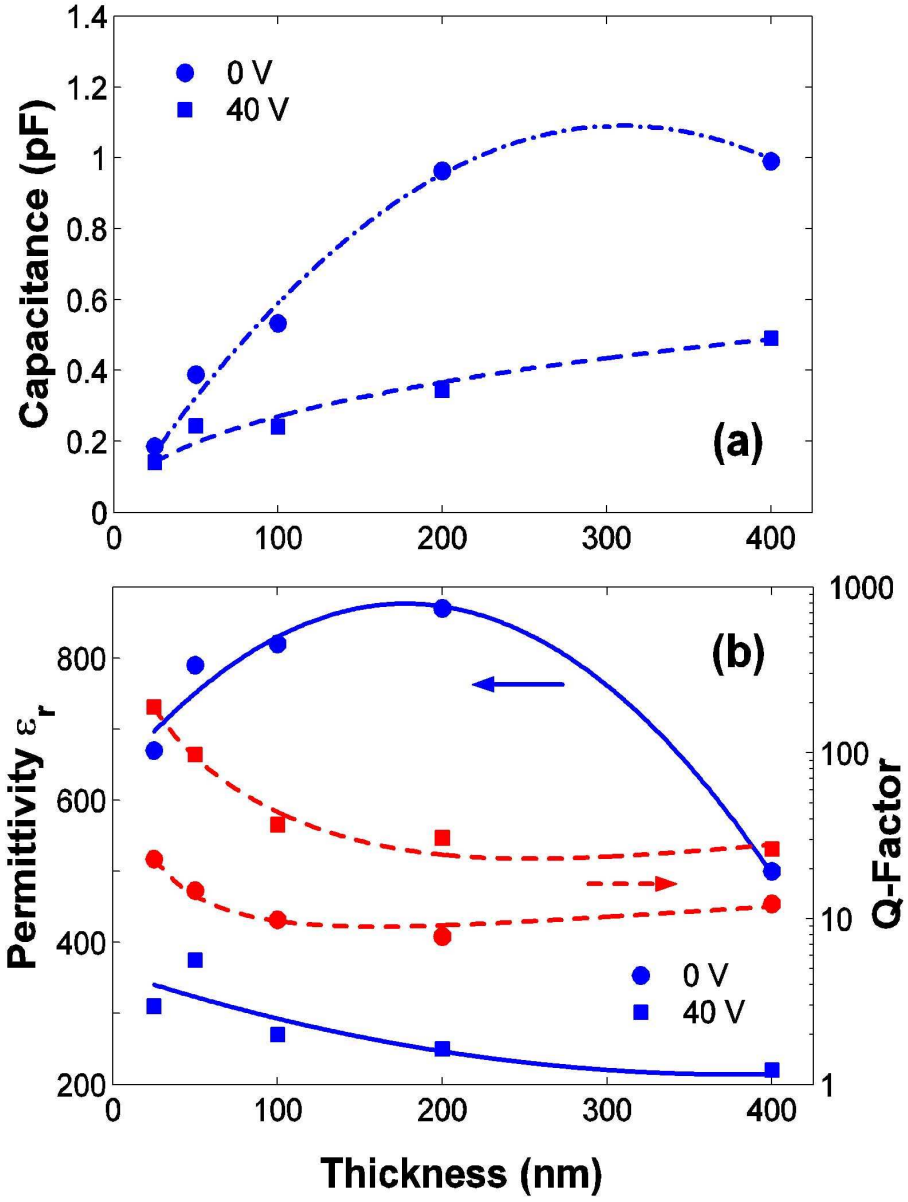


Figure 4.10: Thickness dependence of (a) IDC capacitance and (b) in-plane dielectric permittivity ε_r and Q- factor of the BST films at 0 and 40 V DC bias. The measured values and trend lines are represented by points and dashed lines, respectively.

4.5 Conclusions

This Chapter has presented the thickness dependent dielectric properties of polycrystalline $Ba_{0.6}Sr_{0.4}TiO_3$ films on r-plane sapphire. A series of films with thickness ranging from 25 to 400 nm was prepared by PLD. Tensile residual in-plane strain was measured in the thinnest films using XRD. As the film thickness increased, the strain was relieved at around 200 nm, while compressive strain was measured in the 400 nm film.

Interdigital electrodes were fabricated on the samples using the process developed in Chapter 3, in order to extract the microwave dielectric properties of the films. A high capacitance tunability of $\sim$64% was measured for the strain-relieved 200 nm film; however, this device had a relatively low Q-factor of $\sim$8 at 10 GHz. In general, a tradeoff between tunability and Q-factor was observed, with the thinnest film providing the highest Q-factor ($\sim$23) and lowest tunability ($\sim$24%).

These results demonstrate the potential for integrating BST films into the SoS process. The maximum temperature reached during the deposition and annealing process is 700°C . Providing the BST deposition is done before any metallisation steps in the SoS process flow, it is unlikely that the BST deposition would interfere with the SoS process. Integrating BST with the SoS process would allow the fabrication of BST-based tunable microwave circuits and digital baseband circuitry on a single chip.

Chapter 5

Electronically Tunable Microwave Circuits

5.1 Introduction

The requirement for reconfigurable RF and microwave circuits, based on the proliferation of commercial wireless devices, was discussed in Chapter 2. Both BST and MEMS varactors are emerging as competitors to the established technology of semiconductors for tunable microwave circuits.

Possible alternatives to frequency agile components are to use broad band components, or to switch between multiple narrow band components. However, these solutions often require more circuit real-estate and result in higher cost. Recently, software defined radio has emerged as a promising means of providing access to different wireless protocols using the same hardware. The basis of this approach is to digitise the RF signal as close as possible to the antenna using a high bandwidth analog to digital converter (ADC). The drawback of this method is that ADCs capable of direct analog to digital conversion at GHz frequencies are not likely to be available in the near future [144], at least for low cost, high volume applications. A current practical solution for reconfigurable software defined receivers employs a BPF, low noise amplifier (LNA) and downconversion (mixer) between the antenna and the digital circuitry [145]. Therefore, frequency agile RF front-end designs remain an attractive option.

In order for BST-based components to become commercially successful, a clear advantage over semiconductor varactors needs to be demonstrated. BST varactors with better performance than Si-based semiconductor varactors have been demonstrated at frequencies above 10 to 20 GHz [4]. However, further work is required to compare the performance of BST and semiconductor varactors, particularly at low

GHz frequencies.

The aim of this Chapter is to address practical issues associated with electronically tunable circuits using BST varactors. These issues include lowering the tuning voltage by decreasing the gap between the interdigital fingers, and minimising the generation of intermodulation products. A novel approach to the design of a branch-line hybrid coupler, using varactors to provide frequency agility, is also presented. The circuit was initially implemented in microstrip and lumped element form with commercially available varactor diodes. An integrated version of the coupler was then realised using BST varactors and planar inductors. This approach allows a direct comparison of BST varactors with their semiconductor counterparts.

5.2 Narrow Gap Interdigital Varactors

One of the limitations associated with the BST varactors described in Chapters 3 and 4 is the relatively high tuning voltage of the devices. In order to generate the required 0 to 40 V bias, a DC-DC converter circuit would be necessary for most applications, resulting in added complexity and cost. Therefore, it is useful to consider techniques to reduce the bias voltage.

An obvious approach suitable for interdigital varactors is to reduce the gap between the interdigital fingers. A ten-fold reduction in the finger spacing would reduce the tuning voltage (for a given capacitance tunability) by a similar factor. By reducing the finger spacing from 2 μm to 200 nm in the varactors described in Chapters 3 and 4, >2:1 capacitance tunability with a 0 to 4 V bias range would be expected. However, line widths less than 500 nm are very difficult to realise using the conventional contact mask lithography.

A potential solution to this problem was developed by RMIT PhD student Gorgi Kostovski [146]. The method is based on the standing wave pattern that forms on the sidewalls of photoresist when the resist is exposed to UV light through a contact mask pattern. A step-by-step process for fabricating narrow ($\sim$100 nm) lines of photoresist is illustrated in Fig. 5.1. Essentially, the method relies on casting the sidewall standing wave pattern using polydimethylsiloxane (PDMS) elastomer. The cast sidewall pattern in PDMS serves as a mask, since UV light exposed through the PDMS is scattered by the cast sidewall corrugations, as shown in Fig. 5.1(f).

Figure 5.2 shows some examples of features realised using the PDMS scattering mask technique. Based on these results, it is suggested that the technique could be employed to fabricate interdigital varactors with a finger spacing approaching 100 nm. A lift-off approach would be used to achieve narrow gap features similar to

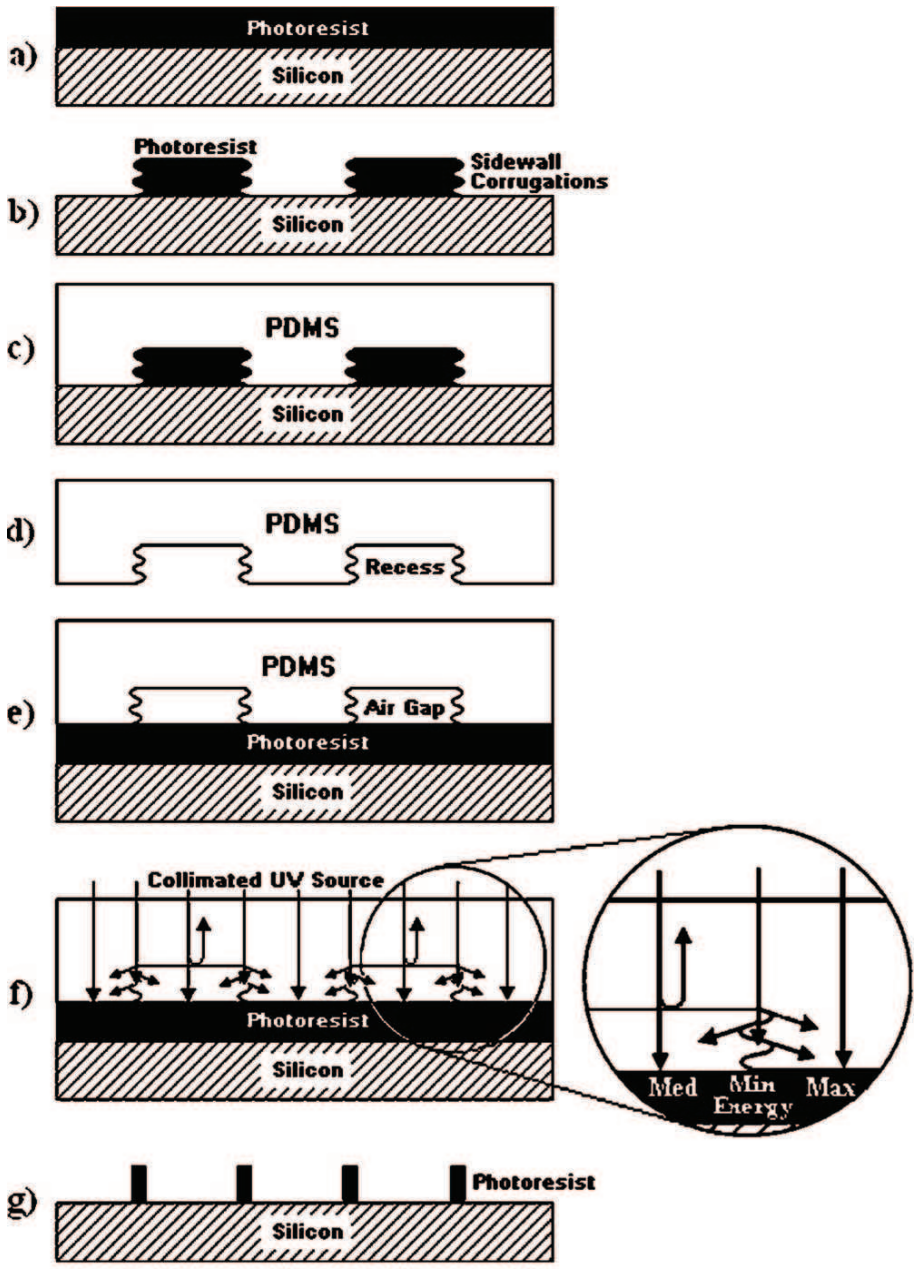


Figure 5.1: Fabrication steps for narrow gap features with PDMS scattering mask [146]. (a) A master structure is realised by spin coating a layer of photoresist onto a substrate, which is (b) photolithographically patterned using a quartz mask. (c) Casting PDMS against this structure realises (d) the PDMS scattering mask. (e) This mask is applied by conforming it to the surface of a new layer of photoresist and (f) illuminating the photoresist through the scattering mask. (g) Developing realises nanoscale line widths.

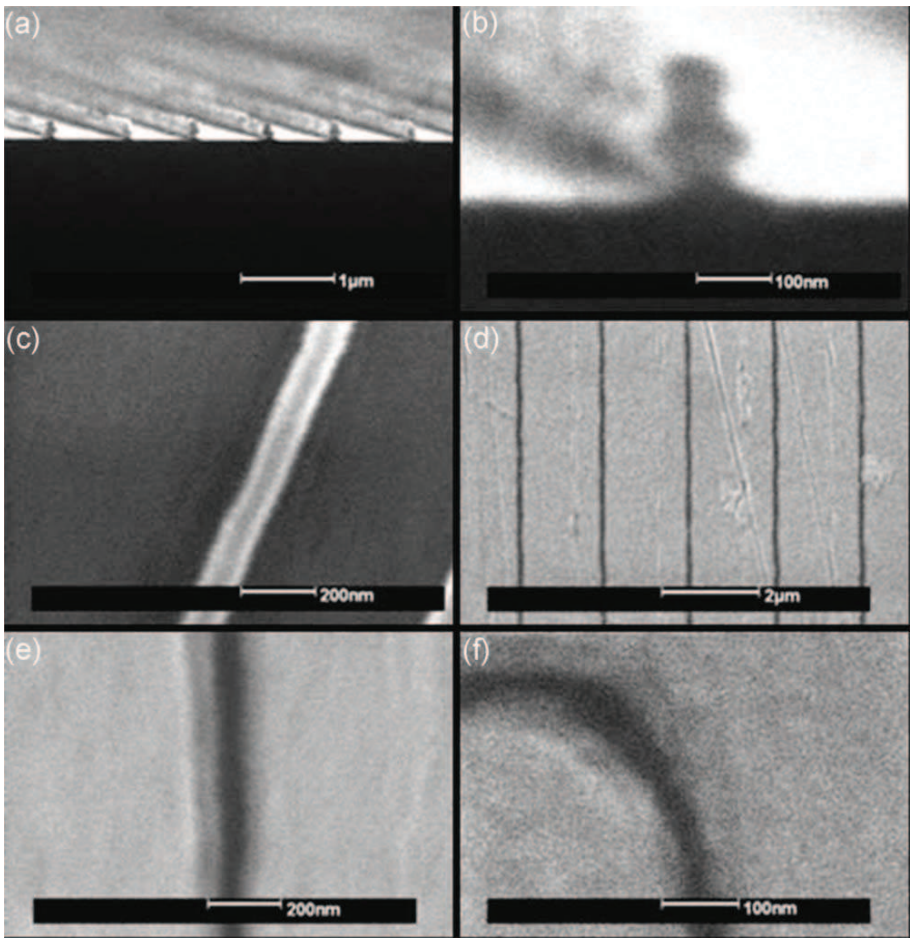


Figure 5.2: SEM images of features realised using the PDMS scattering mask technique [146]. (a) Periodic ∼80 nm lines of AZ5206E photoresist over a large area, and (b) high magnification image of the photoresist profile, demonstrating ∼80 nm lateral dimension. (c) A top view of the photoresist profile. (d) Patterned Au layer formed by lift-off of 50 nm Au film, with a high magnification view shown at (e). Continuity of the lift-off pattern around corners is demonstrated in (f).

those presented in Fig. 5.2. Low loss electrodes would then be fabricated using the electroplating process presented in Appendix B.

Development of narrow gap varactors was not pursued as part of this thesis work, since the priority was to achieve high tunability by minimising residual strain in the BST films. For BST varactor device demonstration purposes, a bias voltage range of 0 to 40 V is acceptable, since most VNA bias tees have an internal bias tee capable of these voltage levels. In commercial applications, a lower tuning voltage may be required; however, most commercial semiconductor processes now include sub-micron lithography steps, which could be used to fabricate narrow gap varactors

with a lower tuning voltage. The scattering mask technique would still be useful in developing low tuning voltage device prototypes using low cost photolithographic tools.

5.3 Nonlinear Properties and IP3 Measurement

In this Section, the nonlinear properties of BST varactors grown on c-plane sapphire by RF magnetron sputtering are considered in the context of microwave circuit applications. Due to the nonlinear C-V curve associated with BST and semiconductor varactors, two carrier signals incident on the device mix to produce intermodulation products. While this property can be exploited to realise mixers and frequency multipliers, the generation of intermodulation products can be a significant problem.

For a general nonlinear device, the output voltage can be expressed as a Taylor series [147]

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \cdots. \tag{5.1}$$

When the input signal v_{in} contains two frequency components f_1 and f_2, second order intermodulation products occur a long way from the passband signals, and are therefore easily removed by filtering. However, the third order intermodulation products $2f_2 - f_1$ and $2f_1 - f_2$ occur very close to or even within the passband, and therefore can be a significant problem.

The nonlinear properties of varactors are particularly relevant in large signal transmit applications, where the voltage levels present in the RF path can be comparable in magnitude to the tuning bias of the varactor. In this case, the RF signal can modulate the capacitance of the varactor, leading to significant capacitance variation over one period of the RF signal. In the case of a semiconductor varactor, it is possible for the diode junction to become forward biased under these conditions. This condition should be avoided, since it could cause distortion of the RF signal and possible damage to the varactor. Because the C-V curve of BST varactors is bipolar, or symmetrical about 0 V bias, the risk of forward biasing the devices does not apply. However, the generation of intermodulation products still needs to be considered.

In most transceiver architectures, a BPF is placed between the power amplifier and the antenna to attenuate out-of-band intermodulation products that are generated in the amplifier. If not properly attenuated, these out-of-band products could interfere with other services. In the case of a tunable BPF implemented with varactors, it is possible that the filter itself could generate intermodulation products. This would mean that there is little or no point in placing a filter between the power

amplifier and the antenna. Similar problems with intermodulation could also occur in other functional blocks of a transceiver which employ varactors.

The nonlinear properties of BST varactors can be characterised by measuring the IP3 of the devices. An experimental setup used to measure the IP3 of interdigital varactors that were fabricated at RMIT is shown in Fig. 5.3. Two signals (<15 dBm) are combined and fed to a BST varactor DUT on the wafer probe station. Note that one of the signal generators had a lower output level, and a power amplifier was used to increase the signal. A BPF centred on one of the intermodulation product frequencies was placed between the DUT and the spectrum analyser to prevent the two fundamental tones from mixing in the detector. A circulator was used to dump the two fundamental tones which are reflected by this BPF.

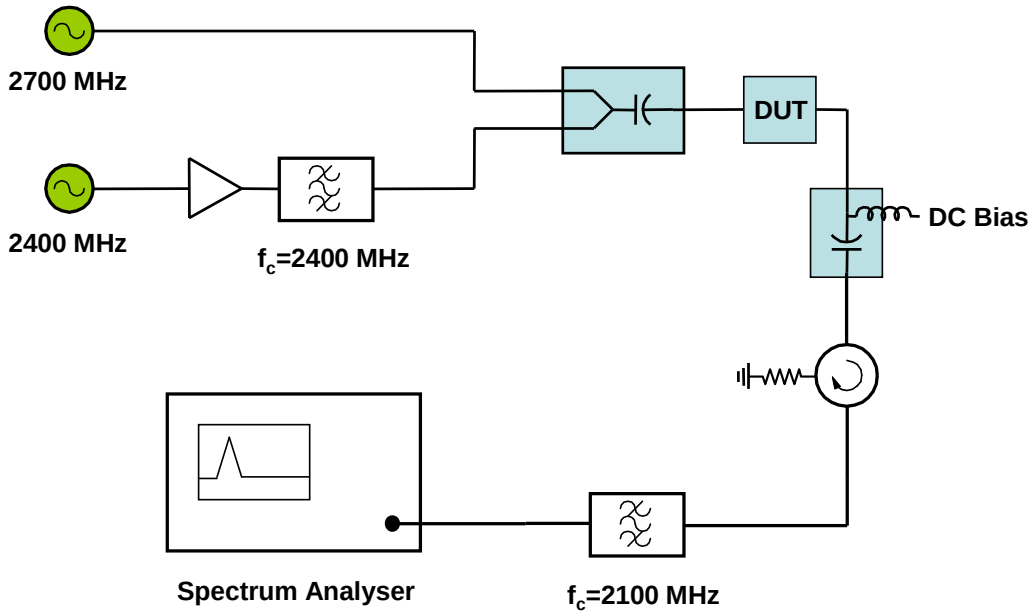


Figure 5.3: Experimental setup for measuring the third order intercept point (IP3) of BST varactors.

Before measuring a BST varactor, a through connection was substituted into the IP3 test setup in place of the BST varactor. For fundamental tone frequencies of $f_1 = 2400$ MHz and $f_2 = 2700$ MHz, no intermodulation product was observed at $2f_2 - f_1 = 2100$ MHz. This confirmed that there was no unwanted mixing of signals in the IP3 test setup.

The power levels were set up by disconnecting the BPF in front of the spectrum analyser and measuring the power level of each fundamental tone using a power

meter. Since the loss of the BST varactors is bias voltage dependent, the signal generator power was re-adjusted each time the bias voltage was changed, in order to ensure constant power level at the output of the device.

Figure 5.4 shows the measured output IP3 (OIP3) of a BST interdigital varactor with ∼56% tunability on *c*-plane sapphire. The OIP3 was calculated using [17]

$$OIP3 = P_{Fund} + \frac{P_{IM3}}{2}, \tag{5.2}$$

where P_{Fund} is the signal level (in dBm) of the two fundamental tones at the DUT output and P_{IM3} is the signal level of the third order intermodulation products, relative to the fundamental tones. The OIP3 is lowest (∼40 dBm) for 0 dBm fundamental tones at around 0 V bias, and improves to ∼58 dBm at 40 V bias. A lower OIP3 is expected around 0 V bias, due to the highly nonlinear shape of the C-V curve. As shown in Fig. 5.4, the OIP3 also improves with larger signals (5 dBm instead of 0 dBm at the device output). This observation is consistent with earlier reports [3]. Although the effect is not well understood, it is suggested that the larger RF signals cause the peak in the C-V curve to flatten out, since the varactor is biased by the large RF signals. This would result in lower tunability, and improved linearity.

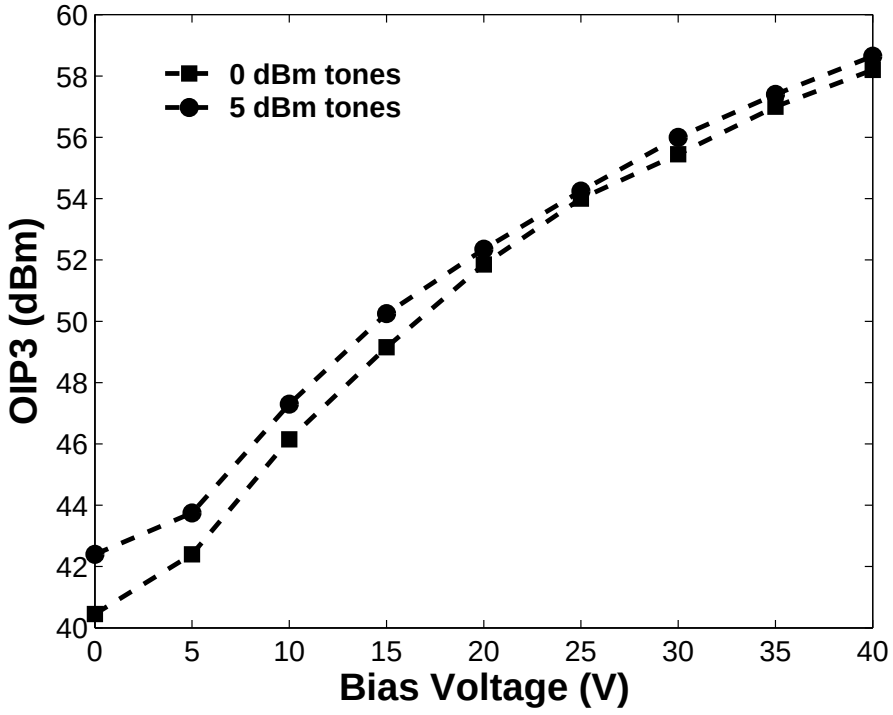


Figure 5.4: Measured OIP3 of 2 μm gap (56% tunability) interdigital BST varactor fabricated on *c*-plane sapphire.

The OIP3 of BST interdigital varactors can be improved by increasing the gap between the fingers, however this would lower the capacitance tunability. Therefore, there is a tradeoff between tuning voltage and linearity which should be considered when designing microwave circuits using BST varactors. For example, it is likely that the narrow gap varactors considered in the Section 5.2 would have a low OIP3, and therefore would only be useful in small signal circuits. Further work is required to determine whether it is possible to improve the IP3 of BST varactors without sacrificing tunability or Q-factor.

5.4 Tunable Hybrid Coupler - Microstrip Implementation

The remaining Sections in this Chapter are concerned with a novel tunable hybrid coupler design, where the centre frequency is adjusted by controlling the varactor bias voltage. Commercial surface mount varactor diodes were used to validate the design, before proceeding to an integrated version using BST varactors. This Section presents a theoretical analysis of the tunable hybrid, along with measured results for a prototype based on varactor-loaded microstrip transmission lines.

Branch-line 90°, 3 dB hybrid couplers are a basic functional block in many microwave circuits. Applications include balanced low noise amplifiers, mixers and reflective-type phase shifters. The conventional design employs two 35 Ω series arms and two 50 Ω shunt arms, 1/4-wavelength long at the centre frequency, to provide 3 dB power split with 90° phase offset between the coupled ports [147]. A fourth isolated port is generally terminated with a 50 Ω resistor. The ports lie at the intersections of the branch lines. Single-section branch line hybrids have a relatively narrow bandwidth of ∼10% [86]. Additional bandwidth can be achieved by adding more series and shunt branch lines, however, this complicates the design procedure and requires more layout space.

As a solution to this problem, a frequency agile version of the single-section branch line hybrid is proposed. A schematic diagram of the varactor tuned hybrid coupler is shown in Fig. 5.5. In this design, four varactors are employed to tune the centre frequency of the hybrid, while maintaining a 3 dB coupling level. Changing the varactor capacitance, C, modifies the electrical length of the series and shunt transmission line sections, and therefore the frequency at which 3 dB coupling is achieved. An electronically tunable single section hybrid may be useful in applications which require switching between multiple narrow bands, for example in a multi-band cellular handset. The single section tunable hybrid can replace several

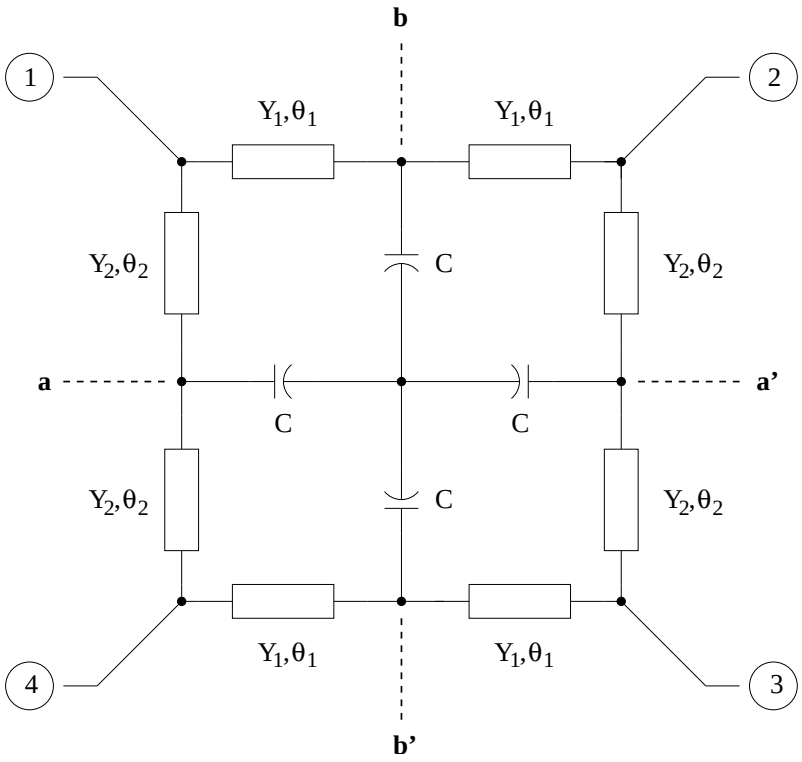


Figure 5.5: Schematic diagram of the varactor tuned hybrid coupler.

fixed hybrids, leading to size and cost reductions.

Varactor diodes have previously been combined with microwave couplers to provide tunability both in frequency and magnitude. In [148] varactors were used in a microstrip directional coupler to vary the coupling level from 4 dB to 20 dB. More recently, a varactor tuned LC resonator was employed to extend the operating frequency range of a microstrip directional coupler [149]. In the resonator-based tunable coupler, the regions of flat coupling, high return loss and high directivity are narrow-band, but the return loss and directivity nulls can be tuned in frequency by controlling the varactor bias voltage.

5.4.1 Even-Odd Mode Analysis

The equations for the S-parameters of the varactor tuned hybrid can be determined by the even-odd mode technique [150]. With aa′ and bb′ in Fig. 5.5 alternately open circuit and short circuit, and by considering the fourfold symmetry of the structure, the four subnetworks shown in Fig. 5.6 are obtained. The capacitor only appears in (b) and (c), since it is open circuit and short circuit in (a) and (d), respectively. Starting with the circuit of Fig. 5.6(a),

$$Y_{in,1a} = jY_1 \tan\theta_1 \tag{5.3}$$

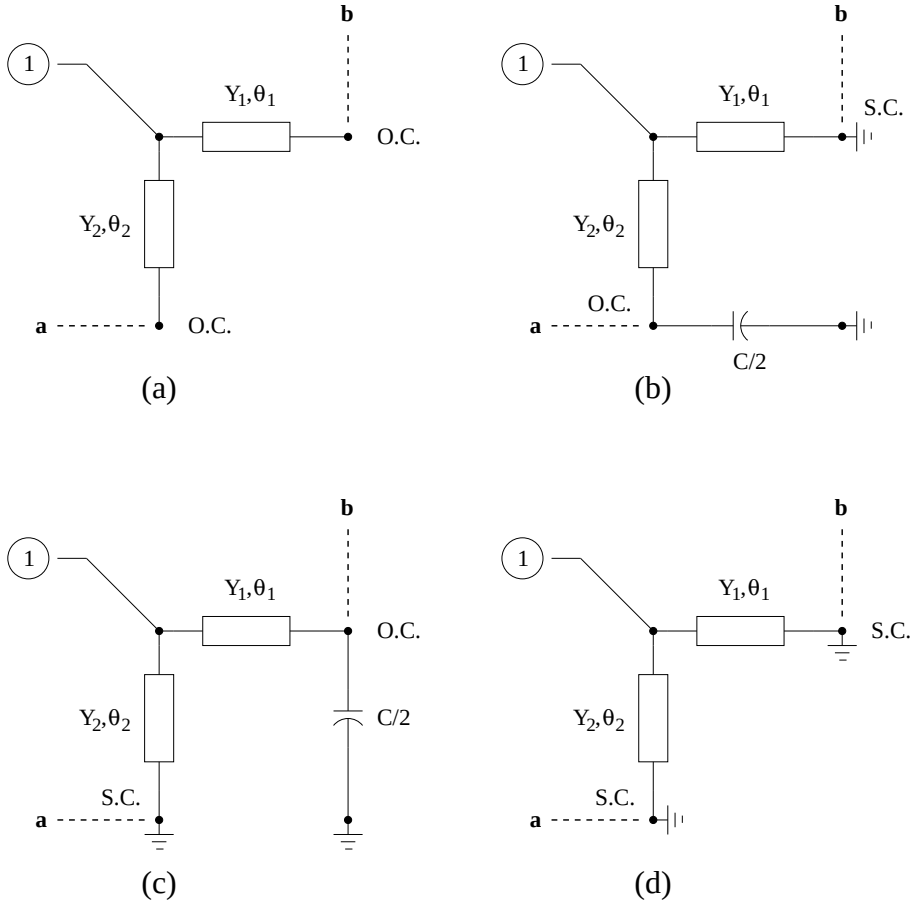


Figure 5.6: Even-odd mode subnetworks (a) aa′ and bb′ open circuit (b) aa′ open circuit, bb′ short circuit (c) aa′ short circuit, bb′ open circuit (d) aa′ and bb′ short circuit.

$$Y_{in,2a} = jY_2 \tan\theta_2 \tag{5.4}$$

where $Y_{in,1a}$ and $Y_{in,2a}$ are the input admittances of the microstrip lines with characteristic admittance Y_1 and Y_2 and electrical length θ_1 and θ_2, respectively. In this case, both microstrip lines are terminated in an open circuit. Therefore, the reflection coefficient at port 1 is

$$\Gamma_a = \frac{Y_o - (Y_{in,1a} + Y_{in,2a})}{Y_o + Y_{in,1a} + Y_{in,2a}} \tag{5.5}$$

where Y_o is the characteristic admittance. Similarly,

$$Y_{in,1b} = \frac{Y_1}{j\tan\theta_1} \tag{5.6}$$

$$Y_{in,2b} = \frac{\frac{1}{Y_2} + (\frac{2}{\omega C})\tan\theta_2}{(\frac{1}{Y_2}) \cdot (\frac{2}{j\omega C} + j\frac{1}{Y_1}\tan\theta_2)} \tag{5.7}$$

$$Y_{in,1c} = \frac{\frac{1}{Y_1} + (\frac{2}{\omega C})\tan\theta_1}{(\frac{1}{Y_1}) \cdot (\frac{2}{j\omega C} + j\frac{1}{Y_1}\tan\theta_1)} \tag{5.8}$$

$$Y_{in,2c} = \frac{Y_2}{j\tan\theta_2} \tag{5.9}$$

$$Y_{in,1d} = Y_{in,1b} \tag{5.10}$$

$$Y_{in,2d} = Y_{in,2c} \tag{5.11}$$

Finally, by superposition, the S-parameters can be calculated using

$$S_{11} = \frac{1}{4}(\Gamma_a + \Gamma_b + \Gamma_c + \Gamma_d) \tag{5.12}$$

$$S_{21} = \frac{1}{4}(\Gamma_a - \Gamma_b + \Gamma_c - \Gamma_d) \tag{5.13}$$

$$S_{31} = \frac{1}{4}(\Gamma_a - \Gamma_b - \Gamma_c + \Gamma_d) \tag{5.14}$$

$$S_{41} = \frac{1}{4}(\Gamma_a + \Gamma_b - \Gamma_c - \Gamma_d) \tag{5.15}$$

where Γ_a, Γ_b, Γ_c and Γ_d are the reflection coefficients at port 1 under the four different conditions illustrated in Fig. 5.6(a)-(d). In order to simulate the circuit, the values of Y_o and Y_2 are set to 1/50 Ω^{-1}, and Y_1 is set to 1/35 Ω^{-1}, as in the conventional design [147]. The electrical length of the microstrip lines can be calculated using

$$\theta = \frac{\omega\ell\sqrt{\epsilon_{r,eff}}}{c} \tag{5.16}$$

where ℓ is the physical length of the line, $\epsilon_{r,eff}$ is the effective dielectric constant of the substrate material, and c is the speed of light.

5.4.2 Microstrip Prototype

In order to validate the design prior to fabrication, the circuit was simulated using the analytical solutions (Equations 5.12 to 5.15). Rogers 4003C ($\epsilon_r = 3.38$, 0.508 mm thick) was used as the substrate material. The simulation results, shown as dashed lines in Figs. 5.7 and 5.8, were obtained with series and shunt branch line lengths of 18 mm. In Figs. 5.7 and 5.8, the varactor capacitance is set to 2.0 and 0.8 pF, respectively. Adjusting the varactor capacitance over this range allows the tunable hybrid to cover 1710 to 2170 MHz with better than 20 dB return loss. The required varactor tuning range of 2.5:1 is well within the capability of commercially available varactor diodes.

A 10 nH chip inductor was placed between the common node of the varactor diodes and ground, in order to establish a bias voltage across the diodes. Simulations

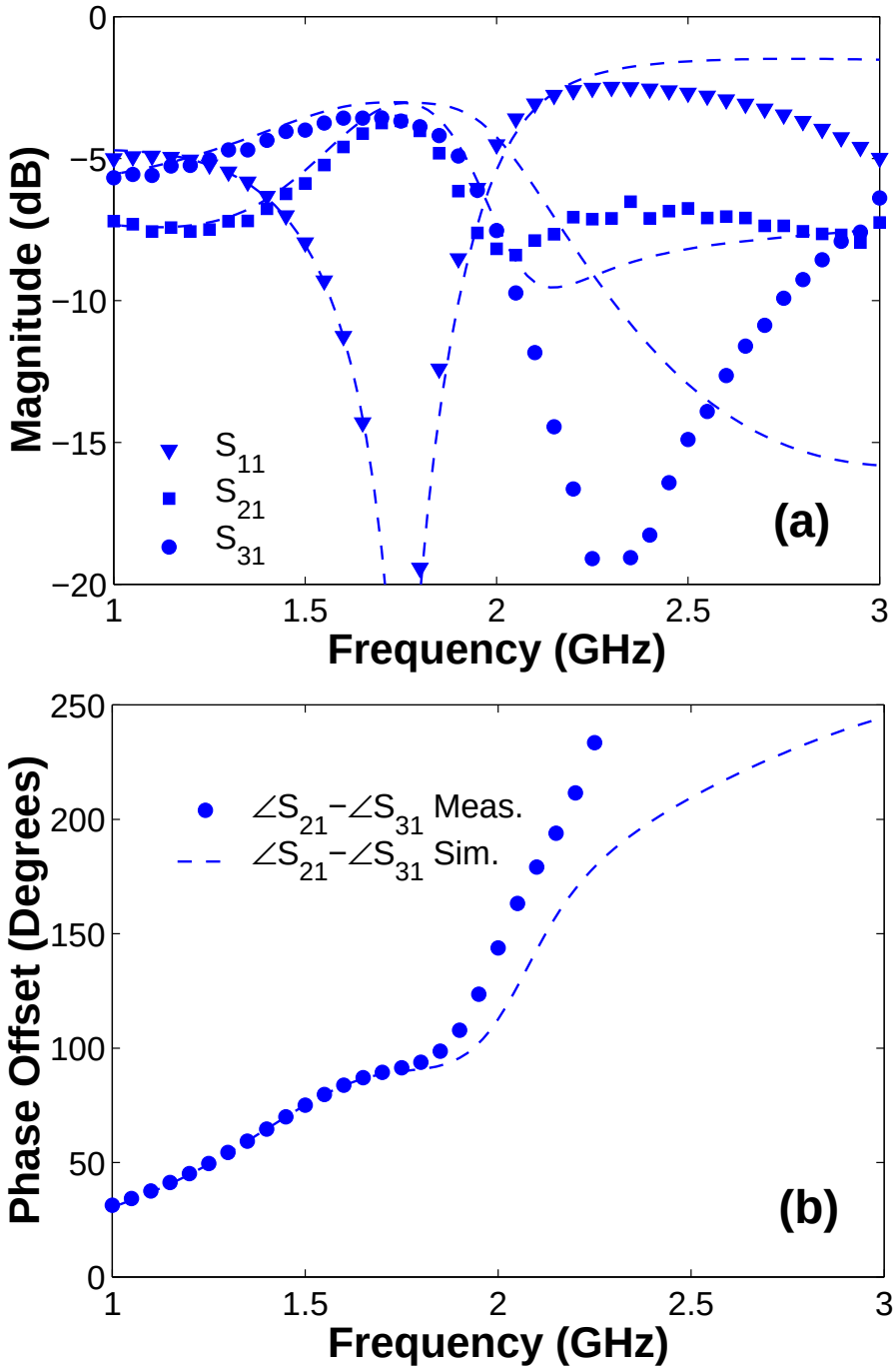


Figure 5.7: Coupler characteristics when tuned to DCS uplink band (a) measured and simulated S-parameters (b) measured and simulated phase offset between coupled ports. The measured and simulated results are presented as point series and dashed lines, respectively.

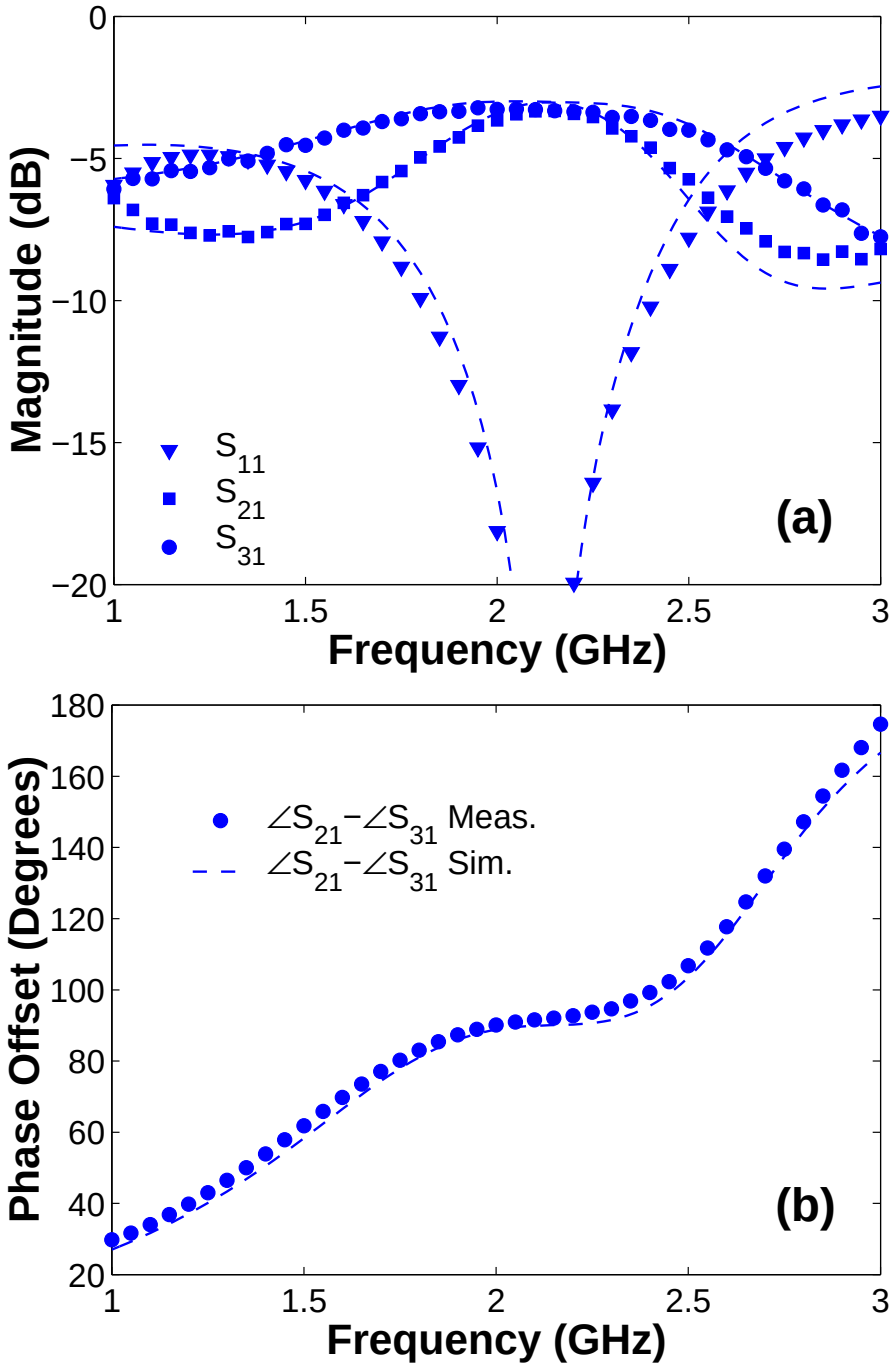


Figure 5.8: Coupler characteristics when tuned to IMT2000 downlink band (a) measured and simulated S-parameters (b) measured and simulated phase offset between coupled ports. The measured and simulated results are presented as point series and dashed lines, respectively.

Frequency Band	**Band Edge**	**Coupling**	**Return Loss**	**Coupled Port Phase Offset**	$\mathbf{V}_{bias}$
	(MHz)	(S_{21}, dB)	(S_{11}, dB)	(°)	(V)
DCS uplink	1710	3.7	21.1	89.8	2.1
	1785	3.8	22.4	92.8	
DCS downlink	1805	3.5	26.8	90.7	2.7
	1850	3.6	25.9	92.0	
PCS uplink	1850	3.5	24.6	90.9	3.2
	1910	3.5	25.0	92.2	
PCS downlink	1930	3.4	24.7	91.0	4.1
	1990	3.5	26.1	92.2	
IMT2000 uplink	1920	3.5	24.7	90.9	4.0
	1980	3.5	26.2	92.0	
IMT2000 downlink	2110	3.3	27.4	91.6	8.0
	2170	3.4	22.3	92.1	

Table 5.1: Summary of measured results for the microstrip tunable hybrid coupler.

in ADS were performed at this stage to check that the inductor did not degrade the RF performance, and to generate the artwork for fabrication of the circuit. A prototype circuit was constructed using Skyworks SMV1231-079 varactors. DC bias was applied to port 1 via a bias tee, and DC blocking capacitors were placed at ports 2, 3 and 4. A photograph of the prototype circuit is shown in Fig. 5.9.

The measured results are presented as marker series in Figs. 5.7 and 5.8. Bias voltages of 2.1 and 8.0 V were applied to tune the hybrid to the DCS uplink (Fig. 5.7) and IMT2000 downlink (Fig. 5.8), respectively. It is evident from these results that the coupler bandwidth decreases as the varactor capacitance increases. The bandwidth should still be sufficient to cover a single cellular uplink or downlink channel with acceptable coupling variation. There is good agreement between measured and simulated results in Fig. 5.8. However, the analytical model loses accuracy beyond 1.8 GHz in Fig. 5.7. This may be attributed to the series resistance and lead inductance of the varactor diodes. Also, a short length of high impedance transmission line must be placed between the anode of each diode and the common node, for layout purposes. The effect of this transmission line was not modelled.

A summary of measured results for each uplink and downlink channel in the DCS,

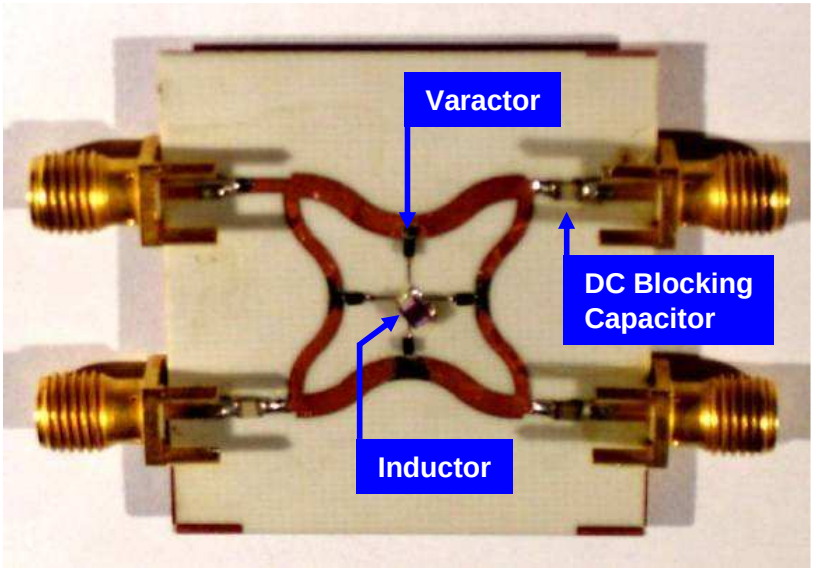


Figure 5.9: Photograph of a prototype microstrip-based tunable hybrid coupler.

PCS and IMT2000 frequency bands is presented in Table 5.1. The coupling level at ports 2 and 3 is within 3±1 dB and the return loss (S_{11}) is better than 20 dB in each case. A coupled port phase offset of 90±3° is achieved. In comparison, the S_{11} response of a conventional single-section branch-line hybrid designed for 1950 MHz has a 20 dB return loss bandwidth of ∼200 MHz. Each of the four branch lines in the conventional design [147] is 23.3 mm long, while the varactor tuned design uses 18 mm branches. Some useful miniaturisation is therefore achieved by the use of varactors.

5.5 Lumped Element Tunable Hybrid

In this Section, the varactor-based tuning technique is applied to a lumped element quadrature hybrid coupler suitable for RFICs. A novel tunable hybrid coupler design was validated in the previous Section using microstrip transmission lines by varactor diodes. However, a limitation of the transmission line approach is the amount of space required, given that each of the branch line lengths is $\sim \lambda_g/4$ long, where λ_g is the guided wavelength.

For RFIC applications, a lumped element implementation of the 90° hybrid can reduce the footprint of the device by up to 80% [86], relative to the microstrip approach. By replacing the fixed capacitors in the conventional lumped element design with varactors, a frequency agile version of the lumped element hybrid can be realised.

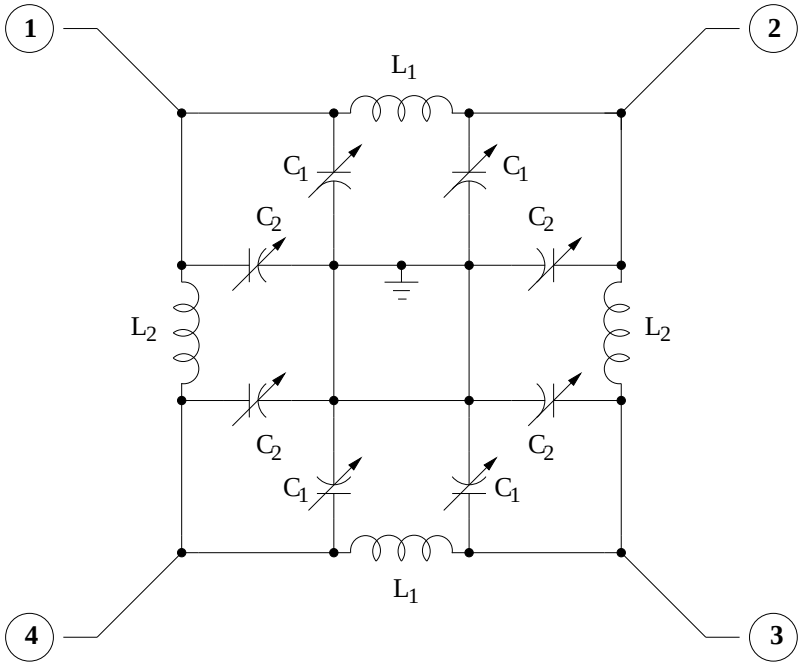


Figure 5.10: Schematic diagram of the lumped element tunable hybrid coupler, based on [86].

A schematic of the tunable lumped element hybrid coupler is shown in Fig. 5.10. In this design, a *pi*-network consisting of two varactors and one inductor replaces each quarter-wave microstrip line. By changing the capacitance of the varactors C_1 and C_2, a phase shift is introduced in each of the *pi*-networks. This phase shift modifies the frequency at which 3 dB coupling is achieved, while maintaining a consistent coupling level and return loss.

In order to verify the design before proceeding to a RFIC implementation, a prototype was constructed using surface mount components. Chip inductors with $L_1 = 3.6$ nH and $L_2 = 5.1$ nH were chosen, using design equations [86]

$$L_1 = \frac{Z_r}{\omega} \tag{5.17}$$

$$L_2 = \frac{Z_p}{\omega} \tag{5.18}$$

$$C_1 = \frac{1}{\omega Z_r} \tag{5.19}$$

$$C_2 = \frac{1}{\omega Z_p} \tag{5.20}$$

where Z_p and Z_r were chosen to be 50 and 35 Ω, respectively, and L_1, L_2, C_1 and C_2 are the lumped component values (see Fig. 5.10). Skyworks SMV1231-079 varactors,

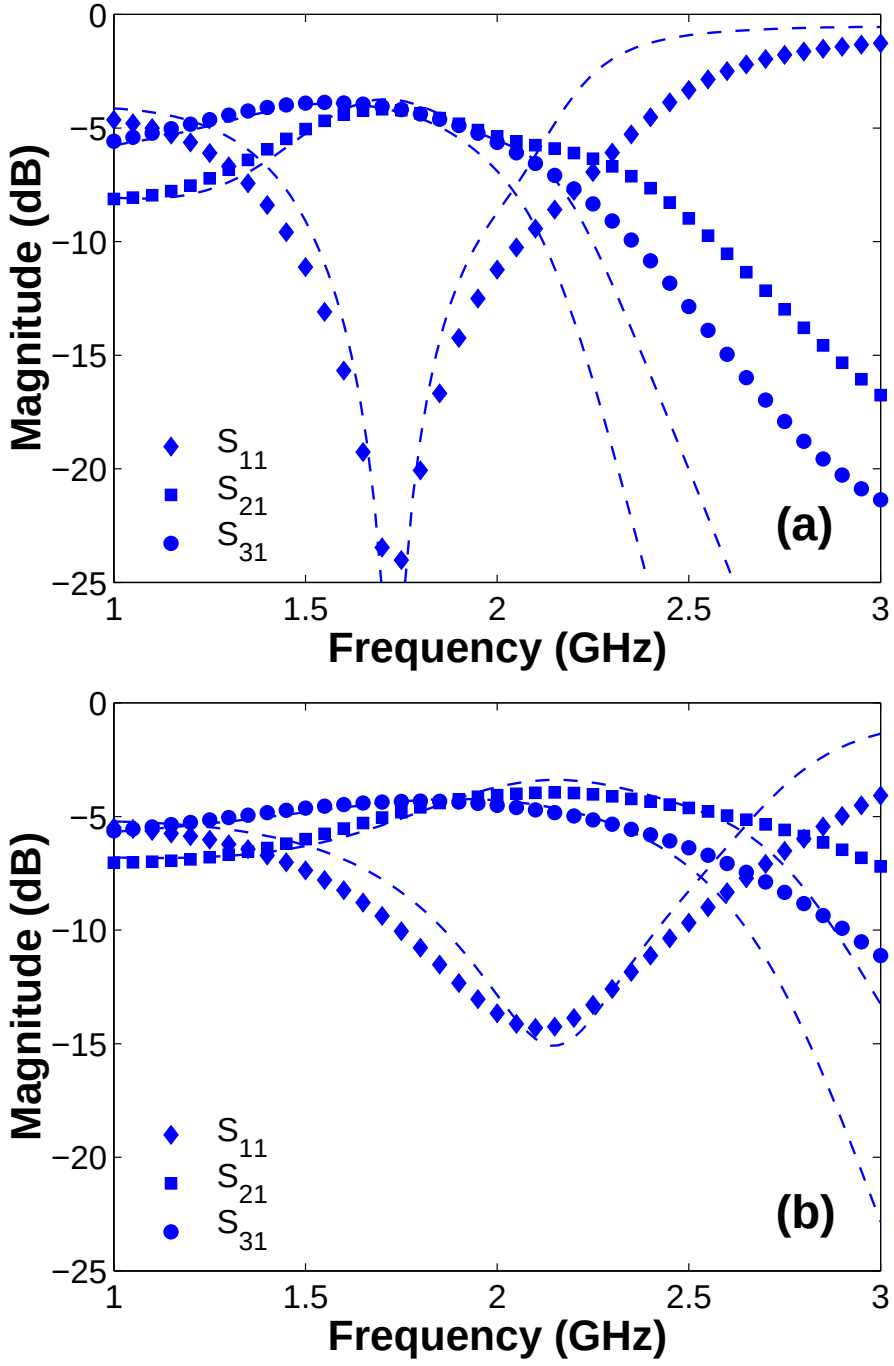


Figure 5.11: Measured and simulated magnitude response of the lumped element hybrid when tuned to (a) DCS uplink and (b) IMT2000 downlink band. The measured and simulated results are presented as point series and dashed lines, respectively; simulations were performed using Agilent ADS.

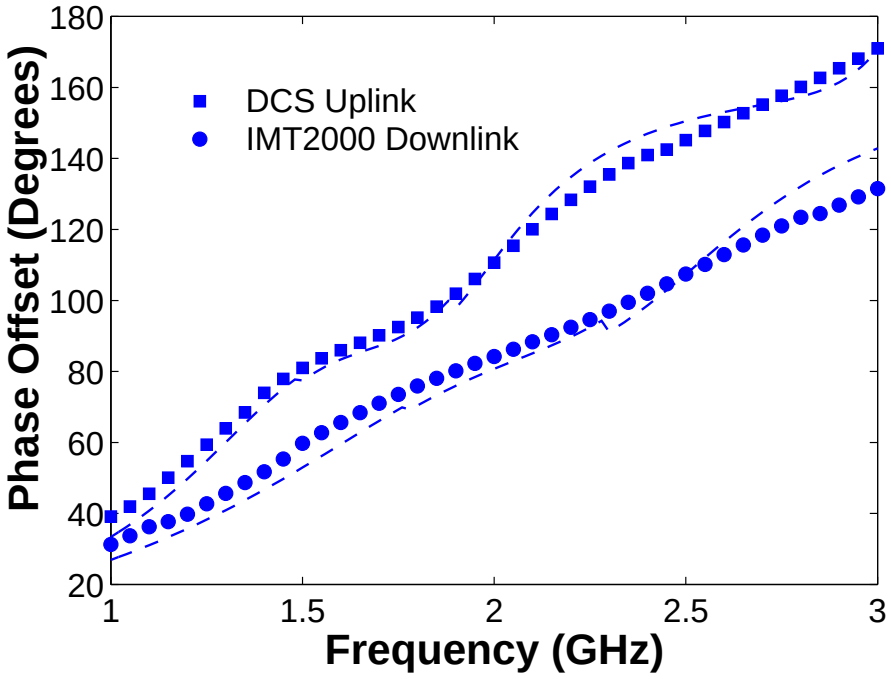


Figure 5.12: Phase response of the lumped element hybrid when tuned to DCS uplink and IMT2000 downlink bands. The measured and simulated results are presented as point series and dashed lines, respectively; simulations were performed using Agilent ADS.

with a tuning range of 0.5 to 2 pF, were used as the tuning elements. In order to simplify the biasing arrangement, the same bias voltage is applied to all varactors. Under this condition, $C_1 = C_2$. A DC tuning bias of 0 to 8 V was applied at port 1, and DC blocking capacitors were placed at the remaining ports. The substrate material was 0.5 mm Rogers 4003C.

The S-parameters of the tunable hybrid were simulated in ADS2004A and measured using an Agilent E5071B vector network analyser. Fig. 5.11(a) shows the simulated and measured magnitude response of the hybrid when tuned to the DCS uplink band (1710-1785 MHz) by applying a 1.6 V DC bias at port 1. The coupling level is 4.3±0.1 dB and return loss (S_{11}) is better than 20 dB across the band. Fig. 5.11(b) shows the simulated and measured results when tuned to the IMT2000 downlink band (2110-2170 MHz) by applying a 3.7 V bias. In this case, the coupling level is 4.4±0.5 dB and return loss (S_{11}) is better than 14 dB across the band. The phase response of the hybrid is shown in Fig.5.12. At the DCS uplink and IMT2000 downlink band, the phase offsets between the coupled ports are 92±3° and 90±2°, respectively, across the band. Note that the band edge frequencies for the DCS and

IMT2000 cellular frequency bands are defined in Table 5.1.

Reasonable agreement between the simulated and measured results is achieved. The discrepancy observed at higher frequencies is likely due to parasitic inductance associated with the solder joints and vias; this was confirmed by ADS simulation. A capacitance of 100 fF in parallel with the inductors was used to obtain the simulated results in Figs. 5.11 and 5.12. This capacitance has contributions from the inductor windings and from coupling between the two varactors in each *pi*-section. According to simulations, the 100 fF capacitance has a significant impact on the amplitude balance between the coupled ports. Lower parasitic capacitance in an RFIC design and separate values for C_1 and C_2 should lead to improved amplitude balance.

5.6 BST Tunable Hybrid

After validating the lumped element implementation of the tunable hybrid coupler, an integrated version of the lumped element hybrid was designed. The important objectives were to replace the surface-mount inductors with on-chip spiral inductors, and to substitute BST varactors in place of the commercial varactor diodes. A *c*-plane sapphire substrate was chosen for the chip, in order to apply the results obtained in Chapter 3 for BST interdigital varactors.

The BST-based tunable hybrid was designed to cover the 1700 to 2200 MHz band, similar to the microstrip and lumped element tunable hybrids described earlier in this Chapter. Values for the lumped element inductors and for the capacitance tuning range of the BST varactors were obtained using Equations 5.17-5.20. Values for L_1 and L_2 were calculated at lowest and highest frequency, and the mean of these two values was taken in order to achieve best performance at ∼1950 MHz, the centre of the tuning range. The final values for L_1 and L_2 were 2.9 and 4.15 nH, respectively. From Equations 5.19 and 5.20, the varactor tuning ranges were 2.1 to 2.6 pF for C_1 and 1.5 to 1.8 pF for C_2.

Interdigital varactors were designed with a 700 nm thick BST film, 5 μm finger width, 2 μm gap and overlap length of 120 μm. The number of interdigital fingers was chosen based on the measured results for interdigital varactors with two sets of eight fingers obtained in Chapter 3. C_1 and C_2 were designed with two sets of 15 fingers and 11 fingers, respectively.

The printed inductors were designed using analytical equations for the initial dimensions and then simulating with Ansoft HFSS software. An inductor line width of 40 μm, line spacing of 20 μm and 150 μm gap to groundplane were chosen. For

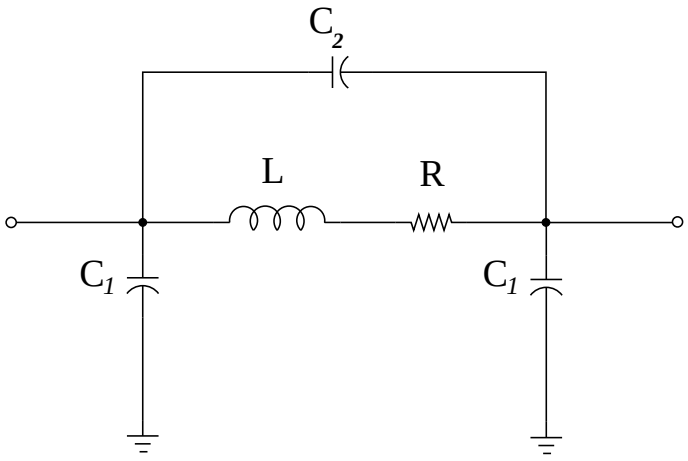


Figure 5.13: Equivalent circuit model of a spiral inductor [86].

and inductor of arbitrary shape, the inductance is given by [86]

$$L = \frac{\mu_o n^2 D_{av} c_1}{2}[\ln(\frac{c_2}{\rho}) + c_3\rho + c_4\rho^2] \tag{5.21}$$

where, n is the number of turns, and for a square inductor geometry, $c_1 = 1.27$, $c_2 = 2.07$, $c_3 = 0.18$ and $c_4 = 0.13$. The fill factor ρ, and average diameter, D_{av} are given by [86]

$$\rho = \frac{D_o - D_i}{D_o + Di} \tag{5.22}$$

$$D_{av} = \frac{1}{2}(D_o + D_i) \tag{5.23}$$

where D_o and D_i are the outer and inner diameter of the inductor, respectively. Using the initial values of D_o and D_i from Equation 5.21, the inductors were simulated in HFSS. The inductor S-parameters were then exported from HFSS and fitted to an equivalent circuit model (Fig. 5.13) in ADS. After a few iterations in HFSS, inductance values for L_1 and L_2 very close to the design values of 2.9 and 4.15 nH were achieved.

A coplanar waveguide (CPW) implementation of the circuit was chosen to eliminate the requirement for vias. For a 50 Ω characteristic impedance, the width of the centre conductor was 50 μm and the gap to the groundplane was 20 μm. Also, to avoid wire bonding, electroplated air bridges were designed to connect to the inner loop of the spiral inductors. Air bridges were also placed at tee-junctions in the CPW and at several points around the circuit in order to equalise the ground plane potential. A scanning electron microscope (SEM) image of an electroplated air bridge is shown in Fig 5.14.

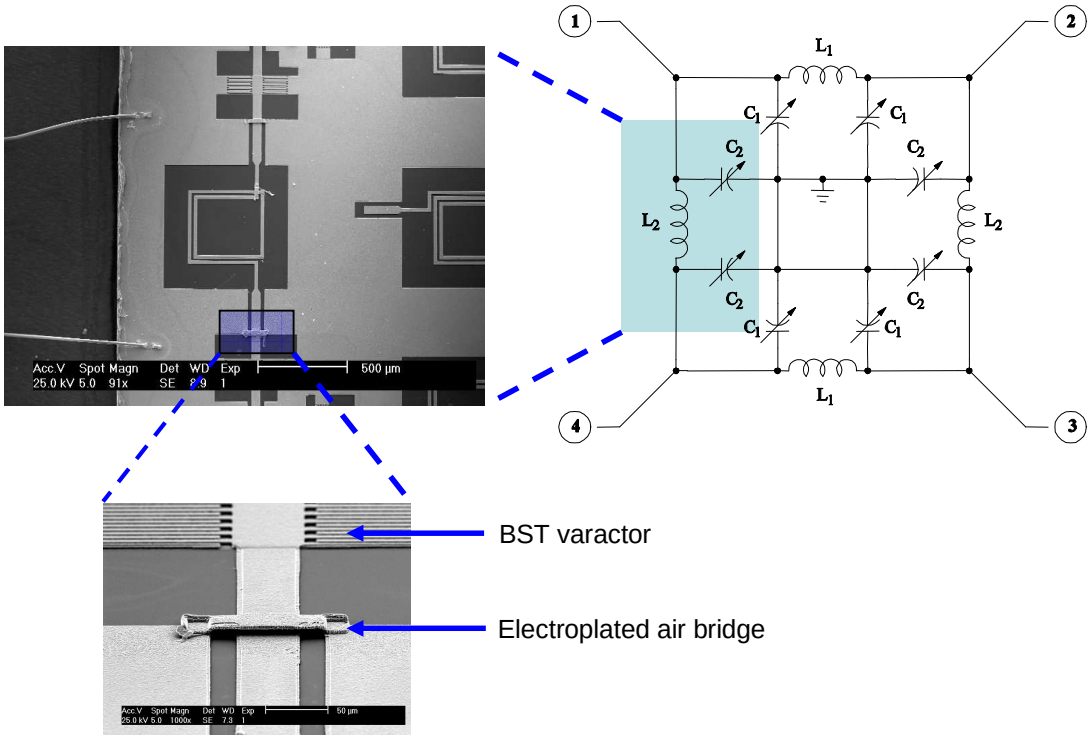


Figure 5.14: SEM images of a *pi*-section and an electroplated air bridge in the tunable hybrid coupler chip.

A full description of the processing steps for the tunable hybrid is provided in Appendix C. Processing conditions for deposition of the BST layer were identical to those of the high tunability devices described in Chapter 3. The substrate temperature was 700°C and the process gas pressure was 40 mTorr. Prior to deposition of the BST layer, the substrate was heat treated in-situ at 700°C and 20 mTorr O_2 . After removing the samples from the sputtering system, the samples were annealed in 1 L/min flowing O_2 at 900°C for 1 hour.

After completing the fabrication steps, a 4 mm^2 chip containing the tunable hybrid circuit was cut from the sapphire substrate using a dicing saw. Figure 5.14 shows a view of a single *pi*-section on the chip, and an close-up view of one of the electroplated air bridges. A full chip micrograph is shown in Fig. 5.15. The S-parameters of the test inductor in the centre of the chip were measured with the wafer probe station, and the inductance was extracted using the equivalent circuit model of Fig. 5.13. These results gave an extracted L_1 value of 3.7 nH, ∼11% lower than the design value of 4.15 nH.

Because the MMTC wafer probe station is limited to two probes, it was difficult to terminate the remaining two ports on the tunable hybrid. Therefore, a four

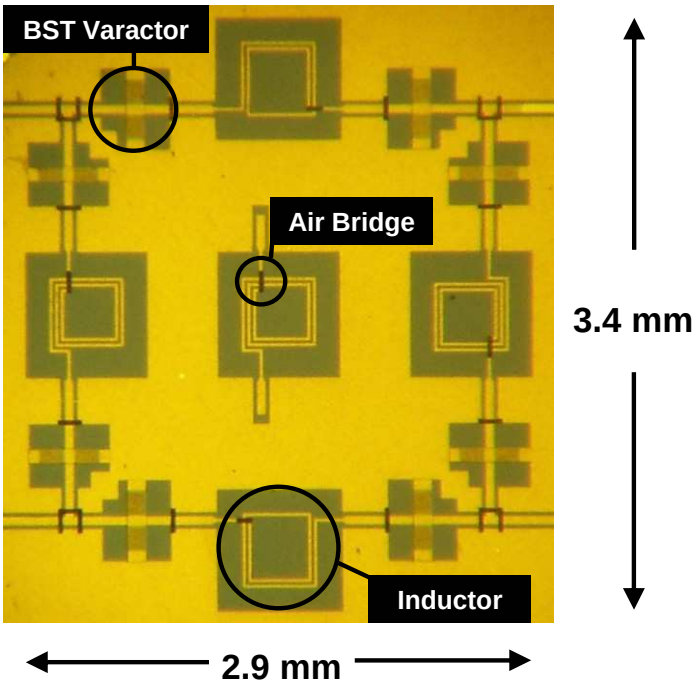


Figure 5.15: A photograph of the BST tunable hybrid chip showing varactors, inductors, and air bridges.

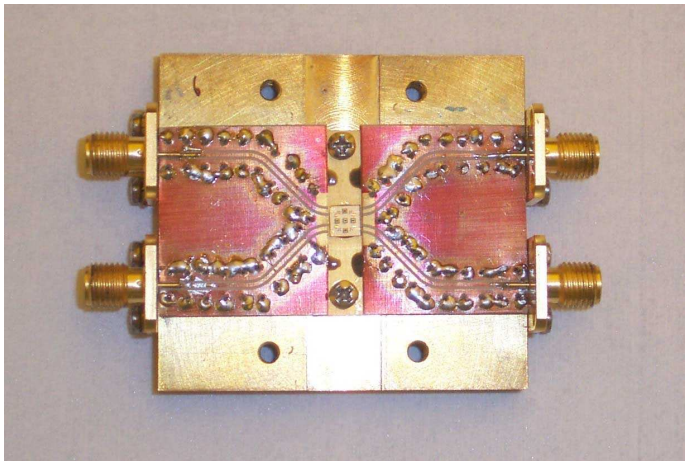


Figure 5.16: A photograph of the BST tunable hybrid chip mounted in a four-port test jig.

port test jig was designed so that SMA cables could be attached for microwave measurements. A photograph of the tunable hybrid chip mounted in the test jig is shown in Fig. 5.16. Without the BST chip in the test jig, the minimum return loss was 17.5 dB and the maximum insertion loss was 0.4 dB over the frequency range 1700 to 2200 MHz. Electrical connections to the tunable hybrid chip were made by wire bonding from gold plated pads on the CPW test jig.

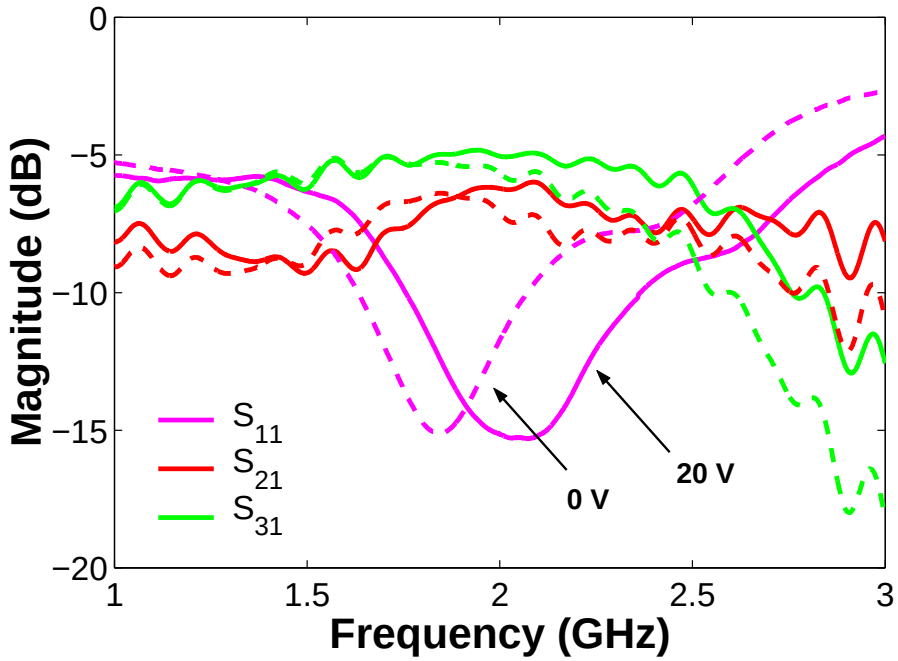


Figure 5.17: Measured insertion loss and return loss of the BST tunable hybrid coupler at 0 V bias (dashed lines) and 20 V bias (solid lines).

The measured insertion loss and return loss at 0 V and 20 V bias are shown in Figs. 5.17. Because the inductor values are below the design value, the hybrid does not tune all the way down to the DCS uplink band. At 1710 MHz, the return loss (S_{11}) is 12.2 dB and the insertion loss (S_{21}) is 6.4 dB. At 2200 MHz, the return loss (S_{11}) is 14.1 dB and the insertion loss (S_{21}) is 6.5 dB. Amplitude unbalance between the coupled ports is ∼1 dB, which is due to the inductances differing from the design values. The excess insertion loss above the ideal 3 dB coupling level is 3.5 dB in the worst case. Note also that the ripple in the insertion loss is associated with the wire bonded transition from the CPW test jig to the hybrid chip.

Figure 5.18 shows the variation in return loss (S_{11}) as the bias voltage is swept from 0 to 20 V. A wider tuning range could be achieved by applying larger bias voltages. However, since the fabrication of the tunable hybrid was somewhat time consuming, the bias voltage was limited to 20 V in order to avoid damaging the device.

The coupled port phase offset is shown in Fig. 5.19. A phase offset of 90±5° is maintained across the frequency range 1700 to 2200 MHz. This phase error is similar to results reported for a miniaturised hybrid coupler design [151].

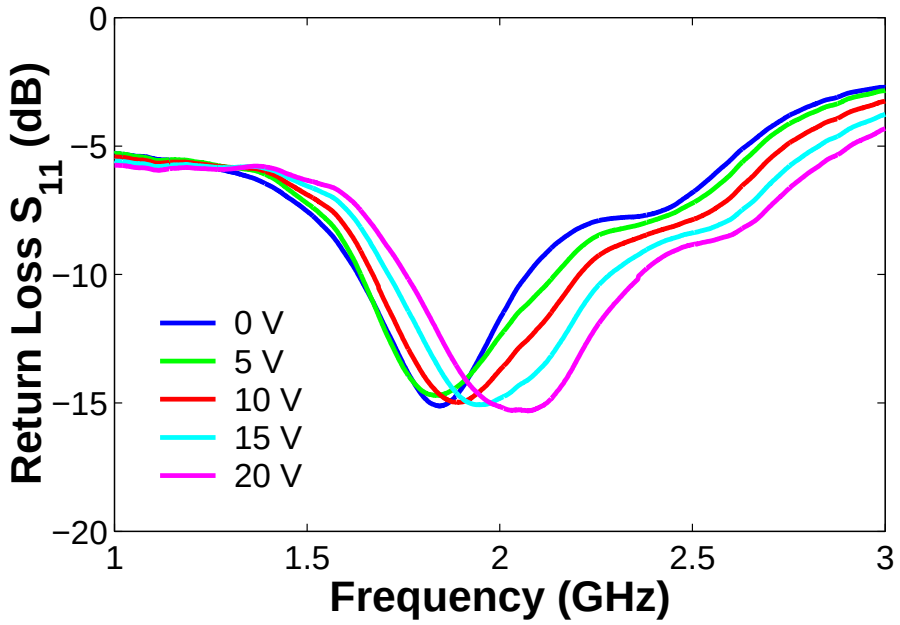


Figure 5.18: Measured return loss S_{11} of the BST tunable hybrid as the bias voltage is swept from 0 to 20 V.

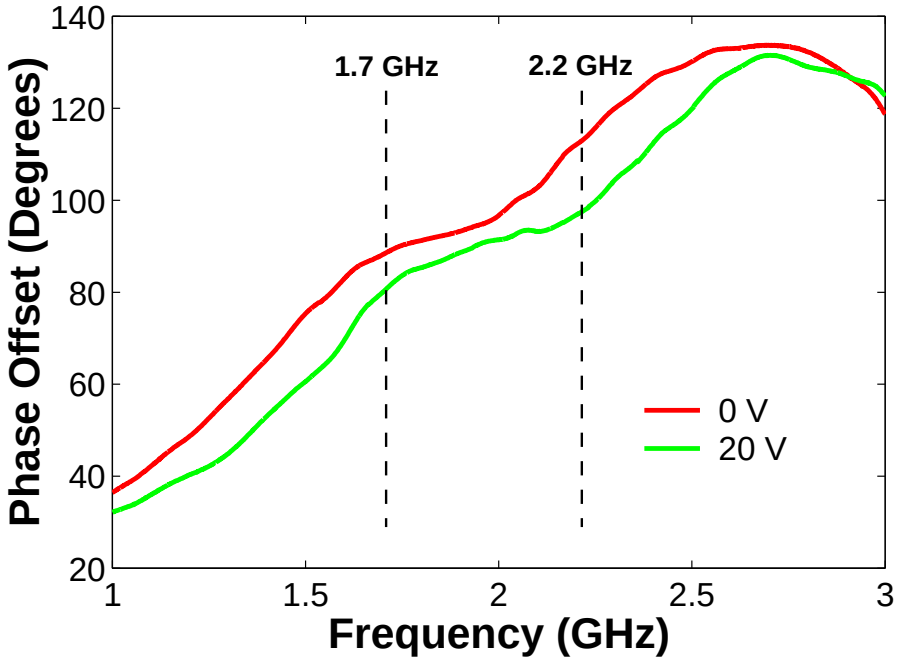


Figure 5.19: Measured coupled port phase offset of the BST tunable hybrid at 0 and 20 V bias.

5.7 Conclusions

This Chapter has investigated practical issues associated with the microwave circuit applications of BST varactors. A PDMS scattering mask technique was presented, which has the potential to reduce the gap between interdigital electrodes from 2 μm to $\sim$100 nm. This would reduce the voltage required to achieve >2:1 capacitance tunability in BST varactors.

The nonlinear properties of BST varactors were also investigated. For 2 μm gap varactors on c-plane sapphire, an OIP3 of 40 dBm was measured. Note that a similar OIP3 can be expected for the high tunability BST varactors on r-plane sapphire, since the tunability and therefore the shape of the capacitance-voltage curve is similar to the high tunability devices on c-plane sapphire. While an OIP3 of $\sim$40 dBm is probably acceptable for most receive systems, it is likely that a higher OIP3 would be required for transmit applications. It was also noted that a tradeoff between tunability and linearity can be made in BST interdigital varactors. Therefore, minimising the tuning voltage may not be advantageous in BST varactors that are to be used in large signal circuits. There is also an opportunity to investigate novel varactor configurations where the linearity is improved without increasing the tuning voltage.

A novel tunable hybrid coupler was also proposed, in which varactors were employed to tuned the centre frequency of the hybrid. The design was validated using commercial varactor diodes and microstrip transmission lines. A reduced-size prototype was then fabricated using surface mount lumped components. Finally, an integrated version of the lumped element hybrid coupler was realised using 2 μm gap BST varactors and planar inductors, with a chip size of 4 $\times$ 4 mm^2. The measured performance compares well with the lumped element prototype using commercial varactor diodes, although the insertion loss is up to 1.6 dB higher, and the tuning voltage was 20 V for the BST-based circuit, and 3.7 V for the semiconductor-based circuit. These results demonstrate the potential of BST varactors on sapphire substrates for tunable microwave circuit applications.

Chapter 6

Conclusions and Future Work

This thesis has investigated BST thin films from both a materials science and a microwave engineering perspective. The motivation for investigating BST films was to produce electronically tunable microwave components based on interdigital varactors. These components have the potential to reduce the component count in microwave circuits, whereby a useful space and cost savings can be realised.

BST thin films for microwave applications have been widely studied for around a decade now. Much of the existing work with interdigital BST varactors employs cubic substrates such as $LaAlO_3$ or MgO. Parallel plate BST varactors have also been reported by several research groups, where the BST film is grown on a Pt or Pt/Au bottom electrode with a silicon or *c*-plane sapphire substrate. Despite the relatively low cost of sapphire wafers, and the very low loss of sapphire at microwave frequencies, there are relatively few reports of BST films grown directly on sapphire substrates.

6.1 BST Thin Films on Sapphire Substrates

To address this gap in the existing body of knowledge, this thesis has investigated the materials and microwave properties of BST films on *c*- and *r*-plane sapphire substrates. A series of BST films were grown on *c*-plane sapphire by RF magnetron sputtering. For these experiments, a stoichiometric $Ba_{0.5}Sr_{0.5}TiO_3$ sputtering target was employed; the depositions were performed in-house at RMIT. Initially, the process gas (Ar/O_2 9:1) pressure was varied from 5 to 40 mTorr while maintaining a 625°C substrate temperature. The stoichiometry of the deposited films was measured by RBS, and films deposited at 40 mTorr were found to be closest in composition to the sputtering target.

The films deposited at 625°C were polycrystalline with weak <110> preferred

orientation. Interdigital electrodes were patterned on the film surface to allow measurement of the dielectric properties at microwave frequencies. In the 625°C series of films, the capacitance tunability was only a few percent, and therefore not useful for microwave circuit applications. Increasing the substrate temperature to 700°C resulted in strong <111> orientation in the BST film, although the growth was not epitaxial. Post deposition annealing of these films in air at 900°C for two hours improved the capacitance tunability to ∼56% at a bias field of 200 kV/cm, greater than the 50% target value for practical devices. The increased tunability was attributed to lower residual strain in the BST film following post-deposition annealing.

A potential limitation of BST films grown on *c*-plane sapphire is that this substrate material is not widely used in commercial semiconductor processes. In order for BST-based devices to achieve commercial success, it is important that the substrate material and processing steps are compatible with existing foundry processes. Since *r*-plane sapphire is used in the commercial SoS process, the materials and microwave properties of BST films grown on *r*-plane sapphire were also explored, with the aim of developing a process that could be used by a commercial SoS foundry. This work was done in collaboration with Rutgers, The State University of New Jersey.

For the study of BST films on *r*-plane sapphire, the films were grown by PLD in the Electroceramics Research Group lab at Rutgers University. A stoichiometric $Ba_{0.6}Sr_{0.4}TiO_3$ target was used for all depositions, with a substrate temperature of 700°C and 100 mTorr O_2 process gas. To establish the thickness dependence of materials and microwave properties of the film, a series of films with thickness ranging from 25 to 400 nm was prepared. The samples were annealed in an oxygen atmosphere inside the deposition chamber at 700°C for six hours before cooling to room temperature.

All of the BST films on *r*-plane sapphire were polycrystalline, with a trend of increasing <111> preferred orientation over the thickness range 25 to 200 nm. The 400 nm film showed a <110> preferred orientation. Residual strain measurements by XRD showed a high tensile residual strain in the thinnest films. As the film thickness increased, the residual strain decreased to zero at around 200 nm film thickness. A compressive residual strain was observed in the 400 nm film.

The microwave properties of the BST films on *r*-plane sapphire were measured by the same interdigital capacitor technique employed for the BST films on *c*-plane sapphire. A high capacitance tunability of ∼64% was achieved with the 200 nm film. The tunability was directly related to the in-plane strain, with lower tunability measured in the films with higher residual strain. However, the highest tunability

film possessed a rather low Q-factor of ∼8 at 10 GHz. The highest Q-factor of ∼23 at 10 GHz was achieved in the thinnest (25 nm) film. An interesting result here is that there is a critical thickness where the BST film is strain relieved, and therefore has high tunability.

6.2 Microwave Circuit Applications

The microwave circuit applications of BST thin films were also investigated as part of this thesis. In order to achieve high tunability, a relatively large bias voltage of 40 V was applied to the varactors. Ideally, the tuning voltage should be less than 5 V for practical microwave circuits. This could be achieved by lowering the gap between the interdigital electrodes. A novel photolithographic technique, based on an elastomeric scattering mask was used to fabricate ∼100 nm gaps in a thin metal film. This technique could be applied to realise interdigital capacitors with a narrow gap between the electrodes, thereby reducing the bias voltage.

Intermodulation distortion is an important parameter in BST devices, due to the nonlinear characteristic of the capacitance-voltage curve. A test setup was designed to measure the OIP3 of the BST varactors on sapphire. For two 0 dBm fundamental tones, the OIP3 of the high-tunability devices on c-plane sapphire was better than 40 dBm over the bias voltage range. While this is likely to be sufficiently high for receive applications, high power transmit applications would likely require a higher OIP3 value.

In order to demonstrate the BST varactors in a practical microwave circuit, a novel tunable hybrid coupler was designed. An initial design used a conventional microstrip branch-line hybrid, with each branch loaded at the midpoint by a commercial semiconductor varactor. While the electrical performance of the circuit was very good, quarter-wave transmission lines are undesirable for integrated circuit applications due to the large amount of layout space required. Therefore, a tunable lumped element hybrid was designed an implemented, also using commercially available surface mount components. Finally, an integrated version of the lumped element hybrid was implemented using BST varactors and planar spiral inductors. The total chip size was 4×4 mm^2. These results demonstrate that BST/sapphire thin film varactors are a viable alternative to semiconductor varactors for electronically tunable microwave circuits.

6.3 Future Work

Perhaps the biggest unresolved issue with BST devices is the relatively low Q-factors achieved in high tunability films. While a Q-factor of greater than 100 is desirable for microwave circuit applications, most BST varactors reported in the literature have a Q-factor of 25 or lower at 10 GHz. Despite many efforts over the last decade or so, achieving simultaneously high tunability and high Q-factor remains difficult.

In terms of the work performed as part of this thesis, further efforts are required to demonstrate the repeatability of the results achieved. Some confidence can be gained from the sputtered BST films on c-plane sapphire, where a capacitance tunability of greater than 50% was consistently achieved on samples from different deposition runs. In order to be able to accurately regulate the stoichiometry, purity and crystal orientation of the BST films, careful control of the deposition conditions, including substrate temperature and process gas pressure, are required. It is possible that optimisation of the processing conditions, in particular the substrate temperature and the post-deposition annealing time, will provide improvements in device performance.

Further work is also required to lower the tuning voltage and to improve the device linearity. While the IP3 normally trades with tuning voltage in conventional interdigital and parallel plate BST varactors, it should be possible to improve the linearity through novel device configurations.

Reliability testing of varactor performance over a wide operating temperature range is desirable, in order to ensure that device tunability and Q-factor are still acceptable at the hot and cold temperature extremes. It may also be useful to measure the intermodulation performance over temperature. The bias voltage could additionally be swept from minimum to maximum over an extended period of time to ensure that the device does not break down and that there are no undesired effects related to charge storage at the electrode–film interface.

In the longer term, it would be useful to perform a pilot run with BST thin films on r-plane sapphire as part of a commercial SoS foundry process. This would help to demonstrate the commercial viability of BST thin films. If the improvements outlined above can be made, and in particular, the device Q-factor improved, it is quite possible that BST-based components will see application in commercial foundry processes in the medium to long term.

6.4 Concluding Remarks

This thesis has investigated the materials and microwave properties of BST thin films grown on single-crystal sapphire substrates. The growth conditions for achieving more than 50% capacitance tunability were established for films deposited on *c*- and *r*-plane substrates. Sputtering was employed for the BST films grown on *c*-plane sapphire, while pulsed laser deposition was employed for the films grown on *r*-plane sapphire. From a commercial perspective, *r*-plane sapphire is of particular interest, since these substrates are used in the SoS process for high performance microwave and mixed signal integrated circuits.

The microwave circuit applications of the BST/sapphire films were also investigated. A technique for lowering the tuning voltage by decreasing the gap between the interdigital electrodes was presented. The nonlinear properties of BST varactors were explored, and an OIP3 of >40 dBm was measured for the *c*-plane sapphire devices. Finally, a novel frequency agile hybrid coupler was developed. The design was initially validated using commercial varactor diodes; an integrated version was then realised using BST varactors and planar inductors. These results demonstrate the potential of BST thin films in tunable microwave circuit applications.

Appendix A

Matlab Code

A.1 Capacitance Extraction from Measured S-parameter Data

```
0001 % Extract frequency dependent R,C from S-parameter data
0002 % Change Log
0003 % 20060220 changed order of arguments to fsolve to fix bug
0004 %           that occurred with R_p
0005
0006 C_i = 0.2; % capacitance guesstimate in pF
0007 L_i = 0.1; % inductance guesstimate in nH
0008 R_i = 1; % 1 Ohm guesstimate
0009 Z_o = 50;
0010
0011 % Parasitic values
0012 C_p = 0.0060; % pad parasitic capacitance in pF
0013 L_p = 0.0140; % pad parasitic inductance in nH
0014 R_p = 0.0495; % pad equivalent resistance in Ohms
0015
0016 NumPoints = 1601;   % number of points in s2p file
0017
0018 %Read input file
0019 fid=fopen('<filename>.txt','r');
0020 [freq,s11_m,s11_a,s12_m,s12_a,s21_m,s21_a,s22_m,s22_a]...
0021 =textread('<filename>.txt','%f%f%f%f%f%f%f%f%f',-1);
0022 fclose(fid);
0023
0024 s11_dB=10*log10(1./((s11_m).^2));
0025 s11_cplx=s11_m.*exp(j.*(pi/180)*s11_a); %port 1
0026 %s11_cplx=s22_m.*exp(j.*(pi/180)*s22_a); %port 2
0027
```

```
0028 R_vec=zeros(1,1601);
0029 C_vec=zeros(1,1601);
0030 Q_vec=zeros(1,1601);
0031
0032 for(index=1:NumPoints)
0033     r=real(s11_cplx(index,1));
0034     i=imag(s11_cplx(index,1));
0035     z_r=real( Z_o*(1+s11_cplx(index,1))/(1-s11_cplx(index,1)) );
0036     z_i=imag( Z_o*(1+s11_cplx(index,1))/(1-s11_cplx(index,1)) );
0037     y_r=real( (1/Z_o)*(1-s11_cplx(index,1))/(1+s11_cplx(index,1)) );
0038     y_i=imag( (1/Z_o)*(1-s11_cplx(index,1))/(1+s11_cplx(index,1)) );
0039     omega=2*pi*freq(index,1)*1E+9;
0040     'V=[R;C]'; % Open, DUT
0041     %'V=[R;L]'; % Short
0042
0043     % Open Standard
0044 %     F=inline('[((1+(((V(2)/1E+12).^2)*(omega.^2)*((V(1).^2)-...
          (Z_o.^2))))/(1+(omega.*(V(2)/1E+12)*(V(1)+Z_o)).^2))-r;...
0045 %     (((-2*omega.*(V(2)/1E+12).*Z_o)./(1+(omega.*...
          (V(2)/1E+12).*(V(1)+Z_o)).^2)))-i]','V','omega','Z_o',...
          'r','i');
0046 %     InitialGuess=[R_i;C_i];
0047 %     Options = optimset('TolX',1E-10,'TolFun',1E-8);
0048 %     XY=fsolve(F, InitialGuess, Options, omega,Z_o,r,i);
0049
0050     % Short Standard
0051 %     %F=inline('[((V(1))/( (1-(omega.^2)*(V(2)/1E+9)*...
          C_p/1E+12).^2 + (omega*V(1)*C_p/1E+12).^2 ))-z_r;...
0052 %       (( omega*(V(2)/1E+9) - omega*(V(1).^2)*(C_p/1E+12) -...
          (omega.^3)*((V(2)/1E+9).^2)*C_p/1E+12 )./...
          ( (1-(omega.^2)*(V(2)/1E+9)*...
0053 %       C_p/1E+12).^2 + (omega*V(1)*C_p/1E+12).^2 ) )-z_i]',...
          'V','omega','C_p','z_r','z_i');
0054 %     F=inline('[((V(1))/( (V(1)).^2 +...
          (omega*V(2)/1E+9).^2 ))-y_r;...
0055 %       ((omega*C_p/1E+12)+(( -omega*(V(2)/1E+9) )./...
          ( (V(1)).^2 + (omega*V(2)/1E+9).^2 )) )-y_i]',...
          'V','omega','C_p','y_r','y_i');
0056 %     InitialGuess=[R_i;L_i];
0057 %     Options = optimset('TolX',1E-10,'TolFun',1E-8);
0058 %     XY=fsolve(F, InitialGuess, Options, omega,C_p,y_r,y_i);
0059
0060     % DUT
0061 F=inline('[(((omega.^2)*(R_p+V(1))*((V(2)/1E+12).^2))/...
     ((1-(omega.^2)*(L_p/1E+9)*(V(2)/1E+12)).^2+...
     (omega*(R_p+V(1))*(V(2)/1E+12)).^2))-y_r;...
```

```
0062 ((omega*(C_p/1E+12))+((omega*(V(2)/1E+12)-...
     (omega.^3)*(L_p/1E+9)*(V(2)/1E+12).^2 )/...
     ((1-(omega.^2)*...
0063 (L_p/1E+9)*(V(2)/1E+12)).^2+(omega*(R_p+V(1))*...
     (V(2)/1E+12)).^2)))-y_i]','V','omega','R_p','L_p',...
     'C_p','y_r','y_i');
0064     InitialGuess=[R_i;L_i];
0065     Options=optimset('TolX',1E-10,'TolFun',1E-12);
0066     XY=fsolve(F,InitialGuess,Options,omega,R_p,L_p,C_p,y_r,y_i);
0067
0068     R_vec(1,index)=XY(1,1);
0069     C_vec(1,index)=XY(2,1);
0070     Q_vec(1,index)=1/(omega*XY(1,1)*(XY(2,1)/1E12));
0071     Z_vec(index,1)=(1/Z_o)*((XY(1,1)+1/(j*omega*(XY(2,1)/1E12))));
0072 end
```

A.2 Permittivity Extraction from Measured Capacitance Data

```
0001 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
0002 % Based on J. Bellotti, "Strain and Thickness Effects on the Microwave
0003 % Properties of BST Thin Films," PhD dissertation, Rutgers, The
0004 % State University of New Jersey, 2003.
0005 %
0006 % Also based on the papers:
0007 %
0008 % 1. "Modelling of thin-film HTS/ferroelectric interdigital
0009 %     capacitors,"
0010 %    S. Gevorgian, E Carlsson, S. Rudner, L.-D. Wernlund, X. Wang,
0011 %    and U. Helmersson, IEE Proceedings - Microwaves, Antennas, and
0012 %    Propagation, vol. 13, no. 5, pp. 307-401, Oct. 1996.
0013 %
0014 % 2. "CAD Models for Multilayered Substrate Interdigital
0015 %    Capacitors," S. Gevorgian, T. Martinsson, P.L.J. Linner, and
0016 %    E. Kollberg, IEEE Trans. on Microwave Theory and Tech., vol. 44,
0017 %    no. 6, pp. 896-904, Jun. 1996.
0018 %
0019 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
0020
0021 eps_0 = 8.854E-18;
0022 epsstn = 100; % Dielectric constant calculated by Touchstone
0023 h2 = 0.05; % Ferroelectric film thickness (microns)
0024 h_sub = 500; % Substrate thickness (microns)
0025 epssub = 9.4; % Substrate dielectric constant
```

```
0026 epsflm = 310; % Ferroelectric film dielectric constant
0027 % w = 40; % finite width terminals
0028 t = 2.5; % Metal film thickness (microns)
0029 if(t<0.01)
0030 t=0.01;
0031 end
0032 gapspace = 2; % Gap space (microns)
0033 g = gapspace/2;
0034 %gend = g;
0035 gend = 5; % 2 um BST varactors
0036 xfactor = 0.5; % End gap factor
0037 fingerwidth = 5; % Finger width (microns)
0038
0039 s =(fingerwidth/2)+(t/(2*pi))*(1+log(4*pi*fingerwidth/t));
0040
0041 % Following is suggested in I.J. Bahl, "Lumped Elements for RF and
0042 %   Microwave Circuits"
0043 % g = gapspace/2-(t/(2*pi))*(1+log(4*pi*fingerwidth/t));
0044 % gend = g;
0045 % fprintf('s = %f\n', s);
0046
0047 length = 80; % Finger overlap length (microns)
0048 n = 8; % Number of fingers
0049 h1 = h_sub + h2;
0050 h3 = h_sub;
0051
0052 % Defining the hyperbolic arguments for the periodic structure
0053 % (Ref. 1)
0054 argn11 = pi*s/(2*h1);
0055 argn12 = pi*(s+g)/(2*h1);
0056 argn21 = pi*s/(2*h2);
0057 argn22 = pi*(s+g)/(2*h2);
0058 argn31 = pi*s/(2*h3);
0059 argn32 = pi*(s+g)/(2*h3);
0060
0061 % Defining the hyperbolic arguments for the outside edge fingers
0062 % (Ref. 2)
0063 arg311 = pi*s/(2*h1);
0064 arg312 =pi*(s+2*g)/(2*h1);
0065 arg313 = pi*(s+2*s+2*g)/(2*h1);
0066 arg321=pi*s/(2*h2);
0067 arg322=pi*(s+2*g)/(2*h2);
0068 arg323=pi*(s+2*s+2*g)/(2*h2);
0069 arg331=pi*s/(2*h3);
0070 arg332=pi*(s+2*g)/(2*h3);
0071 arg333=pi*(s+2*s+2*g)/(2*h3);
```

```
0072
0073 % Defining the hyperbolic arguments for the end gaps (Ref. 1)
0074 % INFINITE WIDTH TERMINALS
0075 arge11 = pi*xfactor*s/(2*h1);
0076 arge12=pi*(xfactor*s+2*gend)/(2*h1);
0077 arge21 = pi*xfactor*s/(2*h2);
0078 arge22=pi*(xfactor*s+2*gend)/(2*h2);
0079 arge31 = pi*xfactor*s/(2*h3);
0080 arge32=pi*(xfactor*s+2*gend)/(2*h3);
0081
0082 % FINITE WIDTH TERMINALS
0083 % arge11 = pi*s/(2*h1);
0084 % arge12 = pi*(s+2*gend)/(2*h1);
0085 % arge13 = pi*(s+w+2*gend)/(2*h1);
0086 % arge21 = pi*s/(2*h2);
0087 % arge22 = pi*(s+2*gend)/(2*h2);
0088 % arge23 = pi*(s+w+2*gend)/(2*h2);
0089 % arge31 = pi*s/(2*h3);
0090 % arge32 = pi*(s+2*gend)/(2*h3);
0091 % arge33 = pi*(s+w+2*gend)/(2*h3);
0092
0093 % For the periodic portion (Ref. 1)
0094 k0 = s/(s+g);
0095 k0pr = sqrt(1-k0^2);
0096
0097 % For the outside edge fingers (Eqn. 10 of Ref. 1)
0098 k03=(s/(s+2*g))*sqrt((1-((s+2*g)/(s+2*s+2*g))^2)/...
0099     (1-((s)/(s+2*s+2*g))^2));
0100 k03pr=sqrt(1-k03^2);
0101
0102 % For the endgap portion (Eqn. 15 of Ref. 1)
0103 % k0end = (xfactor*s/(xfactor*s+2*gend))*...
0104 % sqrt((1-((xfactor*s+2*gend)/(xfactor*s+w+2*gend))^2)/...
0105 % (1-((xfactor*s)/(xfactor*s+w+2*gend))^2)); % finite
0106 k0end = (xfactor*s/(xfactor*s+2*gend)); % infinite
0107 k0endpr = sqrt(1-k0end^2);
0108
0109 % Eqn. 5 of Ref. 1 gives (for the periodic portion)
0110 k1n=(sinh(argn11)/sinh(argn12))*sqrt(((cosh(argn12))^2+...
0111 (sinh(argn12))^2)/((cosh(argn11))^2+(sinh(argn12))^2));
0112 k1npr = sqrt(1-k1n^2);
0113 k2n=(sinh(argn21)/sinh(argn22))*sqrt(((cosh(argn22))^2+...
0114 (sinh(argn22))^2)/((cosh(argn21))^2+(sinh(argn22))^2));
0115 k2npr = sqrt(1-k2n^2);
0116
0117 % This term is also calculated to compare to Touchstone's
```

```
0118 % number for a homogeneous substrate
0119 k3n=(sinh(argn31)/sinh(argn32))*sqrt(((cosh(argn32))^2+...
0120 (sinh(argn32))^2)/((cosh(argn31))^2+(sinh(argn32))^2));
0121 k3npr = sqrt(1-k3n^2);
0122
0123 % Eqn. 14 of Ref. 2 (for ultrathin films only)
0124 % k1n = sqrt(2)*exp(-pi*g/(2*h1));
0125 % k1npr = sqrt(1-k1n^2);
0126 % k2n = sqrt(2)*exp(-pi*g/(2*h2));
0127 % k2npr = sqrt(1-k2n^2);
0128 % k3n = sqrt(2)*exp(-pi*g/(2*h3));
0129 % k3npr = sqrt(1-k3n^2);
0130
0131 fprintf('k1n=%f,\tk1npr=%f\n',k1n,k1npr);
0132 fprintf('k2n=%f,\tk2npr=%f\n',k2n,k2npr);
0133 fprintf('k3n=%f,\tk3npr=%f\n',k3n,k3npr);
0134
0135 % Eqn. 11 of Ref. 1 gives (for the outside edge fingers):
0136 k13=(sinh(arg311)/sinh(arg312))*sqrt(1-(((sinh(arg312))^2)/...
0137 (sinh(arg313))^2)/(1-(((sinh(arg311))^2)/(sinh(arg313))^2)));
0138 k13pr = sqrt(1-k13^2);
0139 k23=(sinh(arg321)/sinh(arg322))*sqrt(1-(((sinh(arg322))^2)/...
0140 (sinh(arg323))^2)/(1-(((sinh(arg321))^2)/(sinh(arg323))^2)));
0141 k23pr = sqrt(1-k23^2);
0142 k33=(sinh(arg331)/sinh(arg332))*sqrt(1-(((sinh(arg332))^2)/...
0143 (sinh(arg333))^2)/(1-(((sinh(arg331))^2)/(sinh(arg333))^2)));
0144 k33pr = sqrt(1-k33^2);
0145
0146 fprintf('k13=%f\n',k13pr);
0147 fprintf('k23=%f\n',k23pr);
0148 fprintf('k33=%f\n',k33pr);
0149
0150 % Eqn. 16 of Ref. 1 gives (for the end gap contribution)
0151 % INFINITE WIDTH TERMINALS
0152 k1end = sinh(arge11)/sinh(arge12);
0153 k1endpr=sqrt(1-k1end^2);
0154 k2end=sinh(arge21)/sinh(arge22);
0155 k2endpr=sqrt(1-k2end^2);
0156 k3end=sinh(arge31)/sinh(arge32);
0157 k3endpr=sqrt(1-k3end^2);
0158
0159 % FINITE WIDTH TERMINALS
0160 % k1end = (sinh(arge11)/sinh(arge12))*sqrt(1-(((sinh(arge12))^2)/...
0161 % (sinh(arge13))^2)/(1-(((sinh(arge11))^2)/(sinh(arge13))^2)));
0162 % k1endpr = sqrt(1-k1end^2);
0163 % k2end = (sinh(arge21)/sinh(arge22))*sqrt(1-(((sinh(arge22))^2)/...
```

```
0164 % (sinh(arge23))^2)/(1-(((sinh(arge21))^2)/(sinh(arge23))^2)));
0165 % k2endpr = sqrt(1-k2end^2);
0166 % k3end = (sinh(arge31)/sinh(arge32))*sqrt(1-(((sinh(arge32))^2)/...
0167 % (sinh(arge33))^2)/(1-(((sinh(arge31))^2)/(sinh(arge33))^2)));
0168 % k3endpr = sqrt(1-k3end^2);
0169
0170 fprintf('k1end=%f\n',k1endpr);
0171 fprintf('k2end=%f\n',k2endpr);
0172 fprintf('k3end=%f\n',k3endpr);
0173
0174 % Eqn. 4 of Ref. 1 gives
0175 q1n=(K(k1n,k1npr)*K(k0pr,k0))/(K(k1npr,k1n)*K(k0,k0pr));
0176 q2n=(K(k2n,k2npr)*K(k0pr,k0))/(K(k2npr,k2n)*K(k0,k0pr));
0177 % q1n = (K(k1n,k1npr)*K(k0pr,k0));
0178 % q2n = (K(k2n,k2npr)*K(k0pr,k0));
0179
0180 % This term is also calculated to compare to Touchstone's
0181 % number for a homogeneous substrate
0182 q3n=(K(k3n,k3npr)*K(k0pr,k0))/(K(k3npr,k3n)*K(k0,k0pr));
0183 % q3n = (K(k3n,k3npr)*K(k0pr,k0));
0184
0185 fprintf('qin=%f,%f,%f\n',q1n,q2n,q3n);
0186
0187 % Eqn. 9 of Ref. 1 gives
0188 q13=(K(k13,k13pr)*K(k03pr,k03))/(K(k13pr,k13)*K(k03,k03pr));
0189 q23=(K(k23,k23pr)*K(k03pr,k03))/(K(k23pr,k23)*K(k03,k03pr));
0190 % q13 = (K(k13,k13pr)*K(k03pr,k03));
0191 % q23 = (K(k23,k23pr)*K(k03pr,k03));
0192
0193 % This term is also calculated to compare to Touchstone's
0194 % number for a homogeneous substrate
0195 q33=(K(k33,k33pr)*K(k03pr,k03))/(K(k33pr,k33)*K(k03,k03pr));
0196 % q33 = (K(k33,k33pr)*K(k03pr,k03));
0197 fprintf('qi3=%f,%f,%f\n',q13,q23,q33);
0198
0199 % Eqn. 14 of Ref. 1 gives
0200 q1end=(K(k1end,k1endpr)*K(k0endpr,k0end))/(K(k1endpr,k1end)*...
0201     K(k0end,k0endpr));
0202 q2end=(K(k2end,k2endpr)*K(k0endpr,k0end))/(K(k2endpr,k2end)*...
0203     K(k0end,k0endpr));
0204 % q1end = (K(k1end,k1endpr)*K(k0endpr,k0end));
0205 % q2end = (K(k2end,k2endpr)*K(k0endpr,k0end));
0206
0207 % This term is also calculated to compare to Touchstone's
0208 % number for a homogeneous substrate
0209 q3end=(K(k3end,k3endpr)*K(k0endpr,k0end))/(K(k3endpr,k3end)*...
```

```
0210      K(k0end,k0endpr));
0211 % q3end = (K(k3end,k3endpr)*K(k0endpr,k0end));
0212 fprintf('qiend=%f,%f,%f\n',q1end,q2end,q3end);
0213
0214 % The effective dielectric constant for the periodic structure
0215 % (Eqn. 3 of Ref. 1)
0216 epseffn = 1+(q1n*(epssub-1)/2)+q2n*(epsflm-epssub)/2;
0217 % The effective dielectric constant for the side strips
0218 % (Eqn. 31 of Ref. 1)
0219 epseff3 = 1 + q13*(epssub-1)/2+q23*(epsflm-epssub)/2;
0220 % The effective dielectric constant for the end gaps
0221 % (Eqn. 13 of Ref. 1)
0222 epseffend=1+(q1end*(epssub-1)/2)+q2end*(epsflm-epssub)/2;
0223 fprintf('epseff=%f,%f,%f\n',epseffn,epseff3,epseffend);
0224
0225 % The capacitance contribution from the periodic structure
0226 % (Eqn. 2 of Ref. 1)
0227 cn=(n-3)*eps_0*epseffn*(K(k0,k0pr)/K(k0pr,k0))*length;
0228
0229 % The capacitance contribution from the side strips
0230 % (Eqn. 7 of Ref. 1)
0231 % ***CORRECTS MISTAKE IN FORMULA IN PAPER***
0232 c3=4*eps_0*epseff3*(K(k03,k03pr)/K(k03pr,k03))*length;
0233 % ***PAPER VERSION***
0234 %c3 = 4*eps_0*epseff3*(K(k03pr,k03)/K(k03,k03pr))*length;
0235 % (Eqns. 12, 15 of Ref. 12) - Gives similar result to
0236 % corrected version above
0237 % c3 = 4*eps_0*(K(k03,k03pr)/K(k03pr,k03))*length +...
0238 % 2*eps_0*(epssub-1)*(K(k23,k23pr)/K(k23pr,k23))*length;
0239 % c3 = 4*eps_0*epseff3*(K(k03,k03pr))*length;
0240
0241 % The capacitance contribution from the end gaps
0242 % (Eqn. 12 of Ref. 1)
0243 cend=4*n*gend*(2+pi)*eps_0*epseffend*(K(k0end,k0endpr)/...
0244      K(k0endpr,k0end));
0245 % EAF Model
0246 % cend = 4*eps_0*epseffend*(K(k0end,k0endpr)/K(k0endpr,k0end))*...
0247 % ((n*s*(2+pi))-pi*s);
0248 % cend = 4*n*s*(2+pi)*eps_0*epseffend*(K(k0end,k0endpr));
0249 %fprintf('k0 = %f,\tk03 = %f,k0end = %f\n', k0, k03, k0end);
0250 fprintf('cterms(n,3,end)=%e,%e,%e\n',cn,c3,cend);
0251
0252 % The total capacitance from Eqn. 1 of Ref. 1 is (in pF)
0253 c = (c3+cn+cend)*1E+12;
0254 fprintf('Total capacitance(pF)=%f\n',c);
0255
```

```
0256 % function arctan2(y_,x_)
0257 % if(x_>0)
0258 %     angle = atan(y_/x_);
0259 % end
0260 % if(x_<0)
0261 %     angle = atan(y_/x_)+pi;
0262 % end
0263 % if((x_=0)&&(y_>0))
0264 %     angle=pi/2;
0265 % end
0266 % if((x_=0)&&(y_<0))
0267 %     angle=-pi/2;
0268 % end
0269 % if((x_=0)&&(y=0))
0270 %     angle=0;
0271 % end
0272 % if(angle>pi)
0273 %     angle=angle-2*pi;
0274 % end
0275 % if(angle<-pi)
0276 %     angle=angle+2*pi;
0277 % end
0278 % arctan2=angle;
0279 % end
0280
0281 % function CH(x)
0282 % CH = (exp(x)+exp(-x))/2;
0283 % end
0284
0285 function K(x,xx)
0286 % The argument of the elliptic integral is x. However, when x = k (rather
0287 % than xx = k) and k << 1, numerical accuracy limits k' = sqrt(1-k^2) = 1.
0288 % This results in y = 1-x + 0 which causes a divide by zero error. To avoid
0289 % this, if x = 1 (due to the numerical truncation) the y is approximated by
0290 % (xx = k is passed as the second argument just for this case): y =
0291 % sqrt(1-k^2) = 1 - (1 - 0.5*k^2) = 0.5*k^2
0292 a0=1.38629436112;
0293 a1=0.09666344259;
0294 a2=0.03590092383;
0295 a3=0.03742563713;
0296 a4=0.01451196212;
0297
0298 b0=0.5;
0299 b1=0.12498593597;
0300 b2=0.06880248576;
0301 b3=0.03328355346;
```

```
0302 b4=0.00441787123;
0303 if(x>=0.999999999)
0304 x=xx^2/2;
0305 else
0306 y=1-x;
0307 end
0308 K=(a0+(a1+(a2+(a3+a4*y)*y)*y)+(b0+(b1+(b2+(b3+b4*y)*y)*y)*y)*log(1/y);
0309 end
0310
0311 % function SH(x)
0312 % SH=(exp(x)-exp(-x)/2);
0313 % end
```

Appendix B

Interdigital Varactor Fabrication

B.1 Process Steps

1. Rinse sapphire substrate in acetone / isopropyl alcohol (IPA) / de-ionised water (DI).
2. Blow-dry sample with N_2.
3. Dehydration bake sample at 110°C for 20 min.
4. Place sample in sputterer/PLD system and deposit BST film.
5. Rinse sapphire substrate in acetone / IPA / DI.
6. Blow-dry sample with N_2.
7. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
8. Spin on AZ5206E photoresist at 2000 rpm for 60 sec (RC-8, closed lid).
9. Soft bake sample on hotplate 95°C for 55 sec.
10. Edge bead exposure MJB3 CR1 25 sec.
11. Develop photoresist in AZ400K:DI 1:4 15 sec.
12. Seed layer pattern exposure MJB3 CR1 8 sec.
13. Develop photoresist in AZ400K:DI 1:4 10 sec.
14. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
15. Deposit 10 nm Ti / 10 nm Ni / 50 nm Au in e-beam evapourator.

16. Perform liftoff of seed layer pattern by placing sample in acetone ultrasonic bath for 5 min.
17. Rinse sample in acetone / IPA / DI.
18. Blow-dry sample with N_2.
19. Dehydration bake sample at 110°C for 20 min.
20. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
21. Spin on AZ P4620 photoresist at 6000 rpm for 60 sec (RC-8, closed lid).
22. Soft bake sample in oven at 90°C for 15 min.
23. Edge bead exposure MJB3 CR1 2 min.
24. Develop photoresist in AZ400K:DI 1:4 1 min.
25. Electroplating pattern exposure MJB3 CR1 25 sec (careful alignment to seed layer pattern is required).
26. Develop photoresist in AZ400K:DI 1:4 40 sec.
27. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
28. Electroplate 2.5 μm Au.
29. Rinse sample in acetone / IPA / DI.
30. Blow-dry sample with N_2.
31. Dehydration bake sample at 110°C for 20 min.
32. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
33. Spin on AZ P4620 photoresist at 4000 rpm for 60 sec (RC-8, closed lid).
34. Soft bake sample in oven at 90°C for 15 min.
35. Edge bead exposure MJB3 CR1 2 min.
36. Develop photoresist in AZ400K:DI 1:4 1 min.
37. Seed layer etch pattern exposure MJB3 CR1 25 sec.
38. Develop photoresist in AZ400K:DI 1:4 40 sec.

39. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
40. Etch Au seed layer in cyanide solution for 40 sec.
41. Rinse sample in DI and blow-dry with N_2.
42. Etch Ni seed layer in Ni-etchant solution for 30 sec.
43. Rinse sample in DI and blow-dry with N_2.
44. Etch Ti seed layer in Ti-etchant solution for 15 sec.
45. Rinse sample in DI and blow-dry with N_2.
46. Dehydration bake sample at 110°C for 5 min.

B.2 Gold Electroplating Procedure

1. Sluice entire fume cupboard with water to ensure clean.
2. Set up Keithley current source, digital multimeter, 3000 ml glass beaker, stirrer/hotplate with temperature probe, wire mesh (cathode), retort stand and clamp, sample holder (anode), and place cyanide labels on fume cupboard sash.
3. Follow all cyanide handling procedures.
4. Thoroughly rinse glass beaker and temperature probe in DI water.
5. Rinse magnetic stirrer widget in DI water and place into glass beaker.
6. Remove plating solution from storage cabinet and place in fume cupboard. Pour 2500 ml plating solution into glass beaker, and return plating solution container to storage cabinet.
7. Carefully place glass beaker containing plating solution on hotplate and insert temperature probe.
8. Cover top of beaker with plastic wrap to avoid evaporation. Turn on hotplate and stirrer (settings marked on front panel) and wait for plating solution to heat to 40°C (∼15 min.)
9. Wash sample to be plated in DI water and place in anode clamp assembly, ensuring that two alligator clips are completely dry. Blow dry with N_2 if necessary.

10. Remove plastic cover from beaker and rinse to remove any cyanide, then discard plastic.

11. Place anode assembly in clamp on retort stand (raised so that sample is not submerged in plating solution).

12. Make electrical connections to anode and cathode.

13. Lower retort stand clamp so that sample is submerged in plating solution. Ensure that bottom of alligator clips are at least 10 mm above plating solution. Fine adjustment can be achieved using knurled knob on anode assembly.

14. Check for gas bubbles on seed layer. If bubbles are present, remove sample and then re-immerse.

15. Switch on current source. Set 'V-LIM' to 10 V, and 'CURRENT' to required value to obtain current density of 3.4 mA/cm^2. This can be calculated from the submerged seed layer area. Important: the current should be set to negative.

16. Press 'OPERATE' on current source to commence plating. Plating rate is $\sim$1'm every 5 min.

17. Monitor process, ensuring that gas bubbles to not form on seed layer. If bubbles do occur, disable current source by pressing 'OPERATE', wait for bubble(s) to dissipate, then re-start plating.

18. After 5 min, record multimeter voltage in log book. Ideally, this should be between -1.3 and -1.4 V if current density is correct.

19. After plating is complete, switch off current source and hotplate/stirrer.

20. Raise clamp on retort stand so that sample lies above plating solution, and remove electrical connections.

21. Remove anode assembly from clamp and rinse thoroughly in DI water. Remove sample.

22. Place gold plating solution container in fume cupboard and return plating solution to container using designated funnel. Allow stirrer widget to fall into funnel while pouring.

23. Return plating solution to storage cupboard.

24. Thoroughly rinse beaker, funnel, stirrer temperature probe and any other equipment that may have been exposed to plating solution in DI water.

25. Return all equipment to storage cupboard.

Appendix C

Tunable Hybrid Fabrication

C.1 Process Steps

1. Rinse sapphire substrate in acetone / isopropyl alcohol (IPA) / de-ionised water (DI).
2. Blow-dry sample with N_2.
3. Dehydration bake sample at 110°C for 20 min.
4. Place sample in sputterer and deposit BST film.
5. Rinse sapphire substrate in acetone / IPA / DI.
6. Blow-dry sample with N_2.
7. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
8. Spin on AZ P4620 photoresist at 6000 rpm for 60 sec (RC-8, closed lid).
9. Soft bake sample in oven at 90°C for 15 min.
10. Edge bead exposure MJB3 CR1 2 min.
11. Develop photoresist in AZ400K:DI 1:4 1 min.
12. BST etch pattern exposure MJB3 CR1 25 sec.
13. Develop photoresist in AZ400K:DI 1:4 30 sec.
14. Etch BST layer in Ti-etchant for 2 min.
15. Rinse sample in DI and blow-dry with N_2.

16. Dehydration bake sample at 110°C for 20 min.
17. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
18. Spin on AZ5206E photoresist at 2000 rpm for 60 sec (RC-8, closed lid).
19. Soft bake sample on hotplate 95°C for 55 sec.
20. Edge bead exposure MJB3 CR1 25 sec.
21. Develop photoresist in AZ400K:DI 1:4 15 sec.
22. Seed layer pattern exposure MJB3 CR1 8 sec.
23. Develop photoresist in AZ400K:DI 1:4 10 sec.
24. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
25. Deposit 10 nm Ti / 10 nm Ni / 50 nm Au in e-beam evapourator.
26. Perform liftoff of seed layer pattern by placing sample in acetone ultrasonic bath for 5 min.
27. Rinse sample in acetone / IPA / DI.
28. Blow-dry sample with N_2.
29. Dehydration bake sample at 110°C for 20 min.
30. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
31. Spin on AZ P4620 photoresist at 6000 rpm for 60 sec (RC-8, closed lid).
32. Soft bake sample in oven at 90°C for 15 min.
33. Edge bead exposure MJB3 CR1 2 min.
34. Develop photoresist in AZ400K:DI 1:4 1 min.
35. Electroplating pattern exposure MJB3 CR1 25 sec (careful alignment to seed layer pattern is required).
36. Develop photoresist in AZ400K:DI 1:4 40 sec.
37. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
38. Electroplate 2.5 μm Au.

39. Rinse sample in acetone / IPA / DI.
40. Blow-dry sample with N_2.
41. Dehydration bake sample at 110°C for 20 min.
42. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
43. Spin on AZ P4620 photoresist at 3000 rpm for 60 sec (RC-8, closed lid).
44. Soft bake sample in oven at 90°C for 15 min.
45. Edge bead exposure MJB3 CR1 3 min.
46. Develop photoresist in AZ400K:DI 1:4 1 min.
47. Air bridge post layer exposure MJB3 CR1 35 sec.
48. Develop photoresist in AZ400K:DI 1:4 50 sec.
49. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
50. Deposit 10 nm Ti / 10 nm Ni / 50 nm Au in e-beam evapourator.
51. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
52. Spin on AZ P4620 photoresist at 4000 rpm for 60 sec (RC-8, closed lid).
53. Soft bake sample in oven at 90°C for 15 min.
54. Edge bead exposure MJB3 CR1 3 min.
55. Develop photoresist in AZ400K:DI 1:4 1 min.
56. Air bridge pattern exposure MJB3 CR1 35 sec.
57. Develop photoresist in AZ400K:DI 1:4 50 sec.
58. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
59. Electroplate 7.5 μm Au.
60. Rinse sample in IPA / DI.
61. Blow-dry sample with N_2.
62. Etch upper Au seed layer in cyanide solution for 30 sec.
63. Rinse sample in DI and blow-dry with N_2.

64. Etch Ni seed layer in Ni-etchant solution for 30 sec.
65. Rinse sample in DI and blow-dry with N_2.
66. Etch Ti seed layer in Ti-etchant solution for 15 sec.
67. Rinse sample in DI and blow-dry with N_2.
68. Rinse sample in acetone / IPA / DI.
69. Blow-dry sample with N_2.
70. Barrel etch for 15 min with 100 W FWD power and 2 L/min O_2 flow rate.
71. Spin on HMDS at 3000 rpm for 60 sec (RC-8, open lid)
72. Spin on AZ P4620 photoresist at 3000 rpm for 60 sec (RC-8, closed lid).
73. Soft bake sample in oven at 90°C for 15 min.
74. Edge bead exposure MJB3 CR1 3 min.
75. Develop photoresist in AZ400K:DI 1:4 1 min.
76. Seed layer etch pattern exposure MJB3 CR1 35 sec.
77. Develop photoresist in AZ400K:DI 1:4 50 sec.
78. Barrel etch for 30 sec with 100 W FWD power and 2 L/min O_2 flow rate.
79. Etch lower Au seed layer in cyanide solution for 40 sec.
80. Rinse sample in DI and blow-dry with N_2.
81. Etch Ni seed layer in Ni-etchant solution for 30 sec.
82. Rinse sample in DI and blow-dry with N_2.
83. Etch Ti seed layer in Ti-etchant solution for 15 sec.
84. Rinse sample in DI and blow-dry with N_2.
85. Rinse sample in acetone / IPA / DI.
86. Blow-dry sample with N_2.
87. Dehydration bake sample at 110°C for 5 min.

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