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Soft Error Rate Estimation in Deep Sub-Micron CMOS

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Abstract

Soft errors resulting from the impact of charged particles are emerging as a major issue in the design of reliable circuits at deep sub-micron dimensions. In this paper, we model the sensitivity of individual circuit classes to Single Event Upsets using predictive technology models over a range of CMOS device sizes from 90nm down to 32nm. Modeling the relative position of particle strikes as injected current pulses of varying amplitude and fall time, we find that the critical charge for each technology is an almost linear function both of the fall time of the injected current and the supply voltage. This simple relationship will simplify the task of estimating circuit-level Soft Error Rate (SER) and support the development of an efficient SER modeling and optimization tool that might eventually be integrated into a high level language design flow.

1. Introduction

The scaling of CMOS technology will continue to offer great improvements in device density and performance. However, as we move further into Deep Sub-Micron (DSM) technology, soft errors are emerging as a new challenge in VLSI and System on Chip (SOC) design. Reduced feature sizes, higher logic density, shrinking node capacitances and lower operating voltages have already resulted in a significant increase in the sensitivity of integrated circuits to radiation induced Single Event Upset (SEU) errors [1] [2] making their use in high-reliability, high radiation environments (e.g., space) problematic. Even for terrestrial applications, SEU errors caused by atmospheric radiation are the fastest growing reliability problem for semiconductors and represent a major challenge to robust design.

When a particle passes through the material, it loses energy by either direct or indirect ionization. Electron–hole pairs are created along its path as it loses energy and SEU errors are induced by the excess charge collected by the drain diodes of the MOS transistors. The SEU rate of a device depends on not only the charge collection but also the device sensitivity to the excess charge. In turn, its ultimate effect on the system output depends on the circuit response to the upset and the design of the system.

As for any other design issue, there will be a tradeoff between SEU sensitivity and other constraints such as performance, power consumption, yield and so on for the designer of VLSI or SOC. Making such tradeoffs early in the design phase requires an efficient predictive methodology. An efficient Soft Error Rate (SER) modeling and optimization tool that is well integrated into the design flow will greatly assist designers to make strategic decisions.

Ideally, to simulate the system effectively we would like to know *a priori* the actual transistor response to the radiation regime. However, it is very expensive to determine this actual response, e.g., using a particle accelerator and even this will still be only partially predictive. We would therefore like to include realistic SER estimates within a higher level simulation environment. In this paper an abstract set of parameters are determined that describe the sensitivity of two basic circuit classes—SRAM and simple inverter—to Single Event Upsets for a range of device technologies from 90nm down to 32nm i.e., through to approximately 2013 on the International Technology Roadmap for Semiconductors (ITRS) [3].

Circuits on a typical chip (e.g., a microprocessor) tend to fall into three basic classes: SRAM cells, sequential elements such as flip-flops and latches, and combinational logic. Further, they may use a broad range of circuit styles, including dynamic and/or domino logic as well as a variety of latch styles. Each will exhibit a unique combination of performance, power, area, and noise margin characteristics. As a result, it will be ultimately necessary to develop models for each of these classes as well as for the interaction between them in a real system. This work represents the first steps towards an abstract SEU model that will eventually support the rapid estimation of soft errors for high-reliability DSM applications that may be described, for example, in a high-level language such as VHDL or C.

The remainder of this paper proceeds as follows. Section

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2 begins with a brief examination of the SEU environment then reviews prior work in this area. In Section 3, a basic SER model is presented and the results of various HSPICE simulations are discussed. Finally, in Section 4 we conclude the paper and discuss further work.

2. Single Event Errors in CMOS

In this section, we look at the mechanisms for the generation of charge upsets in CMOS devices and how these interact at different levels to produce SEU errors.

2.1. Modeling Single Event Upsets

In space-borne applications, the charged particle environment responsible for SEUs is dominated by energetic protons, with smaller contribution from heavier ions. The dominant sources of energetic particles [4, 5] in a space environment are:

1. Protons and Electrons trapped in the Van Allen belts and heavy ions trapped in the magnetosphere;
2. Cosmic ray particles originating outside the solar system, including ions of all elements (with atomic numbers in the range 1-92);
3. A range of energetic ions and protons produced by solar flares.

Ion impacts cause SEUs by direct ionization induced charge, where the charge induced by a heavy ion within a reversed biased or depleted region near the channel of a transistor is subsequently collected at the output node of the circuit. Charge collection occurs first by drift then by diffusion, typically extending the event time scale to hundreds of nanoseconds. By this time, all excess carriers will have been collected, recombined or diffused away from the junction area [6].

On the other hand, for protons and neutrons the effects are typically dominated by indirect ionization. For example, while proton energies are too low to directly generate excess charge, they may experience elastic/inelastic nuclear interactions and transfer part of their energy to more massive recoil atoms that may, in turn, generate excess charge sufficient to produce a SEU.

There are basically four parts to modeling the system Soft Error Rate (SER) induced by SEUs [1] [7]:

1. modeling the radiation particles, nuclear physics reactions, device geometry, and charge track generation;
2. modeling the charge transport in device fields and their collection;
3. modeling circuit response to the excess charge;
4. modeling the manifestation of errors in the system.

Charge track generation and charge collection effects have been modeled at the device level via nucleus reaction models (for protons and neutrons) [7], stopping power tables, also called Linear Energy Transfer (LET) [8], and using carrier transport models [9] [10]. The length of the track is obtained by using the tabulated stopping power (in silicon) and the initial number of electron–hole pairs produced along the track is determined assuming an energy loss of 3.6eV per pair. The most commonly used formalisms for device simulation are based on carrier transport models such as the Drift-diffusion model and the hydrodynamic equations (which are derived, ultimately, from the Boltzmann Transport Equation) [9]. Generally, numerical Monte Carlo (MC) techniques have been used to solve the Boltzmann equation. For example, the IBM Soft-Error Monte Carlo Modeling program SEMM [11] uses this method.

Device/material–level simulations can be used to obtain the shape, amplitude and duration of the transient current induced by the interaction of a particle (ion/proton) with a particular transistor within the integrated circuit. The specific shape and size of the current pulse depends on complex interactions between numerous parameters, including the device type (p- or n-type), feature size and applied bias as well as the magnitude and position of the injected energy. An iterative approach was employed in [12] using the 3D device simulator DESSIS, in which the junction bias was altered based on the time from collision till the effect died out.

Srinivasan [7] [13] used a physical device simulator to investigate the transient current induce by the alpha particle and found that the current waveforms can be fitted to a double exponential function of the form:

$$I(t) = \frac{Q_{total}}{\tau_f - \tau_r}(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}) \quad (1)$$

where τ_f (the fall time, also called the decay time) describes the collection time-constant of the junction, τ_r (the rise time) represents the ion track establishment time constant and Q_{total} is the total charge.

The shape of the transient current due to a neutron strike is characterized in [14] as:

$$I(t) = \frac{Q_{total}}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}e^{-\frac{t}{T}} \quad (2)$$

with T being the pulse time constant. However, the magnitude of charge collection is not sufficient on its own to determine a SEU, as the sensitivity of the device to this excess charge also needs to be taken account. This sensitivity is determined primarily by the node capacitance, operating voltage, and the strength of any feedback transistors, which together define the amount of critical charge (Q_{crit}) required to trigger a change of state.

As we now have the general transient current shapes of (1) and (2) for each type of junction, we can inject current pulses with different pulse time constants to analyze the response of the circuit node to the excess charge due to the particle strike. In the typical case where a current pulse with a form such as (1) is used to model the injected charge, the rise time is kept as a small constant (<10ps) while the fall time is varied [7]. For example, in [13] the rise time was fixed at 1ps while the fall time was varied. This is the general technique we have used in Section 3, below.

2.2. Circuit Level Issues

Adding to the difficulty of determining the effect of a particular particle strike is the fact that a transient voltage on a circuit node will not always cause the circuit to fail. For example, depending on whether the circuit is sensitive to the transient or not, a given transient event in a combinational logic node might or might not propagate to the output of the circuit or be captured by a memory circuit. A particular event may be masked by one of the following three phenomena [1, 2]:

1. *Logical* masking occurs when a particle strikes a portion of the logic where there is no sensitized path from that node to the output of the circuit. Logical masking is not considered in this paper.

2. *Electrical* masking occurs when the disturbance is attenuated by subsequent logic gates due to the electrical properties (e.g. limited bandwidth) of the gates such that it does not affect the result of the circuit. As the pulse propagates, its amplitude may reduce and the rise and fall times increase to a point where the pulse simply disappears.

3. *Latch-window* masking occurs when the disturbing pulse reaches a latch outside the time window during which the clock transition is active and the latch captures its input value.

As a result, all of the following conditions must be met in order for a particular strike on a logic node to result in a circuit error. A particle of sufficient charge must first strike a part of a gate sufficiently close to a sensitive region of a component transistor (e.g., a depletion region). The resulting disturbance in the logic level at the output of the gate must be of a great enough magnitude and duration to affect the logic conditions in subsequent stages of the circuit. Various models (e.g., [2], [15], [16] have been proposed to compute the three types of masking phenomena. In this paper we are dealing only with the issue of generating and propagating an event and do not further consider logic or time masking. In the following section, we examine circuit–level SER estimation.

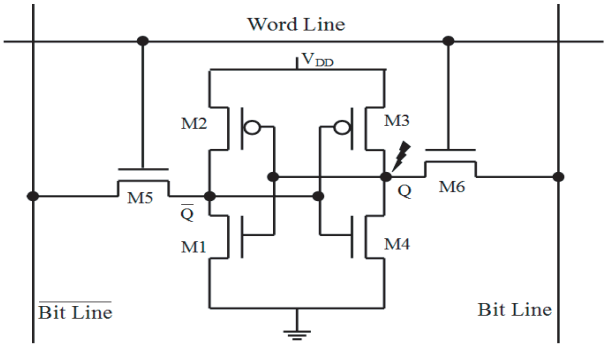

Figure 1. A Conventional 6-T SRAM

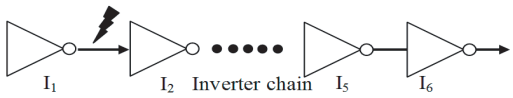

Figure 2. The Inverter Chain Organization

3. Circuit Level SER Estimation

As outlined above, at the circuit level the effect of a particle strike on various circuit classes can be modeled as a current pulse with the form of (1), in order to determine the *critical charge* which results in a circuit upset event. We have used HSPICE to simulate the circuit response to the injected current with a fixed rise time of 0.1ps and with varying fall times. We selected the 6-T SRAM (Fig. 1) to represent both memory and the storage stage of a sequential logic circuit. As we are considering neither logical nor time masking here, a simple inverter chain (Fig. 2) was used to represent the combinational logic class. In this latter case, the *critical charge* can be defined either as the minimum charge that needs to be injected into the inverter input such that the upset is captured by a downstream flip-flop [17], or as the minimum charge that will result an output glitch equal to the magnitude of the switching threshold. In this work, since no flip–flop is present in the test circuits, we use the second definition.

In the case of the SRAM we analyzed the node storing the logic value. By changing the peak magnitude of the waveform, the minimum magnitude that causes an incorrect value to be stored in memory element or FF can be obtained. The critical charge is then the smallest value of Q_{total} for which the circuit changes state. For the inverter chain, the output of the first inverter (I_1 in fig.2) was chosen as the injection point. The other inverter gates (I_2 to I_6 in fig.2) are used to monitor the propagation of the upset signal. All of these circuits use Predictive Technology Models (PTM) [18] over a range of feature sizes from 90nm down to 32nm.

3.1. SRAM and Inverter SER Estimates

It has been observed in many experimental studies that the probability of a particle strike causing a soft error depends exponentially on the critical charge. This is also referred to as the *cross section* of the node as it depends linearly on the sum of the diffusion areas that are sensitive to particle strikes. This approximate relationship has been confirmed using a semi-empirical model in [19] and is commonly used to model Soft Error Rate [20]. Thus, we can use the following model to compute the SER of an SRAM:

$$\begin{aligned} SER_{SRAM} &= flux * CS(V_{DD}, A, Q_{crit}) \\ &= flux * A * K * e^{-\frac{Q_{crit}}{Q_s}} \end{aligned} \quad (3)$$

where $flux$ is the particle flux intensity with energy greater than a given threshold ($particles * cm^{-2} * s^{-1}$), CS is the cross section, A is the drain area, Q_s is the charge collection efficiency which depends strongly on doping and V_{DD} and K is a constant for a particular technology. More generally, the SER of any circuit can be expressed as [17]:

$$SER = \frac{flux}{T_{cycle}} \sum_{n}^{nodes} A_n \sum_{i}^{Q} prob(Q_{i,n}) \Delta q \sum_{t_{inj}}^{T_{cycle}} upset_{j,i,n} \Delta t \quad (4)$$

where A_n is the drain area of node n, $prob(Q_i, n)$ is the probability that charge Q_i is collected for each particle in node n, $upset_{j,i,n} = 1$ if (and only if) the node n was upset by Q_i at time t_{inj}. T_{cycle} is the cycle time. When (4) is used to express the SER of SRAM circuits in terms of the critical charge, it can be expressed as:

$$SER = flux(\sum_{n}^{nodes} A_n \sum_{t_{n,j}}^{T_{cycle}} \frac{dt}{T_{cycle}} \int_{Q_{crit_n}}^{\infty} prob(Q_n) dq) \quad (5)$$

where $\sum_{t_{n,j}}^{T_{cycle}} \frac{dt}{T_{cycle}} = \delta$ is a constant equal to the duty cycle. Combining this with (3), the charge collection probability of the SRAM becomes:

$$prob(Q_n) = \frac{K}{\delta} \frac{1}{Q_s} e^{-\frac{q}{Q_s}} \quad (6)$$

For the inverter chain, we can substitute the charge probability density given by (6) into (4) for the given technology in the same manner as [17]. Because time masking of the downstream sequential logic was not considered, $upset_{j,i,n}$ in (4) is same for each time step Δt so that:

$$SER_{inv} = flux * K * \sum_{n}^{nodes} A_n * \sum_{i}^{Q} \frac{1}{Q_s} e^{-\frac{Q_{i,n}}{Q_s}} \Delta q * upset_{n,i} \quad (7)$$

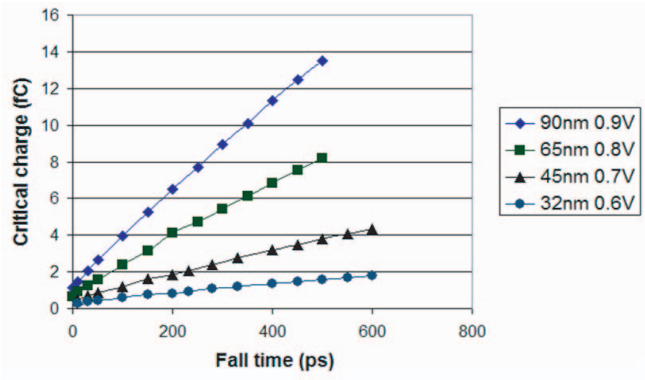

Figure 3. SRAM Q_{crit} vs. fall time (τ_f) at various feature sizes and V_{DD}

When (7) is used to express the SER of inverter circuits in terms of the critical charge, it can be expressed in the same form as (3).

In all of the above, the flux, collection efficiency (Q_s) and the constant K do not depend on the particular circuit, but on technology and supply voltage. From (3), the circuit level SER may be converted to an estimation of Q_{crit} for a given combination of technology, supply and radiation environment. In general, Q_{crit} primarily depends on the supply voltage and parasitic capacitance of the node. Its value is also affected by other parameters such as the radiation pulse characteristics and the operating frequency.

The charge collection induced by heavy ions or by secondary ions can be divided into two cases. The first is the classical one where an ion crosses the drain. The second case corresponds to a track passing close to the drain but not crossing the junction or the space-charge zone. Device simulations in [21] showed that compared with the first case, the duration of the current pulse in the second is larger while its magnitude is reduced. A very small fall time (in the range of 10ps) represents the case where the charge track passes directly through the drain. In this situation the critical charge is closely related to the charge stored on the capacitance of the struck node [21] and it can be approximated as $Q_{node} = V_{DD} * C_{node}$. We used a larger fall time to simulate the situation where the particle track does not intersect the drain. The larger the fall time, the further the track is assumed to be away from the junction.

3.2. Experimental Results

Figs. 3, 4 and 5 illustrate the results of HPSICE simulations carried out on the SRAM circuit of Fig. 1 using PTM CMOS models between 90nm and 32nm. The current was injected into the node labeled 'Q' when the state stored in the SRAM is logic 1 (i.e., M4 is OFF and M3 ON). The

Table 1. Node capacitance vs. feature size for low operating power (ITRS: LOP) technology

L_g (nm) (Drawn)	Nominal Voltage (V)	C_{node} (fF)	Q_{crit} (fC) ($\tau_f = 10ps$)
90	0.9	1.65	1.4820
65	0.8	1.13	0.9013
45	0.7	0.73	0.5094
32	0.6	0.48	0.2888

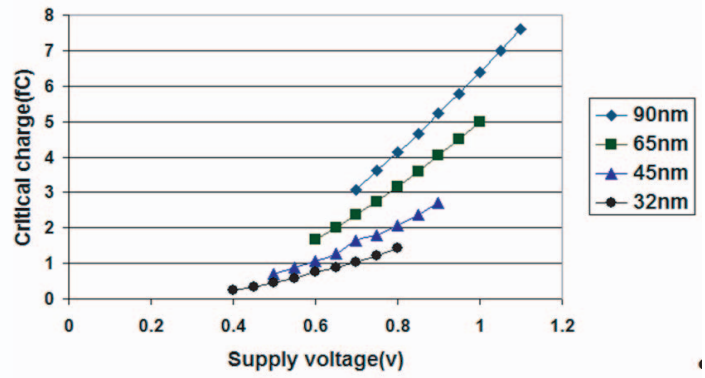

Figure 4. SRAM Q_{crit} vs. V_{DD} at various feature sizes ($\tau_f = 150ps$)

drawn gate lengths (L_g) and corresponding nominal supply voltages are taken from the CMOS roadmap for Low Operating Power (LOP) technology [3].

In Fig. 3 it can be seen that the critical charge for each technology (90nm down to 32nm) is an almost linear function of the fall time of the injected current. As feature size scales down, both C_{node} and V_{DD} are predicted to decrease [3]. Thus, using the approximation $Q_{node} = V_{DD} * C_{node}$ [21], the node charge will reduce approximately $O(L_g^{1.5})$ (see Table 1, derived from Fig. 3). We also observe (Fig. 4) that the critical charge decreases almost linearly with supply voltage.

Fig. 5 illustrates that critical charge is an almost linear function of fall–time constant τ_f over the range of V_{DD} shown. The critical charge becomes a function of supply and injection time constant of the form:

$$Q_{crit}(V_{dd}, T) = C_0 V_{DD} + k * (V_{DD} - V_{th}) * \tau_f \quad (8)$$

where C_0 is the node capacitance, V_{th} is the threshold voltage of the transistor for a given technology and $(V_{DD} - V_{th})$ accounts for the larger drain current at higher V_{DD}. The fitting parameters are given in Table 2.

During the simulation of the inverter chain, electrical masking is automatically taken into account. As identified

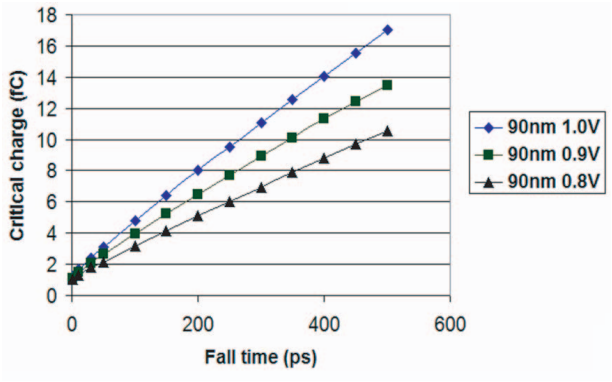

Figure 5. SRAM Q_{crit} vs. τ_f for various V_{DD}

Table 2. Fitting parameters for SRAM

L_G(nm)	C_o(fC)	V_{th}(V)	k
90	1.65	0.4937	0.06126

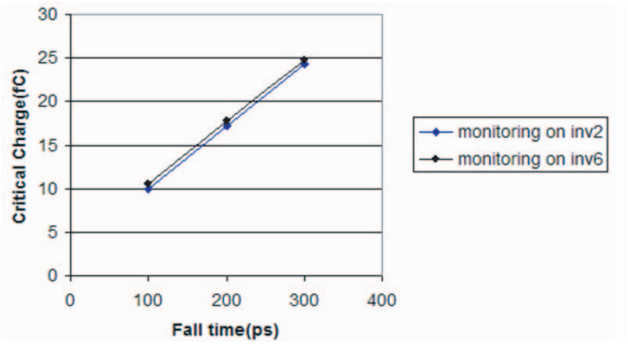

Figure 6. Effect of injected current on the inverter chain at different fall times

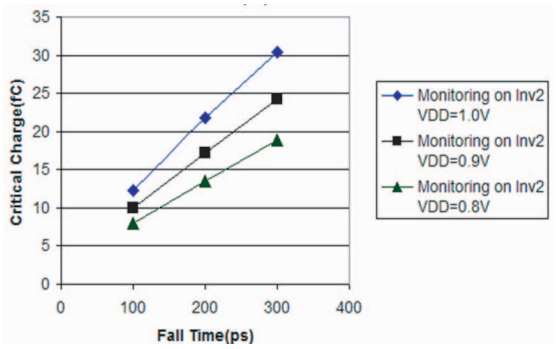

Figure 7. Inverter chain Q_{crit} vs. τ_f at 90nm for various V_{DD}

Table 3. SER derived from Q_{crit}

flux ($cm^{-2}s^{-1}$)	K (fC)	Q_s	Q_{crit} (fC)	SER (FIT)
0.00565	$2.2\text{x}10^{-5}$	13	2.062	$1.356\text{x}10^{-4}$

above, logical masking and time masking are not considered. Fig. 6 shows the dependency of critical charge on fall time as well as on the depth of the inverter chain for 90nm technology. The critical charge becomes larger when the inverter chain is deeper due to electrical masking. In Fig. 7, it can be seen that the critical charge depends on the supply voltage and the fall time, showing the same trend as the SRAM.

As noted in the introduction, the intended application for this work is the estimation of SEU errors within a high level simulation environment. The results shown in Figs. 4–7 imply that the critical charge (Q_{crit}) can be approximated to simple linear functions of both supply (V_{DD}) and the fall time τ_f of the injected current for a particular technology. It may also be observed that the general form of the curves for the various technologies simulated here remain the same—typically only the slope changes with technology. Thus, for a given fall time and node state, Q_{crit} for each node may be determined in a very straightforward manner. From (3), one can then derive the SER of the overall circuit. For example, in Table 3 we have estimated the (sea level) SER for a 90nm SRAM technology, using approximate values from [20] for Q_s and K and assuming a fall time of the transient current waveform of 30ps. SER is measured in Failures in Time (FIT), which is the number of failures that can be expected in one billion (10^9) hours of operation.

The critical charge may also be used as a figure of merit in the comparison of circuit design types and technologies in that it describes the relative vulnerability of a circuit to single events. Since the location of a strike within the device will be random, each ionization track will exhibit a different distance from the junction. If we assume that all tracks pass through the junction (i.e., by setting the fall time less than 10ps), the corresponding critical charge reflects a worst case SEU and the SER calculation is therefore an overestimate. Otherwise, it is underestimated. In this way, worse-case SER predictions can be made for a particular high-reliability architecture under investigation.

4. Conclusions

In this paper, the critical charge Q_{crit} of two basic circuit types—SRAM and a simple inverter chain—has been studied using predictive SPICE models and found to exhibit simple linear behavior from 90nm down to 32nm. It has been shown that Q_{crit} also strongly depends on the supply voltage V_{DD} and the fall time constant τ_f of the injected current. All of these functions exhibit monotonic and approximately linear trends with the device models used in this work.

The overall objective here has been to derive some simple relationships that will allow us to make realistic error predictions for typical circuits. The linear relationships discovered here should greatly simplify the task of estimating the probability distribution of the collected charge and therefore allow the SER for a given circuit to be computed quickly. Future work will expand on the results we have derived for these simple circuit types and will include the effects of logical and time masking on the estimates made at the circuit block level.

Ultimately, it is intended that these estimation techniques will be incorporated into a HLL simulation environment (e.g., one based on C or VHDL), to allow worse-case Soft Error Rates to be quickly and efficiently predicted for a range of potential high-reliability architectures.

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