Universal Error Corrections for Finite Semiconductor Resistivity in Cross-Kelvin Resistor Test Structures

Anthony S. Holland, Geoffrey K. Reeves, and Patrick W. Leech

Abstract—The Cross-Kelvin Resistor test structure is commonly used for the extraction of the specific contact resistance of ohmic contacts. Analysis using this structure are generally based on a two-dimensional model that assumes zero voltage drop in the semiconductor layer in the direction normal to the plane of the contact. This paper uses a three-dimensional (3-D) analysis to show the magnitude of the errors introduced by this assumption, and illustrates the conditions under which a 3-D analysis should be used. This paper presents for the first time 3-D universal error correction curves that account for the vertical voltage drop due to the finite depth of the semiconductor layer.

Index Terms—Cross-Kelvin Resistor (CKR), ohmic contact, specific contact resistance, test structures.

DEFINITIONS

- A Contact area (in square microns).
- *I* Current through the contact (in milliamperes).
- V_i True average voltage drop across interface, does not include parasitic effects (in millivolts).
- R_i True resistance of interface, $R_i = V_i/I$, does not include parasitic effects (in ohms).
- V_k CKR measured voltage drop, Tap1 to Tap2, includes parasitic effects, $V_k \ge V_i$, (in millivolts).
- R_k Contact resistance measured using the CKR which includes parasitic effects, $R_k \ge R_i$ (in ohms).
- R_s Sheet resistance, $R_s = \rho_b/t(\Omega/\Box)$.
- ρ_c True specific contact resistance, $R_i A (\Omega.cm^2)$.
- ρ'_c Specific contact resistance determined using measured voltage, $V_k = R_k I$, $\rho'_c = R_k A (\Omega.cm^2)$.
- *d* Dimension of square contact (in micrometers).
- *w* Width of both taps and current arms (in micrometers).
- δ Overlap around contact (in micrometers).
- *t* Semiconductor active layer thickness or junction depth (in micrometers).
- L_t Transfer length (in micrometers).
- ρ_b Resistivity of semiconductor layer (Ω .cm).
- V_s Vertical voltage drop in the semiconductor layer, below the contact interface (in millivolts).
- η Dimensionless parameter $\eta = V_s/V_i$.

Manuscript received November 18, 2003; revised February 27, 2004. The review of this paper was arranged by Editor T. Skotnicki.

A. S. Holland and G. K. Reeves are with the School of Electrical and Computer Engineering, Royal Melbourne Institute of Technology University, Melbourne, Vic. 3001, Australia (e-mail: anthony.holland@rmit.edu.au).

P. W. Leech is with CSIRO, Manufacturing and Infrastructure Technology, Melbourne, Vic. 3001, Australia.

Digital Object Identifier 10.1109/TED.2004.827385

I. INTRODUCTION

T HE CROSS-KELVIN Resistor (CKR) test structure presented by Proctor *et al.*[1] is commonly used to determine the specific contact resistance ρ_c of a metal-semiconductor ohmic contact [see Fig. 1(a), and (b)]. For the CKR, R_k is the resistance defined by the potential difference V_k measured between two voltage sensing taps, divided by the injected current *I*

$$R_k = \frac{V_k}{I}.$$
 (1)

Using a one-dimensional (1-D) analysis of the CKR, it was shown [1] that V_k is the average voltage across the contact interface V_i . Hence, for the 1-D model, R_k gives the interfacial resistance $R_i(R_i = V_i/I)$ from which ρ_c can be obtained

$$\rho_c = R_i A \tag{2}$$

where A is the contact area. Fig. 1(a) illustrates such a 1-D CKR test structure showing the metal and semiconductor taps through which the current I is passed, and the metal and semiconductor taps used for the measurement of V_k . The model shown in Fig. 1(a) is the same as the model of the ideal CKR presented in [1]. Analysis of the equivalent two-dimensional (2-D) model of the CKR in Fig. 1(b), shows that it behaves like the ideal CKR of Fig. 1(a). In Fig. 1(c), a more realistic CKR test structure is shown where the metal contacts the semiconductor through a via. Errors occur due to voltage drops in the semiconductor layer surrounding the contact, increasing the value of $V_k(V_k \ge V_i)$ [2]. In Fig. 1(d), errors occur due to both the surrounding semiconductor and the finite depth of the semiconductor layer. For all the CKR models shown in Fig. 1(a)–(d), the following definition holds:

$$\rho_c' = R_k A \left(R_k \ge R_i, \rho_c' \ge \rho_c \right). \tag{3}$$

For the ideal CKR $V_k = V_i$ and, thus, $\rho'_c = \rho_c$. Fig. 1(a) and (b) show models of ideal CKR test structures. For practical (nonideal) CKR test structures $V_k > V_i$ and, thus, $\rho'_c > \rho_c$. When the geometry of the semiconductor layer surrounding the contact via is taken into account with a 2-D model, the potential between the voltage taps is no longer the average voltage across the contact interface and thus $\rho_c > \rho_c$. Therefore, corrections are required. In the 2-D model, only corrections for the voltage drop in the semiconductor layer surrounding the via are performed. Error corrections to 2-D CKR test structures have been investigated by several groups [2]–[4]. These groups analyze the errors due to overlap of the semiconductor layer around the contact via and contact misalignment effects. By modeling and analyzing the various sources of error, it is possible to generate a series of correction curves whereby the extracted

0018-9383/04\$20.00 © 2004 IEEE



Fig. 1. Four-terminal CKR. (a) 1-D, (b) 2-D, no overlap of contact, (c) 2-D with overlap, and (d) 3-D with overlap. (Another case is the 3-D model with no overlap but having finite depth; see Fig. 3.)



Fig. 2. Comparison of interface V_i and semiconductor V_s voltage drops for defining $\eta.$

value ρ'_c is compared to the true value ρ_c used at the interface of the model. The majority of these analyses focus on 2-D effects. Loh *et al.* [3] briefly discuss a three-dimensional (3-D) model, but do not analyze the effects of such a model in detail and have not presented error correction curves. By modeling in 3-D, the influence of the voltage drop in the semiconductor layer (having finite depth *t*) in the vertical direction can be accounted for. Hence, its influence on the determination of ρ_c from CKR test structures may be found. In this paper, we use finite element (FE) techniques to model the CKR test structure in 3-D and, thus, analyze the influence of vertical voltage drop in the semiconductor layer. The analysis can be compared to the 2-D results in order to find the conditions under which 3-D effects may be significant. Universal error correction curves are presented using the same presentation method as used in other publications on the 2-D correction curves [3]–[5], e.g., the parameter sheet resistance R_s is used here even though the semiconductor layer has finite depth. Results for the 2-D case examined in this paper compares very well with the 2-D results previously published [3], [4]. Measurements from CKR structures with semiconductor layers with the same R_s , but with different thicknesses, are compared. Universality is maintained by making the thickness t as a ratio of the tap width w.

The 2-D scaling laws developed in [3] showed that the ratio R_k/R_s is the same for any given ratio of d, w, L_t , where L is any finite number

2-D:
$$\frac{R_k}{R_s}(d, w, L_t) = \frac{R_k}{R_s} \left(\frac{d}{L}, \frac{w}{L}, \frac{L_t}{L}\right).$$
(4)

From [6] the specific contact resistance is related to the transfer length by the equation

$$L_t^2 = \frac{\rho_c}{R_s}.$$
(5)

Reference [3] shows that for scaling in the 3-D case none of the parameters d, w, L_t , t are independent of each other, where t is the depth of the semiconductor layer; if one parameter is scaled than they are all scaled the same to maintain scaling equivalence

$$3-D: \quad \frac{R_k}{R_s}(d, w, L_t, t) = \frac{R_k}{R_s} \left(\frac{d}{L}, \frac{w}{L}, \frac{L_t}{L}, \frac{t}{L}\right). \quad (6)$$



Fig. 3. (a) Equipotential distribution within the semiconductor region of a CKR, where $\rho_c = 10^{-7} \Omega.\text{cm}^2$, $V_k = 1.39 \text{ mV}$ (for I = 1 mA), and (b) same as for (a) but with $\rho_c = 10^{-8} \Omega.\text{cm}^2$. $V_k = 0.2 \text{ mV}$ (for I = 1 mA).

II. THREE-DIMENSIONAL EFFECTS

When analyzing the transmission line model (TLM) test structure for ohmic contacts, Berger [6] recognized that the TLM did not account for the vertical voltage drop in the semiconductor layer of the test structure. He pointed out that in certain circumstances this could lead to errors in the derivation of ρ_c . The magnitude of these errors was calculated in terms of the parameter η :

$$\eta = \frac{\rho_c}{\rho_b t}.\tag{7}$$

The reason for using η can be seen from Fig. 2, which illustrates the voltage drop caused by current passing through a semiconductor, V_s and the metal-semiconductor interface V_i . The ratio of V_i : V_s is just $\rho_c/\rho_b t$ or η . When $\eta = 1$, the vertical voltage drop in the semiconductor layer is the same as the voltage drop across the interface (no current crowding effects of a planar contact are considered in Fig. 2). Thus, when $\eta \leq 1$ the vertical voltage drop in the semiconductor will influence the determination of ρ_c from a CKR test structure.

The continued downscaling of device dimensions has led to reductions in the junction depth (or active layer thickness) t, as well as reductions in ρ_b . In addition, the continued improvement in ohmic contact technology has also been accompanied by ever decreasing values of ρ_c . The use of new contact materials, contact structures and processing techniques has resulted in significantly lower values of ρ_c —values as low as $3.3 \times 10^{-9} \Omega$.cm² for TaSi₂ on n⁺-Si have been reported [7]. The International Technology Roadmap for Semiconductors [8] predicts that ρ_c values will be $4.0 \times 10^{-8} \Omega \cdot \text{cm}^2$ in 2010, $2.0 \times 10^{-8} \Omega \cdot \text{cm}^2$

 TABLE I

 Contact Parameters for Simulations in Fig. 3(a) and (b)

Fig.	$\rho'_{c}(x10^{-8} \Omega.cm^{2})$	$\rho'_{c}(x10^{-8} \Omega.cm^{2})$	% error	η
3(a)	10.0	10.67	6.7%	5.0
3(b)	1.0	1.58	58%	0.5



Fig. 4. Values of extracted ρ'_c versus ρ_c , for several values of $\rho_b \cdot t$ for a contact with d = w.



Fig. 5. Extracted ρ'_c as a function of ρ_c for several values of δ . Both 2-D (dashed line) and 3-D (solid line) simulations are shown.

in 2013, and $1.0 \times 10^{-8} \,\Omega \cdot \mathrm{cm}^2$ in 2016 for Si contacts. Thus, values of $\eta \leq 1$ may well arise, and in certain test structures, it may no longer be appropriate to neglect the vertical voltage drop in the semiconductor layer beneath the contact. For example, if $\rho_b = 10^{-3} \,\Omega \cdot \mathrm{cm}$ and $t = 0.2 \,\mu\mathrm{m}$, then, with $\rho_c = 1 \times 10^{-8} \,\Omega \cdot \mathrm{cm}^2$, $\eta = 0.5$ and a 3-D analysis should be implemented.

III. MODELING

To demonstrate the effect of finite depth, the ideal CKR test pattern [shown in Fig. 1(b)] is modified by giving it finite depth and modeled using FE techniques [see Fig. 3(a) and (b)]. In this structure, there is no contact overlap ($\delta = 0$) and therefore it is similar to the ideal CKR presented by Proctor *et al.*[1]. However, unlike the CKR presented in [1] the semiconductor layer is



Fig. 6. Universal error correction curves for CKR structures with different tap depth/width ratios. Shaded areas show $\eta \ge 1$. The 2-D error curves are shown for t/w = 0.1 and 0.5 for comparison with 3-D.

given a finite depth, and hence, vertical voltage drops will occur beneath the contact. Examples of potential distribution in the semiconductor layer are shown in Fig. 3(a) and (b). In this example, the contact is square $(d \times d)$ and since d = w there are no contact overlap errors ($w = 2.0 \,\mu m$). The semiconductor thickness is $t = 0.2 \,\mu\text{m}$, $\rho_b = 10^{-3} \,\Omega.\text{cm}$ and hence, $R_s = 50 \,\Omega/\Box$. The potential of the metal layer is taken as zero in the modeling. Table I gives the contact parameters and the specific contact resistance results for simulations shown in Fig. 3(a) and (b) show the equi-potentials in the semiconductor for 1 mA passing through the test pattern. In Fig. 3(a) and (b), the arrows on the potential scales point to the value of the potential V_k found on the end of the semiconductor tap, truncated in Fig. 3(a) and (b). V_k is the potential used for calculating ρ'_c . Thus, the potential difference used is $(V_k - 0)$. In a 2-D analysis, the semiconductor tap measures the potential at a point directly below the contact interface-this potential being the average value along the tap-edge of the contact. In the 3-D example of Fig. 3, the tap measures the potential at a contour below the contact interface-this potential is the average value of the contours on the face of the semiconductor where the tap abuts the side of the contact.

Using various values of ρ_c , ρ_b , and t, data similar to that in Table I has been obtained and is shown plotted in Fig. 4. ρ'_c is shown as a function of ρ_c for various values of the product $\rho_b t$. In this graph d = w and the points 1 and 2 mark the location of the two sets of data given in Table I. The dashed line indicates where $\rho_b t = 0$ and thus, $\rho_c = \rho'_c$. In order to compare the relative contributions of contact overlap and vertical voltage drop effects with the total correction factors for ρ_c , FE analysis was performed for several different values of contact overlap δ . Results for both 2-D and 3-D analysis were calculated (where the effect of vertical voltage drop is ignored and taken into account respectively). In these analyses, the tap width was fixed at $w = 2.0 \ \mu\text{m}$, and for the 3-D model $t = 0.2 \ \mu\text{m}$ and $\rho_b t = 2 \times 10^{-8} \ \Omega.\text{cm}^2$, while in the 2-D model $R_s = 50 \ \Omega/\Box$. The values of δ used were 0, 0.1, 0.2, and 0.5 μ m. The results are shown in Fig. 5 where ρ'_c is shown as a function of ρ_c for these values of δ . For a test pattern with the geometry and material parameters used in this example, the ρ_c value is easily

found from Fig. 5 once ρ_c' has been determined. In Fig. 5 the difference arising between the use of 2-D and 3-D simulations is presented. As an example, for $\delta = 0.2 \ \mu m$, an extracted ρ_c' of $4\times 10^{-8}~\Omega.{\rm cm}^2$ gives a true ρ_c of $1\times 10^{-8}~\Omega.{\rm cm}^2$ using the 2-D analysis but a ρ_c of $5.0\times 10^{-9}~\Omega.{\rm cm}^2$ using a 3-D analysis. Thus, an additional correction of a factor of two arises (in this example, $\eta = 0.25$). Plots like those in Fig. 5 for determining errors in CKR measurements are convenient to use for specific test structure geometries but modeling tools such as FE modeling software are required to obtain new data when CKR geometry is changed. Some groups have presented similar plots of ρ_c versus ρ'_c for 2-D CKR structures with overlap $\delta \neq 0$ [9]–[11] and each was for different geometry. To avoid having to generate such curves for different geometries universal error correction curves were generated for all possible cases using the scaling laws of equation (4). Loh et al. [3] established universal error correction curves using 2-D analysis and similar results have been presented by Scorzoni et al. [4] and Santander et al. [5]. The error (due to 2-D) effects for CKR test structures of any geometry can be determined using such curves. To extend the applicability of these curves we have modeled CKR test structures for semiconductor layers of different depths, i.e., 3-D universal error correction curves. Fig. 6(a)-(f) show curves that model the effects of the finite depth of the semiconductor layer. Curves are plotted for $L_t/\delta = 9, 9/2, 9/2^2, 9/2^3, \dots 9/2^8$ as done in previous presentations of 2-D universal error correction curves [3]–[5]. The curves for $L_t/\delta = 9/2^8 = 0.035$ has been omitted for clarity as it practically coincides with $L_t/\delta = 9/2^7 = 0.07$. The same method, as in [3]-[5], is used for presentation of the results. With respect to universal error correction curves, the only unknown parameter when undertaking CKR measurements is transfer length L_t , assuming that depth t is known. Values for t/w ratios of t/w = 0.1, 0.2, 0.3, 0.4, 0.5, and 1.0 are presented in Fig. 6(a)–(f). The 2-D curves are plotted on two of the [Fig. 6(a)–(e)] for comparison. For increasing t, the error compared with the 2-D case increases, and this corresponds with reducing η values. To demonstrate the relevance of the parameter η we have shaded the regions in Fig. 9 where $\eta > 1$. This clearly shows that for $\eta \leq 1$ the 2-D and 3-D models give different results and for $\eta \ge 1$ results are the same. For t/w = 0.1 most of the data is obtained for $\eta > 1$ and for t/w = 0.5 most of the data falls in the region of $\eta < 1$. For increasing t/w the increasing discrepancy between the 2-D and 3-D curves corresponds with a decreasing η .

IV. UNIVERSAL ERROR CORRECTION CURVES

To determine the true ρ_c from an experimental measurement requires the following procedure. The value of V_k is measured and hence R_k and R_k/R_s are determined. The universal error correction curves presented here assume that R_s is the same under the contact as outside the contact area. (Separate universal error correction curves are required for the case where the sheet resistance is different beneath the contact such as those generated for the 2-D case in [4].) Knowing R_k/R_s and d/δ then L_t/δ can be determined by choosing the value of L_t/δ which

TABLE II ρ_c Values Obtained for Different Values of η USING 2-D and3-D Error Correction Curves ($t = 0.24 \ \mu m, w = 1.2 \ \mu m, \delta = 0.2 \ \mu m, d/\delta = 4$)

	A: η=3.47	B: η=1.04	C: η=0.347	D: η=0.07
$R_s(\Omega / \Box)$	50	50	50	250
$R_k(\Omega)$	20.5	9.3	5.8	20.4
R_k/R_s	0.411	0.185	0.117	0.0816
L_{l}/δ	2.25	1.2	0.7	0,65
$L_t(\mu m)$	0.45	0.24	0.14	0.13
$ ho_{c} 2D (10^{-8} \Omega.cm^{2})$	10.6	3.4	2.0	4.2
$\rho_c 3D (10^{-8} \Omega.cm^2)$	10.0	3.0	1.0	1.0
% error, $ ho_c$ 2D	6	13	100	320



Fig. 7. Point A in Table II. Equipotential distribution within the semiconductor region of a CKR with semiconductor overlap of the contact and finite semiconductor depth. The input current I = 0.24 mA, t = 0.24 µm, w = 1.2 µm, $\delta = 0.2$ µm, $d/\delta = 4$, $R_s = 50$ Ω/ \Box and $\rho_c = 1 \times 10^{-7}$ Ω.cm².

is closest to the plotted point. From L_t/δ the value of ρ_c can be calculated by using (5).

The model shown in Fig. 7 is an example of a FE model of a 3-D CKR model, including the effects of semiconductor depth and contact overlap. The geometry and equipotentials of the CKR structure shown in Fig. 7(a) relate to point A in Fig. 6(b). The input current I = 0.24 mA, $t = 0.24 \mu$ m, $w = 1.2 \mu$ m, $\delta = 0.2 \,\mu\text{m}, d/\delta = 4, R_s = 50 \,\Omega/\Box \text{ and } \rho_c = 1 \times 10^{-7} \,\Omega.\text{cm}^2.$ Using this model the parameters ρ_c and R_s were varied to compare the effects of different values of η . The results are shown in Table II. This shows the significance of η for assessing the error in using a 2-D model. For $\eta > 1$ the error in using the 2-D correction curves is negligible whereas for $\eta < 1$ the error becomes significant and increases as η reduces. The data points in Table II are plotted in Fig. 8(a) and (b). In these figures, the x and y-axis are identical as are the data points A–D. These two figures clearly show the erroneous results that are obtained by using an inappropriate error correction curve. The curves in Fig. 8(b) are



Fig. 8. (a) and (b) Expanded sections of error correction curves for 2-D and 3-D [t/w = 0.2, Fig. 6(b)] showing data points A–D in Table II.

appropriate, being for t/w = 0.2, whereas the 2-D curves will give erroneous results for L_t and, hence, ρ_c .

V. CONCLUSION

The effect of the vertical voltage drop within the semiconductor layer of a CKR on the determination of ρ_c has been analyzed. Calculations were undertaken using a 3-D finite element model in order to determine values of the extracted specific contact resistance ρ_c' . These results have been compared to those ρ_c' values calculated using a 2-D model. The differences between the 2-D and 3-D models have been interpreted in terms of the parameter η where $\eta = \rho_c / \rho_b t$. When $\eta \leq 1$, the errors due to the vertical voltage drop within the semiconductor become significant as shown by the difference in results from the 2-D and 3-D models. Thus, in order to derive ρ_c , the correction to the extracted ρ'_c should be undertaken using data from a 3-D model. Corrections using 3-D model data will become increasingly necessary as the reductions being obtained in ρ_c are larger than those occurring in $\rho_b t$. 3-D universal error correction curves have been presented which account for the finite depth of semiconductor layers. These curves have been compared to their equivalent 2-D curves to demonstrate the error in incorrectly using 2-D curves.

REFERENCES

- S. J. Proctor, L. W. Linholm, and J. A. Mazer, "Direct measurement of interfacial contact resistance, end contact resistance and interfacial contact layer uniformity," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1535–1542, Nov. 1983.
- [2] M. Finetti, A. Scorzoni, and G. Soncini, "Lateral current crowding effects on contact resistance measurements in four terminal resistor test patterns," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 524–526, Dec. 1984.
- [3] W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson, and K. C. Saraswat, "Modeling and measurement of contact resistances," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 512–523, Mar. 1987.
- [4] A. Scorzoni and M. Finetti, "The effect of sheet resistance modifications underneath the contact on the extraction of the contact resistivity; application to the Cross Kelvin Resistor," *IEEE Trans. Electron Devices*, vol. 35, pp. 386–388, Mar. 1988.
- [5] J. Santander, M. Lozano, and C. Cané, "Extraction of contact resistivity on Kelvin L-resistor structures," *IEEE Trans. Electron Devices*, vol. 41, pp. 1073–1074, June 1994.
- [6] H. H. Berger, "Models for contacts to planar devices," Solid State Electron., vol. 15, pp. 145–158, 1972.
- [7] T. Ohmi, "Ultra-clean processing for ULSI," J. Microelectron., vol. 26, no. 6, pp. 595–619, 1995.

- [8] Semiconductor Industry Association: International Technology Roadmap for Semiconductors, 2001.
- [9] R. L. Gillenwater, M. J. Hafich, and G. Y. Robinson, "Extraction of the minimium specific contact resistivity using Kelvin resistors," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 674–676, Dec. 1986.
- [10] W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson, and K. C. Saraswat, "Analysis and scaling of Kelvin resistors for extraction of specific contact resistivity," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 105–108, Mar. 1985.
- [11] W. J. C. Alexander and A. J. Walton, "Sources of error in extracting the specific contact resistance from Kelvin device measurements," in *Proc. IEEE Microelectronic Test Structures*, vol. 1, 1988, pp. 17–22.



Anthony S. Holland received the B.A.I. degree in electronic engineering from Trinity College, Dublin, Ireland, in 1987, and the M.Eng and Ph.D. degrees from Royal Melbourne Institute of Technology (RMIT) University, Melbourne, Australia, in 1995 and 1999, respectively.

From 1999 to 2002, he was a Research Associate at RMIT investigating diamond films used for surface acoustic wave devices. Since 2002, he has worked as a Research Fellow at RMIT on photonics devices.

Geoffrey K. Reeves received the Ph.D. degree from Monash University, Melbourne, Australia, in 1970.

He worked at the Research Laboratories of Telecom, Australia, where he undertook research on compound materials and optoelectronic devices until 1988. He then took up a research position at the Royal Melbourne Institute of Technology (RMIT) University, where he continued research on semiconductor materials, test structure design, and modeling. Other research interests include the development of fabrication technologies for

microwave integrated circuits.



Patrick W. Leech received the Master of Applied Science and Ph.D. degrees from the University of Melbourne, Parkville, Australia, in 1977 and 1982, respectively.

He was a Research Scientist at the Materials Research Laboratories from 1983 to 1984 and at the Telstra Research Laboratories from 1984 to 1996. Since 1996, he has been a Principal Research Scientist in Manufacturing and Infrastructure Technology (MIT) at the Commonwealth Scientific and Industrial Research Organisation (CSIRO), Melbourne, Australia.

Current research areas include electron beam lithography, fabrication of MEMs devices, and reactive ion etching.