Abstract

MULTILEVEL inverters play a major role in the modern day medium and high power energy conversion processes. The classic two level voltage source inverter generates PWM pole voltage output having two levels with strong fundamental component and harmonics centered around the switching frequency and its multiples. With higher switching frequency, its components can be easily filtered and results in better Total harmonic distortion (THD) output voltage and current. But with higher switching frequency, switching loss of power devices increases and electromagnetic interferences also increases. Also in two level inverter, pole voltage switches between zero and DC bus voltage $V_{dc}$. This switching results in high $dv/dt$ and causes EMI and increased stress on the motor winding insulation. The attractive features of multilevel inverters compared to a two level inverter are reduced switching frequency, reduced switching loss, improved voltage and current THD, reduced $dv/dt$, etc. Because of these reasons, multilevel inverters find application in electric motor drives, transmission and distribution of power, transportation, traction, distributed generation, renewable energy systems like photovoltaic, hydel power, energy management, power quality, electric vehicle applications, etc. AC motor driven applications are consuming the significant part of the generated electrical energy (more than 60%) around the world. The multilevel inverters are ideal for such applications, since the switching frequency of the devices can be kept low with lower output voltage $dv/dt$. Also by using multilevel inverters, the common mode voltage (CMV) switching can be made zero and associated motor bearing failure can be mitigated.

For multilevel inverter topologies, as the number of level increases, the power circuit becomes more complex by the increase in the number of DC power supplies, capacitors, switching devices and associated control circuitry. The main focus of development in multilevel inverter for medium and high power applications is to obtain an optimized
number of voltage levels with reduced number of switching devices, capacitors and DC power sources. In this thesis, a new hybrid seven level inverter topology with a single DC supply is proposed with reduced switch count. The inverter is realized by cascading two three level flying capacitor inverters with a half bridge module. Compared to the conventional seven level inverter topologies, the proposed inverter topology uses lesser number of semiconductor devices, capacitors and DC power supplies for its operation. For this topology, capacitor voltage balancing is possible for entire modulation range irrespective of the load power factor. Also capacitor voltage can be controlled over a switching cycle and this result in lowering the capacitor sizing for the proposed topology. A simple hysteresis band based capacitor voltage balancing scheme is implemented for the inverter topology.

For a voltage source inverter fed induction motor drive system, the inverter pole voltage is the sum of motor phase voltage and common mode voltage. In induction motors, there exists a parasitic capacitance between stator winding and stator iron, and between stator winding and rotor iron. Common mode voltage with significant magnitude and high frequency switching causes leakage current through these parasitic capacitances and motor bearings. This leakage current can cause flash over of bearing lubricant and corrosion of ball bearings, resulting in an early mechanical failure of the drive system. In this thesis, analysis of extending the linear modulation range of a general n-level inverter by allowing reduced magnitude of common mode voltage (CMV) switching (only $V_{dc/18}$) is presented. A new hybrid seven level inverter topology, with a single DC supply and with reduced common mode voltage (CMV) switching is presented in this thesis for the first time. Inverter is operated with zero CMV for modulation index less than 86% and is operated with a CMV magnitude of $V_{dc/18}$ to extend the linear modulation range up to 96%. Experimental results are presented for zero CMV operation and for reduced common voltage operation to extend the linear modulation range. A capacitor voltage balancing algorithm is designed utilizing the pole voltage redundancies of the inverter, which works for every sampling instant to correct the capacitor voltage irrespective of load power factor and modulation index. The capacitor voltage balancing algorithm is tested for different modulation indices and for various transient conditions, to validate the proposed topology.

In recent years, model predictive control (MPC) using the system model has proved to be a good choice for the control of power converter and motor drive applications. MPC
predicts system behaviour using a system model and current system state. For cascaded multilevel inverter topologies with a single DC supply, closed loop capacitor voltage control is necessary for proper operation. This thesis presents zero and reduced common mode voltage (CMV) operation of a hybrid cascaded multilevel inverter with predictive capacitor voltage control. For the presented inverter topology, there are redundant switching states for each inverter voltage levels. By using these switching state redundancies, for every sampling instant, a cost function is evaluated based on the predicted capacitor voltages for each phase. The switching state which minimizes cost function is treated as the best and is switched for that sampling instant. The inverter operates with zero CMV for a modulation index up to 86%. For modulation indices from 86% to 96% the inverter can operate with reduced CMV magnitude ($V_{dc}/18$) and reduced CMV switching frequency using the new space-vector PWM (SVPWM) presented herein. As a result, the linear modulation range is increased to 96% as compared to 86% for zero CMV operation. Simulation and experimental results are presented for the inverter topology for various steady state and transient operating conditions by running an induction motor drive with open loop V/f control scheme.

The operation of a two level inverter in the over-modulation region (maximum peak phase fundamental output of inverter is greater than $0.577V_{dc}$) results in lower order harmonics in the inverter output voltage. This lower order harmonics (mainly 5th, 7th, 11th, and 13th) causes electromagnetic torque ripple in motor drive applications. Also these harmonics causes extra losses and adversely affects the efficiency of the drive system. Also inverter control becomes non linear and special control algorithms are required for inverter operation in the over modulation region. In conventional schemes, maximum fundamental output voltage possible is $0.637V_{dc}$. In that case inverter is operated in a square wave mode, also called six-step mode. This operation results in high $dv/dt$ for the inverter output voltage. With multilevel inverters also, the inverter operation with peak phase fundamental output voltage above $0.577V_{dc}$ results in lower order harmonics in the inverter output voltage and results in electromagnetic torque pulsation. In this thesis, a new space vector PWM (SVPWM) method to extend the linear modulation range of a cascaded five level inverter topology with a single DC supply is presented. Using this method, the inverter can be controlled linearly and the peak phase fundamental output voltage of the inverter can be increased from $0.577V_{dc}$ to $0.637V_{dc}$ without increasing the DC bus voltage and without exceeding the induction motor voltage rating. This new
technique makes use of cascaded inverter pole voltage redundancy and property of the space vector structure for its operation. Using this, the induction motor drive can be operated till the full speed range (0 Hz to 50 Hz) with the elimination of lower order harmonics in the phase voltage and phase current. The five level topology presented in this thesis is realised by cascading a two level inverter and two full bridge modules with floating capacitors. The inverter topology and its operation for extending the modulation range is analysed extensively. Simulation and experimental results for both steady state and dynamic operating conditions are presented.

Zero common mode voltage (CMV) operation of multilevel inverters results in reduced DC bus utilization and reduced linear modulation range. In this thesis two reduced CMV SVPWM schemes are presented to extend the linear modulation range by allowing reduced CMV switching. But using these SVPWM schemes the peak phase fundamental output voltage possible is only 0.55\(V_{dc}\) in the linear region. In this thesis, a method to extend the linear modulation range of a CMV eliminated hybrid cascaded multilevel inverter with a single DC supply is presented. Using this method peak fundamental voltage can be increased from 0 to 0.637\(V_{dc}\) with zero CMV switching inside the linear modulation range. Also inverter can be controlled linearly for the entire modulation range. Also, various PWM switching sequences are analysed in this thesis and the PWM sequence which gives minimum current ripple is used for the zero CMV operation of the inverter. The inverter topology with single DC supply is realised by cascading a two level inverter with two floating capacitor fed full bridge modules. Simulation and experimental results for steady state and dynamic operating conditions are presented to validate the proposed method.

A three phase, 400 V, 3.7 kW, 50 Hz, two-pole induction motor drive with the open-loop V/f control scheme is implemented in the hardware for testing proposed inverter topology and proposed SVPWM algorithms experimentally. The semiconductor switches that were used to realize the power circuit for the experiment were 75 A, 1200 V IGBT half-bridge modules (SKM-75GB-12T4). Opto-isolated gate drivers with desaturation protection (M57962L) were used to drive the IGBTs. For the speed control and PWM timing computation, TMS320F28335 DSP is used as the main controller and Xilinx SPARTAN-3 XC3S200 FPGA as the PWM signal generator with dead time of 2.5\(\mu s\). Level shifted carrier-based PWM algorithm is implemented for the normal inverter operation and zero CMV operation. From the PWM algorithm, information about
the pole voltage levels to be switched can be obtained for each phase. In the sampling period, for capacitor voltage balancing of each phase, the DSP selects a switching state using the capacitor voltage information, current direction and pole voltage data for each phase. This switching state information along with the PWM timing data is sent to an FPGA module. The FPGA module generates the gating signals with a dead time of \(2.5\mu s\) for the gate driver module for all the three phases by processing the switching state information and PWM signals for the given sampling period. For fundamental frequencies above 10Hz, synchronous PWM technique was used for testing the inverter topology. For modulation frequencies 10Hz and below, a constant switching frequency of 900 Hz was used. Various steady state and transient operation results are provided to validate the proposed inverter topology and the zero and reduced CMV operation schemes and extending the linear modulation scheme presented in this thesis.

With the advantages like reduced switch count, single DC supply requirement, zero and reduced CMV operation, extension of linear modulation range, linear control of induction motor over the entire modulation range with zero CMV, lesser \(dv/dt\) stresses on devices and motor phase windings, lower switching frequency, inherent capacitor balancing, the proposed inverter power circuit topologies, and the SVPWM methods can be considered as good choice for medium voltage, high power motor drive applications.