SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices

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Place, Route, and Gate Utilization are Stored in the FPGA Configuration

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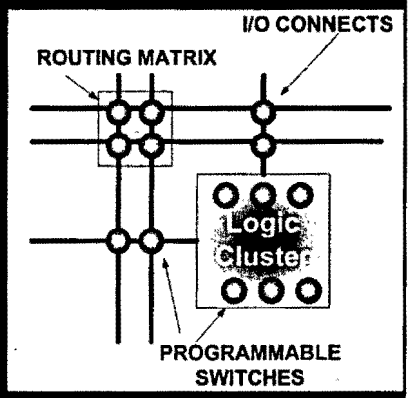
Configuration Defines:

- *Functionality (logic cluster)*
- *Connectivity (routes)*
- *Placement*



Configuration Switch Types:

- *Antifuse: One time Programmable (OTP)*
- *SRAM: Reprogrammable (RP)*
- *Flash: Reprogrammable (RP)*

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Configuration Switch Implementation and Single Event Upset (SEU) Susceptibility

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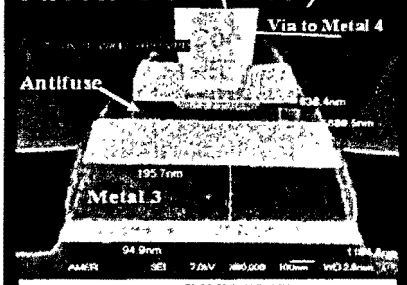
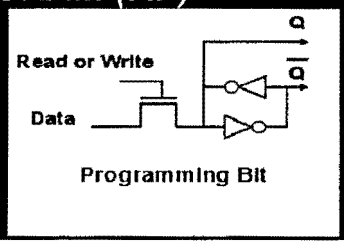
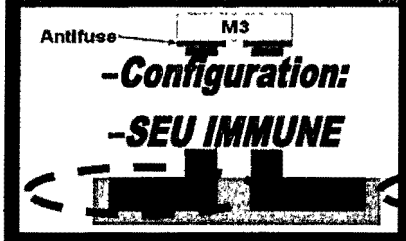
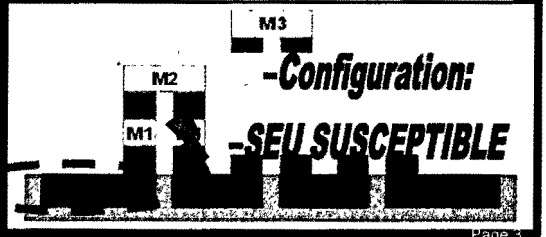
ANTIFUSE (OTP)



SRAM (RP)







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Actel RTAXs -Logic Building Block SEU and SET Susceptibility

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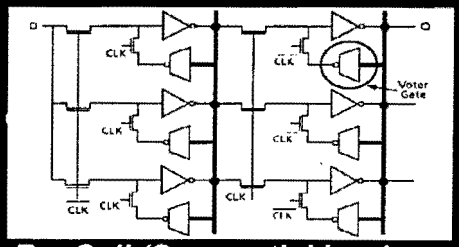
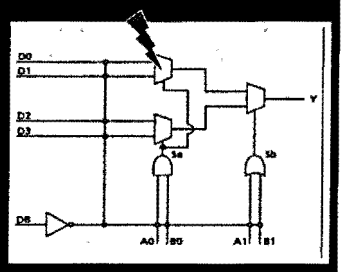
- RTAXs User Logic Blocks and Resources
  - Flip-Flops (DFFs) (R-Cells)
  - Combinatorial Logic (C-Cells)
  - Global Routes (clocks and resets)



R – Cell (Sequential Logic Block)

SEU: Not Frequency dependent



C – Cell (Combinatorial Logic Block)

SET: Frequency dependent

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Actel RTAXs Susceptibility and Mitigation

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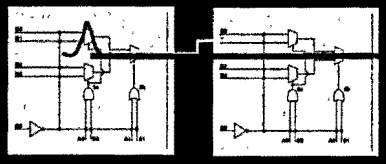
Design Specific SEE upset rate

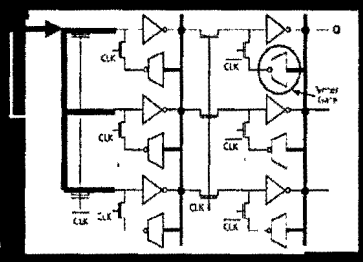
Configuration SEE upset rate

Functional logic SEE upset rate

Single Event Functional Interrupt



Combinatorial logic cells



DFF

Triple DFFs lower P_{DFFSEU} but can not mitigate $P(fs)_{SET \rightarrow SEU}$ (upset rate in Frequency Dependent)

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FPGA Design Under Test Development

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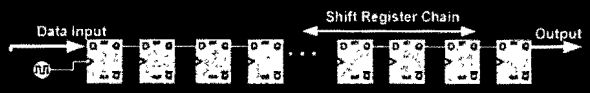
- Repeatability … increase statistics



Traditional FPGA Testing

- Stress and expose building blocks
- Divide and conquer…Determine separate error cross sections that correspond to specific:
  - Frequencies
  - Designs and Building blocks (when applicable)
- Fault Isolation…Create designs that will facilitate error differentiation

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The Predominance of P(fs) $_{SET \rightarrow SEU}$ Requires High Frequency Testing and Combinatorial Logic

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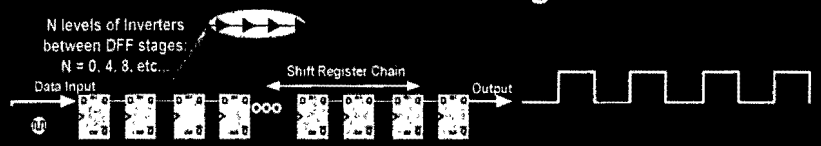
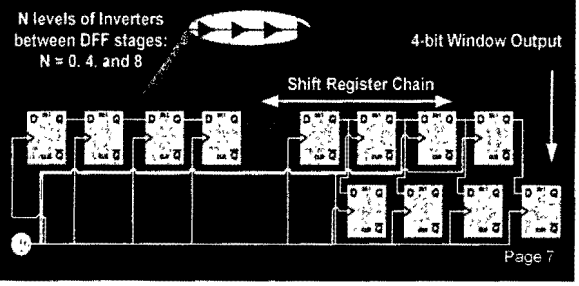


Traditional + Inverters: P(fs) SET→SEU Tests

- Architecture Enhancement: Windowed Shift Register (WSR) for High Speed Signal Integrity

WSR



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The WSR Advantage: Static Output

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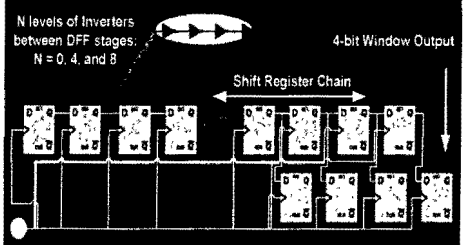
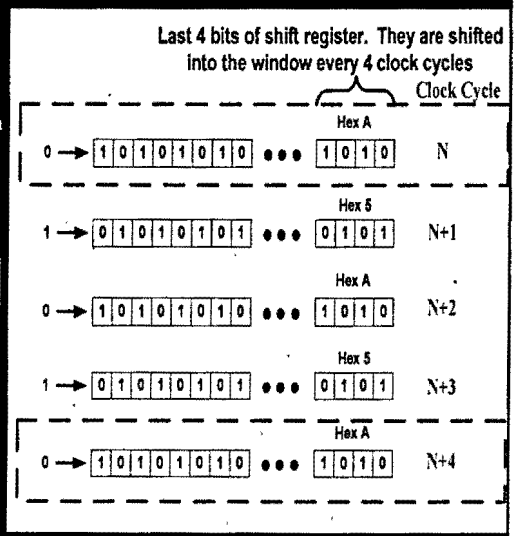


REAG WSR



Static output enhances signal integrity

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Highlights/Accomplishments: REAG WSR SEE Results

- Error rates are significantly dependent on Threshold LET(LET_{th})
- Choice of design impacted LET_{th} … number of C-Cells between DFFs
- Choice of data pattern and frequency of operation impacted LET_{th} (>2 orders of magnitude)

	Low Frequency	Increased Frequency
LET_{th} MeV*cm²/mg	LET_{th} >37	8< LET_{th} <30
Bit Error Rate (errors/bit-day)	$dE_{bit}/dt \approx 1x10^{-10}$	$1x10^{-10} < dE_{bit}/dt < 5x10^{-8}$

If Frequency or data pattern were not varied during testing, then an incorrect LET_{th} and dE_{bit}/dt would had been calculated

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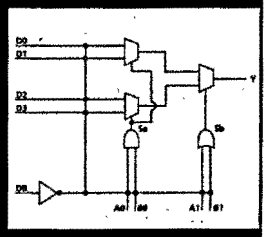
Considerations when Developing a Complex Design under Test Architecture

- Are inverters efficient test structures?
- Want to investigate something more realistic than a shift register
  - It should have the characteristics of a complex design with:
    - fan-out and fan-in > 1
    - contains a mixture of sequential and combinatorial logic.
  - The circuit should be replicated to increase statistics.
  - Its state space can be traversed within relatively short time periods such that all states are equally likely to be subject to particle strikes during radiation testing.



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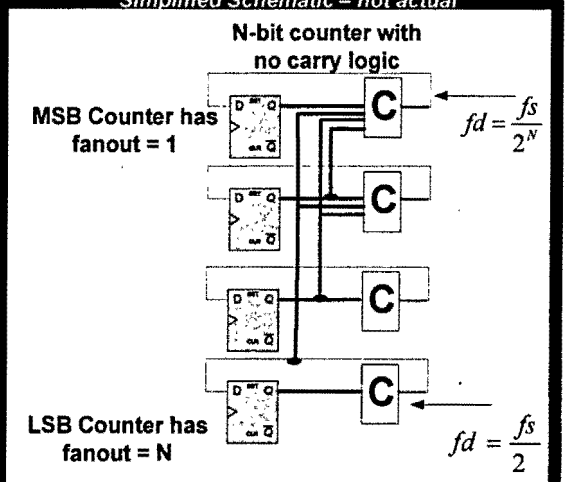
Counters Meet Requirements

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies (f_d)
- State space Traversal = $2^N/f_s$

Simplified Schematic – not actual



fd: data pattern frequency
fs = system frequency

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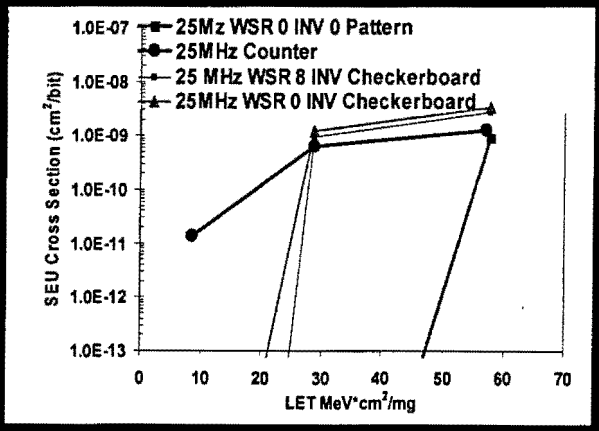
Highlights/Accomplishments:
Texas A&M Heavy Ion Results
Counters versus WSRs



*25MHz Counter LETth is lower than 25MHz WSR but similar to 100MHz CB WSRs (also has a LET_{th} = 8.6MeV*cm²/mg)*

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Summary

- Because configuration, global routes, and configuration is hardened in the RTAXs device, $P_{SET \rightarrow SEU}$ becomes the most significant source of upsets in radiation environments
- The ratio of combinatorial logic delay to clock frequency within a data path will drive $P_{SET \rightarrow SEU}$.
- Hence, Choice of Architecture and frequency can significantly affect SEE cross section and bit error rate RTAXs characterization
- Counter Arrays were driven near their top speed while containing several combinatorial logic levels. Subsequently they produced the lowest LETth→Highest bit error rate versus the shift register designs

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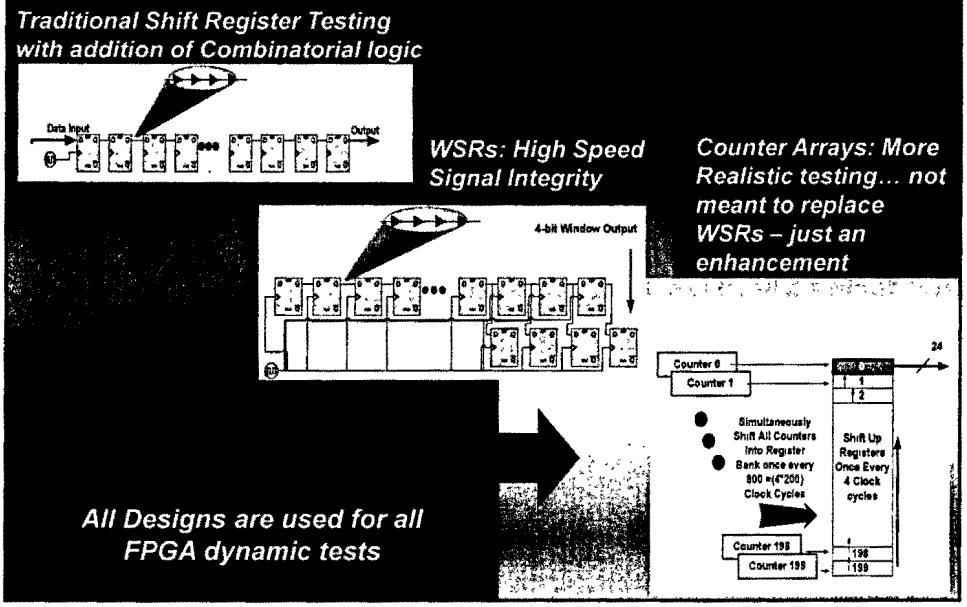
Summary: REAG Evolution of FPGA Designs Under Test



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