Effects of Bias, Electrical and Thermal Stress on DDR2 Total Ionizing Dose Response

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Abstract— We investigate whether bias conditions and electrical and thermal stresses can affect the Total Ionizing Dose response of DDR2 SDRAMs.

Index Terms—radiation effects, reliability estimation, quality assurance

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I. INTRODUCTION

The second generation of double-data-rate (DDR2) synchronous dynamic random access memories (SDRAMs) is of interest to spacecraft designers for a variety of reasons. Their high density makes them ideal for data storage and processing applications. The technology used suggests parts will have good Total Ionizing Dose (TID performance)—an expectation supported by trends observed in previously tested parts.[1] Even single-event performance can be a good match for applications that can tolerate occasional single-event functional interrupts (SEFIs), as between these events per-bit single-event upset (SEU) rates tend to be on the order of 10^{-12} upsets per bit per day. Unfortunately, concerns about the reliability of these purely commercial parts give rise to trepidation about their use in the space environment, especially for missions lasting a decade or more. Although accelerated life testing—using temperature and overvoltage to accelerate degradation mechanisms that compromise parts reliability and performance as it ages—and TID testing can address some of these concerns, to date there has been little testing of potential synergistic interactions between TID damage and damage due to, for example hot-carrier effects (HCE)[1], time-dependent dielectric breakdown (TDDB), etc.

In this work, we examine whether such effects significantly affect TID response of state-of-the-art DDR2 SDRAMs. We will characterize both parametric and functional degradation due to TID alone, accelerated life testing alone and then examine the TID response of the parts that have undergone such accelerated life testing. Because most operations in DDR2s are invisible to the user, we will use a commercial tester for dual in-line memory modules (DIMMs) to maximize visibility into how the parts are operating. Because DIMMs combine several individual smaller memories to achieve 1 Gbit or higher densities, even a single DIMM can provide sufficient statistics to constrain the failure distribution for the technology.

We begin with a brief discussion of the degradation mechanisms that affect DDR2s in normal operation—especially HCE and TDDB—and then discuss how such damage could interact synergistically with damage due to TID. We then describe the Triad TCII 1333ST SDRAM tester, the DIMMs used as test parts and outline the test method. Next we present results to date and list the results we expect to have for the full presentation. We end with a discussion of the implications of the results for TID hardness assurance for DDR2 SDRAMs, their TID sensitivities and evaluate the use of commercial SDRAM testers for evaluation of SDRAM memory performance.

II. DEGRADATION MECHANISMS FOR SUBMICRON CMOS

The Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) that are the building blocks of Complementary Metal-Oxide-Semiconductor (CMOS) technologies are susceptible to several degradation mechanisms that can compromise device reliability and/or performance. Although a full discussion of these effects is beyond the scope of this work, we mention a few mechanisms that impact device dielectrics, since these are also impacted by TID degradation and may interact synergistically with TID mechanisms. Hot carrier effects (HCE) occur when MOSFETs are operated in saturation, and charge carriers attain sufficient energies to generate electron-hole pairs by impact ionization. These carriers can become trapped in bulk dielectics and at dielectric-semiconductor interfaces, shifting threshold voltages and affecting performance of the devices. In time-dependent dielectric breakdown (TDDB), the oxide fails after prolonged use in moderate fields due to the effects of Fowler-Nordheim tunneling and defects in the dielectric. Negative bias temperature instability can also affect device threshold, especially in p-FETs. The effects of these mechanisms on oxide reliability, charge trapping, etc. raise the question of whether the resulting damage can also affect device response to ionizing radiation. In particular, could aging and electrical stress reduce tolerance to TID degradation, resulting in overconfidence of TID hardness assurance based on tests of unstressed parts?

Manufacturer Reliability testing accelerates damage by the above stresses using overvoltage and elevated temperatures. The elevated temperature acceleration is given by the Arrhenius factor:

$$F_A=\exp[(E_A/kT_{app}-E_A/kT_{test})] \quad (1)$$

where T_{test} is the elevated test temperature, T_{app} is the application temperature, k is Boltzmann's constant and E_A is a constant for the technology called the activation energy. Voltage acceleration is

$$F_V=\exp(\beta V_{test}-\beta V_{app}), \quad (2)$$

where V_{test} is the elevated test voltage, V_{app} the application voltage and β a constant for the technology. Unfortunately, the mechanisms given above have different values for E_A and β. Hot carrier effects increase dramatically with voltage and actually decrease as temperature rises, while other mechanisms are accelerated (albeit

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more slowly) with overvoltage and with temperature. As such, an inappropriate choice of T_{test} and V_{test} could result in a very different mix of degradation than would be found after a typical application of several years.[3] While this is not an important factor for accelerated life testing, it could result in incorrect conclusions regarding putative synergies between TID and electrical stresses. One approach to avoiding unrealistic damage is to reproduce as closely as possible the conditions used by manufacturers in accelerated life testing. However, such testing protocols are often considered proprietary and may not be available. In addition estimates for E_a and β vary from 0.3 to 0.9 eV, and from 5 to 10 V^{-1}, respectively. In the full paper, we will discuss more fully how to select testing conditions when collaboration with the vendor is not an option.

III. Test Samples and Test Equipment

Test samples were commercial 1 Gbit DIMMs, part number M379T2863FB3-CF7, obtained from commercial distributors. Each module contains eight 128 Mbit Samsung DDR2 SDRAMs.[2] In this summary, we report only on the performance of modules using Samsung die. However in the full paper, we will also report data for similar 1 Gbit modules from Micron Technology, Inc., module number MT47H128M8HQ. If time permits, we will also report on the performance of DDR3 DIMMs (MT4JTF12864AZ from Micron and MV-3V2G4 from Samsung). Because of the provenance of the test parts, there is no information available for the die used in each module.

Test hardware consisted of the Triad TCII 1333ST SDRAM tester (see figure 1). This tester accommodates up to 4 DIMMs ranging up to 2 Gbits and can operate the parts in a variety of test modes at speeds up to 1.33 GHz (internal). The tester solves one of the most challenging issues for testing SDRAMS—gaining visibility into how the device is functioning. It measures supply currents for a dozen operating modes, ranging from Active-Power-Down to Burst-Auto-Refresh. The tester also performs a range of functional (AC) tests, including AutoRefresh, Marching Ones, Data Retention and Hammer Read (repeated reads and writes to a single address).

The Triad also comes with an optional heating module that allows parts to be tested at temperatures up to 80 °C. We used this heater to provide thermal stress to parts we intended to test for synergistic effects with TID. We also worked with Triad to allow overvoltage conditions for DIMMs in the tester, thereby allowing the TCII 1333ST to serve as both a tester and an environmental chamber.

IV. Test Method

Once the DIMMs were received, they were serialized and verified functional. Bias boards were prepared for the modules that were to be tested with static bias. Dynamic testing was not possible due to the radiation softness of available controllers and the timing demands of DDR2s for stable operation. Since a single module includes 8 DDR2 die, this was deemed to provide adequate statistics to assess part-to-part variability.

One DIMM was placed in the bias fixture, while a second was placed with all pins grounded. Both modules were placed inside a Pb/Al box and placed near the gamma source. The dose rate was measured to be ~66 rad(Si)/s using ionization probes, and then the DIMMs were irradiated up to their first dose (25 krad(Si)) and recharacterized for functional and parametric performance as during prerad. Step irradiation and parametric/functional testing was continued up to the first functional failure to give an indication of the technology's radiation capability.

To gauge the effects of electrical and thermal stress, we first looked at the performance of a DIMM at nominal voltage and room temperature. We then incrementally raised the supply voltage until we were no longer able to reliably control the part, and backed off. This gave us an external stress voltage of 2.7 V, 0.9 V over the nominal supply voltage. (Note that DDR2s have internal voltage regulation that decreases the internally applied voltage. We estimate that the internal voltage is between 0.4 and 0.6 V.)

Parts were operated with a Marching Ones pattern at this voltage and with the heater running (80°C) 20-22 hours per day, 5 days a week (to allow the tester to rest and cool, per vendor guidance). Parametric and functional measurements were made approximately every 24 hours. (Note: In the full paper, we will present data on the TID performance of these stressed parts).

V. Results and Discussion

For the unstressed modules, bias made a big difference in the parametric degradation of the parts. The biased sample exhibited a monotonic increase in supply current for all operating conditions. Supply currents for the 5 most

sensitive operating modes are shown in figure 2. The first parametric failure occurs at 125 krad(Si) for burst Autorefresh (IDD5B), followed by several other parametric failures up to 350 krad(Si). However, none of these parametric failures affected the functionality of the parts.

In contrast, the unbiased module exhibited almost no parametric degradation (see figure 3). However, this module exhibited the first functional failure at 900 krad(Si), when some bits were in error for the Hammer Read test. At 1Mrad(Si) the biased module also failed the Hammer Read test. The unbiased parts failed Marching Ones as well as the Hammer Read test. At 1.1 Mrad(Si), both modules failed both the Hammer Read and Marching Ones tests. There was no appreciable parametric change associated with any of the functional failures.

The fact that the unbiased module failed before the biased module, despite showing no parametric degradation suggests that the culprit in the failure was likely due to degradation of individual memory cells. This is further supported by the fact that the first test the part failed was the hammer test, which looks at the functionality of individual addresses in the memory. Moreover, the fact that the biased parts failed within 100 krad(Si) of the unbiased parts, with very similar signatures (first Hammer Read then Marching Ones), despite the very different parametric degradation shown for the two biased conditions suggests a common failure mode.

In addition to the TID results above, we also report preliminary results for the parts undergoing electrical and thermal stress. Figure 4 shows increases in supply current for one of the modules under stress vs stress time. Supply current increases are very similar for the vast majority of operating modes. IDD6 (self-refresh current) shows little systematic trend. For the other module currently under stress, there is little systematic trend. This indicates that the stresses being applied are at about the right level, but that there seems to be some part-to-part variation in stress tolerance. [Note: In the full presentation, we will report TID results for these stressed parts, as well as stressed and unstressed TID performance for DIMMs using die from Micron Technology, Inc., module number MT47H128M8HQ, and if testing is completed on DDR3 modules MT4JTF12864AZ (Micron), and MV-3V2G4 (Samsung).

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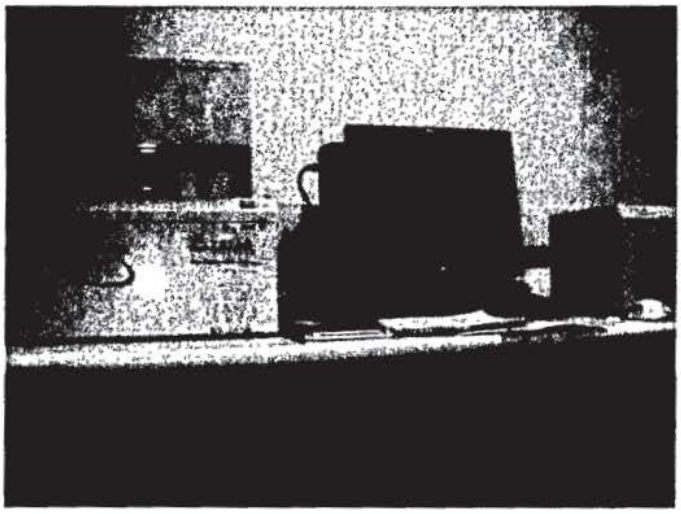

Figure 1 The Triad Triad TCII 1333ST SDRAM tester accommodates up to four 2 Gbit DIMMs, performing parametric and functional testing. On top of the main unit is a heater that allows operation and testing of parts at temperatures up to 80 degrees. The tester interfaces to a Personal Computer (right).

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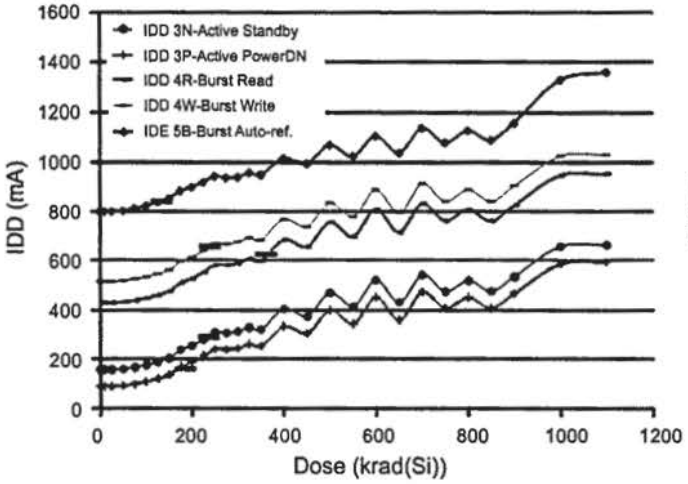

Figure 2 Supply current for various operating modes of Samsung DDR2 DIMMs irradiated with static bias.

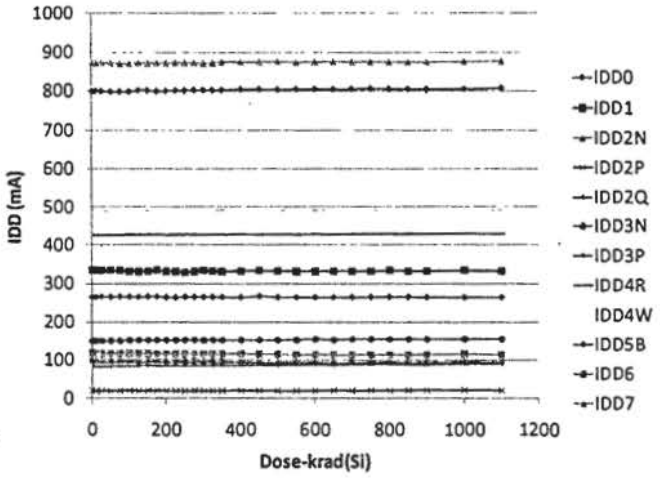

Figure 3 Supply currents Samsung DDR2 DIMMs irradiated unbiased show little change even up to functional failure at 900 krad(Si).

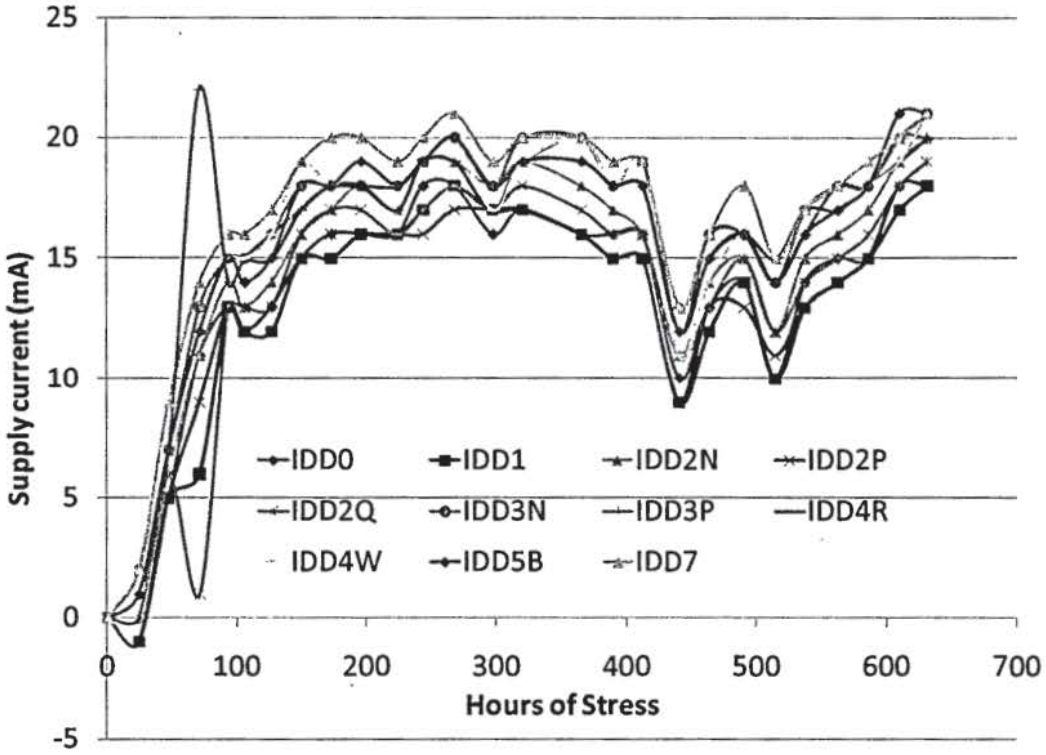

Figure 4 Increases in supply current for most operating modes of Samsung DDR2 DIMMs subjected to thermal and overvoltage stress follow similar trends. The other module being stressed exhibits little change.

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