New Particle-Induced Single Event Latchup Mechanism Observed in a Cryogenic CMOS Readout Integrated Circuit

Cheryl J. Marshall[1], Paul W. Marshall[2], Raymond L. Ladbury[1], Augustyn Waczynski[3], Roger D. Foltz[1], Rajan Arora[4], Nathaniel A. Dodds[5], John D. Cressler[4], Jonathan A. Pellish[1], Dakai Chen[6], Duncan M. Kahle[1], Gregory S. Delo[3], Emily Kan[1], Nicholas Boehm[3], Robert A. Reed[5], and Kenneth A. LaBel[1]

[1]NASA GSFC,
[2]NASA GSFC Consultant
[3]Global Science and Technology, NASA-GSFC
[4]Georgia Institute of Technology
[5]Vanderbilt University
[6]MEI Technologies, Inc.

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For inquiries: cheryl.j.marshall@nasa.gov

Outline

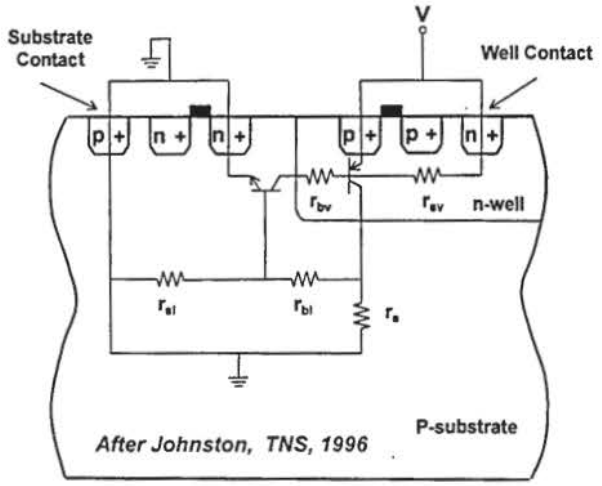
- Introduction & review of classical CMOS LU susceptibility
- Observation of cryogenic electrical latchup (LU)
  - Mechanism for free carrier generation
- Concerns about the possibility of cryogenic ion-induced LU
- Heavy Ion Experiment on ReadOut Integrated Circuit (ROIC)
- Current status for June TAMU Experiment
  - ROIC
  - IBM and TI latchup test structures
- Conclusions

To be presented by Cheryl J. Marshall at the Institute of Electrical and Electronics Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC), Denver, CO, July 19-23, 2010 and published in the IEEE Transactions on Nuclear Science proceedings, Dec. 2010 and on http://radhome.gsfc.nasa.gov and http://nepp.nasa.gov/.

Review of Inherent CMOS LU Susceptibility

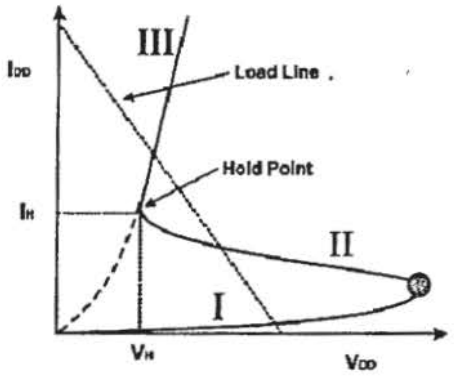
Cross coupled parasitic bipolar transistors inherent to CMOS Technology

- Current produced by ion strike can forward bias the base emitter junction and begin the LU sequence
- Key device parameters for all temperature regimes:
  - Well & substrate resistivities
  - Well & substrate contact proximity
  - Minimum n+ - p+ , or cathode-anode spacing



IV Characteristic for Latchup

- Here LU is triggered by increasing the voltage
- Triggering current and voltage indicated with large red circle.
- Region III latched state and holding voltage and current required to sustain latch.
- Bias supply & associated circuits must be able to provide enough current to sustain LU.
- Temperature dependence of each characteristic current and voltage is different.



Sexton, TNS, 2003

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Classical Picture of LU as the Temperature Drops

- LU susceptibility decreases because:
  - Well & substrate resistances decrease due to increase in mobility & carrier freeze-out.
  - The V_{BE} required to support a given collect current increases.
  - Parasitic bipolar gain product is still decreasing exponentially with T due primarily to the bandgap narrowing in the emitter.
    - Often has little quantitative effect on LU characteristics as it may remain high enough for LU to occur until quite low temperatures.
- Below ~100 K, it is assumed LU is no longer possible, and the simplified metric $\beta_{npn}\beta_{pnp} < 1$ holds for the two parasitic common-emitter current gains.

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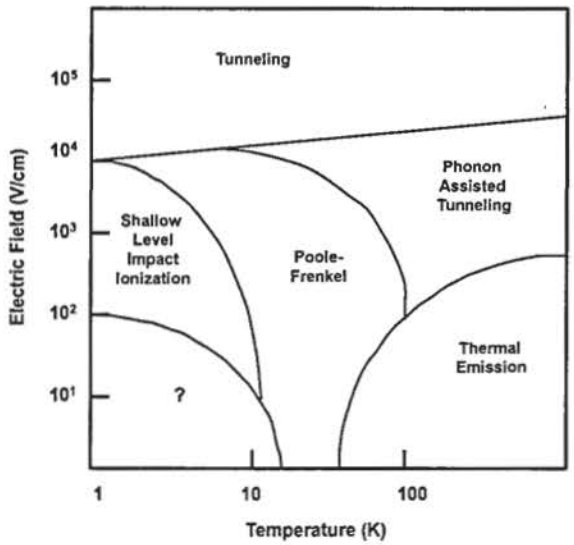
Dominant Impurity Ionization Mechanisms vs Temperature



After Simoen et al., "Charge transport in a Si resistor at liquid –He temperatures," JAP 68 (8), 1990.

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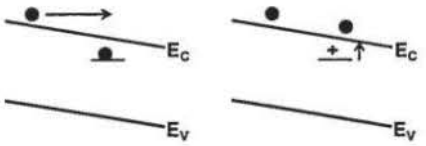
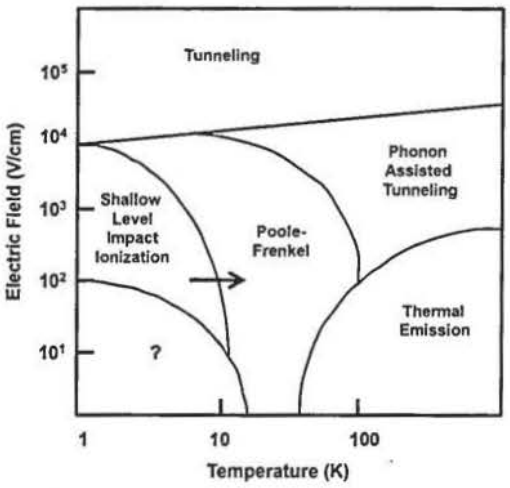


- Shallow-level impact ionization (SLII) is field assisted ionization of frozen-out shallow dopants.
- Research shows SLII can dominate at lower fields out to higher temperatures than shown.
- SLII can lead to significant charge multiplication when moderate electric field threshold is reached and excess carriers are present (e.g. via an ion strike) to be accelerated by the electric field.



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Concerns about the possibility of cryogenic LU

- Flight project with 0.5 µm unhardened ROIC at 40 K
  - Bulk CMOS process with very lightly doped p substrate
  - Design rules pressed hard in logic portion.
- Review of particle-induced LU literature reveals no experimental data and only one modeling paper
  - Iwata, et al. concluded that best LU performance would occur at ~120 K, and that by ~77 K is was on par or worse than at R.T.
    - 2 D model with temperature dependent models only good to ~77K
    - Still, they claimed "extreme LU susceptibility" below 77K
- This led to a search for a mechanism to explain the Iwata claim
    - Temperature dependence of electrical LU is well studied & varies significantly depending on the key device parameters

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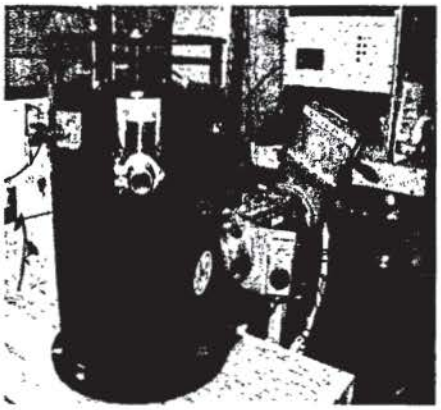
Heavy Ion Test Set-up for ROIC Test

- 1.5 µm aramica films used for both the beam exit port and dewar entrance
- 1 mil Al foils used for thermal, light and noise control
- Beam alignment was verified using internal markers in the dewar as well as full frame data showing particle induced transients in the ROIC unit cells



He cryostat in front of TAMU beam line

TAMU ROIC LU Experiment Instrumentation

- ROIC fully operational (4 channels @ 500 kHz) with continuous frame data acquired for diagnostics and SEFI record
  - Reset of 1 configuration word per frame for full reset every 2 frames
- Key voltages & associated currents monitored every 26 µs:
  - V_{PD} (all digital circuits), V_{POS} (all analog circuits except output MUX and buffer circuits), V_{POSOUT} (output MUX and buffers), V_{DETCOM} (detector) and detector reference signal.
    - Automatic alert when any single reading deviated from a preset threshold (current increase of 25% or voltage drop of 25%).
- Multichannel real time GHz scope captured LU transients with pretrigger
  - Event triggered when any supply voltage dropped by 25%
- ROIC health monitored during entire test

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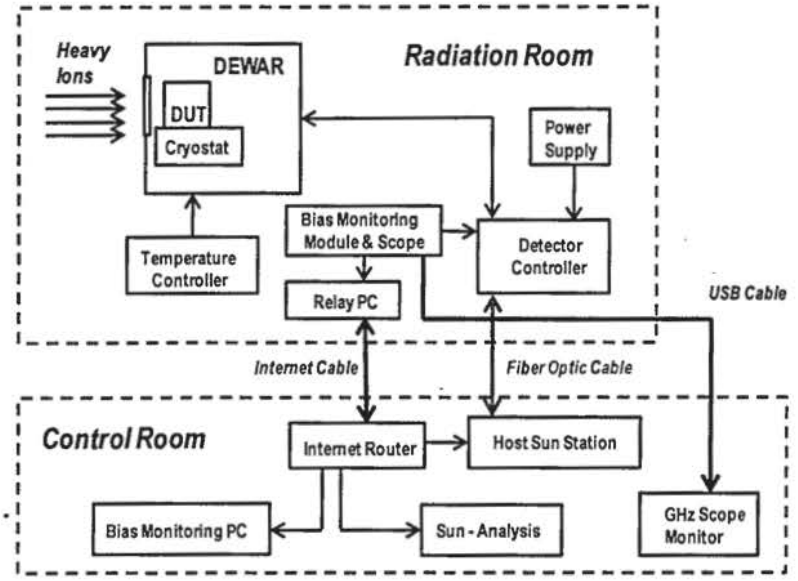
Experimental Set-up For Heavy Ion LU Test



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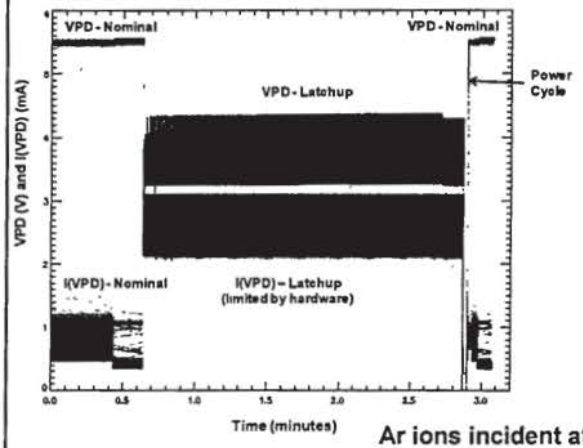
Ion-induced LU Signature at 20 K in 0.5 µm ROIC



We have verified via frame and noise data that ROIC meets all performance specifications at 20 K.

Ar ions incident at 60^0 with LET_{eff} = 12.4 MeVcm^2/mg and a projected range of 189 µm.

I_{VPD} was hardware limited at 4 mA. Serial resets each frame had no effect, and power cycling was required to clear.

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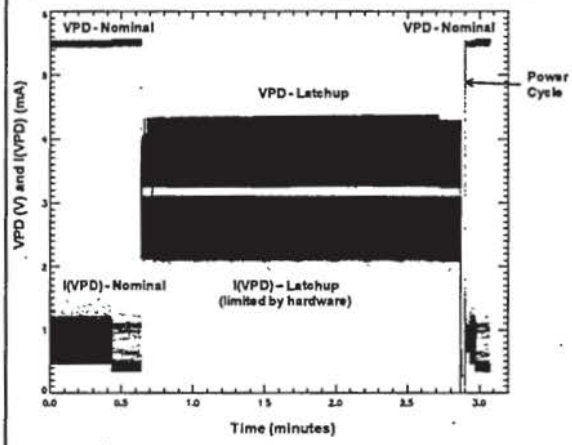

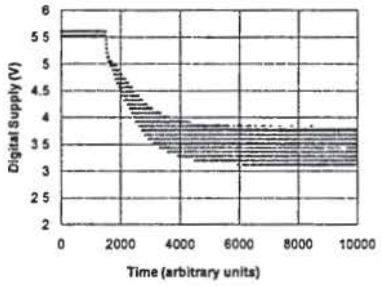

Flight hardware includes 3.3 µF bypass capacitors for noise control, so limited by RC time constant

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Temperature Dependent LU Results

- Latch up observed at 20 K and 32 K
  - All latchup events in digital logic circuitry.
  - Observed LU at 19.5 K for all LET_{eff} tested (110, 47, 24 and 12.4 MeVcm²/mg) and R_p (49, 106, 43, and 189 µm, respectively).
    - Cross sections from $1x10^{-6}$ cm² to $4x10^{-5}$ cm²
  - Observed single LU event at 32 K for cross section ~ 2×10^{-7} cm²
- No latchup observed at 40, 48, and 80 K
  - Extensive testing at application temperature of 40 K with variety of ion energy deposition profiles using 15 MeV/amu Au and 25 MeV/amu Xe beams.
  - No LU at 48 K or 80 K for limiting cross sections of ~2×10^{-7} cm² for LET_{eff} = 110 MeVcm²/mg and R_p=49 µm with 25 MeV/amu Xe.
- Room temperature LU observed for LET_{eff} as low as 20 MeVcm²/mg (R_p=64 µm) with a cross section of ~$2x10^{-6}$ cm² (No LU at LET = 15!)
  - No angular dependence observed for normal incidence and 60^0 tilts in both XY orientations.

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Upcoming TAMU Test

- 0.5 μm ROIC Measurements
  - Similar test set but extend temperature range from 20 – 300 K with more intermediate temperatures
  - Make holding voltage measurements
  - Complete LET characterization of LU at 20 K
- Characterize SCR test structures at 130 nm and 45 nm
  - Test structures represent a range of anode-cathode spacings, hardening techniques and geometries.
  - Electrical LU characterization underway using JEDEC57 and IBM standards for positive injection at anode and negative injection at the cathode
    - Results follow expected trends
  - Plan to perform LU measurements at TAMU over 4 – 300 K
    - Will monitor displacement damage effects via measurements of bipolar gains in vertical and lateral parasitic transistors.

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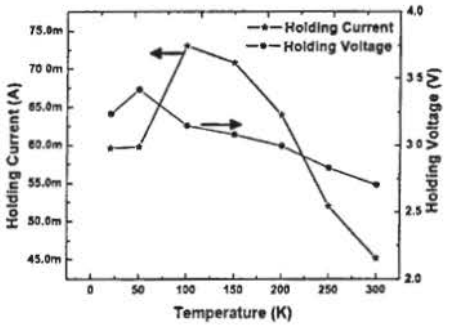
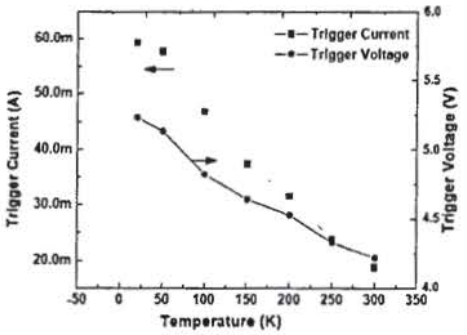
Temperature Dependence of Key LU Parameters



130 nm IBM SCR
Test Structure
with LU via anode injection

Note changes in behavior at ~50 K where shallow level impact ionization becomes important.



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Conclusions

- Cryogenic LU is indeed possible and represents a new qualification concern
  - Shallow-level impact ionization is a very plausible mechanism to provide a source of carriers below roughly 50 K
  - NASA requires cryogenic operation for ROICs, ASICs and other CMOS devices for IR sensor applications as well as extreme environments on the Moon and Mars
- Very little data exists for ion-induced LU below room temperature
  - We see a lower LU threshold at 20 K compared to room temperature.
  - Most of the existing data are for DoD ROICs that would be expected to have incorporated RHBD and/or RHBP hardening for LU
- Data from 50 – 300 K are also needed for NASA has missions at 75, 80, and 210 K, etc.
  - LU susceptibility expected to be lowered but is very dependent on device properties.

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