View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by HSN Open Archive

NTNU – Trondheim
Norwegian University of
Science and Technology

Compensation of Threshold Voltage for Process and Temperature Variations in 28nm UTBB FDSOI

Erlend Strandvik

Master of Science in Electronics
Submission date: June 2015
Supervisor: Trond Ytterdal, IET
Co-supervisor: Carsten Wulff, IET

Norwegian University of Science and Technology
Department of Electronics and Telecommunications

Problem description

The main goal of this thesis is to design a circuit that compensate threshold voltages for process and temperature variations through the use of adaptive body biasing in a commercially available $28nm$ FDSOI transistor technology. Its performance should be tested by designing and optimising a 65.5MHz inverter based ring oscillator to be used with this compensation circuit, in order to see its improvement in frequency stability across processing corners and temperature variations compared to an uncompensated ring oscillator.

Subsidiary goals are listed below.

- Identify transistor behaviour suffering from process and temperature variations.
- Design and analysis of compensation circuits, for both NMOS and PMOS, that provides body bias to compensate the threshold voltage for process and temperature variations.
- Identify the limitations of body biasing and apply techniques to push these limits.
- Design and analysis of sub circuits needed to realise the compensation circuit.
- Design and analysis of thirteen stage inverted based *Ring Oscillator*, operating at a frequency of $65.5MHz$.
- Optimise ring oscillator frequency stability by utilising the compensation circuit, and identify improvements made compared to an uncompensated ring oscillator.

Abstract

As technology scales down in order to meet demands of more computing power per area, a variety of challenges emerge. Devices with channel lengths of a few nano meters require atomic precision when they are manufactured. Small irregularities in the equipment and manufacturing environment can cause large process variations from die–to–die, but also within–die variations. Along with the increasing density of transistors per die which has led to severe performance issues due to temperature variations, these effects may seriously impact operation and cause large deviations in frequency and power across a the chip.

This thesis will present the analysis and design of a circuit with the goal of compensating the threshold voltage, by means of body biasing, in order to mitigate process and temperature variations. The compensation circuit is designed to provide adaptive body biasing for a large number of equally matched devices within the chip, which may be useful in digital systems with many repetitive instances. Its functionality and effect will be tested by designing it to be used with a 13–stage inverter based ring oscillator operating at $65.5MHz$, and observing the improvement in frequency variation across processing corners and a temperature range from $-40°C$ to $80°C$. All circuits were designed using a commercially available $28nm$ FDSOI transistor technology because of its excellent susceptibility to body biasing, and its promise as a competitive technology to continue Moore‘s law.

Results obtained by post–layout simulations on the ring oscillator show that frequency variations across processing corners and temperature has been reduced from 18.69% down to 0.632% by utilising adaptive body biasing provided by the compensation circuit. Ring oscillator frequency temperature sensitivity in a range from $-40°C$ to $80°C$ for the typical corner is shown to be as little as $29.4\frac{ppm}{°C}$

Sammendrag

Som et resultat av behovet for økt datakraft skjer det en kontinuerlig nedskalering i størrelse for transistorteknologier, noe som stadig innfører nye utfordringer. Transistorer har nådd et nivå med kanallengder på noen nanometer, noe som stiller ekstremt høye krav til produksjonen. Små uregelmessigheter i produksjonsutstyr og produksjonsmiljø can føre til store prosessvariasjon mellom hver enkelt chip produsert, men også variasjon innad på hver enkelt chip. Sammen med en økt transistortetthet per chip, som fører til store ytelsesproblemer på grunn av temperaturvariasjoner, har disse effektene sammen stor innvirkning i forskjeller på operasjonsfrekvens og effektforbruk.

Denne masteravhandlingen presenterer analyse og design av en krets med målet om å kompensere terskelspenningen, ved hjelp av bulk–biasering, for å minimere effekten av prosess– og temperaturvariasjon. Kompenseringskretsen er laget for å dynamisk tilpasse bulk biasering for et stort antall transistorer av samme type og størrelse på en chip, som kan være nyttig i digitale systemer hvor det er mange repiterte instanser. Funksjonaliteten og effekten av kompenseringskretsen vil bli testet ved å designe den for og brukes med en 13–stegs inverterbasert ringoscillator som opererer på $65.5MHz$, for så å observere forbedringer i frekvensvariasjon på tvers av forskjellige prosesshjørner og temperaturer mellom $-40°C$ til $80°C$. Alle kretser ble designet i en kommersielt tilgjengelig $28nm$ FDSOI transistor teknologi, på bakgrunn av denne teknologiens utmerkede mottakelighet for bulk biasering og dens lovende utsikter som arvtageren til BULK CMOS for å føre *Moore's law* videre.

Resultater fra simuleringer gjort på nettlister ekstrahert fra utlegg av ringoscillatoren viser at frekvensvariasjon over prosesshjørner og temperatur har blir redusert fra 18.69% ned til 0.632% ved å bruke kompenseringskretsen designet i denne oppgaven. Ringoscillatorens temperatur sensistivitet i temperaturområdet $-40°C$ til $80°C$ for det typiske hjørne viste seg å være bare $29.4\frac{ppm}{°C}$.

Preface

The work in this thesis was carried out during spring 2014, at NTNU, Trondheim. I would like to thank my supervisors, Professor Trond Ytterdal and Carsten Wulff, for their guidance throughout this project. During weekly meetings there has been a lot of coffee drinking, good talks and many laughs. Their skill and passion for the art of analog ic–design has been a great motivator, leading me to pursue a career within this field.

Another thanks goes out to my fellow students and office roommates, Endre Larsen, Harald Garvik and Thomas Nornes. Our office has been a joyful place where we have had lots of fun. We have motivated each other, ideas have been exchanged and many topics discussed. Our camaraderie, along with the exhaustible positivity of our supervisors, has turned hardships into good times.

Table of Contents

Page

Problem description **i**

Abstract **iii**

Sammendrag **v**

Preface **vii**

Table of Contents **xi**

List of Figures **xiv**

List of Tables **xv**

1 Introduction **1**

1.1 Main contributions 3

1.2 Thesis outline 3

2 Theory **5**

2.1 FDSOI 5

2.2 Properties of the Mosfet Transistor 6

2.2.1 Operating Regions 8

2.2.2 Threshold voltage 11
2.3 OTAs 13
2.3.1 Differential input stage 14
2.3.2 Current mirrors 15
2.4 Feedback 16
2.5 Sources of variation in integrated circuits 18
2.5.1 Process variation 19
2.5.2 Random process variation 19
2.5.3 Temperature variation 21

3 Design **23**
3.1 Compensation of process and temperature variations 23
3.1.1 Variation sensing and compensation 24
3.2 PTAT Current Reference 27
3.3 Amplifier design 32
3.3.1 Amplifier layout 34
3.4 Ring Oscillator 34
3.4.1 Ring oscillator layout 38
3.5 Compensation of ring oscillator 38

4 Results and discussion **43**
4.1 PTAT current reference 43
4.1.1 Mismatch 45
4.2 Two–stage miller amplifier 47
4.3 Compensation circuit 47
4.4 Compensation of ring oscillator 51
4.4.1 Mismatch in the ring oscillator 55

5 Conclusion **59**

5.1 Further work 60

Appendix A Design of two–stage miller amplifier **I**

A.1 Implementation of amplifier III

List of Figures

2.1 Illustration of BULK CMOS and UTBB FDSOI CMOS 6

2.2 NMOS intrinsic gain stage. 7

2.3 NMOS Low Frequency Small Signal Equivalent Circuit. 7

2.4 Cross section showing the physical structure of an UTBB FDSOI transistor implemented with triple well. 13

2.5 Differential to singel-ended amplifier. 14

2.6 Differential input stage 15

2.7 A CMOS current mirror. 15

2.8 General feedback system 16

2.9 Configuraion for calculating open loop gain of a feedback system . . 17

2.10 Illustration of spread between corners. 20

3.1 Diode connected transistor. 24

3.2 Derivative of logarithmic drain current versus v_{gs} 25

3.3 NMOS threshold compensation circuit.[29] 27

3.4 V_{eff} dependency on temperature variation with constant I_{ref}. 28

3.5 PMOS threshold compensation circuit.[29] 29

3.6 PTAT current reference. 30

3.7 small signal equivalent circuit of PTAT current reference. 31

3.8 Implemented two-stage amplifier[29] 33

3.9 Layout of two–stage miller amplifier. 35

3.10 Ring oscillator with 3 inverters. 37

3.11 Layout of inverter based ring oscillator with 13 stages. 39

4.1 Corner variation of PTAT current reference for NMOS compensation. . 44

4.2 Corner variation of PTAT current reference for PMOS compensation. . 45

4.3 NMOS threshold voltage versus temperature and process variations, compensated and uncompensated. 49

4.4 PMOS threshold voltage versus temperature and process variations, compensated and uncompensated. 50

4.5 Ring oscillator voltage pulse. 52

4.6 Frequency versus temperature and process variations, compensated and uncompensated. 54

4.7 Frequency versus temperature and process variations, compensated and uncompensated, during monte carlo simulation. 57

A.1 Two-stage Miller Amplifier II

A.2 Implemented two-stage amplifier IV

List of Tables

3.1 Amplifier paramteres 33
3.2 NVTCTRL current reference transistor sizes 40
3.3 PVTCTRL current reference transistor sizes 40

4.1 Results of PTAT current reference for NMOS and PMOS compensation circuits. 46
4.2 Results of 60 monte carlo runs for the PTAT current reference. 46
4.3 Results of amplifier schematic model simulations.[29] 47
4.4 Results of amplifier post–layout simulations. 48
4.5 Variations in NMOS and PMOS–threhsold voltage. 51
4.6 Results of NMOS and PMOS compensation circuits. 51
4.7 Resulting properties for the ring oscillator. 53
4.8 Frequency variation in the ring oscillator as a result of process and temperature variations. 53
4.9 Results of 20 ring oscillator monte carlo runs. 56

A.1 Amplifier paramteres V

1 | Introduction

For the past decades an increasing demand for computational power has emerged as information technology‘s role in society has expanded dramatically. In year 2003, there were 500–million devices connected to the internet, today we have reached 8.9–billion and an estimate show that as a result of the new trend "Internet of Things" several tens of billions of devices will be connected by year 2030 [1, 2]. This increasing demand has resulted in an approximately doubling of processing power for computers every two years from the seventies and up until now, a development which is known as Moore‘s law [3]. To maintain this rise in processing power, transistor sizes have been scaled down to fit more devices onto a single chip, so an increased number of operations can be performed in less area and in less time. As transistor process technology has scaled down, a variety of challenges has emerged [4–7]. Transistors are now being produced at an atomic level, which put stringent requirements on presicion in the manufactoring process. Because transistor operation is based on its physical properties, small variations in the manufactoring process can lead to large deviations in transistor operation, which in turn can degrade the performance of an integrated circuit [5]. A high density of transistors on a chip also generate huge amounts of heat, which have a severe impact on transistor performance as it causes variations and increased leakage across the chip and it is considered one of the great challenges for integrated circuits today [7, 8]. All these variations have larger impact when the supply voltage is reduced to meet the low power demands of an increasing number of battery driven devices. Threshold voltage does not scale proportional to supply voltage, and the difference between supply voltage and transistor threshold voltage is reduced [6, 9, 10].

Threshold voltage is a parameter often used to describe transistor operation, and may be defined as the voltage needed to fully invert the transistor channel[11]. It is not a physical property, but a parameter that is derived for analytical purposes to describe tranistor operation relative to an approximate level of channel inversion. Transistor variation is also often described in terms of threshold voltage, or rather a deviation relative to an expected threshold voltage, which will be the case in this thesis as well [5]. Variations in threshold voltage cause severe variations in operational frequency and may increase leakage currents, in some cases operational frequency may vary up to 30% whitin the same chip [4, 8, 12]. The threshold voltage can therefore be recognized as a critical parameter to control, in order to minimise the impact of variations due to manufactoring and temperature.

One way to control the threshold voltage is by using bulk biasing, or body biasing. The threshold voltage is a funcion of the bulk–source potential V_{bs}, and by applying a postive voltage between bulk and source of a NMOS–transistor, its threshold voltage will be reduced, which will decrease its gate delay, but increase leakage current. By applying a negative voltage between bulk and source of a NMOS–transistor, its threshold voltage will increase which will reduce its gate delay and reduce leakage currents. These two techniques are called forward body biasing and reverse body biasing, and can be exploited to optimise circuit performance in terms of operation frequency and leakge[7, 13].

This thesis will explore body biasing as a technique to compensate the threshold voltage for process and temperature variations in a commercially available $28nm$ *Ultra-Thin Buried oxide and Body Fully Depleted Silicon on Insulator*, UTBB FDSOI CMOS technology. This technology is engineered to achieve low power operation with less leakage than BULK CMOS, and is viewed as one of the top transistor technologies to continue Moore‘s law [13, 14]. Systems capable of compensating threshold voltages in both NMOS and PMOS–transistors will be designed and analysed. These compensation systems will then be tested with a thirteen stage ring oscillator. Ring oscillator frequency depend highly on threshold voltage, and will therefore be vulnerable to both process and temperature variations, which makes them very applicable when characterising variations[5]. The compensation circuits effect can then be determined by looking at frequency variations in the ring oscillator across process corners and temperature. The system will adaptively use both forward body bias and reverse body bias, which sometimes is refered to as adaptive body bias, in order to stabilise the ring oscillator frequency. To the authors knowledge, there are currently no other litterature on ring oscillators with body biasing to compensate for process and temperature variations, so in order to compare its effectivity, published results from a few ring oscillators with other means of process and temperature compensation will be looked at. Only published work with on chip measurement will be used.

Of all oscillators looked at in previous work, the most cited [15] utilises a differential ring oscillator with a control voltage compensating for process and temperature variations. With a band gap reference and voltage regulator providing process and temperature insensitive supply voltage, this oscillator has a power consumption of $1.5mW$. [15] reports a frequency variation of $\pm 0.84\%$ around the typical process corner for a temperature range of $-40°C$–$125°C$. With a variation in frequency of $\pm 2.12\%$ across three corners TT, FF and SS, [15] yields a worst case variation across both process and temperature of $\pm 2.64\%$. A ring oscillator with a much simpler architecture and a total power consumption of $87\mu W$ is given in [16]. This ring oscillator reports a variation in frequency of 5.8% across corners and $85\frac{ppm}{°C}$ over temperature. This means [16] has a lower power consumption and is more insensitive to temperature variations than [15], but has larger variations across process corners.

1.1 Main contributions

This thesis has investigated the effiency of body biasing as a tool for reducing process and temperture variations in an inverter based $65.5MHz$ ring oscillator. This has resulted in the design of a circuit able to compensate the threshold voltages for such variations, which was applied to the ring oscillator reducing its frequency variations across processing corners and temperature dramatically. The main contributions if this thesis are listed below:

- Design and analysis of compensation circuits, for both NMOS and PMOS, that provides body bias to compensate the threshold voltage for process and temperature variations.
- Design of a highly linear low-power low-frequency amplifier with $100.4dB$ DC-gain, a total power consumption of $188.044pW$, and a SNDR$= 57.21dB$.
- Design and analysis of a PTAT–current reference containing a positive feedback loop.
- Design and analysis of a process and temperature compensated thirteen stage inverted based *Ring Oscillator*, operating at a frequency of $65.5MHz$.

1.2 Thesis outline

In chapter 2, background theory which is relevant to the task at hand will be presented. This includes some basic theory concerning the transistor technology used, and some more theory on its physical structure that is of high importance when using body biasing. There will also be presented some classical theory on transistor operation and amplifier design, in order to support different design choices. Lastly there will be a section explaining sources of variation in integrated circuits. Chapter 3 presents the design and analysis of the compensation system, the ring oscillator and all circuits in the compensation system. In chapter 4, results obtained by simulation will be presented, analysed and discussed, providing the insight needed to obtain a conclusion which is presented in chapter 5.

2 Theory

This chapter presents background theory supporting main topics and design choices made throughout this thesis. Much of the basic theory presented in this chapter is based on classical theory that can be found regular text books on analog integrated circuit design, e.g. [11, 17, 18]. However, some less known theory is also presented, and sources for this will be listed were this theory is presented.

First there will be a short presentation of FDSOI–transistors, which will be followed by a section explaining the operation of a MOSFET–transistor, in which an important subsection is dedicated to the threshold voltage and theory concerning body biasing. After a short section about OTAs there will be a section concerning feedback, as feedback is a vital part of the compensation circuit and many of the other circuits designed in this thesis. Lastly, some sources of variation in integrated circuits are present.

2.1 FDSOI

Ultra-Thin Buried oxide and Body Fully Depleted Silicon on Insulator, UTBB FDSOI, is a planar CMOS transistor technology designed for low power applications and show great potential as a successor to BULK CMOS for continuing Moore‘s law [13]. UTBB FDSOI transistors are constructed by placing an ultra-thin undoped silicon film channel on top of a buried oxide layer. This oxide layer provides insulation between the substrate and channel, hence the name silicon on insulator. For $28nm$ FDSOI, the buried oxide is $25nm$ thick and the channel is $7nm$ thick. Because of the channel being undoped and so thin, the transistor is fully depleted, which means that it has no intrinsic charge carriers. The threshold voltage is therefore almost independent of the silicon film thickness, but a strong function of the high-k gate metal workfunction and the doped backplane beneath the buried oxide [14]. As a result the FDSOI transistor has improved variability and electrostatics compared to BULK CMOS, and do not need pocket implants or channel doping in order to control the electrostatic and the threshold voltage variation [13]. Back–plane doping is chosen based on what type of transistor is implemented. For regular-V_{t0} (RVT) devices the back-plane doping is identical to gate-type, and for low-V_{t0} (LVT) devices the back-plane doping is opposite to the gate–type. This means that LVT-NMOS lies in an n–doped well, whereas LVT-PMOS lies in a p–well which is isolated from the substrate by a deep n-well, and they are so called flipped well devices. Because of the buried oxide providing insulation between channel and substrate there is less junction capacitance and a more confined electrical path between source and drain, resulting in reduced leakage. The buried oxide along with the thin undoped channel improves short channel effects and reduces the effect of drain induced barrier lowering, making this technology eligible for further downscaling [13]. Figure 2.1 is an illustration of a BULK CMOS transistors structure compared to an UTBB FDSOI transistor.

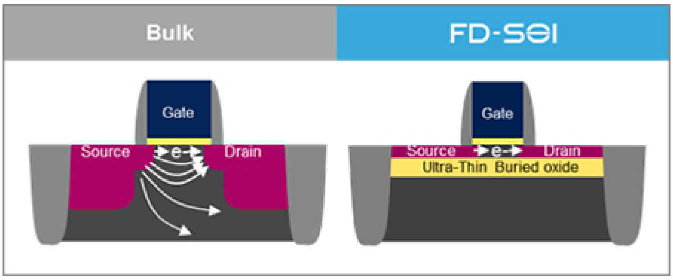

Figure 2.1: Illustration of BULK CMOS and UTBB FDSOI CMOS

The buried oxide will also have an effect as a second gate, due to the capacitive coupling through the undoped depleted silicon. By applying a voltage to this *back gate*, one gate modulate the front channel threshold voltage. This technique of manipulating the threshold voltage is called body biasing, and can be a useful tool for speed enhancement ,power management and to increase performance of a circuit. Compared to BULK CMOS, FDSOI has an improved body effect from increased capacitive coupling causes the threshold voltage to change approximately $85m\frac{V}{V_B}$ compared to $25m\frac{V}{V_B}$ for advanced BULK CMOS [13].

2.2 Properties of the Mosfet Transistor

CMOS transistors are central building blocks in today's high density integrated circuits. Transistors in a digital context are operated as switches in which they represent two different states, either 1 or 0. Transistors used in an analog context are used to modulate signals containing information. Using transistors for amplification is one of the most common forms of doing this, as properties needed for amplification are intrinsic to the transistor across technologies. This section will provide the basic theory for understanding mosfet transistors and their operation in an analog context. Figure 2.2 show a NMOS transistor configured as a *intrinsic gain* stage and figure 2.3 depicts the low frequency small signal equivalent model of a NMOS transistor. With the gate connection (G) serving the input signal, while the bulk (B) is shorted to ground, the intrinsic gain stage can be viewed as a common source configuration loaded by an ideal current source[11].

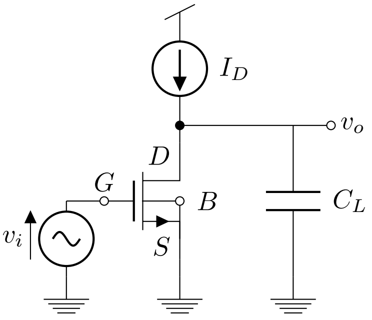

Figure 2.2: NMOS intrinsic gain stage.

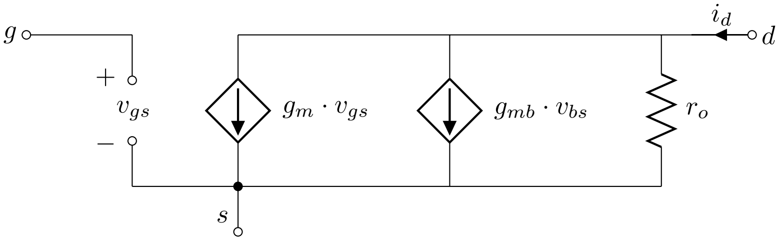

Figure 2.3: NMOS Low Frequency Small Signal Equivalent Circuit.

As we now have defined the intrinsic gain stage we can use figure 2.2 and 2.3 to derive an expression for the transistors intrinsic gain. The intrinsic gain describes the highest possible low frequency small signal voltage gain a transistor can achieve. For low frequencies C_L acts as an open circuit and the current flowing through r_o defines the output voltage v_o, the resulting expression for intrinsic gain is shown in equation (2.1).

$$A_{i,dc} = \frac{v_o}{v_i} = -g_m r_o \tag{2.1}$$

g_m is the transistors transconductance, and r_o is the transistors output impedance, mostly dominated bye the resistance between drain and source. As frequencies rise the impedance at the transistor output gets more and more dominated by C_L which is comprised by the largest capacitances seen at this node. For the intrinsic configuration this means $C_L \approx C_{gs} + C_{gd}$, which is the capacitances between gate to source and gate to drain respectively. These capacitances is not shown in figure 2.3 as this figure represents the transistor for low frequencies. For high frequencies there will be parasitic capacitances between all nodes, where C_{gs} is largest followed by C_{GD} [11]. The expression for intrinsic gain at high frequencies is given by equation

(2.2).

$$A_{i,ac} = \frac{v_o}{v_i} = -\frac{\frac{g_m}{C_L}}{j\omega} \tag{2.2}$$

Here ω is the angular frequency, defined as $\omega = 2\pi f$. By solving the equation for $|A_{i,ac}| = 1$ we can derive another important intrinsic paramater, f_T, the *unity gain frequency.* This parameter is also known as the *transition frequency* and gives an approximation to the frequency range of which a transistor can operate as an amplifying device. Above this frequency the amplitude of the input small signal current $|i_{in}|$ exceeds that of the output small signal current $|i_{out}|$, and equation (2.3) show this approximated frequency.

$$f_T \approx \frac{g_m}{2\pi C_L} \tag{2.3}$$

2.2.1 Operating Regions

Intrinsic gain and transition frequency are the two most fundamental characteristics of a transistor and make a good starting point when designing analog circuits. However, to do an efficient design one needs to relate these paramters to the operation region of the transistor, so the resulting design is optimised for a given set of specifications. Keep in mind that these definitions and equations are analytic expressions and are merely approximations as there are many other effects that will impact the transistor. However, they are very useful as a starting point when designing analog circuits.

Operation regions of a transistor is defined by the voltage difference between source and drain (V_{ds}) relative to the *overdrive voltage* (V_{eff}). The overdrive voltage is defined as $V_{eff} = V_{GS} - V_{tn}$, where V_{tn} is the threshold voltage of an NMOS transistor. If one increases V_{ds} so that $V_{ds} \geq V_{eff}$, the transistor is in *active region* where the drain current becomes approximately constant due to the drain end of the channel being pinched off and the transistor is *saturated.* This region of operation is desired when operating the transistor as a amplifier, because of the drain current being nearly independent of V_{ds} and only changing with V_{gs}. From the overdrive voltage we can approximate the inversion level of the transistor channel, and the inversion level rises gradually with V_{gs}. If $V_{gs} > V_{tn} + 100mV$ the channel is approximately in strong inversion. For a strongly inverted transistor in active region the drain current is dominated by drift current due to an excess of charge carriers, and has an almost quadratic relationship to V_{eff}. The drain current in strong inversion is given by equation (2.4) where λ is the channel-length modulation and £μ_i is the mobility.

$$I_D = \frac{1}{2}\mu_i C_{ox}\left(\frac{W}{L}\right)V_{eff}^2\left(1 + \lambda V_{ds}\right) \tag{2.4}$$

When V_{gs} is decreased and we have V_{gs} in the region of $V_{gs} < V_{tn} - 100mV$, the transistor is in weak inversion. When in weak inversion the drain current is dominated by diffusion and has a exponential relationship to the overdrive voltage and is given by equation (2.5) [11]. Keep in mind that V_{ds} is still sufficiently large enough to keep the transistor in active region.

$$I_D \cong I_{D0}\left(\frac{W}{L}\right)e^{\left(\frac{qV_{eff}}{nkT}\right)} \tag{2.5}$$

Where I_{D0} is given by (2.6) [11],

$$I_{D0} = (n-1)\,\mu_i C_{ox}\left(\frac{kT}{q}\right)^2 \tag{2.6}$$

and n is given by (2.7)

$$n = \frac{C_{ox} + C_{j0}}{C_{ox}} \approx 1.5 \tag{2.7}$$

n is often refered to as the slope factor. When in weak inversion it is possible to obtain useful drain currents in the magnitude of pico amperes [19] due to negative V_{eff}. This is not possible in strong inversion, as drain currents needs to be large enough to dominate the leakage currents.

By differentiating the drain current with respect to V_{gs} we obtain the transconductance g_m. The transconductances in strong and weak inversion is given in equations (2.8a) and (2.8b) respectively.

$$g_m = \frac{\delta I_D}{\delta V_{gs}} = \sqrt{2\mu_i C_{ox}\left(\frac{W}{L}\right)I_D} \tag{2.8a}$$

$$g_m = \frac{\delta I_D}{\delta V_{gs}} = \left(\frac{q}{nkT}\right)I_{D0}\left(\frac{W}{L}\right)e^{\left(\frac{qV_{eff}}{nkT}\right)} = \frac{qI_D}{nkT} \tag{2.8b}$$

By remembering equation (2.3) for the transitional frequency we see that the transconductance tells us the transistors ability to drive a load. By relating the transconductance to drain current, we get a design parameter that gives us a measure of how efficient a transistor translates current, or power if you like, into transconductance. This relation is known as the $\frac{g_m}{I_D}$ ratio and has been recognised as a highly efficient parameter for designing analog circuits [20].

$$\frac{g_{m,strong}}{I_D} = \frac{\sqrt{2\mu_i C_{ox}\left(\frac{W}{L}\right) I_D}}{I_D} = \frac{\sqrt{2\mu_i C_{ox}\left(\frac{W}{L}\right)}}{\sqrt{I_D}} \tag{2.9a}$$

$$\frac{g_{m,weak}}{I_D} = \frac{\frac{qI_D}{nkT}}{I_D} = \frac{q}{nkT} \tag{2.9b}$$

From equation (2.9b) it can be seen that in weak inversion the transconductance is constant and maximised for a given constant current. When moving towars strong inversion we see from equation (2.9a) that the $\frac{g_m}{I_D}$ ratio decreases with the square root of I_D. The transition frequency can also be expressed as $f_T \approx \frac{3\mu_i V_{eff}}{4\pi L^2}$ and the overdive voltage $V_{\mathit{eff}} \approx \frac{2I_D}{g_m}$ [11]. Substituting V_{eff} into f_T results in equation (2.10).

$$f_T \approx \frac{6\mu_i I_D}{4\pi L^2 g_m} \tag{2.10}$$

Equation (2.10) tells us that even though $\frac{g_m}{I_D}$ is maximised in weak inversion it is not very applicable for high frequencies.

Looking at the intrinsic gain in equation (2.1), defining the output resistance $r_o \approx r_{ds}$ which is given by equation (2.11), the intrinsic gain can be expressed by equation (2.12). These equations show that transistors with long channels operated in weak inversion yields highest achievable dc–gain.

$$r_{ds} = \frac{1}{\lambda I_D} = \frac{L}{(L\lambda) I_D} \tag{2.11}$$

$$A_{i,dc} = -\frac{g_m L}{(L\lambda) I_D} \tag{2.12}$$

For $V_{DS} < V_{\mathit{eff}}$ we operate the transistor in triode region, and in this region the drain current varies with V_{ds}. For very low V_{ds} the triode region is often called *linear region* due to its approximately linear relationship between drain current and V_{eff}. In the linear region the drain current is given by equation (2.13). This operation region is often used when using a transistor to model a voltage controlled resistor capable of achieving approximately constant high resistance.

$$I_D \cong \mu_i C_{ox}\left(\frac{W}{L}\right)(V_{\mathit{eff}} V_{DS} - \frac{V_{ds}^2}{2}) \tag{2.13}$$

An approximation of the resistance when operating the transistor in linear region is given by equation (2.14)

$$R_{ds} = \frac{V_{ds}}{I_D} = \frac{1}{\mu_i C_{ox}\left(\frac{W}{L}\right) V_{\mathit{eff}}} \tag{2.14}$$

2.2.2 Threshold voltage

From section 2.2 we saw that transistor operation varies with the inversion level of the channel. This inversion level was defined by V_{gs} and its relation to V_{tn}, and the borders between weak, moderate and strong inversion are not abrupt, but changing gradually. Therefore, these inversion border definitions are very approximate, and not very well defined. One of the reasons for this is that opposite to V_{gs}, V_{tn} is not a well defined voltage applied to the transistor, but a parameter based on measurements. Often, measurements of threshold voltage is done by looking at drain current versus V_{gs} relationships, but other techniques exist, and therefore threshold voltage may vary with the techniques applied for measuring it [5]. The threshold voltage is inherent to the transistor, and is decided by physical proporties. Therefore the threshold voltage can be engineered by manipulating the physical properties of the transistor such as gate metal, channel doping, oxide thickness and pocket implants. Based on these physical quantities one can derive analytical expressions for the threshold voltage, whereas the most famous is given in equation (2.15).

$$V_{tn} = V_{t0} + \gamma(\sqrt{V_{SB} + |2\Phi_F|} - \sqrt{|2\Phi_F|}) \tag{2.15}$$

In 2.15, Φ_F is the fermi potential of the body given by

$$\Phi_F = -\frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.16}$$

where n_i is the carrier consentration of intrinsic silicon, N_A is the substrate doping and $\frac{kT}{q}$ is the temperature dependant potential. When the voltage drop from channel to substrate is equal to two times the fermi fotential, the electron concentration in the channel is equal to the hole concentration in the subtrate and is often used as a definition of when a channel is inverted. V_{t0} is the threshold voltage when $V_{SB} = 0$. γ represents the *body-effect factor* and is shown in equation 2.17

$$\gamma = \frac{\sqrt{2qN_A K_s \epsilon_0}}{C_{ox}} \tag{2.17}$$

K_s is the relative permittivity of silicon, N_A is the substrate doping, q is the charge of an electron and ϵ_0 is the permittivity of free space. The *body-effect factor* models the capacitive coupling between the substrate and the channel. From equation (2.15) it can be seen that for $V_{sb} \neq 0$ the threshold voltage will be modulated as a result of the body effect. Higher substrate doping results in higher capacitive coupling and the voltage potential applied to the bulk has greater influence on the threshold voltage. In BULK CMOS the only insulation between channel and substrate is that formed by the depletion region of their pn–junction, and the voltage that can be applied to the bulk is limited by the reverse biased diode formed by the pn-junction. It should be noted that the capacitive coupling between channel and substrate in BULK CMOS is highly nonlinear and changes with the voltage applied to the bulk as the width of the depletion region changes [11]. In FDSOI, this capacitive coupling is stronger and more reliable as the channel is insulated from the substrate, or well, by a layer of insulating oxide [13, 21, 22]. Equations (2.18) (2.19) (2.20) show the analytic expressions describing the theshold voltage of the FDSOI simulation models used in this project and is listed in the documentation of the design kit.

$$V_{t0} = \frac{1}{1 + (1 - n_{eq}) \cdot (C_{ic} - 1)} \Bigg(n_{eq} \cdot \Phi_T^* \cdot \ln\left(\frac{2n_{eq} \cdot C_{ox} \cdot \Phi_T^*}{q \cdot n_i \cdot T_{si}}\right) + (n_{eq} - 1) \cdot V_{FBB,sub} + V_{FB} + 2n_{eq} \cdot \Phi_T^* \Bigg) \tag{2.18}$$

Φ_T^* is a complimentary to absolute temperature dependant potential including the thermal voltage $\frac{kT}{q}$. T_{si} is the silicon channel thickness, V_{FB} and $V_{FBB,Sub}$ are the flat-band voltages of the metal gate and silicon substrate respectively. V_{FB} corresponds to an initial potential difference between the metal gate and the silicon channel due to a difference in work functions. $V_{FBB,sub}$ corresponds to an initial potential difference between the substrate and the silicon channel due to their different work functions. Engineered work–functions, which decide flat–band voltages, are one of the main components to set the threshold voltage, and is done by a metal gate stack of different materials [13, 22, 23]. There is also a flat-band voltage influencing the bulk threshold (2.15, which is between the metal gate and the silicon channel [11].

$$V_{ts} = V_{t0} + \frac{(1 - n_{eq}) \cdot C_{ic}}{1 + (1 - n_{eq}) \cdot (C_{ic} - 1)} \cdot V_{bs} \tag{2.19}$$

$$V_{tn} = V_{ts} - \Delta V_g \tag{2.20}$$

ΔV_g is the drain induced barrier lowering. n_{eq} is the capacitive divider for the gate, silicon and buried oxide capacitances, also known as the slope factor, and is given in equation (2.21).

$$n_{eq} = 1 + \frac{C_{si} C_{box}}{C_{ox} \left(C_{si} + C_{box}\right)} \tag{2.21}$$

In (2.19), we see that the second term describes the body–effect of FDSOI–transistors describing the influence of V_{bs} on the threshold voltage. C_{ic} is a capacitive coupling factor from substrate to the interface of the channel. n_{eq} is given in equation (2.21) where C_{box}, C_{si}, C_{ox} is the back gate oxide, silicon channel and gate oxide capacitances respectively [22]. Higher back–plane doping will increase C_{box} and C_{si}, resulting in a higher body–effect [21, 22]. Back–plane doping is done by creating a doped well in the substrate with distinct doping concentrations. Figure 2.4

show a simplified cross section of the structure in FDSOI low threhsold LVT–devices. Using an N–well for the NMOS and P–well for the PMOS–transistor helps lowering the threshold voltage. By applying a voltage to the P or N–well via the bulk terminals marked B, you will modulate the threshold voltage according to equation 2.19, which is a technique called body biasing.

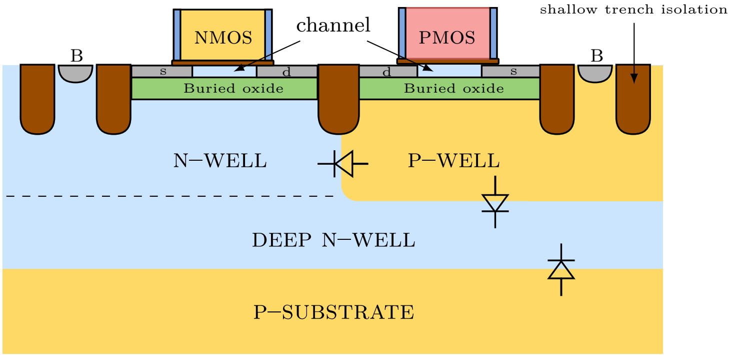

Figure 2.4: Cross section showing the physical structure of an UTBB FDSOI transistor implemented with triple well.

There are two types of body biasing one usually speaks about, *forward body biasing* FBB and *reverse body biasing* RBB. FBB is apply a positive voltage to the bulk connection, which lowers the threshold voltage. This will increase the transistors operational frequency, but it will suffer from more leakage. RBB is the opposite, namely applying a negative voltage to the bulk to increase the threshold voltage. RBB reduces leakage at cost of lower operational frequency. The wells in which the devices lies puts restraints on the voltage-range one can apply to the bulk. For example for LVT–devices, if both NMOS and PMOS lies in the same deep n-well, there will be formed a diode in the pn-junction between the PMOS p-well and NMOS n-well. There will also be a diodes formed between the PMOS p-well and its isolating deep n-well, and between deep n-well of both devices to the p-type substrate. These scenarios are depicted in figure 2.4. The body bias voltage-range is therefore limited to voltages that don‘t cause forward biasing of the diodes in one end of the range, and their breakdown voltage in the other end. Well-diodes becomes forward biased around 200–300mV, whereas the breakdown voltage is approximately 3V [13]. Biasing beyond these limitations may cause significant leakage.

2.3 OTAs

Amplifiers are one of the most common circuit implementations in analog integrated circuits. Amplifiers are key components in signal paths to maintain, or increase, the integrity of signals containing information. Because of the inherent properties of MOSFET-transistors discussed in section 2.2, they are favourable devices when designing small and efficient integrated amplifiers. Section 2.2 explained the intrinsic gain stage, which is also identical to a typical amplifier topology; the common source amplifier. This topology is single-ended, and the ground connection is common to both input signal, supply and output signal. This can be disadvantageous as the output voltage may not only depend on the input signal, but will also follow the supply voltage. This means that ripples and noise in the supply voltage will appear at the output of the amplifier [17]. To circumvent this problem, one can use differential amplifiers. Imagine if you have two identically matched common source stages, then the same ripples and noise will occur at the output of both stages. If you subtract one output from the other, these unwanted effects will be removed from the overall output. A schematic symbol of a differential to single-ended amplifier is shown in figure 2.5.

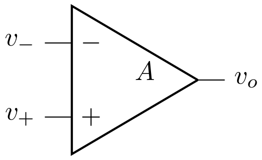

Figure 2.5: Differential to singel-ended amplifier.

The output of this amplifier can be expressed as in equation (2.22), where A is the amplifier gain.

$$v_o = A\left(v_+ - v_-\right) \tag{2.22}$$

As we see in equation (2.22), all signals common between v_+ and v_- will be removed and only the difference will be amplified. Therefore signals applied to the amplifier needs to be differential, signals on input v_- needs to be phaseshifted with respect to v_+. This section will present two common building blocks for realising differential amplifiers which are also central in this project.

2.3.1 Differential input stage

A differential input stage with MOSFET-transistors loaded by Z_L is shown in figure 2.6.

The small signal analysis of the circuit in figure 2.6 is found in every textbook concerning design of analog integrated circuits and will only be summarised shortly [11, 17]. Because of symmetrical branches there will be $\frac{I_{bias}}{2}$ in each branch, and the small signal gain of the differential input stage at low frequencies is similar to that of a common source stage and is seen in equation (2.23).

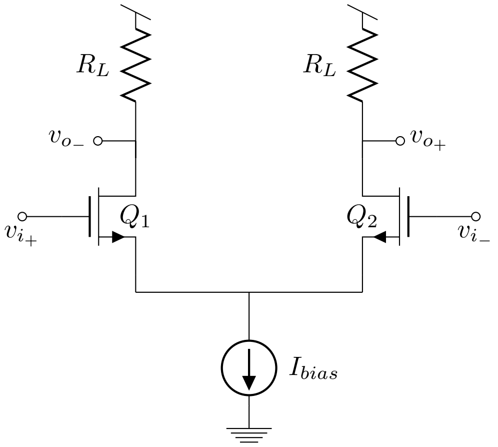

Figure 2.6: Differential input stage

$$A_0 = \frac{\left(v_{o_+} - v_{o_-}\right)}{\left(v_{i_+} - v_{i_-}\right)} = g_m \left(r_o || R_L\right) \tag{2.23}$$

The load R_L is often realised by an active load, such as a current mirror.

2.3.2 Current mirrors

Figure 2.7 show a simple current mirror with NMOS-transistors, chosen because most equations in this chapter is based on NMOS-operation for simplicity. A current mirror is characterised by a relatively low input impedance, $\frac{1}{g_{m_1}}$, and a high output impedance, $r_{out} = r_{ds_2}$, which is given by equation (2.11).

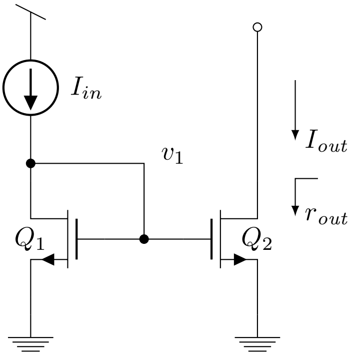

Figure 2.7: A CMOS current mirror.

By assuming that both Q_1 and Q_2 are in the active region and strong inversion their drain currents can be described by the square law voltage-current relationship given in (2.4). As $V_{gs_{Q_1}} = V_{gs_{Q_2}} = v_1$, the relationship between Q_1s drain current, I_{in}, and Q_2s drain current I_{out} is expressed in equation (2.24).

$$\frac{I_{out}}{I_{in}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} = \frac{S_2}{S_1} \tag{2.24}$$

This equation show that the output current is related to the input current by aspect ratios, and is decided solely by transistor geometries [11, 17]. The transistor aspect ratios $\frac{W}{L}$ are often abbreviated by S.

One way of using the current mirror is to load the differential stage shown in figure 2.6 in order to convert to a single ended output. The current mirror needed to load the differential input needs to be realised by PMOS-transistors. Also the bias voltage I_{bias} from figure 2.6 is often fed to the differential input from the current source using current mirrors.

2.4 Feedback

Feedback is a central concept in electronics and crucial to this project. Feedback is often applied when regulation of some system is needed, and can be either positive or negative. Negative feedback is when a part of the output is removed from the input,, making some correction. Positive feedback is when a part of the output is added to the input. Figure 2.8 show a block diagram of a general feedback system. In figure 2.8, **u** is the input of the whole system, **x** is the input to the feed forward system, **A** represents some gain in the *feed forward system*, β is the feedback factor of the feedback system, **v** is the feedback signal and **y** is the output of the whole system. If **v** is negative it will be subtracted from the input, and we have negative feedback. A feedback system is often characterised by its *closed loop gain* and *open loop gain*. To find the closed loop gain for the general feedback system in figure 2.8 we can find its transfer function $\frac{\mathbf{y}}{\mathbf{u}}$. Let us consider the feedback as negative, namely the signal **v** is negative. The output is sensed by the feedback system,

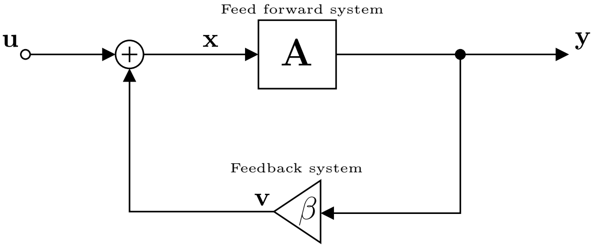

Figure 2.8: General feedback system

and sent back to the input. This gives $\mathbf{v} = \beta\mathbf{y}$. As $\mathbf{v}$ is negative, we can write $\mathbf{x} = \mathbf{u} - \mathbf{v} = \mathbf{u} - \beta\mathbf{y}$. With $\mathbf{x}$ being the input to the feed forward system, $\mathbf{y} = \mathbf{A}\mathbf{x}$, we get $\mathbf{y} = \mathbf{A}\left(\mathbf{u} - \beta\mathbf{y}\right)$. Solving this equation results in the closed loop gain of the general feedback system and is given in equation (2.25)

$$\frac{\mathbf{y}}{\mathbf{u}} = \frac{\mathbf{A}}{1 + \beta\mathbf{A}} \tag{2.25}$$

Figure 2.9 show the necessary configuration for calculation of open loop gain. To calculate the open loop gain, or loop gain, we set all independent signal sources to our system to zero, which in our case means $\mathbf{u} = 0$. Then we break the loop, and apply a test signal $\mathbf{v_t}$ at the point were the loop was broken, and observe the returned value $\mathbf{v_r}$ at the output of the feed forward system. In practice the feedback network will have finite I/O–impedances, so the output should also be loaded by the same impedance as seen at the input of our test signal. This is illustrated with the *sense duplicate* block in figure 2.9 which is a duplicate of the feedback system itself. However, for out calculation now, we will assume an ideal network, so that the sense duplicate does not load the output of our system.

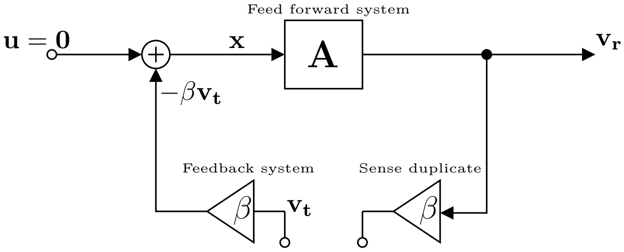

Figure 2.9: Configuraion for calculating open loop gain of a feedback system

From figure 2.9 we see that $\mathbf{v_r} = \mathbf{A}\mathbf{x}$. As we also assume negative feedback in this case, we get $\mathbf{x} = -\beta\mathbf{v_t}$. The resulting expression for loop gain is given in equation (2.26).

$$LG = -\frac{\mathbf{v}_r}{\mathbf{v_t}} = \beta\mathbf{A} \tag{2.26}$$

Consider an amplifier with finite gain A. Whithout feedback, amplifier characteristics such as gain, I/O-impedances and linearity may be very unpredictable. Amplifiers are built using MOSFET–transistors, which are inherently nonlinear devices suffering from unpredictabilities due to many different sources of variations which will be explained later. By using feedback, the amplifiers performance can be stabilised and improved. If $LG >> 1$, equation (2.25) can be simplified to $\frac{1}{\beta}$, which may be more predictable than the amplifier gain if β is set by passive elements. This will often reduce the gain but also it make the gain more constant, reducing nonlinear distortion. By choosing the right feedback topology, one can control the input and output impedances, and also extend the bandwidth of the amplifier.

When using feedback, one should always be concerned by the stability of the feedback system. Negative feedback will always be stable. However, if the feedback network is frequency dependant there might be a phase shift turning the negative feedback positive, resulting in unstable feedback. By looking at figure 2.9 and equation (2.26), one can see that if the loop gain LG becomes negative it will be added to the input, and not subtracted. In this case the feedback will be postive and potentially unstable, which may cause oscillations. Stability of such a system with positive feedback can be obtained by keeping the loop gain below unity. These observations form the base of two properties that describes the stability of a frequency dependant system, namely phase- and gain margin. One can determine if a system is stable based on the closed loop transfer function, and if its poles and zeros are located in the left half plane of the s-plane. However, this may often be complex to analyse. The more simple method determines the phase margin PM based on the loop gain frequency respons. For a frequency dependant loop gain $LG\left(s\right) = A\left(s\right)\beta$, the system is stable if the open loop phase response $\angle LG\left(\omega_t\right) > -\mathit{180}^{\circ}$, where ω_t is the unity gain angular frequency of the loop gain. This term results in the phase margin definition (2.27).

$$PM = \angle LG\left(\omega_t\right) + 180^{\circ} \tag{2.27}$$

Phase margin defines the additional phase shift needed to obtain instability at the unity gain frequency.

Gain margin (GM) is found where the open loop phase shift has reached $-180°$, $\angle LG\left(\omega\right) = -\mathit{180}^{\circ}$ and can be defined as (2.28).

$$GM = 0 - LG\left(\omega_{-180^{\circ}}\right) \tag{2.28}$$

Gain margin tells us how much the signal is dampened at the point in frequency where the feedback becomes positive. If the gain margin is positive, the loop gain is less than one and we still have a stable system.

2.5 Sources of variation in integrated circuits

Transistor technology is continuously scaling down in size to fit more devices into a single chip, and thus achieve more processing power per area resulting in increased performance for modern integrated circuits. There are three main goals motivating transistor scaling: 1) Decreasing transistor gate delay, and thereby increasing the operating frequency; 2) Increasing transistor density; 3) Reducing the energy per operation in order to save power [7, 8]. As a result of technology scaling, one can reduce the supply voltage without lowering the operation frequency, and have a quadratic reduction in power. However, certain limitations arise as process technology reaches atomic levels, and one of the main challenges is variation in the threshold voltage [5]. The threshold voltage does not scale proportionally to transistor size and supply voltage, causing small variations in threshold votage to result in a large impact on performance. For example, by looking back at equation (2.5) one can see that even with $V_{gs} = 0$ there will be some leakage current exponentially dependant on V_{tn}. This leakage current increases with decreasing V_{tn}, which will increase the static power consumption. Along with technology scaling there are continuous innovation being done in the manufacturing processes to overcome the challenges of variation, however the manufacturing can never be completely accurate. Therefore one of the biggest source of these variations may be in the manufacturing process. As a transistors parameters are solely decided by physical quantities of which today are in the sizes of a few nanometers it is not possible to manufacture these 100% precisely. Other variations may origin from degradation of the device over time, or from temperatures influencing the characteristics of the materials in which the device lies.

2.5.1 Process variation

Process variations are variations occuring due to imperfect manufacturing. These variations are spatially correlated and are common to devices within the same area. This means you may observe different process variations between wafers, but also between areas within the same wafer. Process variations occur because it is impossible to maintain the same conditions, e.g. temperature, silicon purity, etc. when manufacturing integrated circuits. Process variations are gaussian distributed, and the expected transistor behavior can be defined as the mean value. Random variations can be seen as fluctuations around this mean, while process variations will change the mean value itself. Random variations will be covered in the next section. To model process variations the production foundries provide different simulation models of the transistors based on measurements to model both typical and various worst case scenarios known as corners. This give circuit designers the possibility to create robust designs capable of maintaining performance over different process corners. Often one may have to add extra overhead in the form of auxiliary circuits to handle these variations, or one must increase device sizes which increases area and may increase power consumption. For this project there will be utilised corner models provided for commercially available $28nm$ UTBB FDSOI transistors to model process variation. Figure 2.10 depict the spread in saturation current between the different corners, where T is for typical, S is for slow, F is for fast and A is for alternative. The first letter in each denomination describes NMOS corners and the second is for PMOS.

2.5.2 Random process variation

Random process variation, also known as mismatch, is variation between two identically matched and identically used devices fabricated under the same conditions. As the performance of analog integrated circuits is often based on ratios between devices, it is very important to characterise how mismatch affect these ratios. Two

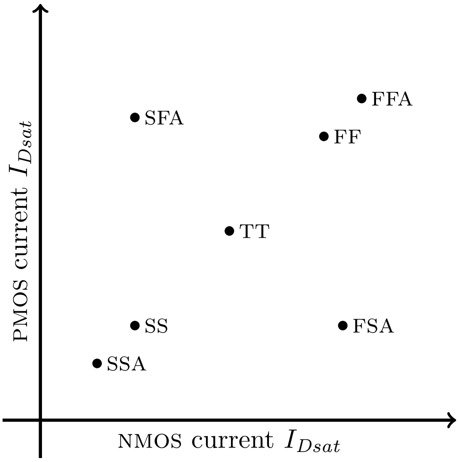

Figure 2.10: Illustration of spread between corners.

of the most important sources of mismatch are threshold voltage variation and β variation, with $\beta = \mu_i C_{ox}$. Random variation is gaussian distributed and the variance in threshold voltage V_{t0} and β for two identical devices is given in equation (2.29a) and (2.29b) respectively.

$$\sigma^2 \left(V_{t0}\right) = \frac{A_{V_{t0}}^2}{WL} + S_{V_{t0}}^2 D^2 \tag{2.29a}$$

$$\frac{\sigma^2 \left(\beta\right)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \tag{2.29b}$$

In (A.9), D is the distance between the two identical devies, W and L are device dimensions and A and S are proportionality constants [11, 24]. Two very common building blocks in analog integrated circuits, and also this project, are current mirrors and differential input pairs. Current mirrors have the same V_{gs}, and at zero input the differential pair also have equal V_{gs}. Because of being biased with the same gate-source voltage, current mismatch in current mirrors and differential pairs can be expressed by equation (2.30).

$$\left(\frac{\sigma\left(\Delta I_D\right)}{I_D}\right)^2 = \left(\frac{g_m}{I_D}\right)^2 \sigma^2 \left(\Delta V_{t0}\right) + \frac{\sigma^2\left(\beta\right)}{\beta^2} \tag{2.30}$$

By assume closely spaced devices, $D \approx 0$, and inserting (A.9) in (2.30) we obtain an expression for current mismatch in a current mirror (2.31).

$$\left(\frac{\sigma\left(\Delta I_D\right)}{I_D}\right)^2 = \frac{1}{WL}\left[A_{V_{t0}}^2 \left(\frac{g_m}{I_D}\right)^2 + A_\beta^2\right] \tag{2.31}$$

From equation (2.31) we see that mismatch in threshold voltage is the dominant, and that current mismatch is largest when transistors are operated in weak inversion, i.e. high $\frac{g_m}{I_D}$. So, in order to achieve high accuracy in current mirrors, operating devices in strong inversion is prefered at the cost of a higher saturation voltage. Whereas for a differential input pair, the mismatch is measured as an offset between the inputs and is given by equation (2.32).

$$\sigma^2\left(V_{OS}\right)=\frac{\sigma^2\left(\Delta I_D\right)}{g_m^2}=\frac{1}{WL}\left[A_{V_{t0}}^2+\left(\frac{I_D}{g_m}\right)^2 A_\beta^2\right] \tag{2.32}$$

And from this equation it can be seen that by biasing the differential input pair with a current and operation the transistors in weak inversion, the offset variance due to variations in β is reduced and V_{t0}-variations becomes dominant. The threshold voltage variations is therefore very important in analog circuits.

2.5.3 Temperature variation

Non-ideal conditions of circuit manufacturing is not the only source of variation that may seriously impact circuit performance. Characteristics inherent to the materials that transistors are made of are dependent on temperature, where two of the most important parameters for transistor operation are carrier mobility μ and threshold voltage V_{t0}. As transistor density on a single die has increased dramatically, the heat generation becomes severe and may impact performance dramatically [7, 8]. From section 2.2 it is clear that these two parameters are involved in almost all aspects of analog circuit performance. Both carrier mobility and threshold voltage decrease with increasing temperature, and their dependence of temperature is modelled by equations (2.33a) and (2.33b) respectively.

$$\mu_0\left(T\right)=\mu_0\left(T_0\right)\left(\frac{T_0}{T}\right)^{k_1} \tag{2.33a}$$

$$V_{t0}\left(T\right)=V_{t0}\left(T_0\right)+\alpha_{V_{t0}}\left(T-T_0\right) \tag{2.33b}$$

In (2.33), T_0 is the reference temperature, k_1 is a fitting constant in the range of $1-2$ in room temperatures, T is the actual temperature and $\alpha_{V_{t0}}=\frac{\delta V_{t0}}{\delta T}$ is a negative constant [25, 26].

3 | Design

The motive behind the circuitry designed in this project is to improve stability and performance of some main functionality carried out by more vital circuitry. Therefore this additional circuitry can be considered overhead, where stability and increased performance is traded for increased power consumption and area. As area has a tendency to increase with complexity, low power and low complexity has been the priority when designing these circuits. All circuits were designed in a commercially available 28nm–FDSOI technology, and circuit design was performed with Cadence Virtuoso. As leakage currents in the bulk 2.2.2 are critical to the performance of bulk biasing, a layout was made of both amplifier and ring oscillator to have an extended verification of these effects. These layouts were made in correspondence with design rules provided by the manufacturer, and passed Layout versus Schematic (LVS) test and Design Rule Check (DRC) performed with Calibre from Mentor Graphic.

3.1 Compensation of process and temperature variations

From section 2.5.1 we defined process variations as fluctuations of a mean value that represents transistor behavior, e.g. threshold voltage. When adding temperature variations to the corners representing worst case mean values, circuits are really at the edge of their operational limit. In this section, we will address these types of variations, and try to compensate these variations so that all corners operates close to the typical mean value for a wide temperature range. As we see in equation (3.20), ring oscillators depend strongly upon paramaters such as threshold voltage. From equation (2.33b) we know that the threshold voltage change with temperature. Section 2.2.2 also demonstrate that the threshold voltage may be sensitive to process variations, as it is based on physical properties in the transistor. We can therefore expect that the oscillation frequency of a ring oscillator will change dramatically over different process corners and temperature. Equation (2.19) show that the threshold voltage in FDSOI–transistors can be modulated by applying voltage to the bulk of the transistor V_{bs}. Therefore, in this first section we will utilise body biasing to compensate for process and temperature variations in a ring oscillator.

3.1.1 Variation sensing and compensation

Variation sensing is done by monitoring the voltage drop over a diode connected mosfet transistor. A diode connected transistor is shown in figure 3.1, and is configurated as a transistor with its gate and drain tied together while source is shorted to ground, which gives $V_{GS} = V_{DS} = V_{out}$. This is a quite common configuration for generation of reference voltages [11].

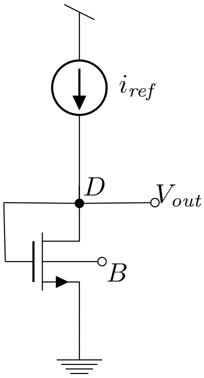

Figure 3.1: Diode connected transistor.

The voltage drop over the diode connected transistor is decided by the reference current applied to it and intrinsic parameters of the transistor, where more current translates to more voltage. An expression for the voltage over the diode in weak inversion is given by equation (3.1) and is derived from the current equation of a transistor in weak inversion given by (2.5). As $V_{eff} = V_{gs} - V_{tn}$, the drain current equation is solved for the diode connected transistor in figure 3.1 with respect to V_{gs} and we obtain

$$V_{gs} = V_{out} = V_{tn} + nV_T \ln\left(\frac{I_{ref}}{I_{D0}\left(\frac{W}{L}\right)}\right) \tag{3.1}$$

This expression (3.1) show the output voltage dependence on drain current and threshold voltage. n is given in equation (2.21) and $V_T = \frac{kT}{q}$ is the thermal voltage. If the diode connected transistor is biased in strong inversion, we can solve equation (2.4) and get the following expression for V_{out} (3.2).

$$V_{gs} = V_{out} = V_{tn} + \sqrt{\frac{2i_{ref}}{\mu_n C_{ox}\frac{W}{L}}} \tag{3.2}$$

However, when sensing the threshold voltage, a reference current i_{ref} is chosen so that $V_{eff} = 0$ and the voltage voltage drop over the diode is $V_{out} \approx V_{tn}$ at room temperatures. This means that the diode connected transistor can be assumed to operate in moderate inversion, where none of the equations above (3.1) (3.2) are valid. Figure 3.2 show a plot of the subthreshold slope $n = \frac{d(\log(i_d))}{d(V_{gs})}$ versus gate–source voltage.

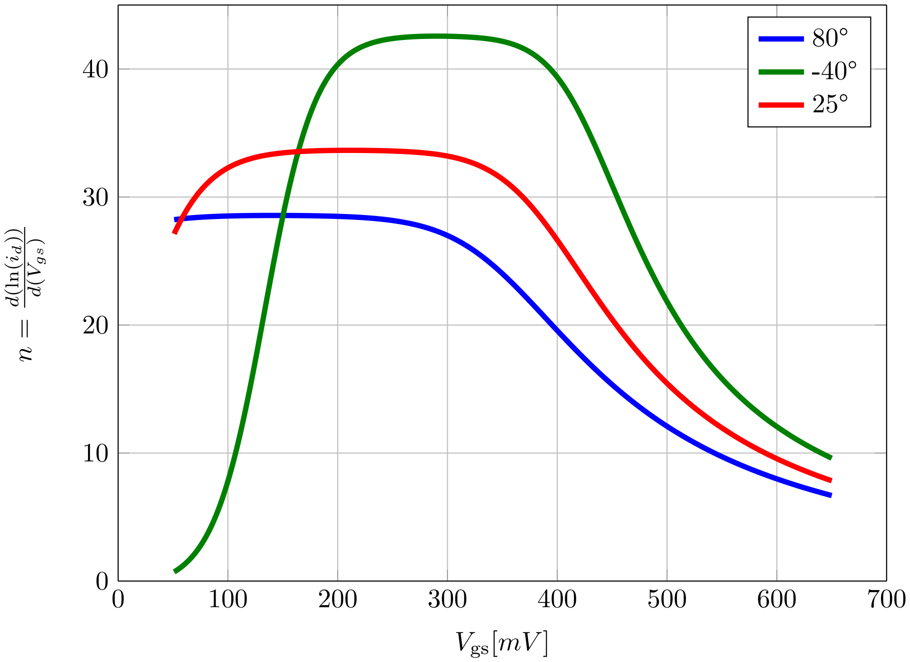

Figure 3.2: Derivative of logarithmic drain current versus v_{gs}

The plateau where n is approximately constant depicts weak inversion operation, where the current exhibits an exponential relationship to the voltage. From simulations, threshold voltage for an LVT–NMOS is shown to be between approximately $350mV$–$430mV$ depending on transistor size. By looking at figure 3.2 we see that in this voltage range, transistor have just exited weak inversion, and the assumption of moderate inversion seems accurate. There are no very accurate equations, that the author is aware of, modelling transistor behavior in moderate inversion. Existing equations for moderate inversion are interpolations between weak and strong inversion operation. One equation for V_{gs} is given in [27] and is an interpolation between equations for weak and strong inversion based on the EKV–transistor model assuming forward current. This approximate interpolated equation describing V_{out}

for the diode connected transistor is given in equation (3.3).

$$V_{out} = V_{tn} + 2V_T \ln\left(e^{\sqrt{\frac{I_{ref}}{2n\beta_n V_T^2 \left(\frac{W}{L}\right)}}} - 1 \right) \tag{3.3}$$

In (3.3), $\beta_n = \mu_n C_{ox}$. In order to get $V_{out} \approx V_{tn}$, the diode must be biased with a current I_{ref} such that the second term in equation (3.3) is cancelled. This occurs for a current such that $e^{\sqrt{\frac{I_{REF}}{2n\beta_n V_T^2 \left(\frac{W}{L}\right)}}} = 2$, as $\ln(1) = 0$, which leads to an expression for the reference current in (3.3) needed to achieve $V_{out} \approx V_{tn}$, and is given in equation (3.4).

$$i_{ref} = 2\ln(2)^2\, n\mu_n C_{ox}\left(\frac{W}{L}\right) V_T^2 \tag{3.4}$$

Temperature dependencies for V_{tn} and μ_n is given in section 2.5.3, and they are both decreasing with temperature. Equation (2.33a) give the following expression for the temperature dependency of mobility, $\mu_0(T_0)\left(\frac{T_0}{T}\right)^{k_1}$, and from [28] we have that the factor $k_1 \approx 1.4$ for SOI–transistors with thin silicon channels. It can therefore be assumed that the temperature dependency of the current in equation (3.4) is positive, and that for temperatures $\pm 60°C$ around room temperatures a PTAT current bias can be applied to the diode connected transistor to approximately cancel the second term in equation (3.3).

The voltage V_{out} will be measured by an amplifier as shown in figure 3.3 and compared to a reference voltage $V_{tref} = V_{tn}$, that should be equal to the typical case threshold voltage. In an ideal scenario with no variations, the output voltage is equal to the threshold voltage $V_{out} = V_{tref}$, and the output voltage of the amplifier is $BN = 0$. If the threshold voltage suffers from variations, leading to $V_{out} \neq V_{tref}$, the amplifiers output voltage will change in order to modulate the threshold voltage via the feedback loop through the diode connected transistors bulk according to equation (2.19).

Figure 3.4 show the change in V_{EFF} for the diode conntected transistor, with threshold voltage compensation, from $-40°C$ to $80°C$. Reference current I_{ref} is constant and adjusted so that $V_{out} \approx V_{tn} \Rightarrow V_{eff} \approx 0$ at room temperature. The plot clearly show that V_{eff} decreases with temperature, and by assuming that the threshold voltage is compensated for temperature variations, it is reasonable to believe that the second term in equation (3.3) decreases with temperature for constant I_{ref}. From this we can expect that a reference current I_{ref} as given in (3.4), which is increasing with temperature, will approximately cancel the second term in (3.3) in agreement with the previous discussion.

Assuming the bias current is correctly adjusted as discussed above, the voltage BN at the amplifier output will be able to compensate for approximately all process and temperature variations influencing the threshold voltage of transistors matched in size with the diode connected transistor of figure 3.3. This compensation scheme

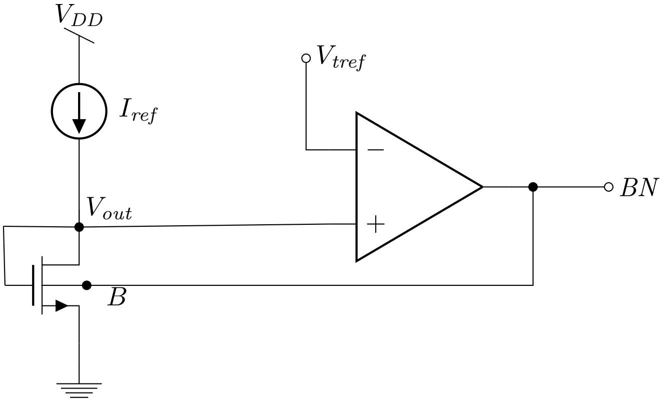

Figure 3.3: NMOS threshold compensation circuit.[29]

may therefore be efficient in systems containing a large number of matched transistors, such as digital systems, and its efficiency will be tested out on a thirteen stage inverter based ring oscillator. Figure 3.5 depicts the circuit model for compensating variations in PMOS–transistors.

3.2 PTAT Current Reference

To realise a low power current reference capable to supply the compensation circuitry with currents in the magnitude of nano amperes it is favourable to use transistors operating in weak inversion as current sources. A simple architecture achieving this with weak inversion transistors was presented already in 1977 [19]. However, this design relies on a resistor to degenerate the source of a weak inversion transistor. As the system presented in this project should focus on keeping circuit area at a minimum, the resistor was replaced by a transistor operating in the triode region. This resistorless current reference architecture was presented earlier in [30] in is shown in figure 3.6.

In figure 3.6 the PMOS–transistors form current mirros with ratios $1:1$ between P2 and P1, and $1:M$ between P2 and P3. Based on current mirror accuracy given by (2.30), all transistors are saturated and operated in strong inversion, forcing equal currents, i_1, in all branches multiplied by the mirror ratios according to (2.24). Current mirror transistors N1 and N2 should be operated in weak inversion, with an aspect ratio for N2 that is K–times largen than N1. N3 operates in triode region with a low drain–source voltage and therefore replaces the resistor in [19]. The diode connected transistor N4 is saturated and generates a bias voltage V_4 to keep transistor N3 in triode region.

If we first look at the current reference core and consider N3 as a constant resistor.

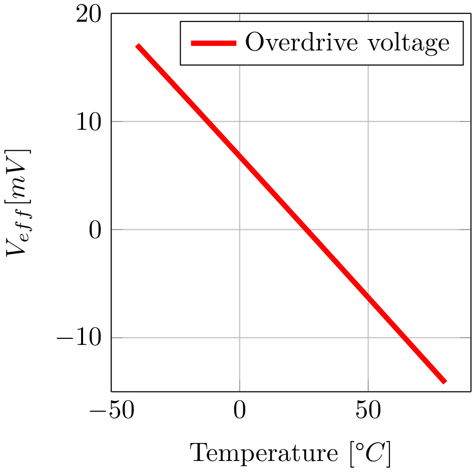

Figure 3.4: V_{eff} dependency on temperature variation with constant I_{ref}.

We have $V_{g_{N1}} = V_{g_{N2}} = V_1$ and $V_{g_{P1}} = V_{g_{P2}}$. Because N1 and N2 both are in weak inversion their drain current can be described by (2.5), and the source voltage of N2, V_3, can be expressed as shown in equation (3.5).

$$V_3 = V_T \ln\left(\frac{S_{N2}S_{P1}}{S_{N1}S_{P2}}\right) \approx V_T \ln(K) \tag{3.5}$$

This equation (3.5) form the base of the PTAT current reference, as the thermal voltage V_T is proportional to temperature and multiplied by a constant which is decided by dimensions in the current mirror transistors, S_{N1}, S_{N2}, S_{P1} and S_{P2}. As long as N1 and N2 is kept in weak inversion, V_3 is independent of current level.

Reference current i_1 can now be defined by the resistance that is source degenerating transistor N2. This leads to $i_1 = \frac{v_3}{R}$, and with R being the equivalent resistance of transistor N3 in triode region given by equation (2.14) i_1 is given by eqation (3.6).

$$i_1 = n\mu_n C_{ox} S_{N3}\left(V_4 - V_{tn} - \frac{n}{2}V_3\right) V_3 \tag{3.6}$$

Where n is for correction due to low drain–source voltage V_3 over N3 [30]. From this equation we can see that V_4, which is the voltage over the diode connected transistor N4, decides the equivalent resistance of the triode transistor. This voltage is given by current through N4. This current is mirrored by P2 and P3 and is therefore equal to Mi_1. N4 is saturated and operating in strong inversion, so its drain current is expressed by the square law equation (2.4) and voltage V_4 can be expressed as follows (3.7).

$$V_4 = V_{tn} + \sqrt{\frac{2Mi_1}{\mu_n C_{ox} S_{N4}}} \tag{3.7}$$

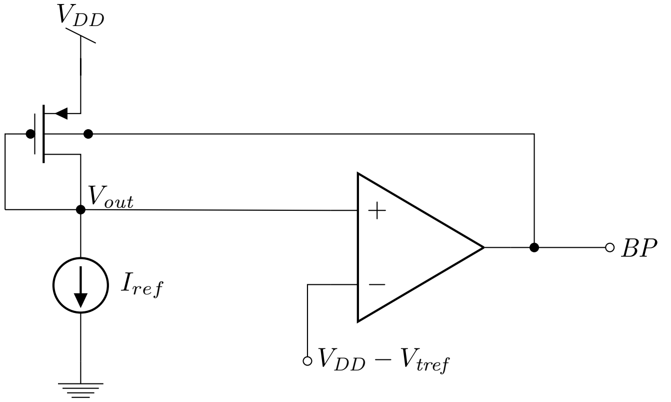

Figure 3.5: PMOS threshold compensation circuit.[29]

By inserting this equation and equation (3.5) in (3.6) we obtain a new expression i_1' in equation (3.8).

$$i_1' = n\mu_n C_{ox} S_{N3} \left(\sqrt{\frac{2Mi_1}{\mu_n C_{ox} S_{N4}}} - \frac{n}{2} V_T \ln(K) \right) V_T \ln(K) \tag{3.8}$$

As we can see, the reference current is now expressed by a bit more complex equation. This comes from adding the network of triode and bias transistors to realise a resistor. From [30] we have a closed form solution for equation (3.8) which is given in equation (3.9).

$$i_1 = n^2 \mu_n C_{ox} V_T^2 K_{eff} \tag{3.9}$$

where

$$K_{eff} = \left(K_2 - 0.5 + \sqrt{K_2 (K_2 - 1)} \right) \ln^2(K) \tag{3.10a}$$

$$K = \frac{S_{N2} S_{P1}}{S_{N1} S_{P2}}, K_2 = \frac{S_{N3} M}{S_{N4}} \tag{3.10b}$$

Equation (3.9) for the PTAT–current source have the same temperature depencies as equation (3.4), which is the current needed to approximately cancel the second term in equation (3.3). As K_{eff} given in equation (3.10a) is a function of transistor dimensions $S = \frac{W}{L}$ given in equation (3.10b), it should be possible to design the PTAT current source so that its output current (3.9) matches equation (3.4), making the diode connected transistor in figures 3.3 and 3.5 insensitive to temperature variaions other than that of the threshold voltage.

An advantage of this circuit is that the reference current is not dependent on threshold voltage, but proportional to more robust properties as transistor dimensions and thermal voltage. However, as the triode transistor $n3$ that defines the

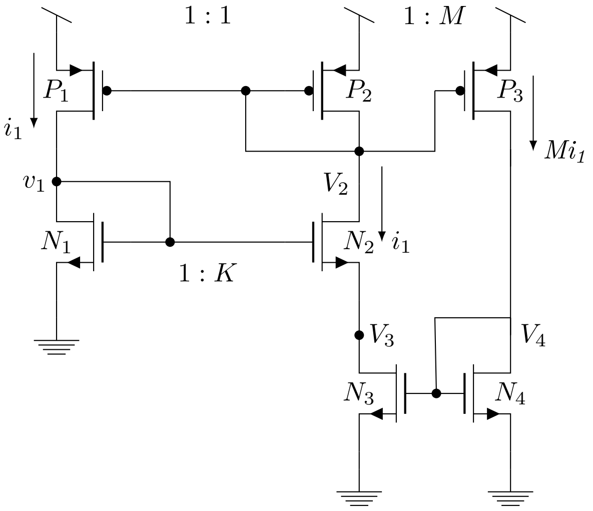

Figure 3.6: PTAT current reference.

reference current is biased by the voltage drop over $n4$, which again is decided by the reference current, we have a feedback loop. It is therefore needed to identify the loop gain of this feedback system to ensure that stable behavior of the current reference is achieved. As we operate on relatively low frequencies, a low frequency small signal circuit model of the current reference is used to calculate the loop gain. This equivalent circuit is shown in figure 3.7.

The loop gain is calculated as discussed in section 2.4. By breaking the feedback loop of the current reference at the gate of transistor P3, which at low frequencies have infinite input impedance, the output is also terminated by infinite impedance, which simplifies loop gain calculations. r_{ds} of P1, P3 and N2 are removed as the dominating impedance connected to these nodes is the impedance of the diode connected transistors P2, N1 and N4. This is because the impedance in these nodes is a result of the parallell connection $\frac{1}{g_m}||r_{ds}$ and $r_{ds} >> \frac{1}{g_m}$, which yields $r_{eq} \approx \frac{1}{g_m}$. The PMOS current mirrors ensure equal currents in all branches, only adjusted by mirroring factor, and is represented as voltage controlled current sources. These current sources are controlled by the input voltage v_i to the gate of current mirror transistor P3 and the transconductance of $p2$ multiplied by mirror factor and is given in equation (3.11).

$$i_1 = v_i\, g_{mp2} \tag{3.11}$$

The triode transistor is represented by a resistor $\frac{1}{g_{ds3}}$, with g_{ds3} given in equation (3.12a), which is controled by the voltage v_4 over diode connected transistor $n4$ given in equation (3.12b).

$$g_{ds3} = \beta_3 v_4 \tag{3.12a}$$

$$v_4 = \frac{M i_1}{g_{m4}} = \frac{M v_i\, g_{mp2}}{g_{m4}} \tag{3.12b}$$

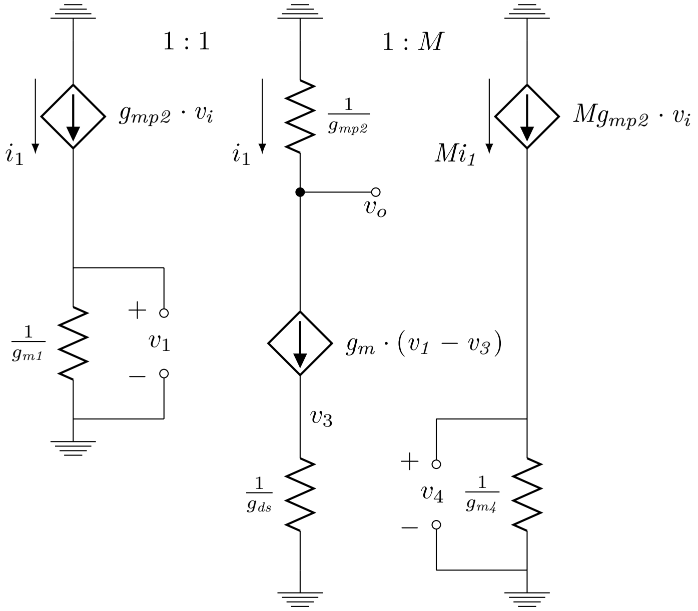

Figure 3.7: small signal equivalent circuit of PTAT current reference.

In equation (3.12a), $\beta = \mu_n C_{ox} \left(\frac{W}{L}\right)_{N3}$. Transistor N2 operating in weak inversion is represented as a voltage controled current source. Because of this current we can express the output voltage v_o as shown in equation (3.13), where the mirroring factor between N1 and N2 results in $g_m = Kg_{m1}$.

$$v_o = -\frac{g_m}{g_{mp2}}\left(v_1 - v_3\right) = -\frac{Kg_{m1}}{g_{mp2}}\left(v_1 - v_3\right) \tag{3.13}$$

In equation (3.13), voltages v_1 and v_3 is obtained by the current through resistors $\frac{1}{g_{m1}}$ and $\frac{1}{g_{ds3}}$. By using equations By inserting (3.11), (3.12a) and (3.12b), resulting voltages v_1 and v_3 is given in expression (3.14a) and (3.14b).

$$v_1 = \frac{i_1}{g_{m1}} = \frac{v_i g_{mp2}}{g_{m1}} \tag{3.14a}$$

$$v_3 = \frac{i_1}{g_{ds3}} = \frac{v_i g_{mp2}}{\beta_3 v_4} = \frac{v_i g_{mp2} g_{m4}}{\beta_3 M v_i g_{mp2}} = \frac{g_{m4}}{\beta M} \tag{3.14b}$$

By inserting these expressions into (3.13), the following expression for output voltage is obtained (3.15).

$$v_o = -\frac{Kg_{m1}}{g_{mp2}}\left(\frac{v_i g_{mp2}}{g_{m1}} - \frac{g_{m4}}{\beta_3 M}\right) \tag{3.15}$$

The resulting loop gain $-\frac{v_o}{v_i}$ is given in equation (3.16).

$$LG = -\frac{v_o}{v_i} = -\frac{g_{m1} g_{m4}}{\beta_3 M g_{mp2}} \tag{3.16}$$

Equation (3.16) reveals that there is positive feedback in the feedback loop of the current reference in figure 3.6. Therefore it is important to ensure that transistors are sized so that the loop gain of equation (3.16) is less than one, $LG << 1$, so that the circuit stabilises and we get a stable reference current. With this condition satisfied, the current will rise until a point of equilibrium. Sizing for a stable loop gain should be achievable. Transistor N1 is in weak inversion and according to (2.9b) $\frac{g_{m1}}{i_1}$ is therefore around $30 - 35$. g_{m4} and g_{mp2} on the other hand might be around three times smaller as transistor N4 and P2 is operated in strong inversion according to (2.9a) and yielding a $\frac{g_m}{i_1}$ around $10 - 12$. It is therefore fair to assume a loopgain less than one $LG < 1$ as $\beta = 2\mu_n C_{ox}\frac{W}{L} > \frac{g_m}{V_{eff}}$ and $M > 1$, where $\beta \approx 20 g_m$ for an overdrive voltage of $V_{eff} \approx 100mV$.

3.3 Amplifier design

The amplifier in this project was designed with focus on low power consumption, high gain and maximum signal swing. Transistor operation was reviewed in section 2.2, and weak inversion is favourable when low power consumption has a high priority. Operating a transistor in weak inversion also gives the highest transconductance normalised to current, which means highest power effiency for a given capacitive load and given current. A transistor in weak inversion becomes saturated for a drain–source voltage larger than a few thermal voltages [19], which means weak inversion results in wider signal swing for a given topology than strong inversion. According to equation (2.12), it can be shown that maximum gain is achieved in weak inversion. This gain may become very large when using very low currents in long transistors. From section 2.5.2 equation (2.32), it can be seen that offset between transistors in a differential input pair is minimised in weak inversion.

Trade–offs when operating transistors in weak inversion are, according to equation (2.31), high mismatch in current mirrors, and that it is not possible to achieve a very high frequency of operation. Also, when using very long transistors to achieve high gain, the result is severely reduced operational frequency as the frequency (2.10) decline with the length squared. Because of the slow rate of change in temperature and process variations, a low unity gain frequency is a tolerable tradeoff and the amplifier was designed with transistors operating in weak inversion. As the FDSOI–technology features reduced leakage, the amplifier was designed for a bias current of $50pA$ in each stage, meaning $25pA$ in each input branch and $50pA$ for the output stage. I_{bias} supply the amplifier with $25pA$, which is mirrored by a factor of 2 to each stage.

Figure 3.8 show the two–stage miller amplifier used in the compensation circuit. The main design of this two–stage miller amplifier was performed during the specialisation project that this thesis is based on, and the design methodology is given in appendix A. Its schematic 3.8 and a table 3.1 with transistor sizes are repeated here for convenience.

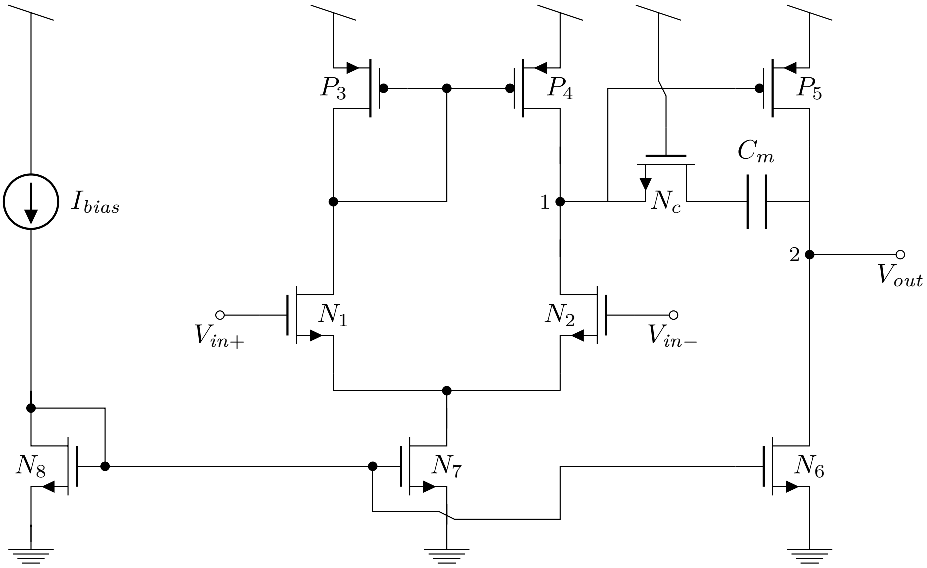

Figure 3.8: Implemented two-stage amplifier[29]

Table 3.1: Amplifier paramteres

Element	**Type**	**Width** *(nm)*	**Length** *(nm)*	**M-factor**
N_1	EG–LVT–NMOS	160	1800	1
N_2	EG–LVT–NMOS	160	1800	1
P_3	EG–RVT–PMOS	640	1500	1
P_4	EG–RVT–PMOS	640	1500	1
P_5	EG–RVT–PMOS	640	1500	1
N_6	EG–LVT–NMOS	160	1800	1
N_7	EG–LVT–NMOS	160	1800	2
N_8	EG–LVT–NMOS	160	1800	1
N_c	EG–LVT–NMOS	160	1200	1

Transistors annotated with EG in table 3.1 are I/O–transistors.

3.3.1 Amplifier layout

In order to do a more extended verification than simulation of schematic transistor models, a layout was made of the amplifier. As the amplifier operates with very small currents, there exists a possibility that leakage currents in the amplifier are larger than this current, making the amplifier useless. By making a layout of the amplifier, one can run simulations on a netlist extracted from this computer model of the amplifiers physical layout, which includes more parasittical effects than schematic models that can influence the performance. With such an extracted netlist, leakage currents will be better represented, as extra parasittic capacitances are included, and also the bulk leakage is modelled, which is not the case for transistor schematic models. Low area was prioritised when making the layout of the amplifier. The finished layout can be seen in figure 3.9. The area is approximately $252\mu m^2$ for the amplifier layout in figure 3.9. The capacitor used in layout was designed prior to this project. This layout is not tape out ready, as there has not been laid out any dummy devices and dummy layers to create equal border conditions, nor any other measures for reducing systematic mismatch has been taken.

3.4 Ring Oscillator

Oscillators are circuits generating a pulse without the need of an input. A popular choice for digital output MOSFET–oscillators are ring oscillators. Ring oscillators are widely used as on–chip clocks for microprocessors, memory circuits and some communication systems as they generate a quadratic pulse suitable for digital systems. They are also used in some circuits characterising process, random and temperature variations as their frequency of oscillation is highly dependant on parameters vulnerable to these variations [5].

Ring oscillators are implemented by connecting an odd number of inverters in a feedbackloop. Inverters are gain elements, and from section 2.4 we know that for oscillation to happen for amplifiers with feedback, there must be sufficient phase shift through the inverters, $\angle LG(\omega) = -180°$, resulting in a total phase shift of 360° around the loop. This phase requirement ensure positive feedback, furthermore one needs sufficient gain for the circulating signal to grow $|LG(\omega)| = 1$. If only one inverter is used we only achieve 90° phase shift, which makes it inherently stable. If only two inverters are used, each one provides 90° phase shift, but this is at frequencies of $\omega = \infty$ where there is no gain. Therefore an odd number of $n \geq 3$–inverters are needed to achieve sufficient gain and phase shift.

Figure 3.10 show a three stage inverter based ring oscillator. Assuming it is oscillating and node Y makes a transition to 0 as a result of node X being 1, node Z will with a small delay transition to 1. Because of the feedback loop, Z = 1 will cause a delayed transition at node X to 0 and we will have an ongoing selfsupporting

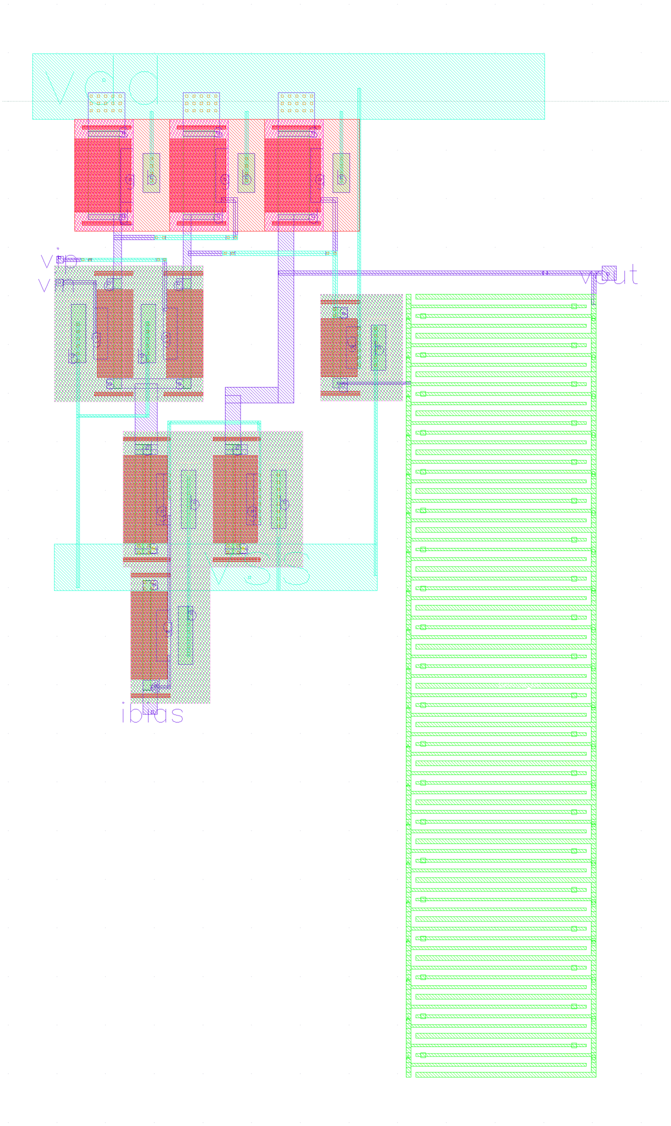
vdd
vin
vip
vout
vss
ibias

Figure 3.9: Layout of two–stage miller amplifier.

oscillation. The initial 0 at node Y propegates through all inverters and back to Y in half a period $\frac{T_0}{2}$ defined in equation (3.17a), leading to an expression for the oscillation frequency in (3.17b) [11].

$$\frac{T_0}{2} = nT_d \tag{3.17a}$$

$$f_0 = \frac{1}{T_0} = \frac{1}{2nT_d} \tag{3.17b}$$

T_d is the propagation delay, delay between input and output signals, of an inverter and n is the number of inverters in the ring oscillator. Propagation delay of an inverter is the average of propagation delay through both NMOS and PMOS, which is the time it takes to charge/discharge half of the load capacitance. If both NMOS and PMOS are sized to have equal gate delays, so rise time equals fall time, the propagation delay of an inverter is given in equation (3.18) [31].

$$T_d = \frac{1}{2}\left(T_P + T_N\right) \approx \frac{C_L V_{DD}}{\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{DD} - V_{ti}\right)^2} \tag{3.18}$$

This equation (3.18) show progagation delay through an inverter supplied by a voltage. It can be seen that the delay is depends on the threshold voltage squared and depends linearly on mobility. Using a voltage supply for the ring oscillator might therefore be unsuitable as these two parameters suffer highly from temperature and other variations as shown in section 2.5. If the ring oscillator is supplied by a current as shown in figure 3.10 the propagation delay of an inverter can be rewritten as in equation (3.19).

$$T_d \approx \frac{C_L\left(V_{ti} + \sqrt{\frac{2I_{sup}}{\beta_i}}\right)}{I_{sup}} \tag{3.19}$$

In (3.19) V_{ti} and β_i are averaged threshold voltages and $\beta = \mu_i C_{ox}\left(\frac{W}{L}\right)$ between the NMOS– and PMOS–transistors of one inverter in the ring oscillator. C_L is the capacitance loading each inverter stage and is a combination of parasittic capacitances, e.g. wiring capacitance, drain–bulk capacitances in the inverter and gate–source capacitance of the following inverter stage. The oscillation frequency can now be expressed by inserting (3.19) into (3.17b) resulting in equation (3.20).

$$f_0 \approx \frac{I_{sup}}{2nC_L\left(V_{ti} + \sqrt{\frac{2I_{sup}}{\beta_i}}\right)} \tag{3.20}$$

From section 2.5.3 we have that both threshold voltage and mobility μ_i decrease with temperature. From equation (3.19) and (3.20) we see that for low currents, temperature variations in V_{ti} will dominate and the delay will decrease with temperature, which in turn will increase the frequency. If the current is increased, the expression $\sqrt{\frac{2I_{sup}}{\beta_i}}$ will dominate. This expression will cause the delay to increase with temperature, decreasing the frequency as temperature rises. It should therefore be possible to tune I_{SUP} so that for a given temperature the temperature dependencies of these two expression cancel eachother out. The bias point for this to happen is called *zero temperature coefficient*–point [26]. Most of the temperature variations in the threshold voltage should be cancelled by the compensation circuit, but ring oscillators are nonlinear unstable circuits, and unwanted effects might occur so that second order effects may influence the temperature dependency of the threshold voltage. A zero temperature coefficient bias point should be investigated in simulations and the supply current should therefore be chosen for this point.

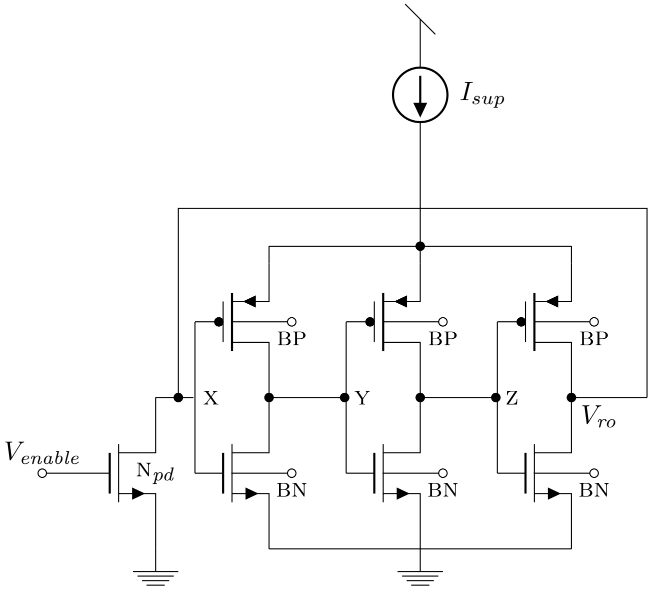

Figure 3.10: Ring oscillator with 3 inverters.

Figure 3.10 show the type of ring oscillator implemented in this project in a reduced version with only three of thirteen stages. Transistor N$_{pd}$ is a pull down transistor to control the ring oscillator. Terminals BP and BN on the transistors are connections to the bulks of transistors, where the threshold compensation voltages are applied. V_{ro} symbolises the clock signal generated by the ring oscillator.

In order to test the effectivity of the compensation circuit, the ring oscillator was designed with small transistor sizes as large sizes might help in reducing process variation [5]. NMOS and PMOS in the ring oscillator was designed to have equal strength so that gate delays are approximately equal and the approximation of inverter propagation delay (3.19) fholds. By assuming parasittic capacitance to be approximately $C_L = 1fF$ the supply current was chosen to be $I_{sup} = 1\mu A$. NMOS was chosen to be a reference transistor because its electron mobility is higher than hole mobility in PMOS–devices. From simulations, the device length was chosen to be $100nm$, giving a threshold voltage of $\approx 390mV$. β was extracted to be $\approx 60\mu$ from simulation models. PMOS was matched to NMOS by choosing equal device lengths for PMOS–devices and increasing its width to achieve approximately equal threshold voltage and β. LVT–devices was used for both NMOS and PMOS, with gate lenghts of $100nm$ and widths of $80nm$ and $402nm$ for NMOS and PMOS respectively. The estimated delay of an inverter stage was then calculated to be $T_d \approx 572.6ps$ by using equation (3.19), which results in a oscillation frequency of $f_0 \approx 67.2MHz$ for thirteen inverter stages $n = 13$ by using (3.20).

3.4.1 Ring oscillator layout

The limitations for the compensation circuitry are large leakage currents that might occur due to diodes between the different doped wells as seen in figure 2.4 and discussed in section 2.2.2. There will be leakage currents if these diodes become forward biased or if they break down. These two scenarios define the range of applicable bulk bias voltages. In order to properly model these leakage currents a layout of the ringoscillator had to be made, as the well diodes are not present in schematic models of the transistors. To provoke these diodes when extracting the netlist from layout, extra modelling layers for the different wells was needed. PMOS and NMOS was also laid out in different deep N–wells, in order to extend the range of reverse body bias which is needed when the threshold voltage has decreased for high temperatures. From figure 2.4 we see a diode between the N–well of the NMOS and P-well of the PMOS when they both lie in the same deep N–well. This diode becomes forward biased for a voltage difference of approximately $200mV$–$300mV$ between P–well and N–well, which means the reverse body bias is restricted to a minimum of $-100mV$ for NMOS and maximum $100mV$ for PMOS–transistors. Another measure one can take in order to prevent forward biased well diodes is to apply a positive voltage to the deep N–well to provide a large reverse bias for the well diodes, which may extend the range of applicable bulk bias voltages. One drawback of separating devices in different deep N–wells is increased area as they need to be separated by a minimum distance in layout. The finished layout can be seen in figure 3.11. The area is approximately $145\mu m^2$ for the ring oscillator layout in figure 3.11.

3.5 Compensation of ring oscillator

To achieve good compensation of variations in the ring oscillator, the compensation circuitry from section 3.1.1 must be tailored and optimised for this. This means that the diode connected NMOS and PMOS–transistors sensing variations as shown in figure 3.3 and 3.5 respectively must be matched to NMOS and PMOS–transistors in the ring oscillator inverter–stages. Individual compensation circuitry is needed for every type of transistor, as the compensation relies on the equality and matched

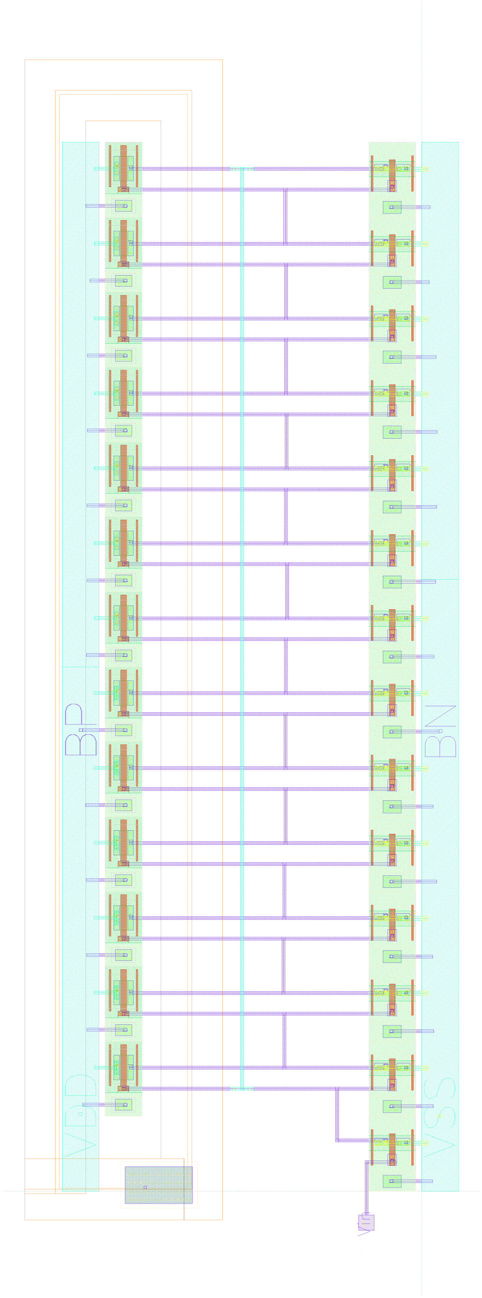
BP
VDD
BN
VSS

Figure 3.11: Layout of inverter based ring oscillator with 13 stages.

properties between the diode connected transistor and transistors being compensated. This means that this compensation scheme is most suitable for system with many repetitive matched instances, as the cost of overhead in this case is less.

The sizes for NMOS and PMOS–transistors in the ring oscillator was given in section 3.4 to be $\frac{W}{L}_n = \frac{80nm}{100nm}$ and $\frac{W}{L}_p = \frac{402nm}{100nm}$, which results in the same size for the diode connected transistors in 3.3 and 3.5 respectively. When these sizes are decided upon, the bias current from the ptat current reference in section 3.2 is fitted so that the expressions from equation (3.4) and (3.9) are equal and the temperature dependence of the voltage drop over the diode connected transistors in 3.3 and 3.5 only relies on that of the threshold voltage. The resulting temperature dependant expression for V_{out} can then be expressed as (3.21).

$$V_{out} = V_{t0}\left(T_0\right) + \alpha_{V_{t0}}\left(T - T_0\right) \tag{3.21}$$

Where the threshold voltage temperature dependence is taken from (2.33b). This variation, along with process variation, will be compensated by the amplifier and feedback loop in figures 3.3 and 3.5 and the compensation voltages BN and BP will be applied to bulk connections of transistors in the ring oscillator shown in figure 3.10. Large transistors were used in the current reference to minimizing process and random variations according to section 2.5, and resulting sizes for the current references are listed in tables 3.2 and 3.3.

Table 3.2: NVTCTRL current reference transistor sizes

Element	**Type**	**Width** *(nm)*	**Length** *(nm)*	**M-factor**
N_1	LVT–NMOS	2800	130	1
N_2	LVT–NMOS	2800	130	5
N_3	LVT–NMOS	300	1992	1
N_4	LVT–NMOS	200	1100	2
P_1	LVT–PMOS	200	2000	1
P_2	LVT–PMOS	200	2000	1
P_3	LVT–PMOS	200	2000	4

Table 3.3: PVTCTRL current reference transistor sizes

Element	**Type**	**Width** *(nm)*	**Length** *(nm)*	**M-factor**
N_1	LVT–NMOS	3000	130	1
N_2	LVT–NMOS	3000	130	7
N_3	LVT–NMOS	326	2280	1
N_4	LVT–NMOS	202	1205	2
P_1	LVT–PMOS	200	1800	1
P_2	LVT–PMOS	200	1800	1
P_3	LVT–PMOS	200	1800	4

The loop gain of the feedback loop in figure 3.3 will be the feed forward systems gain multiplied by the feedback networks gain. This gain can be found by breaking the loop at the bulk connection of the diode connected transistor and perform the method described in section 2.4. In this case, the feed forward system is the two–stage miller amplifier and the feedback network is the diode connected transistor. The input impedance is infinite, the bulk connection has infinite input impedance, and the feed forward system is terminated by the same impedance. By adjusting the small signal model in figure 2.3 to fit a diode connected tranistor, and then calculating $\frac{v_{ds}}{v_{bs}}$, we multiply the result with equation A.2 which is the gain of the two–stage miller amplifier in figure 3.8. Resulting loop gain is given in equation 3.22.

$$LG = -\frac{BN}{V_{bs}} = \frac{g_{m1} g_{m5} g_{mb} \left(r_{ds2} || r_{ds4}\right) \left(r_{ds5} || r_{ds6}\right)}{g_{m,diode} + \frac{1}{r_{ds,diode}}} \tag{3.22}$$

Equation (3.22) of the loop gain show that at low frequencies, the feedback loop is stable. If the amplifier gain is high enough, the systems closed loop gain is decided by the feedback network gain, resulting in $A_{cl} \approx \frac{1}{\beta} \approx \frac{g_{m,diode} + \frac{1}{r_{ds,diode}}}{g_{mb}}$ where $g_{mb} = \frac{d(i_d)}{d\left(V_{bs}\right)}$ is the body transconductance.

4 | Results and discussion

This chapter presents the achieved results for circuits presented in the design chapter, and results will be continuously discussed as they are presented. Results were obtained by simulations executed with Spectre. Simulations of modules with layout were executed on a netslist containing parasitics extracted from layout. Both resistive and capacitive parasitics were extracted from the layout, and netlist extraction was performed with Cadence QRC extraction.

Process variations were simulated with transistor corner models as discussed in section 2.5.1. Seven different corners were used, TT, SS, FF, FFA, SSA, FSA and SFA, and an illustration of their spread relative to the typical corner TT is shown in figure 2.10. Performance for different temperatures were performed with both doing a DC–sweep of temperature and running transient simulations at different temperatures. The temperature range used in this project is from $-40°C$ to $80°C$, and when results are presented in tables T_0 represents room temperature at $25°C$ and T represents simulation the whole temperature range. Results are presented with the typical corner TT as a reference point, best case results are denoted BC and worst case results WC. Testing for random variations was performed with Monte Carlo simulations.

First, results for different modules in the compensation circuit is presented individually and discussed before the compensation circuit is presented all together. Lastly, results from ring oscillator simulations, with and without compensation, is presented and discussed. It is taken for granted that the reader is familiar with chapter 3.

4.1 ptat current reference

Figure 4.1 and 4.2 show simulation results of the PTAT–current reference presented in 3.2, where figure 4.1 correspond to the current reference of table 3.2 fitted for NMOS–transistors and figure 4.2 correspond to the current reference of table 3.3 for PMOS. Both plots are results from DC–sweeps over temperature for all corners, and the resulting currents show proportional to temperature behavior PTAT. Figure 3.6 is the reference when addressing instances in the current reference throughout the discussion.

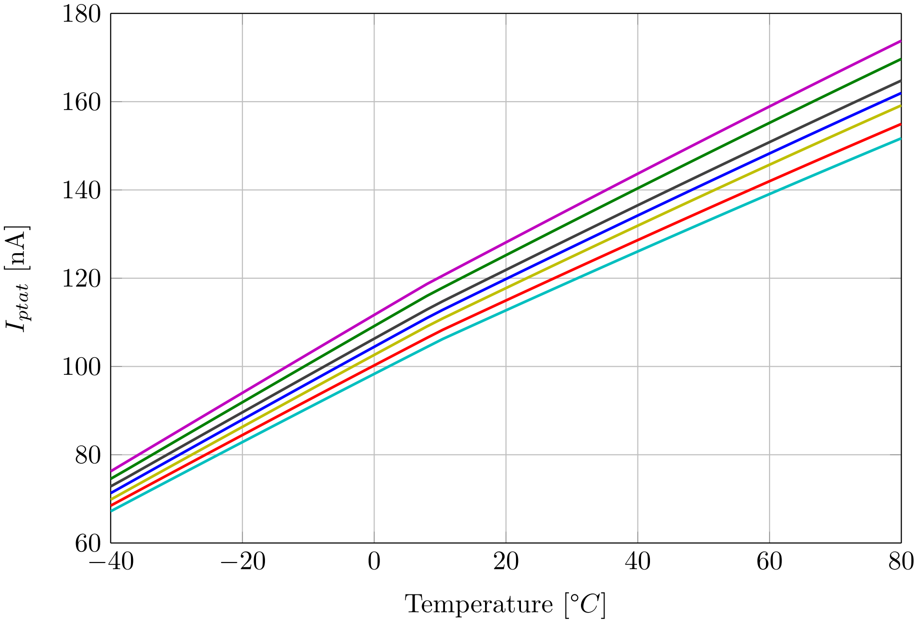

Figure 4.1: Corner variation of PTAT current reference for NMOS compensation.

In both figure 4.1 and 4.2, the blue curve corresponds to typical corner TT. A summary of key results for the PTAT current references are given in table 4.1. In table 4.1, ΔI_{ptat} is calculated as the difference between maximum and minimum current across corners at a given temperature, and percentage is relative to the typical corner at the same temperature. Results are given for room temperature $T_0 = 25°C$, $T = 80$ and $T = -40°$ As we can see, even though transistors in the current references were sized rather large, variations across corners are quite substantial for both references, and it is at its worst for high temperatures. One reason for this may be that threshold voltages are decreasing with increasing temperature, so that small threshold voltage variations might have a larger overall impact on these lower threshold voltages than for higher thresholds at low temperatures.

As the triode transistor N3 establishes the reference current, its bias voltage generated in diode connected transistor N4 should be kept stable across corners. To reduce variations, the size of N4 was increased, which led to an proportional increase of current in this branch in order to maintain equal I_{ptat} for the compensation circuit. These increased transistor dimensions led to a proportional increase in power consumption. Evidently, power consumption is highest at high temperatures, because of the PTAT current. From table 4.1 we see that the current reference designed

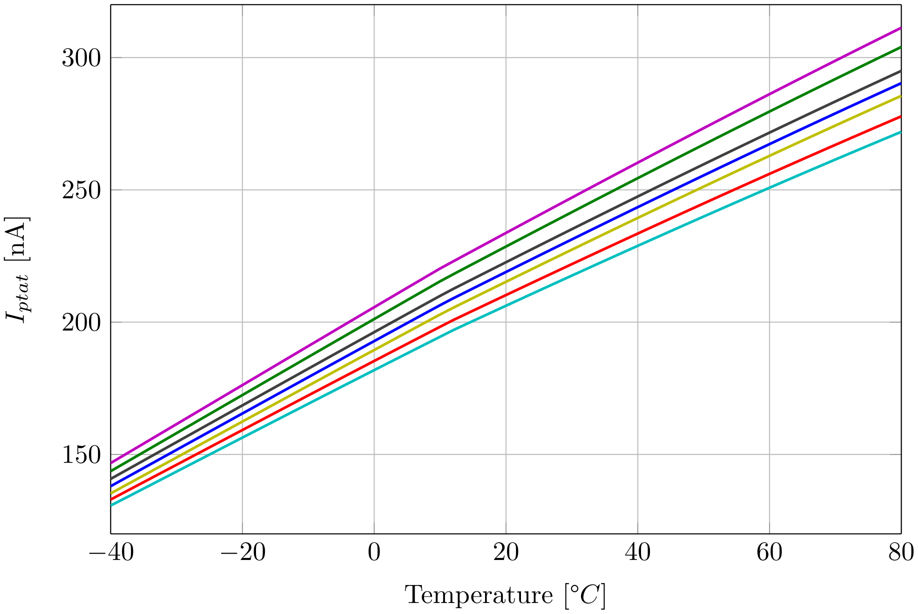

Figure 4.2: Corner variation of PTAT current reference for PMOS compensation.

for PMOS–compensation has almost twice the power consumption to its NMOS counterpart. One of the reasons for this is that the variation sensing PMOS–transistor has a higher threshold voltage than the variation sensing NMOS. One measure that can be taken to reduce the power consumption is to design this current reference for very low currents, as demonstrated in [30], then adjust and multiply this low current with current mirros to the output in order to obtain the PTAT current needed. In [30], the reference current generated is between $6nA$ to $15nA$, which would reduce the power consumption by a factor of ≈ 5–10. Some extra power consumption would of course be added to scale and trim this current.

Table 4.1 also show that the loop gain for both references are below 1. Both references had a small variation in loop gain across corners which was about $\Delta LG \approx \pm 0.03\frac{V}{V}$. This meas that the reference is stable for all corners and the assumption made in section 3.2 that it was possible to design for a loop gain in equation (3.16) less than 1 is valid. The temperature coefficient show the rise in current per °C increased.

4.1.1 Mismatch

Table 4.2 show results from 60 Monte Carlo simulations for both current references. These results give further indication that the current references robustness are poor, as already proved by corner simulations in the previous section. In table 4.2, the

Table 4.1: Results of PTAT current reference for NMOS and PMOS compensation circuits.

Parameters	NMOS–reference	PMOS–reference
I_{ptat}TT@T_0 [nA]	123	225
I_{ptat} TT @$T = -40°C$[nA]	71	138
I_{ptat} TT @$T = 80°C$[nA]	162	290
Temperature coefficient $\frac{nA}{°C}$[nA]	0.755	1.26
ΔI_{ptat}@T_0 all corners [nA]	15.95 (12.9%)	28.5 (12.65%)
ΔI_{ptat}@$T = -40°C$ all corners [nA]	9.04 (12.7%)	16.1 (11.65%)
ΔI_{ptat}@$T = 80°C$ all corners [nA]	22.1 (13.64%)	39.34 (13.5%)
Loop gain $\frac{V}{V}$	0.789	0.751
V_{dd}	$1V$	$1V$
Power consumption TT@T_0	$854.56nW$	$1.57\mu W$
BC power consumption SSA@$T = -40°$	$447nW$	$913nW$
WC power consumption FFA@$T = 80°$	$1.208\mu W$	$2.1748\mu W$

minimum value for reference currents in both cases are $0nA$, as the NMOS–reference failed to generate a reference current in 3 out of 60 runs, and the PMOS–reference fail 1 out of 60. One could suspect weak inversion transistors N1 and N2, which generate voltage V_3 in figure 3.6, of causing variations because of weak inversions exponential relationship between drain current and threshold voltage. However, from equation (3.5) we see that voltage V_3 is solely based on transistor dimensions and temperature. It is therefore reasonable to believe that the current mirrors, along with the triode transistor and its bias voltage may be the main contributers to mismatch. One way to increase robustness is to implement the current references with digital trimming. Both current mirrors and the diode connected transistor N4 could be implemented with a trimming scheme to tune their performance and adjust bias voltage for the triode connected transistor N3.

Table 4.2: Results of 60 monte carlo runs for the PTAT current reference.

Parameters	NMOS–reference current			PMOS–reference current		
	$-40°C$	$25°C$	$80°C$	$-40°C$	$25°C$	$80°C$
Min. [nA]	0	24.5	64.3	0	134	202.2
Max. [nA]	190.1	248.5	288.2	284.1	379.3	441.7
Mean μ [nA]	68.52	122.1	162.2	136.3	225.4	290.5
Std. deviation σ [nA]	38.8	42	42.85	49.69	49.28	49.61
$\frac{\sigma}{\mu}$ [%]	56.6	34.4	26.41	36.4	21.8	17

4.2 Two–stage miller amplifier

Table 4.3 show simulation results of the amplifier schematic model presented in section 3.3, which was performed during the specialisation project in [29]. Table 4.4 show results from simulations performed on netlists extracted from layout shown in figure 3.9 of the amplifier presented in section 3.3.

Table 4.3: Results of amplifier schematic model simulations.[29]

Parameters	**Value**
Supply voltage V_{DD}	$1.8V$
Small-signal gain	$100.4dB$
Unity-gain frequency f_T	$2.536kHz$
Load capacitance	$500fF$
Miller capacitance	$40fF$
Phase Margin at unity gain	63.1°
Gain Margin	$31.21dB$
Ibias	$25pA$
Power consumption	$183.88pW$

From table 4.3 and 4.3 we see that post–layout simulations correspond quite well to simulations of the schematic design. Gain has increased $3dB \approx 3\%$, which is not a significant increase, and may be explained by resistive parasitics which are not present in the schematic models. The amplifier also show quite good noise performance with a signal to noise ratio of $57.21dB$. As one of the arguments for choosen weak inversion operation for the amplifier was that it would give increased signal swing, the amplifier was simulated with both $1V$ and $1.5V$ peak–to–peak input values, and as we can see from table 4.4 harmonic distortion is very low. It is therefore verified that the amplifier is highly linear, and can be used for a large input voltage range. The same amplifier is therefore used in both NMOS and PMOS compensation circuits, even though common mode levels are quite different.

4.3 Compensation circuit

This section presents and discuss obtained results for the compensation circuits presented in section 2.5.1, depicted in figure 3.3 and 3.5. The NMOS and PMOS transistors realising the diode connected transistor in this circuit is the same used in the ring oscillator, and simulations are performed on netlists extracted from layout.

Figure 4.3 show simulations of the threshold voltage for an NMOS–transistor across all corners and the whole temperature range from $-40°C$ to $80°C$, both with

Table 4.4: Results of amplifier post–layout simulations.

Parameters	**Value**
Supply voltage V_{DD}	$1.8V$
Small-signal gain	$103.04dB$
Unity-gain frequency f_T	$2.1kHz$
Load capacitance	$500fF$
Miller capacitance	$48fF$
Phase margin	69.23°
Gain margin	$31.2dB$
Ibias	$25pA$
Average power consumption	$188.044pW$
SNDR $V_{p-p} = 1V$	$57.21dB$
SFDR $V_{p-p} = 1V$	$71.4dB$
Total harmonic distortion $V_{p-p} = 1V$	0.028%
SFDR $V_{p-p} = 1.5V$	$57dB$
Total harmonic distortion $V_{p-p} = 1.5V$	0.175%
Monte Carlo	**Value**
Phase Margin μ	68.7°
Phase Margin σ	2.68°
Phase Margin $\frac{\sigma}{\mu}$	3.9%
Loop gain μ	$102.3dB$
Loop gain σ	$1.627dB$°
Loop gain $\frac{\sigma}{\mu}$	1.6%

and without compensation. Figure 4.4 show the same simulations for a PMOS–transistor.

Figure 3.4 showed the temperature dependence of V_{eff} for the variation sensing transistor in the compensation circuit with a constant current bias and bulk bias. This figure showed a decreasing V_{eff} as a result of equation 3.4 not being satisfied with a constant current bias. In figures 4.3 and 4.4, the PTAT–current reference from section 4.1 has been used to bias the diode connected transistors. A summary of the resulting variations from these simualations is shown in table 4.5. Threshold voltage variation for the NMOS–transistor in typical corner TT has been reduced from 16.6% to 0.23% across temperatures, while PMOS varies 0.33% from minimum to maximum temperatures. Worst case variations across both temperature and corners has been reduced from 25.2% and 30% for NMOS and PMOS respectively, down to 0.68% and 0.9%, which is ±0.34% and ±0.45% around V_{tref} at room temperature. It is hereby clear that it is possible to establish quite constant threshold voltages by using bulk biasing. As to the small inaccuracy still left, it is reasonable to think that this inaccuracy is a result of the spread in reference current across corners as shown in figures 4.1 and 4.2.

A summary of results obtained for the compensation circuits are given in table

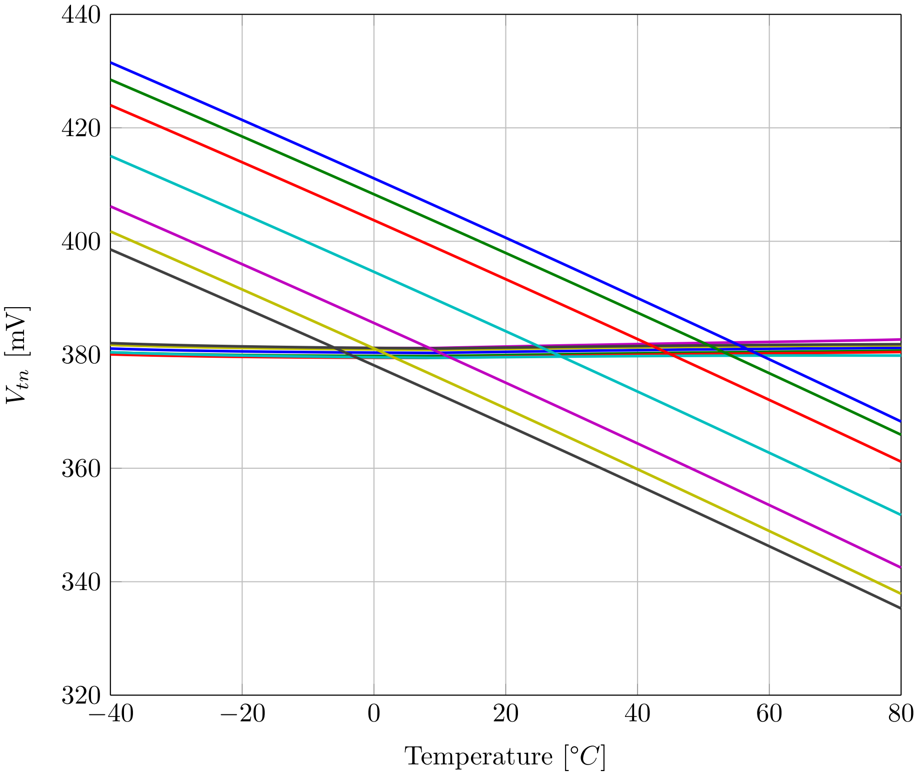

Figure 4.3: NMOS threshold voltage versus temperature and process variations, compensated and uncompensated.

4.6. Simulations show that the body transconductance g_{mb} is approximately 11.7 times smaller than g_m for the NMOS and approximately 13.5 for the PMOS in the compensation circuit. This means that the loop gain for the compensation circuit given in equation (3.22) is accurate, as resulting loop gain is the amplifier gain from 4.4 multiplied by $\frac{g_{mb}}{g_{m,diode}}$, as $\frac{1}{r_{ds,diode}} << g_{m,diode}$. This results in the amplifier gain in 4.4 being diveded by 11.7 for the NMOS–compensation circuit and 13.5 for the PMOS compensation circuit, which is reasonable close to the loop gain listed in table 4.6. Both loop gain varies less than $\pm 0.5dB$ across corners. However, the phase margin drops for both NMOS and PMOS–compensation circuits down to 54° and 58° in the SFA corner. The compensation circuit still has a good phase margin, but in order to prevent this drop, a viable solution may be to use both NMOS and PMOS transistors instead of only transistor N_c in figure 3.8 to provide lead compensation for the two stage miller amplifier.

The power consumption in the compensation circuit is given in table 4.6. Contributers to this figure are the current reference and amplifier, which means that the generation of V_{tref} is not included. Generation of the voltage reference is

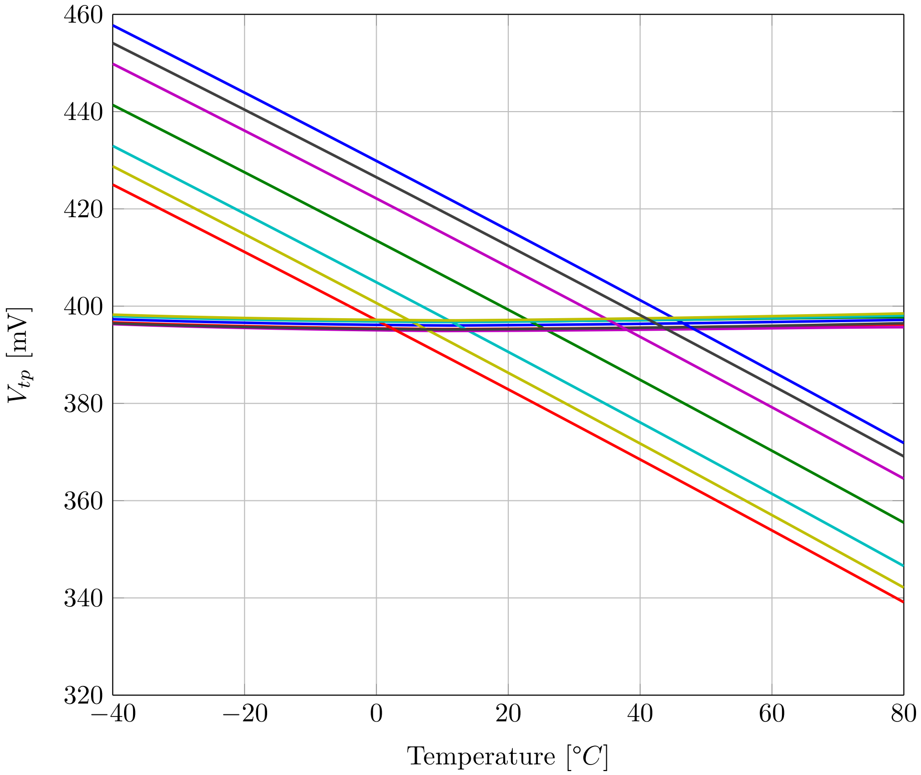

Figure 4.4: PMOS threshold voltage versus temperature and process variations, compensated and uncompensated.

therefore an additional source of power consumption when using the compensation circuit, and low power methods for this should be looked at. Power consumption in the compensation circuit is dominated by the PTAT–current reference. The amplifiers power consumption is in the order of pico watts, so its contribution compared to the current reference is very little. In section 4.1, the high power consumption of the current reference is addressed, and the author believes that it is possible to reduce this. It should also be noted that both a circuit generating V_{tref} and the PTAT–current reference can be used by other circuits on the same chip, which would divide their power consumption amongst more modules. In a scheme where the PTAT–current is generated as a small current in its source and then digitally trimmed and scaled by current mirrors, both NMOS and PMOS–compensation circuits could use the same source, as current mirrors could fit the current to the application.

Table 4.5: Variations in NMOS and PMOS–threhsold voltage.

Configuration	NMOS	PMOS
TT no comp.	63.28 (16.6%)	85.88 (21.7%)
TT comp.	0.9 (0.23%)	1.3 (0.33%)
All corners, no comp.	96.2 (25.2%)	118.6 (30%)
All corners, comp.	2.6 (0.68%)	3.6 (0.9%)

Table 4.6: Results of NMOS and PMOS compensation circuits.

Parameters	NMOS	PMOS
width $[nm]$	80	402
length $[nm]$	100	100
Vtref $[mV]$	381	396
Loop gain	$83.3dB$	$81.9dB$
Unity-gain frequency f_T	$207.25Hz$	$227.85Hz$
Phase Margin at unity gain	85.19°	94.3°
Power consumption TT@T_0	$854.72nW$	$\approx 1.57\mu W$

4.4 Compensation of ring oscillator

This section presents simulation results of the ring oscillator presented in section 3.4. Simulations were performed on the netlist extracted from layout shown in figure 3.11. As mentioned, extracted netlist contains both resistive and capacitive parasitics.

The ring oscillator layout was made to model the well–diodes as shown in figure 2.4, which are not present in schematic models, so leakage effects discussed in section 2.2.2 could be simulated in order to improve verification of the bulk biasing scheme. For these diodes to be included in the extracted netlist, layers modelling different well regions, e.g. deep n-well, and triple well structure, needed to be added in the layout. A diode created is formed in the pn–junction between the N and P–well beneath the buried oxides of the NMOS and PMOS as shown in figure 2.4. This diode put severe limitations on the reverse body bias range of the transistors. As NMOS is reverse body biased with a negative voltage, and PMOS is reverse biased with a positive voltage, one can only apply $-100mV$ to the NMOS bulk and $100mV$ to the PMOS bulk before this diode is starting to become forward biased. To overcome this problem, and prevent the diode to become forward biased, the NMOS and PMOS transistors in the ring oscillator were laid in individual deep N-wells. This isolates the N–well from the P–well. In addition, by connecting the deep N-well under the PMOS–transistor to positive supply rail, both the diode from P–well to deep N–well and the diode from P–substrate to deep N–well gets more reverse biased, extending the reverse body bias range further. One drawback with this modification is increased area, as the two different deep N–wells need to separated by a minimum distance of $2.5\mu m$, which is the reason for NMOS and PMOS in figure 3.11 being spaced far apart.

Figure show the voltage pulse generated by the thirteen stage ring oscillator, oscillating at a frequency of $65.5MHz$ with an amplitude of $526.4mV$. Properties of the ring oscillator are summarised in table 4.7.

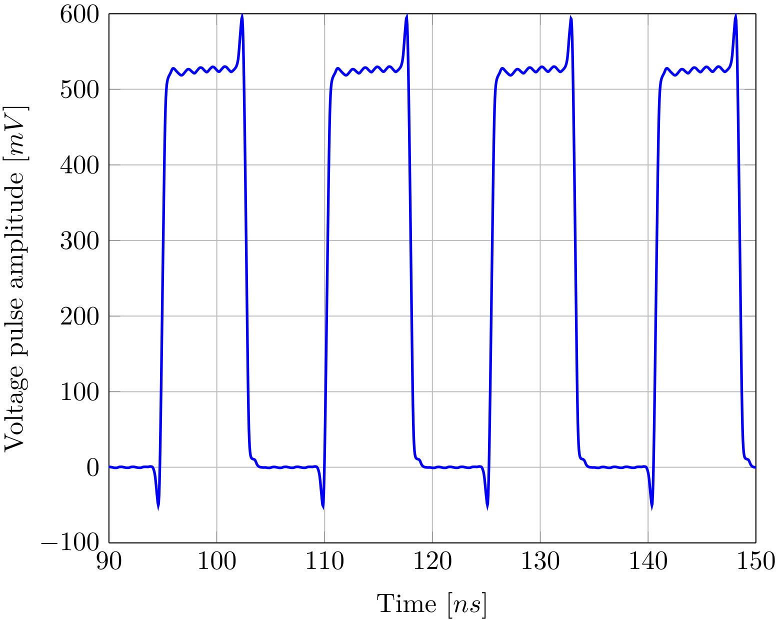

Figure 4.5: Ring oscillator voltage pulse.

As we see from table 4.7, the oscillation frequency is a bit lower than the target frequency from section 3.4. It is reasonable to believe that this decrease in frequency stems from parasitic capacitances which are not present in schematics, but appears when making layout. The supply current has been increased a bit compared to the one used for calculations in section 3.4 in order obtain minimum temperature sensistivity for the oscillation frequency, zero temperature coefficient, as discussed. Theory on zero temperature coefficient is presented in [26], and it is the point where temperature dependance of the threshold voltage and mobility cancels out for a current biased transistor. In [26] the current needed to achieve this is quite large, $192\mu A$, as V_{tn} is larger than the second term in equation (3.2), which is dependant on drain current. Note that the ring oscillator frequency is dependant on the same term (3.20), but since most of the temperature depence for the threshold voltage V_{ti} is compensated, as seen in figure 4.3 and table 4.5, it may be that this point is reached at a much lower current for the ring oscillator. Therefore, the supply current was chosen to be $1.05\mu A$, as simulations showed the frequency to decrease with increasing temperatures for higher supply currents, and increase with temperatures for lower currents. Power consumption listed in 4.7 is for the ring oscillator stand–alone, and total power consumption for the whole system should the compensation circuits, resulting in a total power consumption of $2.98\mu W$, in which the current references dominate.

Table 4.7: Resulting properties for the ring oscillator.

Parameters	**Value**
NMOS W,L	$80nm$,$100nm$
PMOS W,L	$402nm$,$100nm$
Oscillation frequency	$65.5MHz$
Number of inverter stages	13
Pulse amplitude	$526.4mV$
I_{sup}	$1.05\mu A$
Power consumption	$552.3nW$

Figure 4.6, show simulated frequency variation across corners and temperature, with a summmary of results with and without compensation listen in table 4.8.

Results clearly indicate that bulk biasing is an efficient technique for reducing variations. As seen in table 4.8 the worst case variation across all corners and the whole temperature range is 0.632%, which corresponds to a variation in frequency of ±0.3155% around the typical corner TT frequency $65.5MHz$.

By looking at temperature sensitivity alone, we see that for the typical corner, the frequency variation is 0.353% for the whole temperature range, which can be expressed as $29.4\frac{ppm}{°C}$ in parts per million. Corner SSA has the worst temperature coefficient with a variation in frequency of $47\frac{ppm}{°C}$

It is also quite reasonable to believe that the main source of error, the biggest contributer to frequency variations, is the PTAT current reference. As seen in section 4.1, the reference current varies quite a lot across corners, which might produce small offsets in the compensation circuits output voltage. However, even with a reference current that varies approximately 12% across corners, we achieve frequency variations of just 0.632%, which indicate that the compensation circuit is quite robust.

Table 4.8: Frequency variation in the ring oscillator as a result of process and temperature variations.

Parameters	VARIATION no comp. $[\Delta f]$	VARIATION comp. $[\Delta f]$
CORNERS var. $@T_0$	$3.14MHz$ (4.79%)	$72kHz$ (0.109%)
TT $@T$	$9.04MHz$ (13.80%)	$231.39kHz$ (0.353%)
WC var. $@T$	$12.247MHz$ (18.69%)	$414.5kHz$ (0.632%)

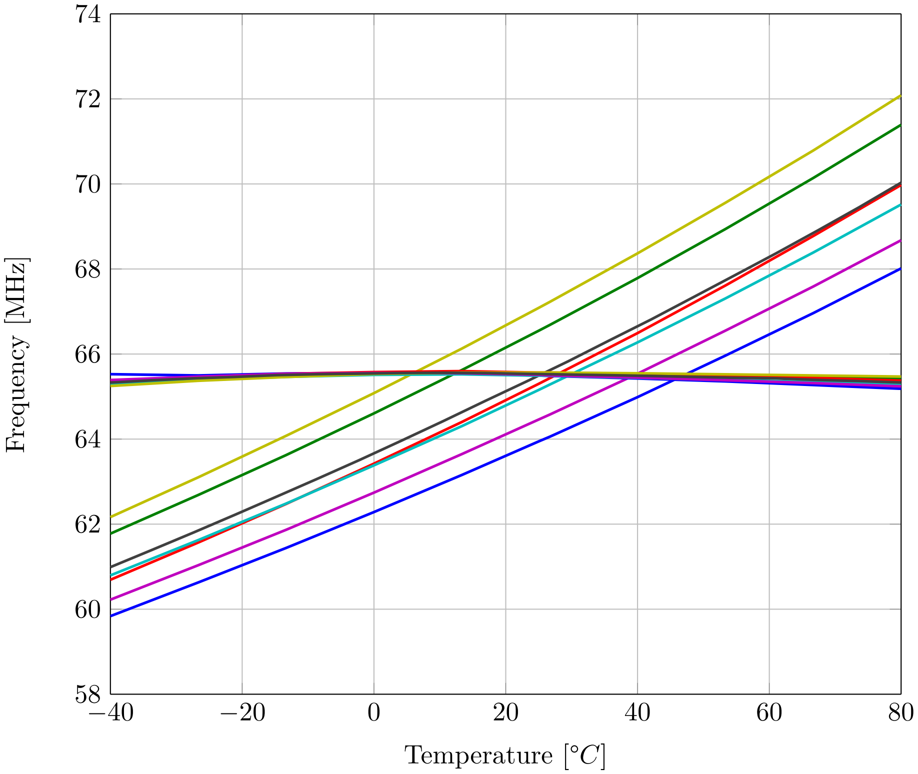

Figure 4.6: Frequency versus temperature and process variations, compensated and uncompensated.

To see how the ring oscillator behaves with a variation in supply current, it was simulated with a supply current that was temperature sensitive. Temperature sensitivity was also added to the reference voltage V_{tref} in the compensation circuits. A pessimistic temperature sensitivity of $50\frac{ppm}{°C}$ was chosen to add a little margin, as published works on both current and voltage references show a temperature which is drift of half of the chosen value [32, 33]. Simulation of the typical corner TT showed a frequency variation of $\pm 0.866\%$ from $-40°C$ to $80°C$ with temperature sensistive supply and voltage references.

During simulations, leakage currents in the reverse biased diodes, which are formed between the pn–junctions as shown in figure 2.4, were observed across temperatures. These simualtions show that the leakage currents increase with temperature and reaches a maxumim of approximately $10pA$ at $80°C$ with the compensation circuit connected, and approximately the same without the compensation circuit. As body bias increases the threshold voltage to compensate for high temperature there should be less leakage according to (2.5), however leakage components in reverse biased pn–junctions are expected to increases significantly with temperature, and therefore the author believes these leakages should be investigated more in future work. Capacitance for the ring oscillator NMOS–bulk connection were simulated to be $13.36fF$, which results in approximately $1fF$ per device. Bulk capacitance for the PMOS–connection were simulated to be approximately $18.33fF$, resulting in approximately $1.5fF$ per device. As the amplifier is designed for a capactive load of $500fF$, the NMOS–compensation circuit can compensate almos 500 devices, while the PMOS–compensation circuit can compensate approximately 350 devices.

4.4.1 Mismatch in the ring oscillator

Even though the compensation circuitry in not designed to compensate for mismatch, it is interesting to see how the system behaves, and how the ring oscillator frequency is influenced with mismatch present. Monte carlo simulations were run on the ring oscillator both with and without compensation to get a sense on how the compensation system acts under these conditions. The PTAT current reference was not a subject to monte carlo variations, as section 4.1.1 showed that this was quite sensible to mismatch, and was only simulated in the typical corner TT in this section. In a realistic scenario on chip, mismatch would be corrected by trimming the current reference.

As mentioned in section 3.4, the ring oscillator was designed with small transistors to obtain significant variation over corners. From section 2.5.2 we see that small devices also leads to increased mismatch, so the expected results from these simulations is a large spread in frequency. However, it will still be interesting to look at compensated versus uncompensated ring oscillator.

From table 4.9 it can be seen that the spread, from minimum to maximum, in frequency is signifact for both compensated and uncompensated ring oscillator runs. However, the standard deviation of the compensated ring oscillator is below half compared to that of the uncompensated ring oscillator. By observing the plots of frequency versus temperature for these 20 monte carlo simulation, it could be observer that maximum and minimum values for the compensated ring oscillator occured as unconsistent spikes for single temperature points within one monte carlo runs. As it is unlikely that the frequency will jump from $65MHz$ to $71MHz$ when changing from $T = -15°C$ to $T = -14°C$ and then back to $65MHz$ when $T = -13°C$, these inconsistent runs were removed and the 10 first monte carlo runs for both compensated and uncompensated ring oscillators are shown in figure 4.7

From 4.7 it can be seen that the compensation circuit is robust for mismatch, and temperature variations are severely reduces even in the presence of mismatch. The uncompensated vary from around $61MHz$ to $70MHz$, which is consistant with table 4.9. Figure 4.7 show that the ring oscillator with compensation has significant die–to–die variations, but within–die variations are good and can be compared with results obtained in 4.8, with a frequency variation with temperature below 0.5% for the whole range of $-40°C$ to $80°C$. The die–to–die variations can be further

Table 4.9: Results of 20 ring oscillator monte carlo runs.

Parameters	Uncompensated	Compensated
Min. [MHz]	60.58	61.76
Max. [MHz]	70.69	70.21
Mean μ [MHz]	65.41	65.8
Std. deviation σ [MHz]	2.693	1.039
$\frac{\sigma}{\mu}$ [%]	4.11	1.57

reduced by calibration, or trimming, of I_{sup}.

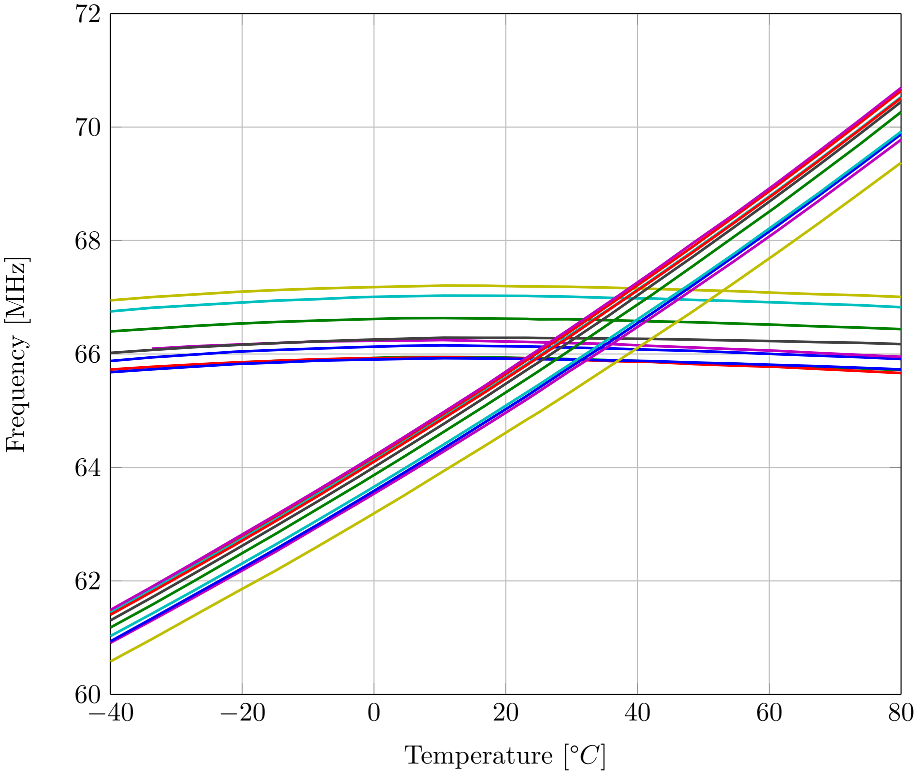

Figure 4.7: Frequency versus temperature and process variations, compensated and uncompensated, during monte carlo simulation.

5 | Conclusion

In this thesis, there has been designed a circuit compensating the threshold voltage for process and temperature variations by using adaptive body biasing in $28nm$ *Ultra-Thin Buried oxide and Body Fully Depleted Silicon on Insulator* UTBB FDSOI CMOS technology. Compensation circuitry, which has been implemented for both NMOS and PMOS transistors, were designed and optimised to be used with a 13–stage inverter based ring oscillator operating at a frequency of $65.5MHz$, in order to obtain a stable frequency across corners and temperature. The compensation circuit is realised with a feedback loop and features a highly linear low power high gain amplifier operating in weak inversion, a PTAT–current reference and diode connected transistor sensing variations.

An analysis of the temperature dependence in the compensation circuit has been made and verified by simulation. Also, an expression for the loop gain in the PTAT–current reference has been derived and analysed, as this reference contains a positive feedback loop, and its stability has been verified by simulations. A layout was made of the amplifier designed in the specialization project [29], and its operation and results has been verified by post–layout simulation. The amplifier has $100dB$ gain and highly linear, with a power consumption below $200pW$.

Results obtained for the compensated ring oscillator show a great reduction in frequency variation across both process corners and a temperature range of $-40°C$ to $80°C$ compared to the uncompensated ring oscillator, as variations was reduced from 18.69% to 0.632%. These results were achieved in spite of varitions of up to 13.5% across corners for the PTAT reference current in the compensation circuit, which may indicate that the adaptive bulk bias compensation circuit is robust. Monte carlo simulations showed a larger die–to–die spread in frequency, but within–die frequency variations with temperature were typically below 0.5%, implicating that the compensation circuit may perform well in the presence of mismatch. Compared to other published work [15, 16] on process and temperature compensated ring oscillators, the ring oscillator of this thesis performs quite well, and has less variations across process corners and temperature for both best and worst case scenarios. However, as results in this thesis are only based on simulations, even if simulations on netlists extracted from layout, they are optimistic compared to values measured on chip.

5.1 Further work

The biggest contributor to both variations and power consumption in the compensation circuit is the PTAT–current reference. It should therefore be added some effort in redesigning this in a more power efficient way, and introduce some calibration schemes to reduce the effect of mismatch in the reference current. One way to do this is to use trimming in a current mirror were the reference current is copied to the chip, were several smaller sized current mirror transistors can be switched in parallell to realise the equivalent of a wider current mirror transistor. The same can also be applied to the diode connected transistor N4 which generates a bias voltage for the triode region transistor N3.

In order to get a fully functional system, one also needs to generate voltage references for the compensation circuits. This can be done with a band gap reference and voltage regulators, low power and insensitivity to process and temperature variations should be the focus when designing these. There is also need to generate a process and temperature insensitive supply current for the ring oscillator itself.

Leakage currents in between transistor wells and substrate should also be further investigated. Even with the presence of parasitic diodes between all wells extracted from layout, the leakage current seems too low to be true.

Bibliography

[1] *How many things are currently connected to the "Internet of things" (IoT)?*, http://www.forbes.com/sites/quora/2013/01/07/how-many-things-are-currently-connected-to-the-internet-of-things-iot/. [Online]. Available: `http://www.forbes.com/sites/quora/2013/01/07/how-many-things-are-currently-connected-to-the-internet-of-things-iot/`.

[2] D. Evans, "The internet of things, how the next evolution of the internet is changing everything", *White paper, Cisco Internet Business Solutions Group (IBSG)*, no. 1, Apr. 2011.

[3] G. Moore, "Progress in digital integrated electronics [Technical literaiture, copyright 1975 IEEE. reprinted, with permission. technical digest. international electron devices meeting, IEEE, 1975, pp. 11-13.]", *IEEE Solid-State Circuits Society Newsletter*, vol. 20, no. 3, pp. 36–37, Sep. 2006, ISSN: 1098-4232. DOI: `10.1109/N-SSC.2006.4804410`.

[4] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration", *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 183–190, Feb. 2002, ISSN: 0018-9200. DOI: `10.1109/4.982424`.

[5] K. Kuhn, M. Giles, D. Becher, P. Kolar, A. Kornfeld, R. Kotlyar, S. Ma, A. Maheshwari, and S. Mudanai, "Process technology variation", *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2197–2208, Aug. 2011, ISSN: 0018-9383. DOI: `10.1109/TED.2011.2121913`.

[6] R. Gonzalez, B. Gordon, and M. Horowitz, "Supply and threshold voltage scaling for low power CMOS", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1210–1216, Aug. 1997, ISSN: 0018-9200. DOI: `10.1109/4.604077`.

[7] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture", in *Design Automation Conference, 2003. Proceedings*, Jun. 2003, pp. 338–342. DOI: `10.1109/DAC.2003.1219020`.

[8] S. Borkar, "Designing reliable systems from unreliable components: the challenges of transistor variability and degradation", *IEEE Micro*, vol. 25, no. 6, pp. 10–16, Nov. 2005, ISSN: 0272-1732. DOI: `10.1109/MM.2005.110`.

[9] K. Kuhn, "Considerations for ultimate CMOS scaling", *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012, ISSN: 0018-9383. DOI: `10.1109/TED.2012.2193129`.

[10] O. Unsal, J. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalez, and O. Ergin, "Impact of parameter variations on circuits and microarchitecture", *IEEE Micro*, vol. 26, no. 6, pp. 30–39, Nov. 2006, ISSN: 0272-1732. DOI: `10.1109/MM.2006.122`.

[11] T. C. Carusone, D. Johns, and K. W. Martin, *Analog Integrated Circuit Design.* Wiley, 2012, ISBN: 9781118092330.

[12] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits", *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003, ISSN: 0018-9219. DOI: `10.1109/JPROC.2002.808156`.

[13] D. Jacquet, F. Hasbani, P. Flatresse, R. Wilson, F. Arnaud, G. Cesana, T. Di Gilio, C. Lecocq, T. Roy, A. Chhabra, C. Grover, O. Minez, J. Uginet, G. Durieu, C. Adobati, D. Casalotto, F. Nyer, P. Menut, A. Cathelin, I. Vongsavady, and P. Magarshack, "A 3 GHz dual core processor ARM cortex TM -A9 in 28 nm UTBB FD-SOI CMOS with Ultra-Wide voltage range and energy efficiency optimization", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 812–826, Apr. 2014, ISSN: 0018-9200. DOI: `10.1109/JSSC.2013.2295977`.

[14] S. Vitale, P. Wyatt, N. Checka, J. Kedzierski, and C. Keast, "FDSOI process technology for Subthreshold-Operation Ultralow-Power electronics", *Proceedings of the IEEE*, vol. 98, no. 2, pp. 333–342, Feb. 2010, ISSN: 0018-9219. DOI: `10.1109/JPROC.2009.2034476`.

[15] K. Sundaresan, P. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator", *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 433–442, Feb. 2006, ISSN: 0018-9200. DOI: `10.1109/JSSC.2005.863149`.

[16] C. Zhang, M. Lin, and M. Syrzycki, "Process variation compensated voltage controlled ring oscillator with subtraction-based voltage controlled current source", in *2011 24th Canadian Conference on Electrical and Computer Engineering (CCECE)*, May 2011, pp. 000 731–000 734. DOI: `10.1109/CCECE.2011.6030551`.

[17] B. Razavi, *Fundamentals of Microelectronics*, 2 edition. Hoboken, NJ: Wiley, Apr. 2013, ISBN: 9781118156322.

[18] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 6 edition. New York: Oxford University Press, Dec. 2009, ISBN: 9780195323030.

[19] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations", *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977, ISSN: 0018-9200. DOI: `10.1109/JSSC.1977.1050882`.

[20] F. Silveira, D. Flandre, and P. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996, ISSN: 0018-9200. DOI: `10.1109/4.535416`.

[21] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding", in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, Dec. 2008, pp. 1–4. DOI: `10.1109/IEDM.2008.4796663`.

[22] J. Noel, O. Thomas, M. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, and A. Amara, "Multi- UTBB FDSOI device architectures for Low-Power CMOS circuit", *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2473–2482, Aug. 2011, ISSN: 0018-9383. DOI: `10.1109/TED.2011.2155658`.

[23] O. Weber, F. Andrieu, J. Mazurier, M. Casse, X. Garros, C. Leroux, F. Martin, P. Perreau, C. Fenouillet-Béranger, S. Barnola, R. Gassilloud, C. Arvet, O. Thomas, J. Noel, O. Rozeau, M. Jaud, T. Poiroux, D. Lafond, A. Toffoli, F. Allain, C. Tabone, L. Tosti, L. Brevard, P. Lehnen, U. Weber, P. Baumann, O. Boissiere, W. Schwarzenbach, K. Bourdelle, B. Nguyen, F. Boeuf, T. Skotnicki, and O. Faynot, "Work-function engineering in gate first technology for multi-VT dual-gate FDSOI CMOS on UTBOX", in *Electron Devices Meeting (IEDM), 2010 IEEE International*, Dec. 2010, pp. 3.4.1–3.4.4. DOI: `10.1109/IEDM.2010.5703289`.

[24] M. Pelgrom, A. C. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors", *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989, ISSN: 0018-9200. DOI: `10.1109/JSSC.1989.572629`.

[25] A. Osman and M. Osman, "Investigation of high temperature effects on MOSFET transconductance (gm)", in *High Temperature Electronics Conference, 1998. HITEC. 1998 Fourth International*, Jun. 1998, pp. 301–304. DOI: `10.1109/HITEC.1998.676808`.

[26] I. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876–884, Jul. 2001, ISSN: 1057-7122. DOI: `10.1109/81.933328`.

[27] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, Jul. 1995, ISSN: 0925-1030, 1573-1979. DOI:

`10.1007/BF01239381`. [Online]. Available: `http://link.springer.com/article/10.1007/BF01239381`.

[28] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selmi, and E. Sangiorgi, “Low field electron and hole mobility of SOI transistors fabricated on ultrathin silicon films for deep submicrometer technology application”, *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2842–2850, Dec. 2001, ISSN: 0018-9383. DOI: `10.1109/16.974714`.

[29] E. Strandvik, “Compensation of threshold voltage for process variations in 28nm utbb fdsoi”, *NTNU,TFE4540 Specialization project*, no. 1, Dec. 2014.

[30] H. Oguey and D. Aebischer, “CMOS current reference without resistance”, *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1132–1135, Jul. 1997, ISSN: 0018-9200. DOI: `10.1109/4.597305`.

[31] V. Michal, “On the low-power design, stability improvement and frequency estimation of the CMOS ring oscillator”, in *Radioelektronika (RADIOELEKTRONIKA), 2012 22nd International Conference*, Apr. 2012, pp. 1–4.

[32] F. Fiori and P. Crovetti, “A new compact temperature-compensated CMOS current reference”, *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 11, pp. 724–728, Nov. 2005, ISSN: 1549-7747. DOI: `10.1109/TCSII.2005.852529`.

[33] K. N. Leung and P. Mok, “A sub-1-V 15-ppm/ deg;C CMOS bandgap voltage reference without requiring low threshold voltage device”, *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002, ISSN: 0018-9200. DOI: `10.1109/4.991391`.

A Design of two–stage miller amplifier

This appendix A is taken from the specialisation report written during the fall of 2014 [29]

The amplifier topology chosen in this project is a MILLER AMPLIFIER with two cascaded gain stages. The stages are an input differential stage converting to a single ended output, followed by a common source stage. A simplified model of a two-stage MILLER AMPLIFIER is shown in figure A.1. Two cascaded stages results in a total small-signal amplification given by the product of the amplification factor in each stage as seen in equation A.1.

$$A_{tot} = A_1 \cdot A_2 \tag{A.1}$$

Where A_1 is the amplification for the differential stage from the input to node 1, and A_2 is the amplification for the common-source stage from node 1 to node 2 in figure A.1.

Transistors Q_1 and Q_2 in the differential stage is matched. The same goes for Q_3 and Q_4, making the differential pair symmetrical and half of the bias current flow in each branch. This makes $g_{m1} = g_{m2}$ and the total small-signal gain of the first stage is $A_1 = g_{m1} \cdot r_{out1}$ where r_{out1} is the parallell combination of r_{ds2} and r_{ds4}. The small-signal gain can therefore be expressed as $A_1 = \frac{-g_{m1}}{g_{ds2}+g_{ds4}}$ and is equal to that of a common-source amplifier with an active load. Hence, the gain of the second stage, if replacing the bias current sources with an *nmos current mirror*, is $A_2 = \frac{-g_{m5}}{g_{ds5}+g_{nmos,load}}$. Equation A.1 can therefore be rewritten A.2.

$$A_{tot} = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right)\left(\frac{g_{m5}}{g_{ds5} + g_{nmos,load}}\right) \tag{A.2}$$

According to [11] the amplifiers frequency response is dominated by a low-frequency pole in node 1. The main contributing factor to this pole is the miller capacitor

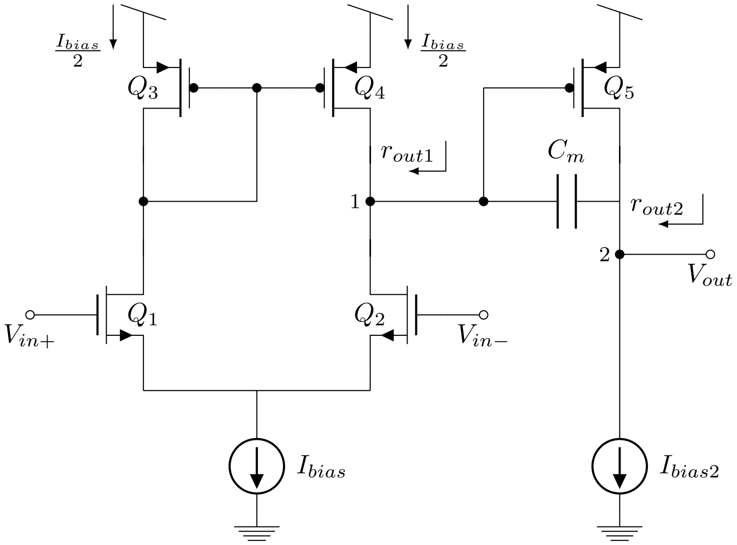

Figure A.1: Two-stage Miller Amplifier

C_m introduced for feedback between the stages in order to obtain stability for the amplifier. The low-frequency pole is given in equation A.3 and is also regarded as the bandwidth of the amplifier. As we can see from this equation the internal feedback capacitor C_m appears larger at the output of the first stage than its physical value by a factor of the amplification in the second stage. This is due to the *Miller Effect* [11].

$$\omega_{p1} \cong \frac{1}{A_2 \cdot C_m r_{out1}} \tag{A.3}$$

Combining the dominant low-frequency with the total amplification of the amplifier leads to an approximation of the *unity-gain angular frequency* given in equation A.4.

$$\omega_{ta} = \frac{g_{m1}}{C_m} \tag{A.4}$$

This *unity-gain angular frequency* is also known as the *gain bandwidth product* and gives a description of the amplifiers behavior for midband frequencies. A second pole will appear at the output of the second stage because of the load capacitance and parasitic capacitance at the drains of q_5 and its active load. However, this pole can be approximated to A.5 when the load capacitance is much larger than the parasitics.

$$\omega_{p2} = \frac{g_{m5}}{C_L} \tag{A.5}$$

In order to obtain stability in a *Miller amplifier*, C_m is introduced to provide internal feedback from the output to node 1. This specific type of compensation is often called *pole splitting compensation.* This can be seen from equation A.3 and A.3. The introduced feedback results in ω_{p1} being pushed to lower frequencies and ω_{p2} to higher frequencies when g_{m5} is increased. Increasing C_m will also push ω_{p1} to even lower frequencies without affecting ω_{p2}. A drawback of the internal feedback is the introduction of a right half plane zero leading to a negative phase shift in the transfer function of the amplifier. This zero often has to be compensated for by introducing *lead compensation. Lead compensation* can be realised by connecting a resistor, or transistor operating in triode region, in series with C_m in the feedback network. *Lead compensation* can therefore cancel the right half plane zero, or move it into the left half plane [11] according to

$$\omega_z = \frac{-1}{C_m\left(\frac{1}{g_{m5}} - R_C\right)} \tag{A.6}$$

where ω_z is the zero which becomes positive when *lead compensation* is sufficiently large. When appropriate one can also choose the *lead compensation* large enough to cancel the non-dominant pole ω_{p2}. This solution might be relevant when increasing g_{m5} is out of the question in order to obtain stability. An approximate value for the *lead compensation* to achieve this is found by setting A.5 equal to A.6, resulting in

$$R_C = \frac{1}{g_{m5}}\left(1 + \frac{C_L}{C_m}\right) \tag{A.7}$$

A.1 Implementation of amplifier

Process variations, temperature variations and variations caused by ageing give rise to changes in the circuit, but at a very slow rate. This results in very eased requirements for the speed of the amplifier, thus speed can be traded against low power consumption and high gain. Low power consumption is therefore considered one of the most important features for this amplifier. One of the reasons for this, is that the compensation circuit is auxiliary circuitry aiming to improve the perfmance on the circuitry its used in, and should therefore add as little overhead as possible. However, the amplifier should be able to drive a significant capacitive load equivalent to the bulk capacitance of a high number of tranistors. Using the simulation tool to measure the bulk capacitance of a NMOS transistor by connecting an ac-source to the bulk and running a frequency sweep while measuring the

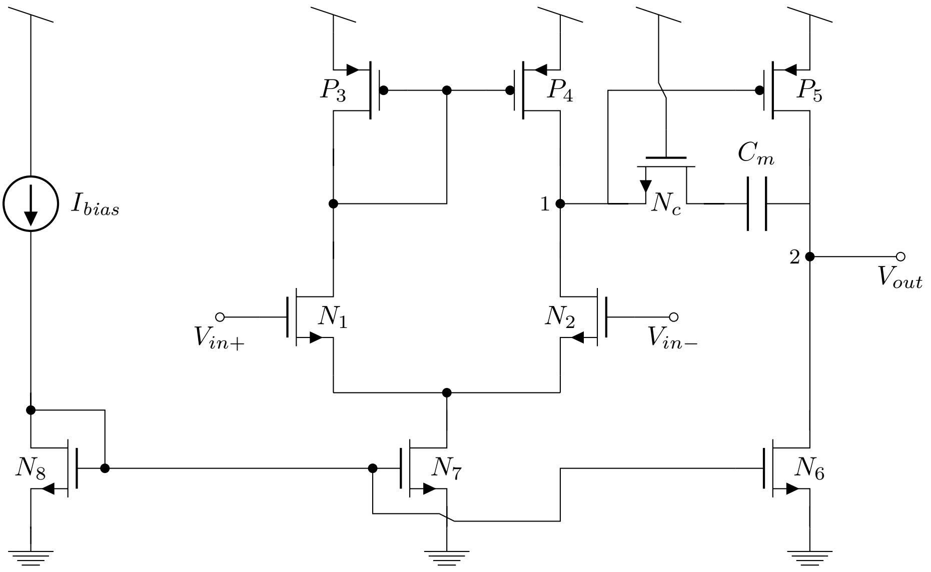

Figure A.2: Implemented two-stage amplifier

current. Using

$$C = \frac{I}{\frac{\delta V}{\delta t}} = \frac{I}{2\pi f \cdot V} \tag{A.8}$$

to calculate the resulting bulk capacitance, $C_b \approx 16aF$. By choosing $C_L = 500fF$, around 30000 transistors can be compensated. However, this is a simplified model of the bulk capacitance as there exists a diode in the junction between the well and the substrate. This well diode will be an object of further investigation. Owing to the fact that low power consumption and high gain is wanted, one should choose a high $\frac{g_m}{i_D}$-ratio [20]. This can be seen in equations (2.8b, A.2, 2.11). The highest $\frac{g_m}{i_D}$-ratio is obtained in weak inversion. Hence $\frac{g_m}{i_D}$ is selected to be 30 and $i_D = 25pA$, resulting in a $g_m = 750pS$. Using the equation for the gain bandwidth product, (A.4), and choosing a unity gain frequency of $3kHz$ with a transconductance of $g_m = 750pS$ a miller capacitor of $C_m = 40fF$ is obtained. The non-dominant pole given by equation (A.5) occurs around $240Hz$. This is well below the *unity-gain* frequency, and the amplifier might be unstable. As a result of this, a *lead compensation* calculated by equation (A.7) of $18T\Omega$ is used to cancel ω_{p2}.

Iterative simulations on transistors with bias current a of $25pA$, positive supply $V_{dd} = 1.1V$ and negative supply $V_{ss} = -0.7V$ resulted in the widths and lengths shown in table A.1 correnspondig to the designed amplifier in figure A.2. The amplifier is implemented using FDSOI I/O-transistors.

Table A.1: Amplifier paramteres

Element	**Type**	**Width** *(nm)*	**Length** *(nm)*	**M-factor**
N_1	NMOS	160	1800	1
N_2	NMOS	160	1800	1
P_3	PMOS	640	1500	1
P_4	PMOS	640	1500	1
P_5	PMOS	640	1500	1
N_6	NMOS	160	1800	1
N_7	NMOS	160	1800	2
N_8	NMOS	160	1800	1
N_c	NMOS	160	1200	1

It should be noted that the amplifier satisfy the requirement given by

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4} = 2\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_7} \tag{A.9}$$

to ensure no systematic offset voltage present at the input [11].