# Design, Analysis and Implementation of DLL clock generator

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*Abstract*— **In this paper we present design, analysis and implementation of Delay Locked Loop (DLL) based clock generator circuits. In this work a DLL has been proposed the design uses dynamic phase detector (PD) for phase detection. Voltage controlled delay line (VCDL) of proposed DLL consists of twelve delay elements. Current starved inverters have been used as delay element. In this paper, a proposed duty cycle corrector solves the problem of the sensitivity to half transparent (HT) architecture and the stuck locking error in the DLL simultaneously proposed DLL is designed to work at an input frequency of 250MHz. The design also generates an output of 3GHz using a frequency multiplication block. The design uses 180nm CMOS process technology and consumes 1.88mW of power at 1.8V.**

***Index Terms*—Delay locked loop, phase detector (PD), voltage control delay line (VCDL), CMOS**

## I. Introduction

DLL use the phase difference to increase or decrease delay. DLL is categorized either as analog DLL or digital DLL. An analog DLL has higher power, higher substrate noise rejection, smaller area, low power consumption, and great phase resolution. A digital DLL is more robust, enabling better process portability, requiring lower supply voltage, and being simpler design. DLL delays input clock rather than creating a new clock with an oscillator. The jitter performance of DLL is better than PLL. It is more stable and easier to design first order rather than second order. The most important metrics for a DLL are locking time, lock range and jitter performance. Here, locking time refers to the time interval a DLL takes to reach a stable locking state from an initial state. DLL is necessarily a nonlinear negative feedback system.

DLL is typically locking the delay to 1 or ½ input clock cycles. If locking to ½ clock cycle the DLL is sensitive to clock duty cycle. A DLL can be used to generate multiple clock phases with precise phase spacing. DLL is useful in CDRs and RF modulation and up/down-conversion. The delay cell matching are a function of Phase error. DLL delay cell mismatch, due to process variation, causes the delay of the cells to deviate from the ideal value. This results in phases that are not in the ideal position. DLLs have the potential to delay lock to undesired multiples of the reference cycle. In this paper, it shows an issue of duty-cycle sensitivity of half transparent (HT). There are many advantages of Half-transparent like small dead zone, usable in high speed and low area cost. And due to the dynamic structure, its operating frequency is minimum. There is only one signal to detect the difference between Ref. Clock and VCDL Out to check whether the phase is lead or lag. There are two types of locking errors for the multiphase application in a DLL. The first one is the difference between Ref. Clock and VCDL Out is less than 0.5 cycle time, and it would trace to an impossible case which is called stuck locking problem. Another one is the difference between Ref. Clock and VCDL Out is bigger than 1.5 cycle time and it would trace to lock in the nth cycle which is called harmonic locking.

## II. BLOCKS of the Delay locked loop

**A delay locked loop (DLL) has similar structure as phase - locked loop (PLL). It consists of voltage controlled delay line (VCDL) in place of voltage controlled oscillator (VCO), phase detector (PD), and a low pass filter (LP). The output of the low-pass filter controls the delay of VCDL, changing its supply voltage, capacitive load, or the conductance of the driving transistor are some ways to control the delay of delay line. The major blocks of DLL clock generator are shown below in the block diagram.**

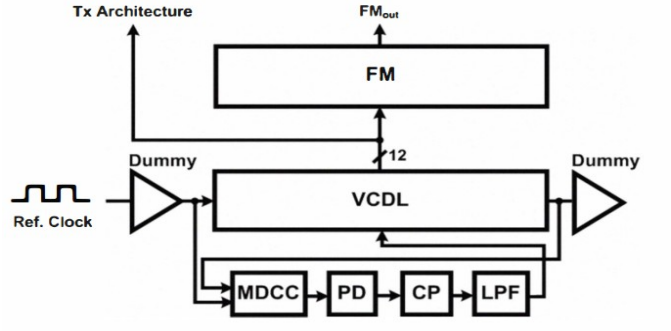


**Fig.1. DLL clock generator**

The blocks of the DLL circuit are consisting of Voltage Controlled Delay Line (VCDL), Modified Duty Cycle Corrector (MDCC), Phase Detector (PD), Charge Pump (CP), Low Pass Filter (LPF), and Frequency Multiplier (FM). Following bottom up design approach the blocks were designed and simulated separately using transistor level schematics. These blocks were integrated in top module to complete the design of multiphase clock generator. The design and simulation was carried out using set of SPICE tools. Schematic design of the circuit was carried out in Electric CAD GNU tool and LT Spice from Linear technologies was used for simulation of SPICE deck generated by Electric CAD. Block wise description and simulation results of the circuit will be discussed in next few paragraphs.

## III.DLL DESIGN

A delay-locked loop (DLL) is a digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a delay line. Fig.1. shows the block diagram of DLL.

### *A. Charge Pump*

The schematic of the charge pump is shown in Fig.2. A single ended switch at the source charge pump is used. The current mismatch between source current and sink current is reduced by ensuring that the source current is the same as the sink current; thus experiencing the same process variations. Studies show that in CMOS circuits, current switching provides a faster switching speed than voltage switching.

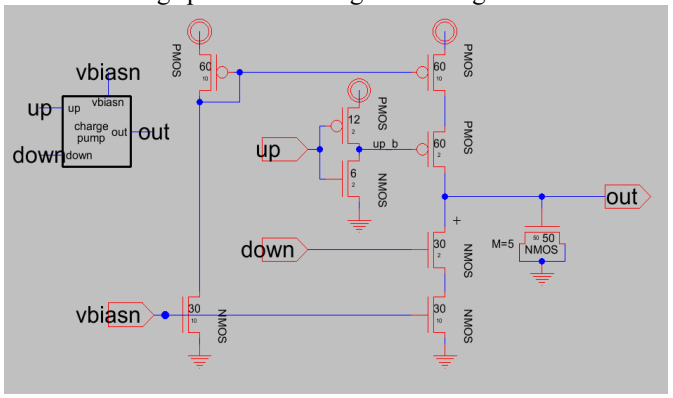


**Fig.2. schematic design of charge pump**

*B. Phase Detector*

The Phase detector used in the current design is based on two Half transparent (HT) structures. PD takes Reference Clock and Output clock form VCDL as inputs and produces two Up and Down depending on Lag or Lead in phase of VCDL out with respect to reference clock respectively. Snapshot of schematic of HT block and PD using HT is shown in figures below.

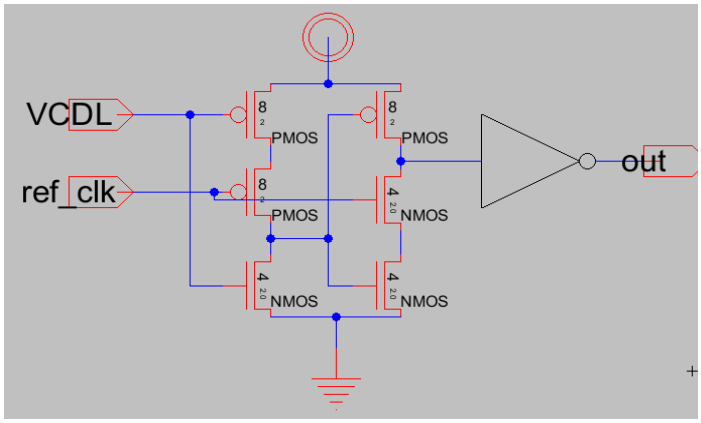


Fig.3. HT block used in Phase Detector

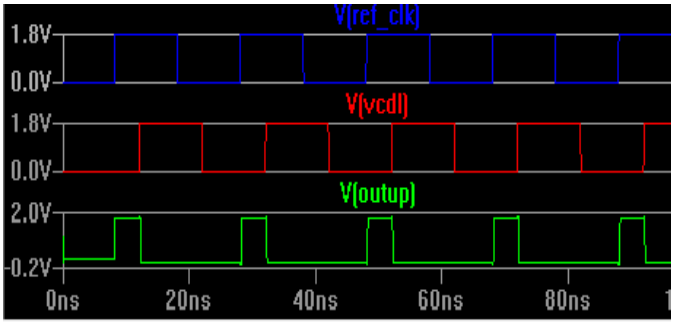


Fig.4. snapshot of simulation of HT

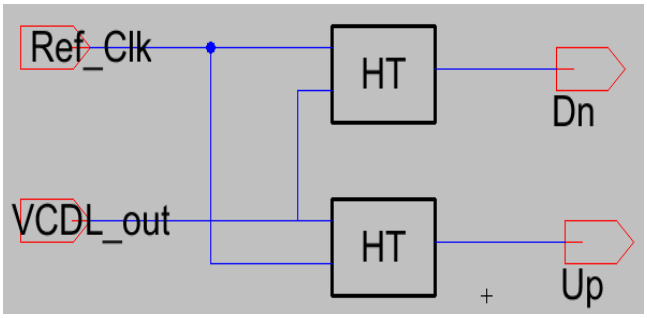


Fig.5. phase detector

*C. Voltage- controlled delay line(VCDL)*

VCDL is main part of DLL which corresponds to VCO in PLL. Although its function is not same as VCO. It cannot generate clock signal itself. VCDL has variable delay controlled by control voltage. This variable delay is used to lock output phase with input reference clock. The main parts of VCDL are: control voltage biasing circuit, dummy buffers and Buffer chain. The control voltage biasing circuit is used to generate biasing for current starved buffers. These biasing are used to control the delay of buffers. Dummy Buffers are use to achieve full output swing at the end of the chain and also to provide equal load capacitance to end inverter in the chain.

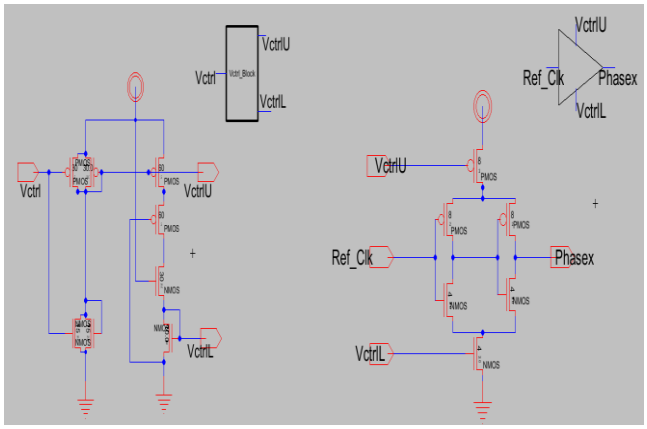


Fig.6. Control voltage biasing and current starved buffer circuits

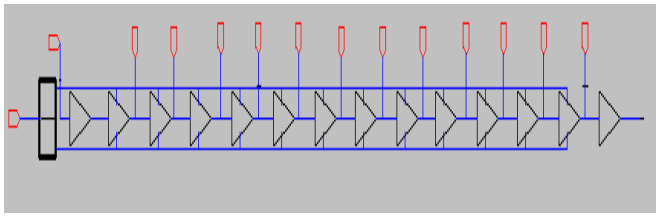

Fig.7. VCDL with 12 phase outputs and two dummy blocks at beginning and end

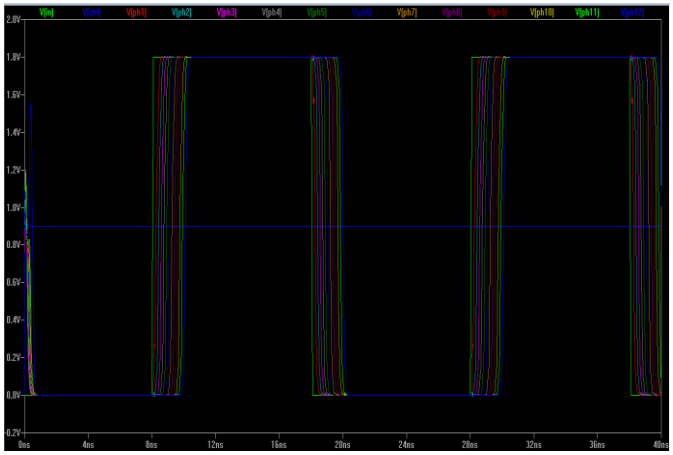

Fig.8. Input clock and delayed outputs from VCDL at Vctrl=0.9v

*D. Modified Duty Cycle Corrector (MDCC)*

MDCC uses MUX and T- Flip Flops to correct duty cycle. The circuit takes 0°, 180° and 360° phases of signals as inputs and generates two outputs which are further fed to phase detector.

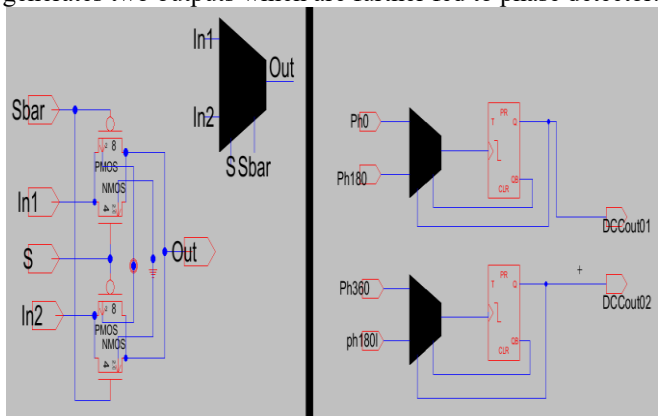


Fig.9. Schematic TG based MUX used in MDCC (left) and structure of MDCC (right)

*E. Frequency Multiplier*

The frequency multiplier, shown in Figure , consists of One Shot and symmetric AND. The One Shot is a pulse generator that can transfer signal to a pulse. The symmetric AND is the edge combiner that can combine the pulses to get a faster clock. In the Figure5.11, it shows the timing diagram of frequency multiplier. Signals are transferred by the One Shot circuits and they can be combined stage by stage with the symmetric AND. The multiplication factor of this architecture is 12. As the DLL operates at 250 MHz, the FM can generate a 3 GHz output.

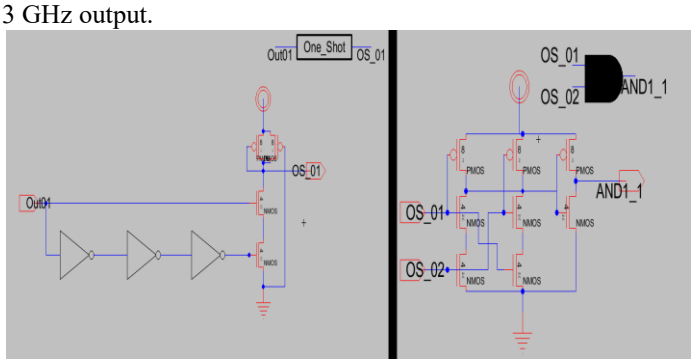


**Figure.10.** Schematic of One shot (left) and Symmetric AND gate (right) use in FM

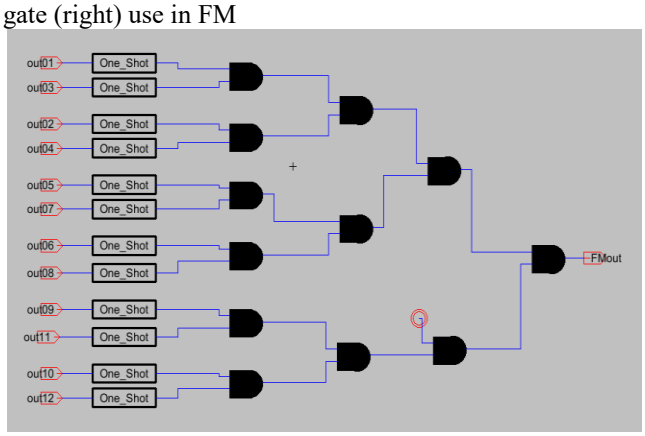


Fig.11. Schematic of FM

## IV. SIMULATION AND RESULT ANALYSIS

Designing of DLL in electric CAD consist of different components that are VCDL, frequency multiplier (FM),phase detector, charge pump, low pass filter, modified duty cycle corrector (MDCC). The designed DLL achieves operation frequency of 280 MHz with a multiplied output of 3GHz considerable power improvement was achieved in the design. The multiplication factor is 12, and, therefore, the operation frequency of proposed DLL-based frequency multiplier can operate at 3 GHz. The 12 multiphase outputs are shown in Fig.12, and there are also the statistics of phases' difference.

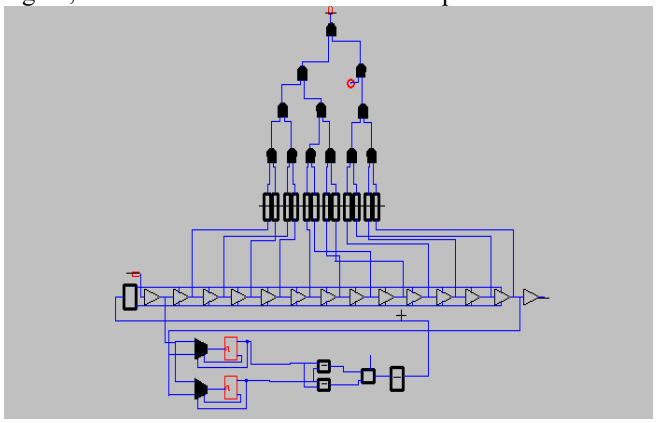

Fig.12. Schematic of delay locked loop (DLL)

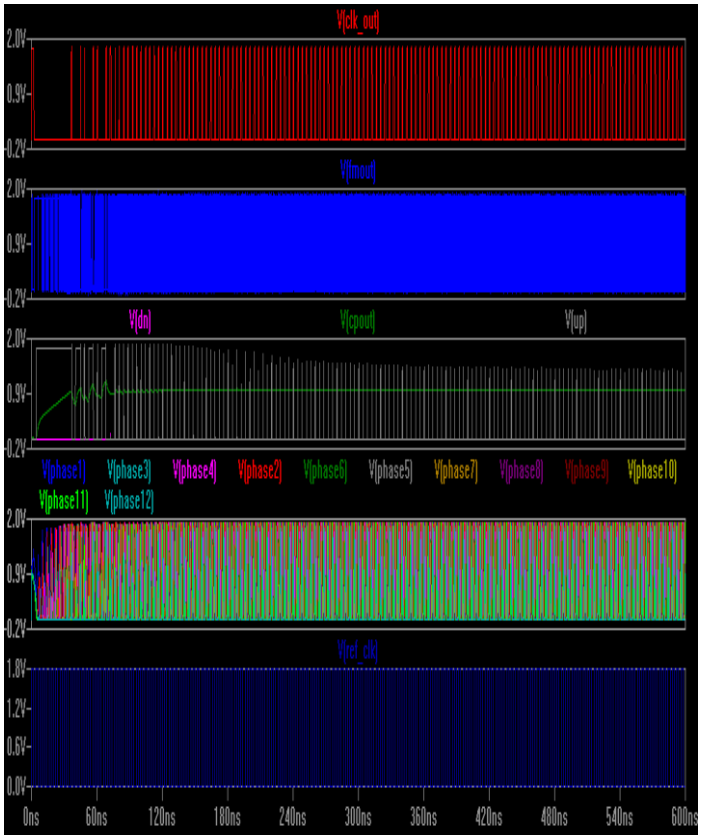


Fig.13. Simulation of DLL

## V. DESIGN ANALYSIS OF DLL

Table 1.1 Different design performance of DLL

| Property | Ref [1] | Ref[2] | Ref[3] | result |
|---|---|---|---|---|
| Process technology | 180nm | 180nm | 180nm | 180nm |
| Supply | 1.8V | 1.8V | 1.8V | 1.8V |
| Operating freq. range | 150MHz -2GHz | 100MHz-1.2GHz | 5-120MHz | 250MHz @DLL (4ns period) |
| Jitter (RMS) | 2.94 ps @ 250 MHz 31.17ps @ 3 GHz | - | 9.7ps@ 120MHz | - |
| Multipli-cation factor | - | 1x-8x | 0.5x-8x | 12x |
| Power consumption | 20.9Mw @3GHz | 23.87mW @800MHz | 15.56mA @120MHz | 1.88mW @3GHz |
| Estimated area | 0.13mm$^2$ | 0.14mm$^2$ | 0.27mm$^2$ | - |

**VI. Applications**

Dll can be used in various fields. Some of the applications of DLL are Delay Compensation, Multiphase Clock Generation, generation of multiple input Frequency and Clock & Data Recovery Systems

**VII. Conclusion**

**In this work the designed DLL achieves operation frequency of 280MHz with a multiplied output of 3GHz consideration power improvement was achieved in the**

**design. The design shows improvement in power consumption but for better jitter performance different delay element can be used in place of current starved inverter. Further work can be carried out on implementation of programmable FM.**

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