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GaN LNAs for Robust Receiving Systems in Radar and Space Applications

Marco Vittori, Sergio Colangeli, Walter Ciccognani, Riccardo Cleriti, Ernesto Limiti

University of Rome Tor Vergata, Dept. of Electronics Engineering, Via del Politecnico 1, 00133 Rome, Italy
E-mail: limiti@ing.uniroma2.it

Abstract - **In this contribution a series of integrated circuits and methodologies, purposely developed for application in microwave receiving subsystems, will be presented. The integrated circuits, realized in GaN integrated technologies by different suppliers, find their applications in telecom systems as well as in RADAR ones, mainly for space-based apparatuses. The respective performance, as well as the key design methods will be presented in the contribution for bandwidths ranging from S-Band up to K-Band.**

Index Terms – **Gallium Nitride, low-noise amplifier, robustness, survivability, microwaves.**

I. INTRODUCTION

Gallium Nitride (GaN) is gaining momentum as the key semiconductor compound for electronic circuits operating well into the microwave and millimeter-wave ranges. The applications range from communication systems to electronic instrumentation, from RADAR systems to Space payloads for Earth Observation. The main role of GaN-based electronic components has historically been identified in the front-end power stages of the transmitting sections, due to the inherently superb performance of GaN in terms of output power, efficiency and power handling, related to the wide-bandgap properties (higher breakdown and thermal conductivity). Nevertheless, more recently, the intrinsic robustness of GaN devices to impinging interfering signals suggested its introduction also in the receiving section, where traditional GaAs stages suffered from the lower dynamic range and robustness, often necessitating the introduction of limiting stages, in turn worsening the low-noise performance. This contribution will present several MMIC designs based on GaN to illustrate key aspects of that technology as applied to the function of low-noise amplification, namely high survivability and linearity (Section II), then low noise (Section III) and integration (Section IV). Finally, Section V details the design of GaN LNA targeted to reach medium-level output power in conjunction with linear performance aligned to the state of the art of GaN technology.

II. HIGH SURVIVABILITY AND LINEARITY

As compared to GaAs, GaN HEMT technologies are inherently more robust and survivable [1]. The former property indicates that GaN-based circuitry (LNAs in this case) keep working with acceptable performance (in particular, noise figure and gain) also for driving levels beyond the normal range of operation: as such, it is quite related to linearity in the specific case of low-noise amplification. The latter, namely survivability, means that a circuit can withstand a very out-of-range driving level without receiving permanent damage, although not working as desired during and soon after the overdrive.

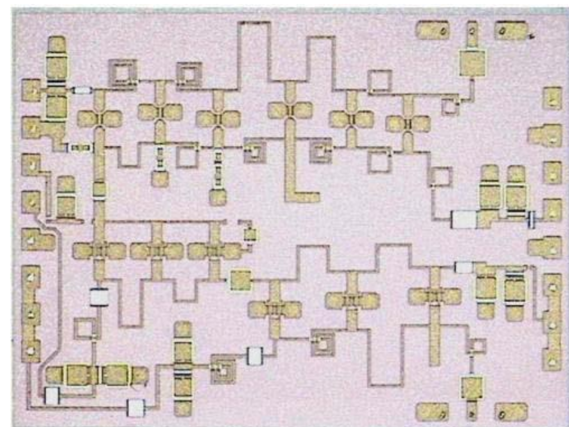

Fig. 1. Microphoto of the robust cascaded distributed LNA from [1-3]. Chip size is 3.8×2.9mm^2.

Fig. 1 shows the microphoto of a robust/survivable broadband LNA comprising three distributed stages in cascade [1-3] realized on a 0.25 μm GaN HEMT technology

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provided by Leonardo's foundry (Selex-SI at the time of design). The LNA is featured by a remarkable OIP3 level, namely 52 dBm, which is in line with the best results reviewed in [4, 5], but with a much broader bandwidth. Even if the DC power consumption is not low (12 W), nevertheless the OIP3/P_{DC} ratio compares very well with state-of-the-art realizations specifically oriented to maximize this figure of merit [6]. Output power versus a continuous-wave (CW) excitation up to 10 W at 4 GHz is reported in Fig. 2. The LNA did not show signs of damage after such a high stress level.

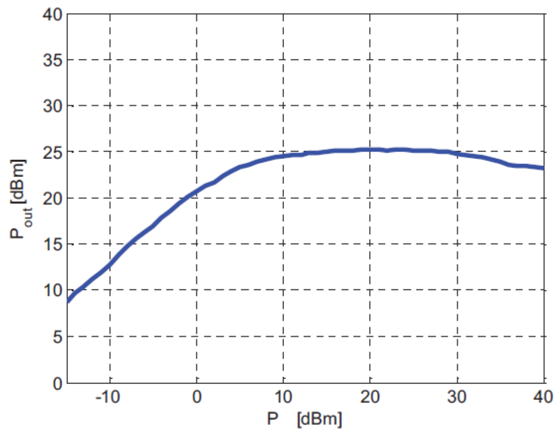

Fig. 2. Measured Pin/Pout curve of the robust cascaded distributed LNA from [1-3].

As a further example, the X-band LNA of [1, 2], depicted in Fig. 3, shows a noise figure of ~ 2.2 dB at the optimum drain voltage V_{DS} = 10 V, and a linear gain higher than 25 dB with an associated ripple of ± 0.5 dB from 8.6 GHz to 10.6 GHz. The technology was a more mature version of that used for the previous broadband LNA and MMIC size is 3 × 2.5 mm^2. Fig. 4 shows an example of output power measurement with a 9.6 GHz CW input up to more than 20 W. Unlike in the cascaded distributed LNA discussed above, for which the input power was split among several transistors and a resistive termination, in this single-ended design all of the excitation is incident on the only device of the first stage. This makes it so that the first-stage device enters direct conduction earlier, causing a noticeable gain drop. The input power sweep is so high in this case that even the second and third stages experience direct conduction, until the LNA is irreversibly damaged at some 41 dBm. Since the main cause of disruption is the high DC gate current under strong driving, the use of a large series resistor along the DC bias network is commonly exploited in high-survivability GaN designs such as this one. On the contrary, voltage peaks across the gate-source and, more importantly, gate-drain junctions are usually far from breakdown values. This makes survivability of GaN-based LNAs approximately independent of device size [1].

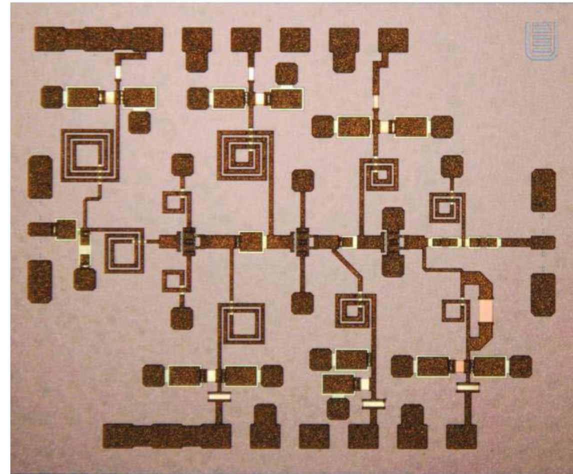

Fig. 3. Microphoto of the robust single-ended LNA from [1, 2]. Chip size is 3.0×2.5mm^2.

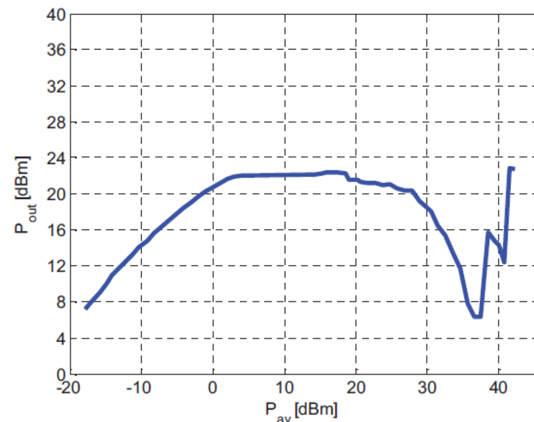

Fig. 4. Measured Pin/Pout curve of the robust single-ended LNA from [1, 2].

III. LOW NOISE

Two more single-ended LNAs [7] based on Leonardo's 0.25 µm GaN HEMT technology are presented in this Section. Although they both encompass the whole X band, each is optimized for best linear performance in a sub-band, namely 8-10 GHz (LNA A) and 10-12 GHz (LNA B). Chip size is 3×1.5 mm^2

for both amplifiers, the former of which is shown in Fig. 5 (LNA B has a similar layout). As illustrated in Table 1, these two amplifiers show state-of-the-art noise performance, if compared with recently published GaN LNAs operating in the neighborhood of X band. The noise performance of most examples from Table 1 helps making the point that GaN LNAs are a viable alternative to GaAs-based ones, since the latter are inherently less survivable and must be preceded by limiters: in turn these introduce loss (around 1 dB, therefore causing a chain noise figure as much higher) and typically cannot be integrated (PIN diodes are required).

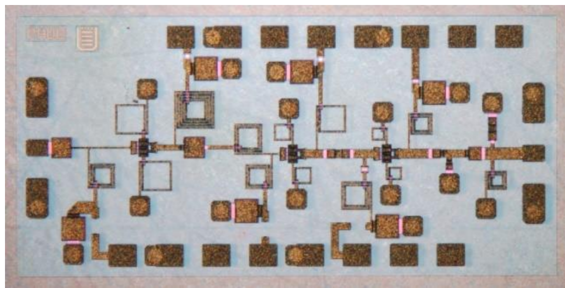

Fig. 5. Microphoto of the linear single-ended “LNA A” (8-10 GHz). Chip size is 3.0×1.5mm^2.

Table 1: Comparison of recently published GaN LNAs operating approximately in X band.

Ref	f [GHz]	G_T [dB]	NF [dB]	P_{diss} [W}
[8]	8.5÷10.5	> 25	< 2.5	0.5
[9]	7.4÷11.4	> 23	1.6	1.2
[10]	14÷18	18÷19	2.5÷3.6	0.75÷1.5
[11]	10÷13	19÷26	1.7÷2.1	/
[12]	8÷12	14÷16	1.6÷1.8	0.21
[13]	12.8÷14.8	> 20	<1.85	0.84
[14]	8	6.8	1.9	0.4
[15]	8÷11	> 17	<2.5	1.6
LNA A	8÷10	25.5±1.5	<1.3	0.9
LNA B	10÷12	24.8±0.4	1.3÷1.75	0.9

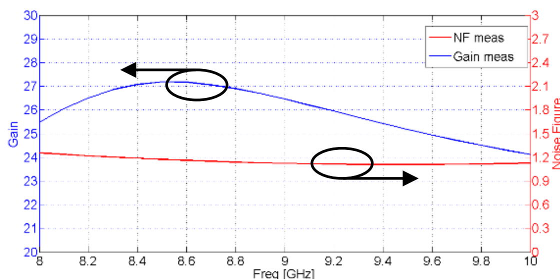

Fig. 6. Measured transducer gain (left axis) and noise figure (right axis) of the linear single-ended “LNA A” (8-10 GHz).

As reported in Table 1, LNA A is featured by a noise figure lower than 1.3 dB and a nominal gain of 25.5 dB (see also Fig. 6), whereas LNA B shows a noise figure between 1.3 dB and 1.75 dB, as well as a gain of 24 dB with a small ripple. Although not specifically designed for high linearity, LNAs A and B are featured by an output IP3 of about 33.9 dBm (see Fig. 7) and 32.9 dBm, respectively, measured at 10 GHz.

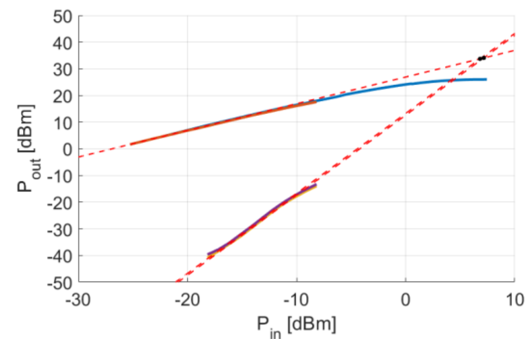

Fig. 7. Measured output power (fundamental and third-order inter-modulation) of the linear single-ended “LNA A” (8-10 GHz).

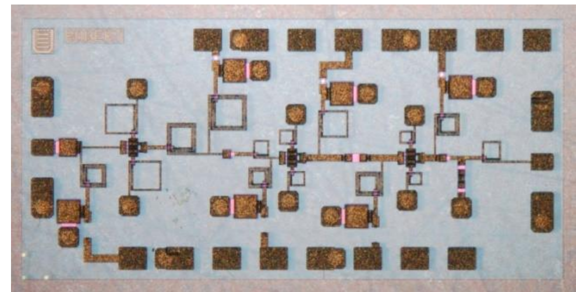

Fig. 8. Microphoto of the linear single-ended “LNA B” (10-12 GHz). Chip size is 3.0×1.5mm^2.

IV. INTEGRATION

Although GaN HEMT technology’s most important use at microwave frequencies is today for high-power amplifiers (HPAs), its exceptional survivability and reasonably low noise figure allows to integrate on the same chip both the HPA and LNA, plus a single-pole double-throw (SPDT) switch to select between the transmit and receive modes.

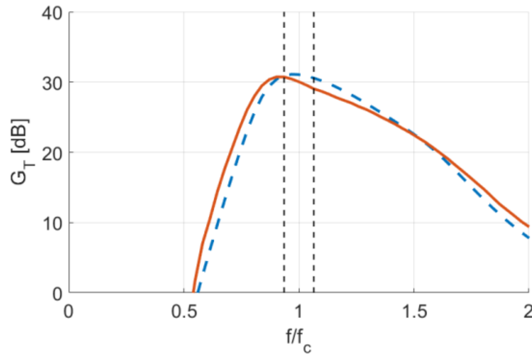

Fig. 9. Simulated (dashed) and measured (continuous) transducer gain versus normalized frequency of the UMS SCFE in Rx mode (switch plus LNA).

The resulting "single-chip front end" (SCFE), as such a design is typically called, is becoming a fundamental building block in modern phased-array applications since the integrated solution enormously simplifies mounting and reduces size. As an example, the Rx linear performance of an S-band SCFE recently designed on UMS's 0.25-µm commercial GaN process is here briefly presented. The first-run MMICs, on which a measurement campaign is still running, present a transducer gain around 30 dB (see Fig. 9) and a simulated noise figure below 1.8 dB (see Fig. 10): both figures include the SPDT switch. The relative operating bandwidth is about 14%.

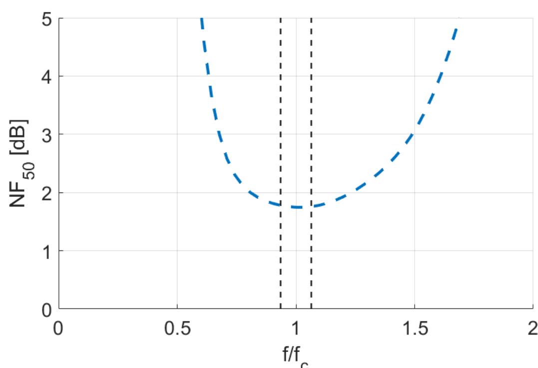

Fig. 10. Simulated noise figure versus normalized frequency of the UMS SCFE in Rx mode (switch plus LNA). The nominal value is 1.8 dB.

Another example of integration of the front-end functionalities is in [16]. Unlike the previous example, this SCFE was developed in a 0.5-µm technology, provided by Leonardo's foundry. A second version of the project has been recently developed, this time adopting Leonardo's 0.25-µm process: fabrication is foreseen in the next few months.

Fig. 11 shows the layout of the first-version SCFE, with the LNA building block highlighted in the black dashed box.
This SCFE was designed to operate in C-Band with a central frequency of 5.405 GHz and a percent bandwidth about 5%.
The performance obtained in simulations is as follows: gain greater than 36 dB, input return loss better than 10 dB and output return loss better than 15 dB, noise figure lower than 2.5 dB (see Fig. 12). It is important to remark that all these figures of merit refer to the whole Rx chain, thus including the SPDT ahead of the LNA. In order to minimize the overall noise figure, significant effort was spent during the design phase in optimizing the switch and LNA simultaneously.

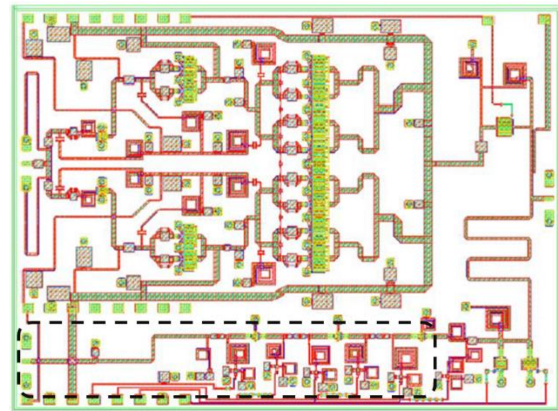

Fig. 11. Layout of the Leonardo SCFE. MMIC size is 7.28×5.40 mm^2. The LNA is in the lower part of the chip, highlighted by the black dashed box. The meandered line on the right is a quarter-wave transformer which is part of the single-pole double-throw switch. LNA output is on the lower-left side.

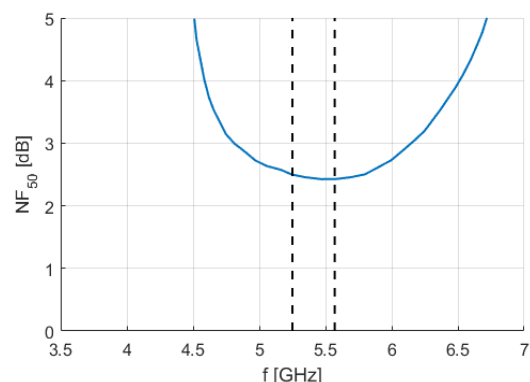

Fig. 12. Simulated noise figure of the Leonardo SCFE in Rx mode (switch plus LNA). The nominal value is 2.45 dB.

V. MEDIUM POWER LNA

In this section will be shown the possibility to realize in GaN LNAs with specific goals on delivered power [17]. The design goal of the presented realization was to achieve a survivable low-noise amplifier tailored to the 8.5÷11.5 GHz bandwidth, featured by state-of-the-art noise and gain performance, but also with a good level of output power.

The large number, variety and importance of applications today demonstrated in the X-band (among which earth monitoring, radar, satellite) led to the choice of this band for the medium-power LNA.

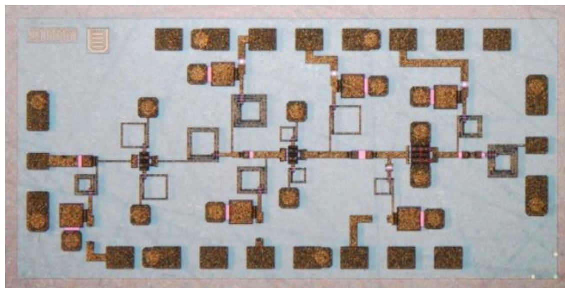

Fig. 13. Microphoto of the medium power LNA (8.5÷11.5 GHz). Chip size is 3.0×1.5mm^2.

To reach good performance, a cascade of three single-ended stages was chosen. The first and second stages use the same active device geometry, whereas the third one has a larger periphery: see Fig. 13 for a photograph of the realized MMIC.

As is typical of LNA designs, the first stage and its input matching network were optimized for noise performance; on the other hand, the third stage was designed to have a good level of output power at the center of the bandwidth. All three stages adopt a common-source configuration, although inductively degenerated in the first and the second stage.

The total current absorption is 150 mA, the drain voltage for each stage is 20 V, thus the power consumption is approximately equal to 3 W.

In this type of LNA a correct design of the output network is essential. In the present case the output network was designed based load pull measurements to achieve the desired value of delivered power. As can be seen from Fig. 14, the load shown by the output matching network to the active device (thick blue line) in the sub-band of interest is well located in the load-pull contours. Only the contours for 10 GHz are reported, since little variations are observed in the sub-band of interest.

The chart shows that the obtained output load (with respect to the third-stage active device) always stays within the 27.5-dBm contour. The actual output power of the medium-power LNA is easily computed by taking into account the operative loss of the output matching network, which is here reported to be 1.5 dB, 0.8 dB and 0.9 dB, respectively, at the following three significant frequencies: 9.5 GHz, 10 GHz and 10.5 GHz.

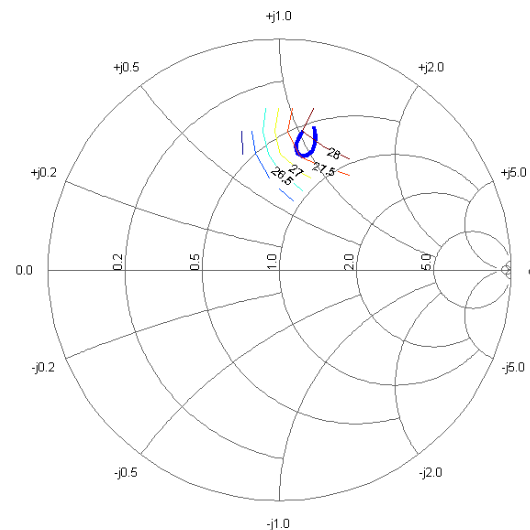

Fig. 14. Load pull contours of the 4×100 μm device at 10 GHz and S_{11} of output matching network over the whole band.

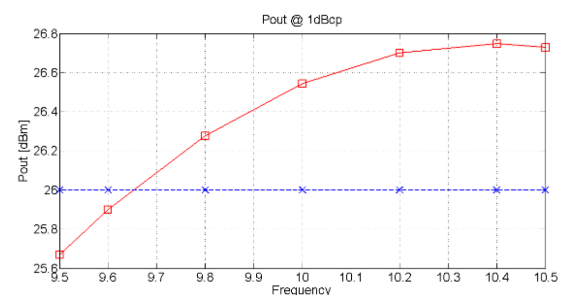

Fig. 15. Pout at 1 dB compression point of the realized LNA.

The expected value for output power is between 26÷26.7 dBm. In

Fig. 15 is shown the measured output power of the realized LNA. Only for the first 150 MHz the value is below 26 dBm; the maximum value, obtained at 10 GHz, is 26.7 dBm. The measured results agree well with the estimations made during the design.
The main measured figures of merit besides output power include a gain equal to 24.7±1 dB and a noise figure down to 1.6 dB. Both input and output return losses are typically better than 10 dB, although with localized deteriorations.

VI. CONCLUSION

Several examples of GaN LNAs from European foundries have been presented, each highlighting a key feature of Gallium Nitride technology. In particular, state-of-the-art realizations have been overviewed as to survivability, linearity and noise figure. Also, the feasibility of integrating complementary functionalities on a same chip has been demonstrated by presenting two MMIC SCFE designs. Finally, it has been shown how the high power handling of GaN makes it possible to design and realize single-ended LNAs with a good output power levels.

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