Performance predictions for a silicon velocity modulation transistor

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A Monte Carlo simulation has been devised and used to model submicron Si velocity modulation transistors with the intention of designing a picosecond switch. The simulated devices have nominal top and back gate lengths of 0.1 μm, and the conduction channels have similar thickness. Mobility modulation has so far been achieved by heavily compensated doping and interface roughness at one side of the channel. The simulated devices have a high intrinsic speed; simulations performed for $T=77$ K suggest that current can be switched between the low and high mobility regions of the channel within 1.5 ps. However, in unstrained Si devices the main obstacle to practical device operation is the rather small current modulation factor (the ratio of the steady drain currents for the device operating in the high and low mobility regimes), which decreases towards unity with increasing drain–source bias. Such a device should work best for small electric fields along the channel ($\sim 10^5$ V m^{-1}), the regime where impurity scattering has its greatest influence on the electron mobility. © *1999 American Institute of Physics.* [S0021-8979(99)05502-4]

I. INTRODUCTION

Sakaki originally proposed velocity modulation as a means of obtaining fast switching in a field effect transistor by transferring electrons between high and low mobility channels. The motivation for this approach is to remove or reduce the capacitive limitation on device speed that arises through modulation of the channel carrier density in a conventional field effect transistor. Sakaki suggested the use of GaAs/AlGaAs as the materials system[1] and a few GaAs devices have been reported since then,[2,3] including the dual channel high electron mobility transistor (HEMT).[4] One advantage of using GaAs is that low-temperature-grown GaAs, with naturally occurring arsenic islands, can form the low mobility side of the channel. These islands serve as scattering centers for electrons. In principle, these, along with ionized impurities, could yield a high/low electron mobility ratio of 40.[2]

Kizilyalli *et al.* have modeled the operation of a GaAs/AlGaAs velocity modulation transistor, which had a 0.4 μm long gate and a channel 1 μm long and 0.1 μm wide.[5,6] This simulated device made use of separate source and drain contacts to the high and low mobility sides of the GaAs channel. Mobility modulation was achieved using compensated doping at one side of the channel. The predicted current modulation factor which defines the ''on'' and ''off'' states of the device was 1.6. (It should be noted that a current modulation factor of at least 10 is the requirement for a commercial device).[7] Although charge could be transferred across the channel within 0.5 ps, it took rather longer (3 ps) for the drain current to reach a new steady state once the gate biases had been switched. The simulated devices were driven by drain–source electric fields $\sim 10^6$ V m^{-1}; consequently the velocity profiles along the undoped and heavily compensated sides of the channel differed by at most 25% at 300 K.

While interest has focused on GaAs, the motivation here is to devise a terahertz transistor based on Si where the better developed fabrication technology could facilitate the implementation of appropriate structures. The geometries of the modeled Si devices are smaller than the GaAs devices described above ($\sim$0.1 μm gate length, $\sim$0.1 μm long$\times$0.1 μm wide channel). Such devices are not compact enough to be true quantum transport devices and a semiclassical description of the transport should be applicable at temperatures above 77 K. Monte Carlo simulations of the devices have been carried out and the electron transport model is summarized in Sec. II. In Sec. III, results are discussed for simulations of unstrained Si devices, showing how the doping profile and drain/gate bias conditions influence the device operation.

II. MONTE CARLO MODEL

Superparticles that represent electrons in the ensemble Monte Carlo simulation are described by nonparabolic ellipsoidal valleys in reciprocal space and obey classical statistics. Herring–Vogt transformations are used to map carrier momenta into spherical valleys when particles are drifted, scattered, or cross heterojunctions. The electric field equations are solved self-consistently with the electron transport,[8] and the device grid potentials are updated at each ensemble drift timestep (1 fs). The electric field cell size is $\sim 5 \times 5$ nm^2. For these submicron transistors, 1000 electron superparticles are sufficient to get a good idea of the current switching properties, but for the calculation of $I-V$ curves and smooth switching characteristics an initial count of 4000 superparticles has been used. Electrons in bulk Si may be scattered by ionized impurities and by bulk acoustic and nonpolar optical phonon modes. Acoustic phonon scattering is assumed to be elastic and the absorption and emission rates are combined under the equipartition approximation, which is valid for lattice temperatures at and above 77 K. Ionized impurity scattering in doped and compensated regions of the device is described using the screened Coulomb potential of

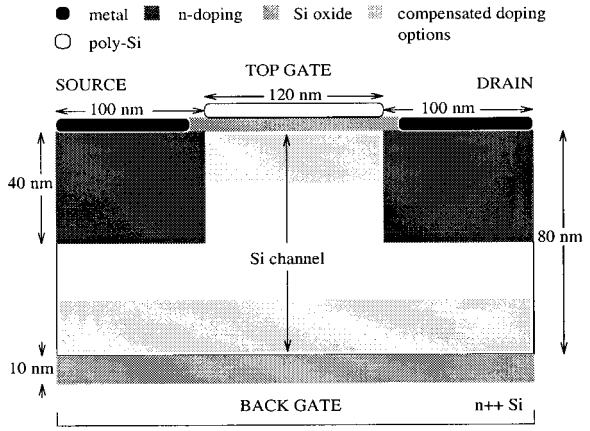


FIG. 1. Schematic for a possible Si based velocity modulation transistor, as modeled in Sec. III. Simulations have been performed for devices in which the compensated doping is placed under the top or back gate sides of the channel or it is some hybrid of the two extremes indicated above.

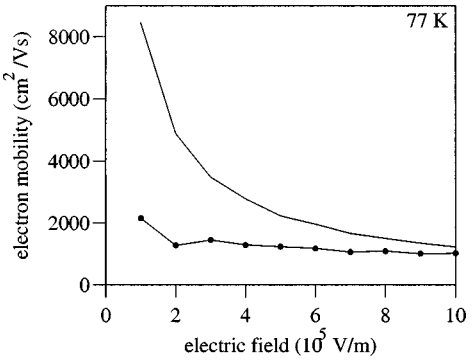


FIG. 2. Mobility-field curves for *X*-valley electrons in pure Si (solid curve) and in heavily compensated Si (solid curve with symbols) at 77 K. The impurity concentrations in the compensated Si are donor density 2×10^{25} m^{-3} and acceptor density 1.99×10^{25} m^{-3}.

the Brooks–Herring model. The impurity scattering rate for electrons with energy E in an ellipsoidal valley of nonparabolicity α is

$$R_{\text{impurity}}(E)=\frac{N_a+N_d}{8\sqrt{2m^*}\pi\epsilon_r^2\epsilon_0^2(1+2\alpha E)[E(1+\alpha E)]^{3/2}}\times\left[\alpha^2E^2+\frac{[1+\alpha E(1+\xi)]^2}{\xi^2-1}+\alpha E[1+\alpha E(1+\xi)]\ln\left(\frac{\xi-1}{\xi+1}\right)\right], \quad (1)$$

$\xi=1+l_s^{-2}/4m^*E(1+\alpha E)$ where m^* is the density of states effective mass and l_s^{-1} is the reciprocal screening length such that $l_s^{-2}=|N_a-N_d|/\epsilon_r\epsilon_0k_BT$. N_a is the acceptor density and N_d the donor density.

A very simple model for scattering particles off a rough oxide layer has been included, although this is not listed as a process in the scattering rate ladder. Instead, when a superparticle is bounced off a rough heterojunction barrier, rather than suffer a specular reflection it is deflected back into the Si at a random angle to its initial path. Band effective masses, scattering potentials, and other device parameters are those reported in Refs. 9 and 10. The effect of doping under a metal–oxide–semiconductor (MOS) contact is accounted for in the definition of the flat-band potentials that define the offset between the Fermi levels of the n^{++} polysilicon and the doped Si layers.[11] A fixed charge concentration of 10^{15} m^{-2} has been assumed to be present in the oxide layers.

In this article, the modeled devices are of the simplest kind, that is, a region of selectively doped Si grown between two SiO_2 layers which serve as top and back gates to the device. The aim is to demonstrate that velocity modulation can be achieved using Si as the basic material. The basic design for the simulated unstrained Si velocity modulation transistor is shown in Fig. 1. The device resembles a short channel field effect transistor, but the key difference is that the device would be fabricated using the silicon-on-insulator technique which would allow the Si channel to be backgated by biasing the n^{++} polysilicon in the substrate. Ideally, the back gate oxide layer should be pared to within 10 nm to maximize any depletion effect due to negative gate bias relative to the top gate, and therefore sweep carriers from one side of the channel to the other efficiently. The top gate oxide thickness is 5 nm. Devices with different doping profiles have been modeled—compensated doping has been placed either under the top gate, above the back gate to the channel, or is a hybrid of the two extremes.

For these submicron devices to operate successfully, ideally three main constraints should be met.

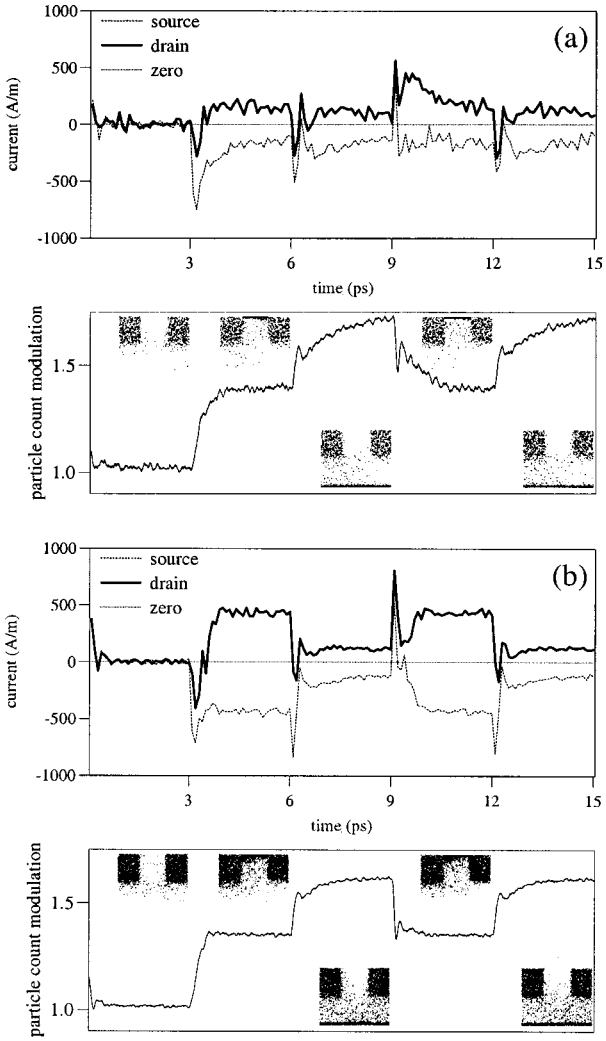
(i) The carrier density modulation in the channel should be small in order to minimize charging/discharging time constants when switching the top and back gate biases.

(ii) The gate biases, hence the lateral electric fields generated across the channel, must be large enough to create two distinct low and high mobility conduction paths within the channel.

(iii) The drain–source bias should be large enough for the carrier drift velocity along the high mobility conduction path to be maximized, but small enough for the impurity-limited drift velocity in the low mobility path to be a fraction of that at the high mobility (pure Si) side.

This third point is illustrated by Fig. 2, which shows drift mobility-field plots for electrons in pure bulk Si and in heavily compensated Si at 77 K. The compensated Si is of the type used in the devices discussed in Sec. III (donor density 2×10^{25} m^{-3}, acceptor density 1.99×10^{25} m^{-3}). At moderate fields along the Si channel $\sim10^5$ V m^{-1}, it ought to be possible to modulate the velocity by a factor of ~4 from impurity scattering alone. Because ionized impurity scattering events are elastic and small scattering angles are favored, at high electric fields and carrier kinetic energies this process has less impact on the electron mobility, hence the convergence of the two curves in Fig. 2.

From the outset, it is clear that a velocity modulation transistor of this kind would be most suitable as a fast, low power device. The results of Sec. III suggest that successful velocity modulation is limited to a small drain bias range over which charge in the channel can be well controlled. The



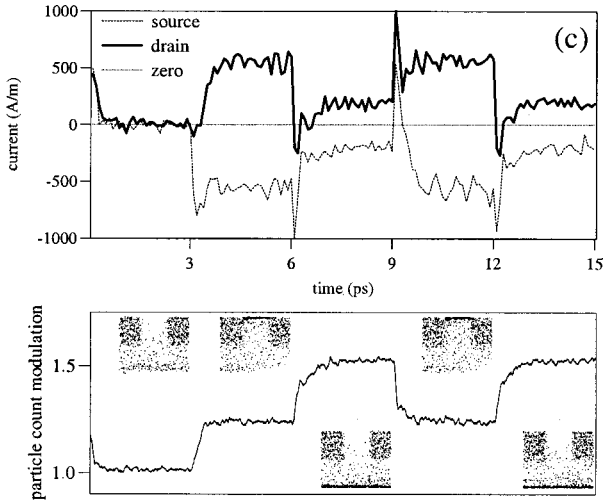


FIG. 3. Demonstration of current switching for three devices of the kind shown in Fig. 1, at a lattice temperature of 77 K. The velocity modulation transistors have a 0.1 μm top gate length and a 0.08 μm wide Si channel. The devices differ in their channel doping profile. In (a), heavily compensated doping is distributed under the top gate, halfway into the channel. In (b) compensated doping is placed above the back gate, again halfway into the channel. The doping level in both these cases is donor density 2×10^{25} m^{-3} and acceptor density 1.99×10^{25} m^{-3}. In (c), a higher background density of electrons is maintained above the back gate in an effort to reduce capacitive charging at the back gate side of the channel when the device operates in the low mobility mode. The simulation in (b), was carried out using a minimum of 4000 particles, but a minimum of 1000 was used to generate (a) and (c). At times $t<3$ ps, the unbiased devices are shown converging to their steady state. At $t=3$ ps, each device is switched into the high mobility regime, with a drain–source bias of 0.3 V and a top gate bias of 1 V. The back gate is unbiased. At $t=9$ ps, the gate biases are reversed, switching the transistor into the low mobility regime. This abrupt switching is repeated at 3 ps intervals. The small inset cartoons show the distribution of electrons in the device at $t=0,3,6,...15$ ps (unbiased, high mobility regime, low mobility regime, etc.).

optimum device design also has to be a compromise between fast switching [low resistance–capacitance (RC) time constant] and a large current modulation factor.

III. RESULTS AND DISCUSSION

Figures 3(a)–3(c) provide a comparison of the switching behavior of three devices which have similar geometry but different arrangements of the compensated doping. The parameters and bias conditions which are common to all three simulations are as follows. The Si channel thickness (back gate oxide to top gate oxide separation) is 80 nm, and the top gate extends 100 nm along the channel. The implants with n doping under the source and drain contacts are both 10^{24} m^{-3} and extend half way into the Si channel. For Fig. 3(a), the device has compensated doping in the top half of the channel not occupied by the contact implants (donor density 2×10^{25} m^{-3}, acceptor density 1.99×10^{25} m^{-3}). For Fig. 3(b) the compensated doping is identical to that of Fig. 3(a), but instead this doping occupies the lower half of the channel. The shorter current path through Si under the top gate serves as the high mobility side of the channel in this instance. The device of Fig. 3(c) is similar to that of Fig. 3(b), but the doping in a layer 10 nm thickness above the back gate is less compensated for (donor density 2×10^{25} m^{-3}, acceptor density 1.9×10^{25} m^{-3}). Note the greater background density of electrons in that for Fig. 3(b).

Figures 3(a)–3(c) show the results of a sequence of simulations at 77 K with different bias conditions applied at 3 ps intervals. At time $t=0$, each device is allowed to relax from an initial charge neutral state and it remains unbiased for 3 ps. At $t=3$ ps, each device is switched on with 0.3 V drain–source bias for the $t=3-15$ ps. However, gate biases are switched abruptly at 3 ps intervals. At $t=3$ ps, 1 V is placed on the top gate while the back gate is unbiased; at $t=6$ ps, the top gate is at 0 V and the bias applied to the back gate is 1 V, and so on. (Note: The gate biases are absolute, not relative, to the flat-band voltages.) The inset cartoons in Figs. 3(a)–3(c) show the spatial distribution of X-valley electrons in the Si channel at $t=3,6,...15$ ps.

Figure 3(a) is an example of poor current modulation. The device is also the most capacitive; when the back gate is forward biased relative to the top gate, excess electrons are injected and populate the back gate side of the device, with a time constant of at least 3 ps. Figures 4(a) and 4(b) show the electric displacement currents at the gates for the simulations of Figs. 3(b) and 3(a), respectively. Figure 3(b) is capacitive, but the turn on and the charging (discharging) times for switching from the high to low mobility (low to high mobil-

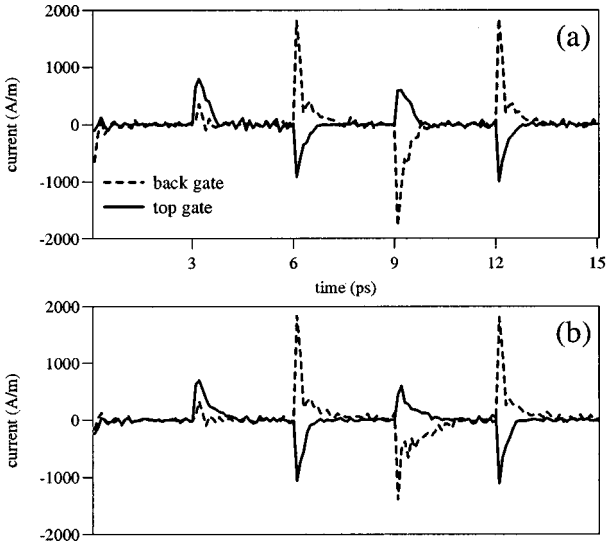


FIG. 4. (a),(b) Electric displacement current at the top and back gates for the 77 K simulations illustrated in Figs. 3(b) and 3(a), respectively.

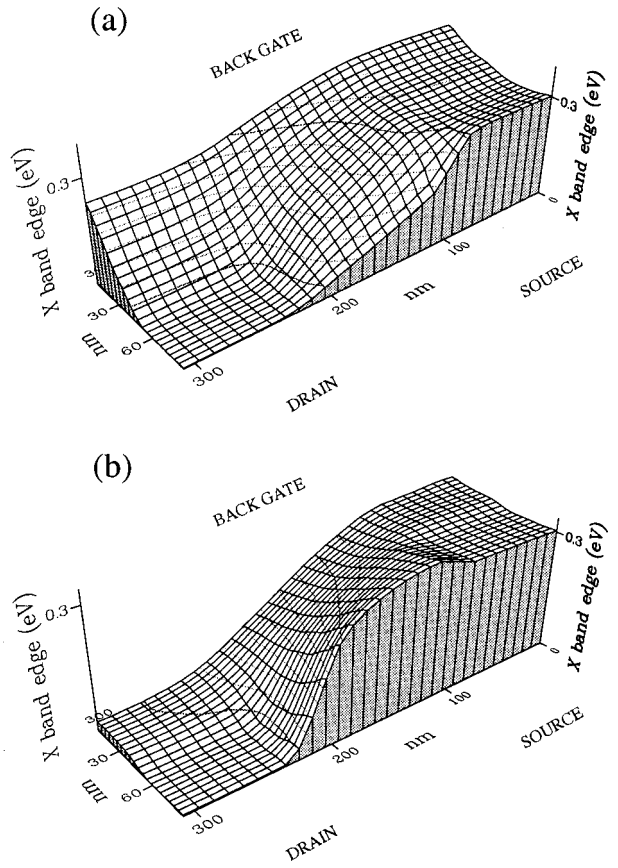


FIG. 5. Conduction band edge throughout the channel of the velocity modulation transistor illustrated in Fig. 3(b). The device is shown operating in the high mobility mode (a) with a drain–source bias of 0.3 V and and a top gate bias of 1 V, and also in the low mobility regime (b) with 1 V applied to the back gate and the top gate at 0 V.

ity) regimes are ~1.5 (1.0) ps. In addition, the current modulation factor is ~3. Note that at $t=9$ ps when the device is switched from the low to high mobility mode, there is a transient peak in the drain current (duration <0.5 ps), due to the expulsion of charge that occupied the back gate side of the structure. Figure 3(c) shows an attempt to reduce charging/discharging of the channel by having a higher background electron concentration at the back gate than for the device of Fig. 3(b). Comparison of Figs. 3(b) and 3(c) shows that, while the electron density modulation is reduced, there is no obvious reduction in the switching time and it does lead to a reduced high/low drain current ratio of 2. Note that longer time taken to establish stable field conditions at the back gate side of the channel in Fig. 4(b).

Having described the basic switching action of the Si velocity modulation transistor, Figs. 5–8 show some microscopic details of the more successful device illustrated in Fig. 3(b). Figure 5(a) shows the conduction band profile across the channel when a steady current flows through the top gate side of the channel (the drain–source bias is 0.3 V, the top gate bias is 1 V, and the back gate is unbiased). Note that the electric field along the top gate channel is $\sim 10^6$ V m^{-1} in this case. Figure 5(b) shows the band profile for the device operating in the ''low mobility'' regime, with 1 V applied to the back gate and 0 V at the top gate. Note that the steady drain–source electric field along much of the back gate side of the channel is also $\sim 10^6$ V m^{-1}. Figures 6(a) and 6(b) show the steady state electron densities that correspond to Figs. 5(a) and 5(b). It is clear that charge is switched satisfactorily from one side of the channel to the other. However, it is also interesting to note the small but significant background density of $\sim 10^{23}$ m^{-3} electrons under the contact doping at the drain end of the device that provides the principal path for electrons to leave the device when it is operating in the low mobility regime.

Figure 7(a) shows the electron flux along the source–drain direction (labeled the x axis) for the device operating in the high mobility regime, with a peak flux at the drain end of the top gate approaching 25×10^{28} m^{-2} s^{-1}. In contrast, the peak x-axis flux along the back gate side of the channel is $\sim 3\times 10^{28}$ m^{-2} s^{-1} [Fig. 7(b)]. The y-axis flux (the back gate to top gate direction) is also included [Fig. 7(c)]. Figures 8(a) and 8(b) show the average kinetic energies recorded for electrons detected at different positions in the channel, but some care must be taken when interpreting these data. In Fig. 8(a), carriers are clearly heated as they drift under the top gate, but a minority of electrons are heated up to the threshold for intervalley phonon scattering (~0.06 eV) and their final wave vectors are randomized such that they follow a parallel conduction path along the edge of the compensated side of the channel. The average kinetic energy recorded under the drain contacts in Figs. 8(a) and 8(b) is small, close to the average thermal energy at 77 K; this should not be interpreted as rapid cooling of the heated carriers by phonon scattering, instead most electrons under the drain are thermal carriers neutralizing the charge of the ionized donor centers. Although the drain–source electric fields along the top and back gate sides of the channel are comparable, clearly the compensated doping/rough oxide interface has some impact on the carrier mobility, because electrons drifting along the back gate side of the channel are less readily heated [Fig. 8(b)]. However, Fig. 8(b) also demonstrates that the heating of carriers that are drawn across the channel from the back to

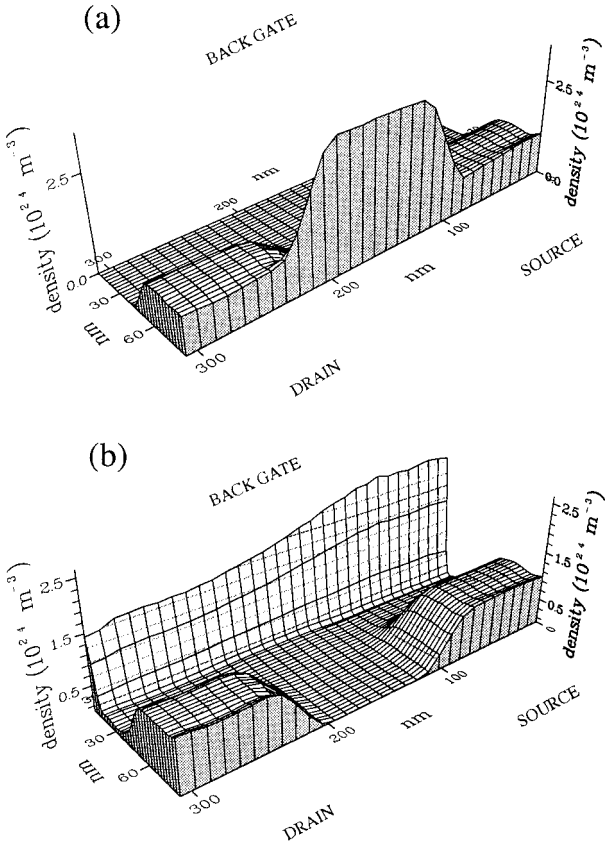


FIG. 6. Steady state electron density in the channel of the velocity modulation transistor illustrated in Fig. 3(b). The device is shown operating in the high mobility mode (a) with a drain–source bias of 0.3 V and and a top gate bias of 1 V, and also in the low mobility regime (b) with 1 V applied to the back gate and the top gate at 0 V.

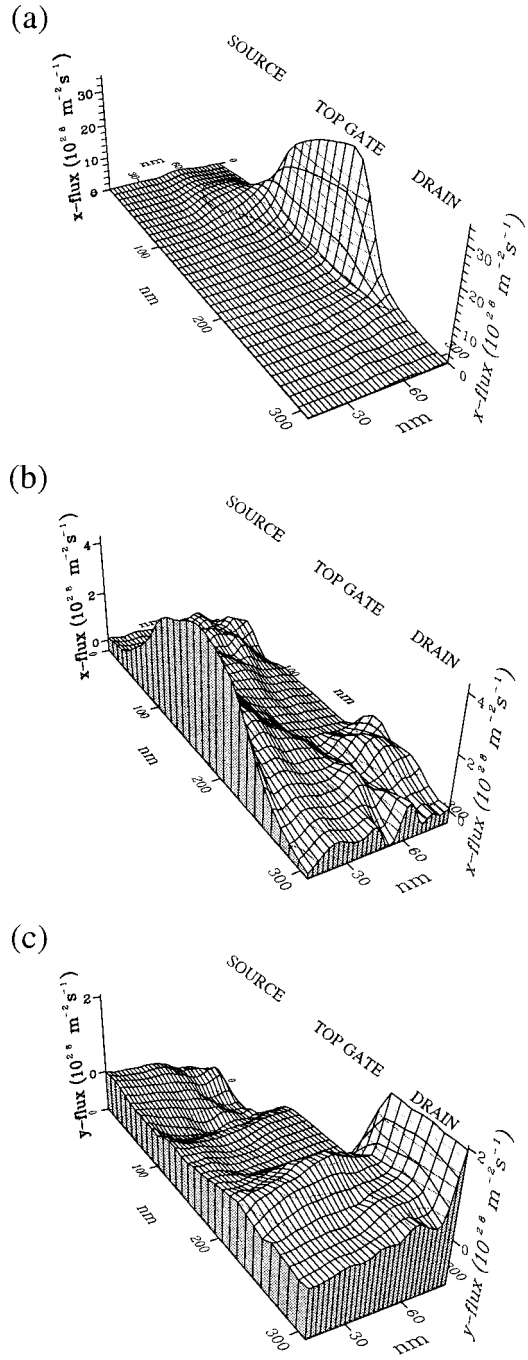


FIG. 7. Steady state electron flux in the channel of the device illustrated in Fig. 3(b). The source–drain direction is labeled as the *x* axis and the back gate–top gate direction is labeled as the *y* axis. The device operating in the high mobility mode and (b) and (c) correspond to the low mobility regime. The peak flux under the top gate of (a) is 10 times that at the back gate in (b). The drain–source bias is 0.3 V. The gate biases switch between 0 and 1 V.

the top gate is comparable to that of Fig. 8(a).

Further simulations have been carried out on the device of Fig. 3(b). A range of bias conditions has been studied in an effort to predict the current–voltage characteristics for the device operating in the low and high mobility regimes, and also the transconductance.

Figures 9(a) and 9(b) show current–voltage curves for simulations carried out at 77 K, with biases of 0.3–1 V applied to the back and top gates, respectively. Figure 9(c) shows the ratio of the steady currents flowing in the high and low mobility regimes as a function of drain–source bias. The scattered points show the current modulation factor that can be achieved at moderate gate bias, while the solid curve shows the higher modulation factor (i.e., more effective confinement to either side of the Si channel) that can be achieved with a combination of a larger (1 V) gate bias and a small (<0.2 V) drain–source bias. Estimates for the intrinsic transconductance in the high mobility regime [solid curve in Fig. 9(d)] and low mobility mode [dashed curve of Fig. 9(d)] have been calculated from the current–voltage curves for the device.

Finally, Fig. 10 shows the simulated current switching behavior at 77 K for the device of Fig. 3(b), which has compensated doping, placed above the back gate, extending halfway into the channel. The device is switched off (all metal contacts are unbiased) during the interval $t=0-3$ ps, and from $t=3$ ps a steady drain–source bias of 0.3 V is applied. However, instead of alternating the top and back gate biases between 0 and 1 V at 3 ps intervals, in this simulation the back gate is unbiased at all times, and only the top gate is switched between 0 (low mobility mode) and 1 V (high mobility mode). Similar current characteristics were obtained when the same voltage modulation procedure was simulated for a conventional MOS field effect transistor (MOSFET) with the same gate and channel lengths.

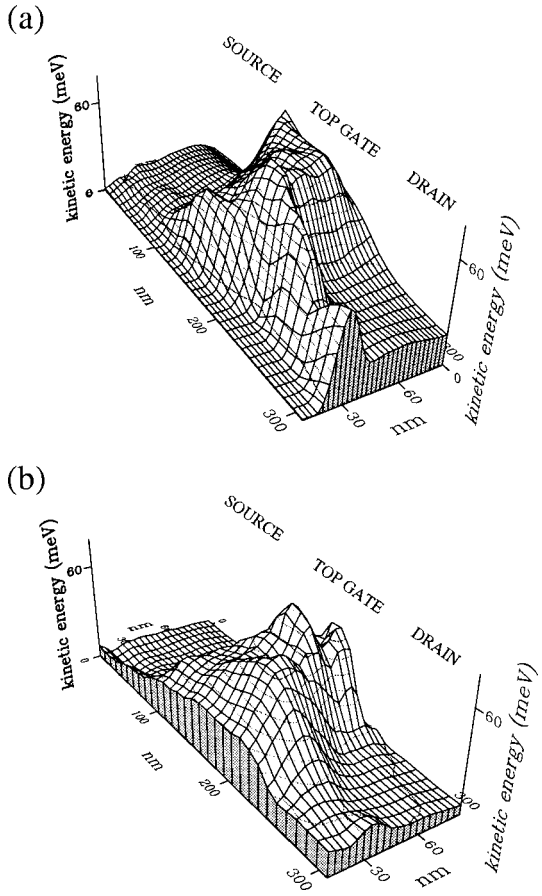


FIG. 8. Steady state electron kinetic energies recorded for different positions in the channel of the velocity modulation transistor illustrated in Fig. 3(b). (a) The high mobility mode with 1 V applied to the top gate; (b) the low mobility regime with 1 V on the back gate. Note the carrier heating under the top gate region of the channel in which the drain–source electric field is the largest for both cases.

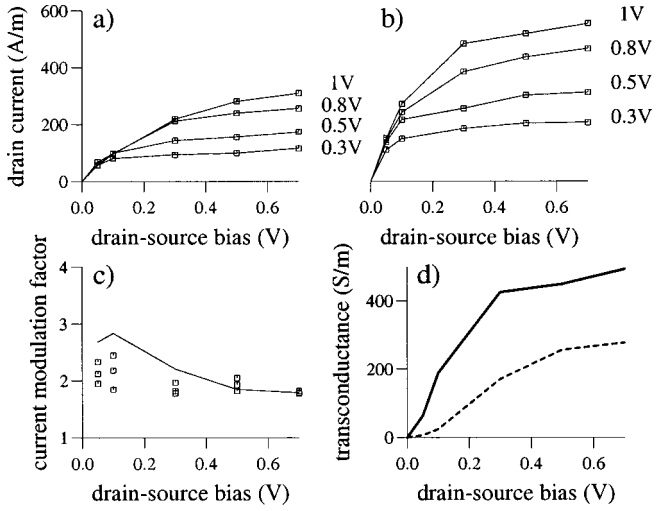


FIG. 9. Simulated current–voltage characteristics at 77 K for the device illustrated in Fig. 3(b) in the (a) low and (b) high mobility regimes. (c) The ratio of the steady currents recorded in the high and low mobility regimes, a quantity termed the ''current modulation factor.'' In (c), the solid curve shows the current modulation factor as a function of drain–source bias for the case of 1 V applied to the top or back gate. The transconductance for the intrinsic device operating in the high mobility (solid curve) and low mobility (dashed curve) modes.

In comparing Figs. 3(b) and 10, it should be noted that the turn on and switching times into the high mobility mode/high drain current mode are the same, ~1 ps. It is not clear if the velocity modulation regime offers faster switching into the low current ''off'' state, because the time taken to discharge the channel in Fig. 10 matches the charging time along the back gate in Fig. 3(b). This is in spite of the fact that carrier density modulation in the velocity modulation regime is roughly half that for conventional top gate modulation; any reduction in the capacitive term of the RC time constant has been offset by the increased resistance of the current path along the back gate.

IV. SUMMARY AND FURTHER WORK

A Monte Carlo simulation has been used to demonstrate drain current modulation in a Si velocity modulation transistor. Current switching between the top and back gate sides of the Si channel is sensitive to the drain/gate bias conditions and also to the doping profile in the channel. Rapid switching (1–1.5 ps) between high and low electron mobility modes can be achieved. There is significant charging/discharging of the channel (>20% variation in channel charge density) when switched between the two modes, but this is smaller than in the case of a conventional field effect transistor (~45%). The results suggest that the basic device could handle switching cycles of at least 300 GHz operating either in standard top gate modulation or in the velocity modulation mode. The main obstacle to good device operation in the velocity modulation regime remains the predicted current modulation factor, typically 2–3, obtained from a combination of heavily compensated doping and interface roughness

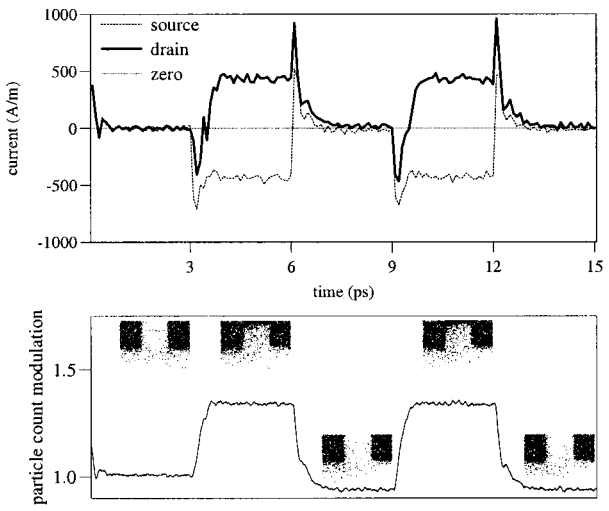


FIG. 10. Demonstration of current switching at 77 K for the device first shown in Fig. 3(b) with compensated doping placed above the back gate extending halfway into the channel. The device is switched off (unbiased) during the interval $t=0-3$ ps. From $t=3$ ps, a steady drain–source bias of 0.3 V is applied, but instead of swapping the top and back gate biases between 0 and 1 V at 3 ps intervals, the back gate is unbiased at all times, and only the top gate is switched between 0 and 1 V. The same voltage modulation procedure carried out on the equivalent short-channel MOSFET produced similar current switching behavior.

scattering. For velocity modulation to have a speed advantage over top gate modulation, it is clear that a way must be found to reduce the carrier density modulation still further.

There is potential for improvement in device performance by including strained SiGe layers within the device. A layer of compressive strained SiGe could provide a low mobility channel for electrons since they would suffer alloy scattering and mainly occupy $X4$ valleys (half of which have a large effective mass along the source–drain axis). However, the larger heterojunction offset between Si and SiGe presented to $X2$-valley electrons could create current switching difficulties if the electrons cannot readily tunnel between the two valley types across a Si/SiGe heterojunction. A preliminary simulation carried out on a design similar to that reported here suggests little benefit to current modulation, but further investigation is planned. It would be better to have a device put down on a SiGe virtual substrate. This would allow the possibility of a tensile strained Si channel, which offers the prospect of a high mobility conduction path for $X2$-valley electrons. The present difficulty with growing such a device, however, is that of producing an appropriate back gate within 100 Å of the conduction channel in a SiGe structure.

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