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Deposited in DRO:

17 December 2010

Version of attached file:

Published Version

Peer-review status of attached file:

Peer-reviewed

Citation for published item:

Further information on publisher's website:

Publisher's copyright statement:

Additional information:

Monte Carlo Simulations of High-Speed InSb–InAlSb FETs

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Abstract—Self consistent Monte Carlo simulations which include impact ionization are used to study the high-speed potential of InSb field-effect transistors. It is found that the impact ionization has a strong influence on the performance of InSb for high speed. The ionization leads to a high electron drift velocity and substrate bias can be used to extract the holes which are generated in the channel. Residual hole density within the channel, however, limits the maximum speed. The substrate bias and buffer doping are critical for extracting holes from the channel without inducing excess ionization. Simulations yield a peak cutoff frequency of 820 GHz with a 0.03125-μm gate, a source to drain voltage of 0.58, and a sheet doping density of 1.7×10^{12} cm^{-2}.

Index Terms—High-speed response, impact ionization, InSb, low power, MODFET, Monte Carlo simulation.

I. INTRODUCTION

InSb FIELD-EFFECT transistors (FETs) are of interest for low-power, high-frequency applications. The low bandgap with a very small electron mass and a very high mobility leads one to expect that a very high-speed response is possible for cooled transistors. At room temperature, however, the high energy tail of the thermal carrier distribution extends above the bandgap energy where impact ionization processes and Auger generation are possible. This leads to high leakage currents. By using minority carrier exclusion techniques and carrier extraction, it is possible to greatly reduce these leakage currents, making room-temperature operation feasible [1], [2]. Early work with a 1-μm gate enhancement-mode FET has suggested an intrinsic f_T of about 90 GHz [2]. More recent work concentrating on reducing parasitics has demonstrated an f_T of 74 GHz with a 0.7-μm gate [3]. This latter work has also presented drift diffusion simulation results suggesting that a very high-frequency response approaching 1 THz may be possible with sub–0.1 micrometer gates. Very recent work using quantum-well channels has reaffirmed the prediction of an f_T of 1 THz for a 0.1-μm gate [4]. This prediction neglects hot-carrier overshoot effects which might lead to even better high-frequency performance, however, it is not clear how the impact ionization has been included in the modeling, and whether low mobility holes in the channel will degrade the response. One aim of the present work is to include hot-carrier

transport and ionization by using a Monte Carlo approach. It should be noted, however, that although InSb has the higher saturated drift velocity, the InP-based high-electron mobility transistors (HEMTs), have given the highest measured f_T values to date. For example, a 550–GHz pseudomorphic InP-HEMT using a 30–nm gate has been reported by Shinohara *et al.* [5].

In this paper, we use the self-consistent SLURPS two-dimensional Monte Carlo code [6] to explore the factors limiting the very high-frequency response of narrow bandgap FETs. It is clear that inclusion of impact ionization is essential for realistic studies and suitable subroutines have been added to the SLURPS software to make this possible. We have chosen to focus on the InSb–InAlSb material system and find that controlling the ionization through doping profile and substrate bias is critical for achieving high-frequency response. This is particularly the case as the channel sheet charge density is raised to reduce channel resistance and minimize gate fringing fields. The resulting potential drop at the drain side of the gate leads to strong ionization effects. To control these effects we find it necessary to limit the source/drain bias to less than 0.6 V and use a substrate-source bias of about -1.0 V. If defects and impurities reduce the channel mobility, then the carrier heating in the high field at the drain edge of the gate becomes less effective and the bias constraints are relaxed. The presence of Al in the channel region also reduces the mobility and therefore the speed, but increases the bandgap and therefore reduces the ionization. If the highest speeds are not a priority then using a low concentration of Al for the channel region could be a useful option.

II. VELOCITY-FIELD CHARACTERISTICS

In Fig. 1, we show the computed velocity-field characteristics for InSb. The calculation included Γ, X, and L electron valleys and HH and LH valence bands. The results were calculated at room temperature using electron material parameters assembled from data in [7]–[10] and listed in Table I. SLURPS obtains the material parameters for the alloys used in transistor modeling, by interpolating between the values for InSb and AlSb so parameters for both materials are listed in Table I. It should be noted that there remains some considerable uncertainty for the values of hot-carrier material parameters. For the Γ–X and Γ–L intervalley phonon scattering coupling constant, we have used 5×10^{10} eV/m, a typical value for III-V compounds, from estimates based on pseudopotential wavefunctions [11], [12]. The indirect gap for InSb used here is also smaller than reported in earlier pseudo-potential band structure calculations [13]. Velocity-field calculations using a wider indirect gap, however, gave similar results to Fig. 1, but with a gradually increasing
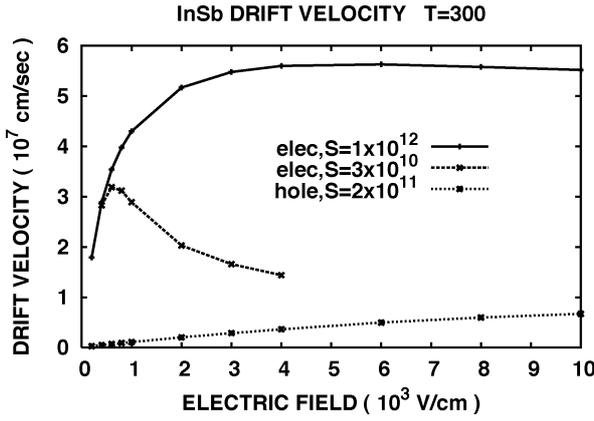
Fig. 1.   Velocity-field curves for InSb at room temperature.

TABLE I
ELECTRON MATERIAL PARAMETERS

Material	InSb	AlSb
Lattice const (Å)	6.48	6.136
Density (kg m^{-3})	5790	4288
Direct gap (eV)	0.174	2.3
Indirect gap Γ-X (eV)	0.456	-0.684
Indirect gap Γ-L (eV)	0.756	-0.09
m_Γ^*	0.013	0.14
m_Γ^*-non-parab (eV^{-1})	5.6	0.32
m_X^* long.	1.357	1.357
transv	0.123	0.12
m_L^* long.	1.64	1.64
transv.	0.23	0.23
ε_0	17.65	12.04
ε_∞	15.68	9.88
Sound vel (m s^{-1})	4060	4600
LO phonon energy (meV)	28.2	36.0
Acoustic deformation (eV)	5.96	4.5
IV deformation (eV/m) Γ-X	5x10^{10}	5x10^{10}
Γ-L	5x10^{10}	5x10^{10}
L-X	1x10^{11}	1x10^{11}

drift velocity rather than the weak tendency toward negative differential mobility shown in Fig. 1 at the highest fields considered with $S = 1 \times 10^{12}$ s^{-1}. This indicates that the electron transport is dominated by the gamma valley where the material parameters are well established and is fairly insensitive to the other, more uncertain material parameters, associated with the satellite valleys.

Fig. 2 shows the computed impact ionization coefficients. A Keldysh form for I, the ionization scattering rate, was used

$$I = S \left(\frac{E - E_{\text{th}}}{E_{\text{th}}} \right)^2 \qquad (1)$$

where S is the rate constant. The ionization coefficient is obtained by dividing the averaged value of I by the drift velocity and is a measure of the number of ionization events per unit length. There is uncertainty concerning the appropriate value for S. We favor a value of $S = 1 \times 10^{12}$ s^{-1} for electrons, with the threshold energy E_{th} taken as 1.08 E_g where E_g is the direct gap. The hole ionization calculation used $S = 2 \times 10^{11}$ s^{-1} and

Fig. 2.   Impact ionization coefficients for InSb at room temperature.

$E_{\text{th}} = 1.5 \, E_g$. In a previous work on detectors [16], we found that these values gave good agreement with measured ionization data in both InSb and CdHgTe with a similar band gap. The lowest threshold energies are estimated by using energy and wave vector conservation, assuming that the electron ionization involves the conduction band and heavy hole band and the hole ionization involves the light hole band and conduction band. Electron ionization dominates over hole ionization within the transistor channel. It is however important to allow for the weak hole ionization in the bulk of the buffer region as this generates electrons which then avalanche while flowing toward the drain. For electrons, a value of $S = 2 \times 10^{12}$ s^{-1} has been obtained by fitting (1) to experimental data on photo-quantum efficiency [14]. A first principles calculation, however, has yielded a much smaller value of about 3×10^{10} s^{-1} [15]. This latter calculation used zero field wave functions and we would expect that the very small electron mass and bandgap will make the observable value of S very sensitive to electric fields, both applied and from random charged impurities and defects, through the associated band tailing. This implies that fitting S to experimental data should give the most reliable values. To check on the sensitivity to S we have included some electron drift velocity and ionization coefficient calculations obtained with the smaller value of S in Figs. 1 and 2. It is interesting to note that the ionization coefficient, which controls the carrier generation, is fairly insensitive to the precise value of S at the highest fields where the ionization is dominating the energy relaxation and electrons are predominantly in the Γ valley. A major effect of reducing the value of S, however, is an increase in the rate of electron transfer to satellite valleys and consequently a strong negative differential mobility with reduced drift velocity. Reference [4] quotes a measured saturation velocity $> 5 \times 10^7$ cm s^{-1} which from Fig. 1 would favor the higher value for S.

In Fig. 1 we see that by using the high value for the electron ionization coefficient, impact ionization prevents a large intervalley transfer and keeps the carriers within the Γ-valley where the low mass leads to a high drift velocity. This result has some similarity to a "high field Ohms law" effect obtained in wider gap materials [17], in that the ionization by cooling the carriers, leads to velocity enhancement. From Fig. 2 it is striking that for low electric fields the electron ionization dominates the hole ionization with implications for low noise avalanching structures.
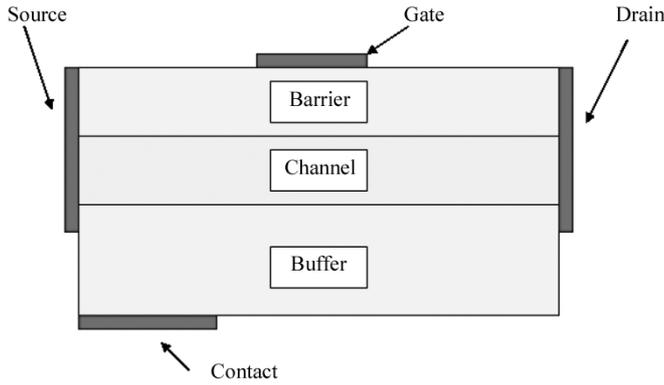
Fig. 3. Schematic geometry for the SLURPS transistor model. The detailed layer structure for barrier, channel and buffer are given in Table II. The source-to-drain separation was taken as 3.0 μm.

TABLE II
LAYER STRUCTURE USED IN SLURPS MATERIAL $In(x)Al(1-x)Sb$, DOP DENOTES DOPING IN THE SUPPLY LAYER

x	Thickness (μm)	Doping(cm^{-3})	Function
0.6	3.75×10^{-3}	1×10^{15} N	Barrier
0.6	3.75×10^{-3}	dop (3.0×10^{18}) N	Doped Barrier
1.0	2.25×10^{-2}	1×10^{15} N	Channel
0.94	3.75×10^{-2}	1×10^{15} P	step grade buffer
0.9	5.25×10^{-2}	1×10^{15} P	step grade buffer
0.8	3.125×10^{-2}	1×10^{15} P	step grade buffer
0.8	3.906×10^{-2}	dop1 (1×10^{17}) P	Doped buffer
0.8	3.2×10^{-1}	1×10^{15} P	Buffer
0.8	1.09×10^{-1}	1×10^{17} P	contact layer

III. TRANSISTOR MODELLING

To model the InSb-InAlSb transistors we used the approach described previously for AlGaN transistors [6]. A source-to-drain separation of 3 μm was used with the Schottky gate electrode located on the surface of the wide gap InAlSb barrier material, midway between source and drain. This barrier material contains a heavily doped layer to supply carriers to the narrow gap InSb channel material. A P-type buffer with substrate contact is used both to allow hole injection within the Monte Carlo model and to extract the holes generated in the channel by impact ionization. A schematic of the SLURPS model geometry is shown in Fig. 3. The 3–μm separation of source and drain was modeled with 192 mesh points. The barrier and channel regions perpendicular to the surface to a depth of 0.12 μm were modeled with 32 mesh points and the remaining 0.5 μm of buffer depth was modeled with 64 mesh points. Finer meshes were not possible due to memory limitations with our current machines.

Initial explorative modeling suggested that both channel ionization and buffer ionization could be problematic. At low substrate bias, holes generated in the channel tend to flow through the channel toward the source. Low breakdown voltage then results and the holes slow the transistor response. It was observed that in this situation, excessive charge was injected from the source contact to maintain charge neutrality. This electron charge led to further ionization with a positive feedback loop causing breakdown. This effect was eliminated by increasing the substrate reverse bias to an optimum value of about −1.0 V. To minimize spurious hole ionization in the buffer, the Al concentration was increased gradually in layers below the InSb channel toward the substrate. For modeling convenience the Al concentration was increased in steps. Increasing the negative bias much beyond −1.0 V caused avalanche breakdown as the electrons resulting from weak hole ionization in the buffer material, flowed toward the drain.

The layer structure used for the first simulations is shown in Table II. A value of $(1-x)$, the Al fraction, was taken as 0.4 for the barrier material supporting the gate electrode. This barrier material consisted of two layers of thickness 3.75×10^{-3} μm. The top layer was low doped and the second layer was used to supply carriers to the channel. The doping in this second layer (dop) was varied to obtain high f_T and remote impurity scattering was neglected. The barrier thickness was chosen to be about 0.24 of the smallest gate length to be considered (0.031 μm) in order to minimize spreading of the gate field within the channel. Simulations varying barrier thickness indicated that this was adequate for the present structures. For convenience this barrier thickness was retained for the various gate lengths considered. It may be difficult to fabricate such a thin barrier layer and thicker layers may be suitable in practice for longer gates, but in this paper, we are aiming to establish potential high-frequency limits. In practice recessed gate structures would be employed for the short gate length transistors. The channel thickness was fixed at 2.25×10^{-2} μm and below the channel three layers are used to step grade the material toward a composition of $x = 0.8$. The value of $x = 0.8$ and $x = 0.4$ used for buffer and barrier respectively are not critical and are chosen to give effective modulation doping and suppression of buffer hole ionization. Fabricated transistors have been reported with $x = 0.85$ for both buffer and barrier [3], [4] and for practical designs it may be desirable to increase the value of x used in our simulations in order to achieve pseudomorphic growth of the strained channel and barrier material. For convenience the simulations also place the Schottky gate directly on the barrier material while in practice a layer of SiO_2 may be used to separate the gate metal from the semiconductor. Below the step grading layers we have included a P-doped layer, with variable doping density dop1, which has the effect of increasing the field driving holes away from the channel. It turns out that the value of this doping density is important for preventing the hole flow toward the substrate generating a self-consistent hole potential barrier below the channel. If the doping is too low, this potential barrier acts to increase the residual hole density within the channel and consequently reduces the transistor speed. The initial value used for dop1 is given in brackets in Table II. Our final result for the maximum obtainable f_T is obtained by simultaneously tuning the values of dop and dop1. In this case, an optimal substrate bias value of $V_{sub} = -1.0$ V, together with the optimized doping layer within the buffer, overcomes the residual potential barriers from the step grading and the potential barrier resulting self-consistently from the hole flow. Below the p-doped layer we include a low doped layer and a doped contact layer. The total thickness below the channel is 0.55 μm.

To compute the cutoff frequency f_T for various transistor structures, we applied a harmonic voltage with amplitude of 0.05 V to the gate electrode and computed the terminal currents for times exceeding 50 periods. The harmonic component of the currents was extracted by using Fourier integration and the current gain, defined as drain current $I_d(\omega)$ divided by gate current $I_g(\omega)$ at frequency ω, was averaged over the periods. The gain was computed for several frequencies spanning the unit gain value. f_T was then obtained by interpolation. The error in f_T was estimated to be typically less than 5% for the number of periods used in the simulations. We found that plotting gain in dB against frequency on a log scale approximated quite well to a straight line as commonly assumed for extrapolating experimental data to estimate f_T. In this paper, however, we always interpolate to estimate f_T.

In general for the InSb transistors we found that f_T increases with increasing drain bias until the transistor gets close to breakdown. The sharp potential drop at the drain edge of the gate also increases in magnitude with increasing drain bias. This leads to increases in velocity under the gate and velocity overshoot and also increases the effect of ionization on the drift velocity. In practice we found that a drain to source bias $V_d = 0.58$V was close to optimum.

In Section IV we present detailed results using a value of dop1 equal to 1×10^{17} cm^{-3} in order to illustrate the various effects which can limit the frequency response. We then consider tuning both dop and dop1 in order to estimate the maximum available f_T.

IV. RESULTS

We initially settled on the layer structure shown in Table II, where the doping in the supply layer was chosen to maximize f_T for fixed buffer doping. Fig. 4 shows results for the variation of f_T with supply layer doping for gate length $L_g = 0.03125$ μm and bias voltages $V_s = 0$, $V_d = 0.58$, $V_{sub} = -1.0$, and $V_g = -0.1$. It is seen that f_T peaks for a doping density of about dop $= 3.0 \times 10^{18}$ cm^{-3} which corresponds to a sheet density of 1.125×10^{12} cm^{-2}. The source and drain currents are also shown on the plot and it is seen that the difference, Id-Is increases with supply layer doping. This corresponds to increasing current injection from ionization and the decrease in f_T above the peak is caused by increasing hole density within the channel flowing toward the source. This interpretation was confirmed by further calculations in which the electron-hole injection due to ionization was turned off. The cooling effect of the ionization for increasing the electron drift velocity was retained so that the correct electron drift velocity is used. The results are shown in Fig. 5 and do indeed give higher values for f_T, confirming that the hole injection is limiting the high-frequency performance. It is interesting to note that for the doping density of 3.0×10^{18} cm^{-3}, the f_T in Fig. 5 is very close to the maximum of 690 GHz obtained with electron-hole injection. This indicates that the hole extraction process is working well at this value of dop. The peak in f_T with no electron-hole injection was, however, shifted to the higher value of 936 GHz at the higher doping level of dop $= 6.0 \times 10^{18}$ cm^{-3}.
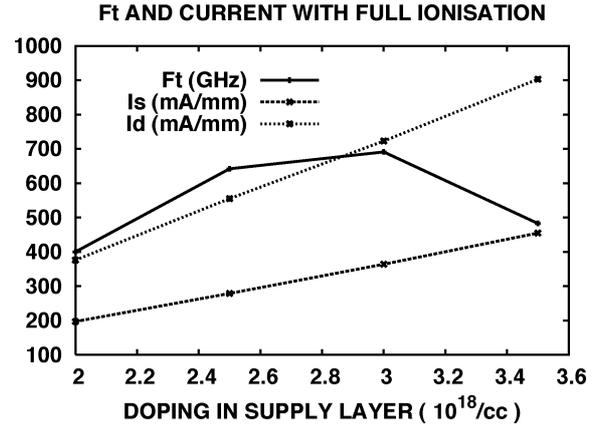
Fig. 4. Dependence of cutoff frequency on doping density in the supply layer of Table II. The simulations were performed at room temperature and included both electron and hole ionization. The bias voltages were $V_s = 0$, $V_d = 0.58$, $V_g = -0.1$, $V_{sub} = -1.0$. The buffer doping was dop1 $= 1.0 \times 10^{17}$ cm^{-3}.
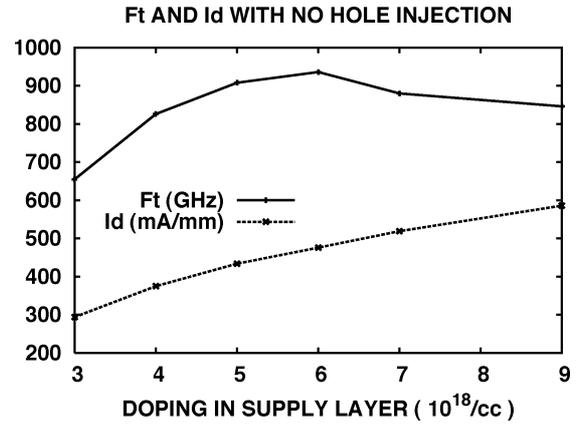
Fig. 5. Variation of cutoff frequency with doping, dop in the supply layer of Table II. These simulations were performed at room temperature and excluded electron-hole injection from the ionization process. The effect of ionization on the electron drift velocity was allowed for. The results indicate the high-frequency potential from the high electron drift velocity. The bias voltages were $V_s = 0$, $V_d = 0.58$, $V_g = -0.1$, and $V_{sub} = -1.0$.

To try to understand the peak f_T for no electron-hole injection as shown in Fig. 5, we have plotted the potential variation along the channel from source to drain obtained with no electron-hole injection, for different values of doping. The results used the optimum bias of $V_g = -0.1$, $V_d = 0.58$, $V_{sub} = -1.0$. The results in Fig. 6 show the variation of potential energy (or conduction band edge) along a line six mesh points (0.0225 μm) from the surface with the source as origin. It appears that the potential drop between gate and drain, which corresponds to a channel resistance, falls with increasing values of dop up to about 6.0×10^{18} cm^{-3}, which correlates well with the increase in high-frequency performance. The magnitude of the sharp potential drop at the drain side of the gate also varies with doping and affects the electron drift velocity under the gate. For values of dop above 6.0×10^{18} cm^{-3}, the gate to drain resistance appears unchanged but the magnitude of the sharp potential drop at the drain edge of the gate decreases, which will reduce the velocity under the gate. There is also a noticeable increase in the
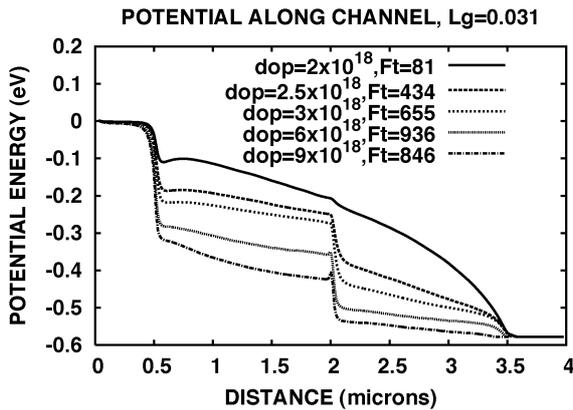
POTENTIAL ALONG CHANNEL, Lg=0.031

Fig. 6. Variation of potential energy (conduction band edge) along the channel from source to drain at a distance of 0.0225 μm from the surface. The source contact metal is located at the origin and the flat potential region corresponds to a heavily doped contact layer. The gate is located midway between the source and drain at 2 μm. The bias voltages were $V_s = 0$, $V_d = 0.58$, $V_g = -0.1$, and $V_{\text{sub}} = -1.0$. This calculation switched off the electron-hole generation but included the effect of ionization on the electron drift velocity. The buffer doping was dop1 $= 1.0 \times 10^{17}$ cm^{-3} and curves are shown for a range of values of dop, the supply layer doping.

source to gate channel resistance for dop$> 6.0 \times 10^{18}$ cm^{-3}. The channel resistance affects the f_T through the RC time constants [5] and the behavior of f_T in Fig. 5 can be explained as caused by a combination of channel resistance and drift velocity variation. It is interesting to note that there is a sharp potential drop at the source end of the channel between the heavily doped contact region and the intrinsic channel region. This high field region also causes ionization, but the generated holes immediately flow into the heavily doped source contact region and have no effect on the transistor speed.

The case with electron-hole generation fully allowed for is more complicated. The hole current flowing toward the substrate contact leads to an Ohmic potential drop and the positive space charge from holes below the channel can cause a weak repulsive hole potential which retards the hole flow away from the channel. This results in a buildup of hole charge within the channel which flows toward the source contact. The slow moving holes then degrade the frequency response. These effects can be seen in Fig. 7 which plots the variation of the valence band edge with position in a direction from gate to substrate. The different curves correspond to different values of dop and dop1 and are obtained with the optimum bias for the 0.03125-μm gate transistor. One curve shows the result with no electron-hole injection and in this case the valence band edge rises to its value at the substrate contact with no de-biasing. The curve labeled "dop $= 3.0$" (units of 10^{18} cm^{-3}), corresponds to the peak f_T in Fig. 4 and the curve labeled "dop $= 3.5$" corresponds to the situation where f_T has fallen from its peak value. It can be seen that a weak hole repulsive potential barrier has developed below the channel confirming our explanation of the peak f_T. It should be noted that the potential has been plotted such that electrons flow "downhill" and holes flow "uphill" in this paper. The remaining curve shows results where dop has been increased to 5.0×10^{18} cm^{-3} and dop1 has simultaneously been increased to 3.5×10^{17} cm^{-3} in order to maximize f_T with respect to both of these parameters. In this case, the

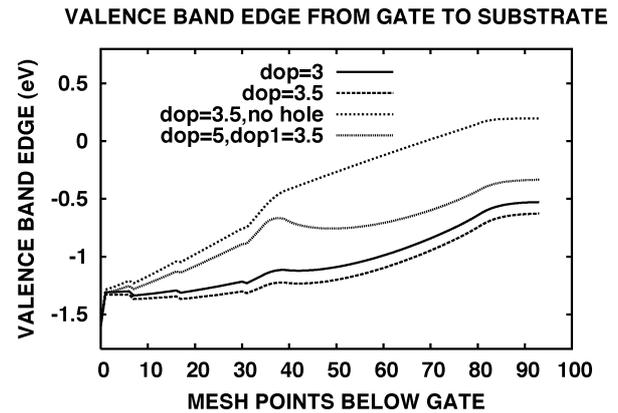**VALENCE BAND EDGE FROM GATE TO SUBSTRATE**

Fig. 7. Variation of valence band edge with position along a direction from gate to substrate. The potential is defined such that holes flow up hill. Dop (units 10^{18} cm^{-3}) and dop1 (units 10^{17} cm^{-3}) are defined in Table II. The case with no electron-hole injection is labeled "no hole."
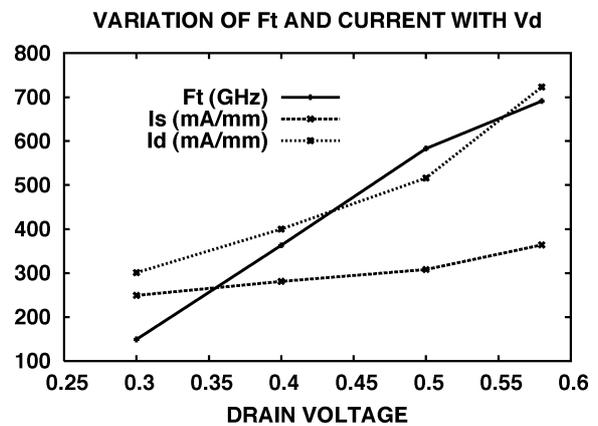
VARIATION OF Ft AND CURRENT WITH Vd

Fig. 8. Variation of f_T with V_d using $V_{\text{sub}} = -1.0$, and $V_g = -0.1$. $L_g = 0.03125$ μm and dop $= 3.0 \times 10^{18}$ cm^{-3}, dop1 $= 1.0 \times 10^{17}$ cm^{-3}. The fixed bias voltages were $V_s = 0$, $V_g = -0.1$, $V_{\text{sub}} = -1.0$. The calculation included electron-hole injection.

p-doping in the buffer layer dop1 is sufficient to overcome the hole flow retarding barrier.

The justification for using a drain voltage of 0.58 V is given in Fig. 8. We show results for f_T as a function of drain voltage obtained with electron-hole injection for gate length $L_g = 0.03125$ μm and a supply layer doping of 3.0×10^{18} cm^{-3}. We see that f_T increases linearly with V_d at low voltages and flattens out for $V_d > 0.5$ V. In practice, 0.58 V is close to optimum. Using higher drain bias takes the transistor too close to breakdown.

Having set the doping density and bias values as dop $= 3.0 \times 10^{18}$ cm^{-3}, dop1 $= 1 \times 10^{17}$ cm^{-3}, $V_d = 0.58$, $V_{\text{sub}} = -1.0$, $V_g = -0.1$, we performed a series of calculations of f_T keeping the geometry and bias voltages fixed but varying gate length. The results in Fig. 9 show the flattening of performance at very short gate lengths which we interpret as caused by increasing hole density in the channel, flowing toward the source. It is also noticeable that the source and drain currents start to increase quite rapidly for very short gate lengths. This implies an increasing hole current flowing toward the substrate with associated debiasing and the possibility of a weak self-consistent barrier developing to impede the flow.
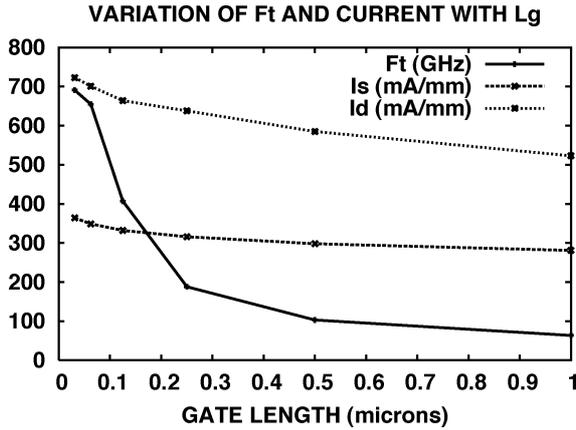
VARIATION OF Ft AND CURRENT WITH Lg

Fig. 9. Variation of f_T with gate length at room temperature. The bias voltages were $V_s = 0$, $V_d = 0.58$, $V_g = -0.1$, $V_{sub} = -1.0$. Doping values were $dop = 3.0 \times 10^{18}$ cm^{-3}, $dop1 = 1.0 \times 10^{17}$ cm^{-3}. Electron-hole injection from ionization is included.

CURRENTS Lg=0.03125 Vg=-0.1 Vsub=-1.0

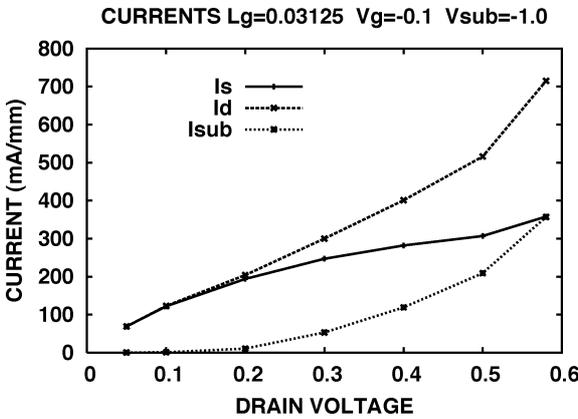Fig. 10. Steady-state currents for the 0.03125 μm gate transistor. The fixed biases are $V_g = -0.1$, $V_{sub} = -1.0$. Doping values were $dop = 3.0 \times 10^{18}$ cm^{-3}, $dop1 = 1.0 \times 10^{17}$ cm^{-3}.

The steady-state currents for the 690–GHz transistor are shown in Fig. 10. The fixed bias voltages were $V_g = -0.1$, $V_{sub} = -1.0$. The sheet doping in the supply layer was 1.125×10^{12} cm^{-2}, the gate length was 0.03125 μm and dop1 was 1×10^{17} cm^{-3}. It is seen that the ionization current sets in for $V_d > 0.2$ V. The source current gradually increases over the entire range of drain voltage. For $V_d > 0.4$ V this is in part caused by some holes flowing into the source contact. The predominant hole current, however, flows to the substrate as indicated by the larger slope of the substrate and drain currents. This indicates that the substrate bias is effective in extracting the ionization induced holes.

If the substrate voltage is reduced to -0.5 V with $V_d = 0.58$ V and $V_g = -0.1$ V then the efficiency of hole extraction is reduced, the hole current flowing to source increases and the transistor breaks down. This breakdown occurs on a timescale which is noticeably longer than conventional avalanche breakdown. We think that this is caused by the process of carrier injection from the source contact required to maintain charge neutrality with the slow moving hole charge in the channel. The source injected electrons induce more holes by ionization creating a positive feed back loop. A similar breakdown process has been described in the literature for short channel Si MOSFETs where it is explained as a parasitic
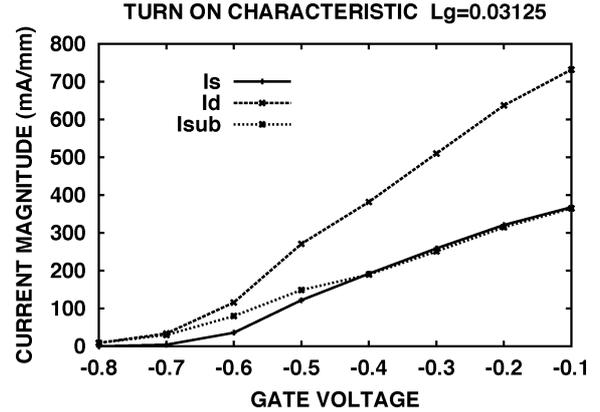
TURN ON CHARACTERISTIC Lg=0.03125

Fig. 11. Turnon currents for the 0.03125-μm gate transistor. dop= 3.0×10^{18} cm^{-3}, dop1 = 1.0×10^{17} cm^{-3}, $V_d = 0.58$ V, and $V_{sub} = -1.0$ V.

n-p-n (source-substrate-drain) bipolar transistor action with the source/substrate junction forward biased by hole current flowing to source [19], [20].

In Fig. 11 we plot the turnon currents for the $L_g = 0.03125$ μm, 690-GHz transistor. The pinchoff voltage is around -0.7 V. It can be seen that the substrate current locks to the drain current near pinch off. This is caused by the source current being blocked by a potential barrier in the channel under the gate. The residual ionization current flows such that the holes move to the substrate contact and the electrons move to the drain contact. It is interesting to note that the substrate current locks to the source current for gate voltages above about -0.4 V. This effect is not observed for lower drain voltages and is thought to indicate that the current multiplication in the high field region close to the gate happens to be close to two. The result indicates that the channel current multiplication is independent of gate voltage for $V_g >= -0.4$ and that the generated holes are flowing predominantly toward the substrate, away from the channel as required for high speed operation.

Having observed that the high-frequency performance is limited by an increasing hole density within the channel, which in turn is caused by debiasing and the formation of a weak hole potential barrier below the channel, it was a simple matter to adjust dop and dop1 simultaneously in order to maximize f_T. In this way, we estimated the optimum values as dop = 4.5×10^{18} cm^{-3}, dop1 = 4.0×10^{17} cm^{-3} which yielded $f_T = 819$ GHz. This value is still significantly below the 936 GHz obtained with no electron-hole injection and indicates that a small residual hole charge remains in the channel, degrading the performance. In practice, however, we expect that the technical difficulty of fabrication and elimination of parasitics will dominate any further development so that loss of the last 10% of potential performance may not seem so important!

V. CONCLUSION

Extensive self consistent Monte Carlo simulations are reported for the InSb material system at room temperature. It is found that impact ionization, by cooling electrons and reducing intervalley transfer to low mobility satellite valleys, leads to unusually high drift velocities. This high saturated drift velocity can be exploited in FETs by optimising the substrate bias and buffer doping to extract holes generated in the channel. The very high-frequency performance expected from electron drift

velocities alone is however limited by residual hole charge in the channel. The peak f_T for a 0.03125 μm gate is predicted to be about 820 GHz which is well above the demonstrated 550 GHz for a 0.03-μm gate in the InP material system. It should be noted, however, that in practice channel mobility can be reduced from the ideal and parasitics can limit the highest frequency response so that comparing an ideal theoretical number with an experimental value may be unduly optimistic. If one could completely remove the ionization induced holes from the channel, then the peak f_T could be increased to around 940 GHz according to Fig. 5. For the structures considered in this paper this does not appear possible. One could perhaps consider quantum well channels to exploit the higher 2 DEG mobility and better carrier confinement [4], however in this case the confining barriers may also impede the hole flow away from the channel and degrade performance. The predicted peak f_T for the structures considered is impressive, confirming that this material system has the potential for extremely high speed low power devices, in overall agreement with the conclusions of other authors [3], [4].

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G. C. Crow, photograph and biography not available at the time of publication.

M. Walmsley, photograph and biography not available at the time of publication.