Cape Peninsula
University of Technology

DESIGN AND DEVELOPMENT OF A FUEL CELL POWER SUPPLY UNIT

by

MAKANI MWINGA

Thesis submitted in fulfilment of the requirements for the degree

Master of Engineering: Electrical Engineering

in the Faculty of Engineering

at the Cape Peninsula University of Technology

Supervisor: Mr B. Groenewald
Co-supervisor: Prof M. McPherson

Bellville Campus
MAY 2017

DECLARATION

I, Makani Mwinga, declare that the contents of this dissertation/thesis represent my own unaided work, and that the dissertation/thesis has not previously been submitted for academic examination towards any qualification. Furthermore, it represents my own opinions and not necessarily those of the Cape Peninsula University of Technology.

Makani Mwinga — **19th MAY 2017**

Signed — **Date**

ABSTRACT

Fuel cell (FC) technology is one of the most sought-after renewable energy technology. However, the output voltage of FC stacks is inherently unstable; as such, it is of little or no use for most power supply applications. In addition to the unstable output voltage, FC stacks are susceptible to high current ripple, which can reduce the system's life expectancy. The work carried out in order to stabilise the output voltage, and to reduce the current ripple of FC stacks involves a review of some existing converter topologies used for power conditioning units (PCUs), modelling, design, control and simulation of different converter topologies and the experiment of the prototype circuit for the interleaved boost voltage multiplier (IBVM) converter topology. In the process to stabilise the stack output voltage and to reduce the stack output current ripple, it is also required to improve the system response to load changes. This work presents results that show that system works, with the voltage stabilised, the stack output current ripple reduced and the response time reduced.

A relative evaluation of the dynamic behaviour of four converter topologies in power conditioning units is carried out, and these are the isolated current-fed full-bridge (ICFFB) converter, the boost converter, the sepic converter and the IBVM converter. The simulation results of the four topologies show that the output voltage of a PEMFC stack was stabilised, and that the IBVM topology is a better topology compared to the others, especially when it comes to reducing the stack current ripple.

ACKNOWLEDGEMENTS

I wish to thank:

- My supervisor and co-supervisor, Mr B. Groenewald and Prof M. McPherson for their support, guidance, advice, and patience during the course of the research. I would also wish to thank them, specifically, for the financial assistance rendered during each registration period, for the guidance on the write up of the thesis, for the provision of materials required to build a prototype circuit for the research work and for their continued willingness to assist. Furthermore, I wish to thank them for sending me to CHARISMA conference and ENTECH'14 conference, and for the guidance in the preparation of the presented and published work.

- Dr G. Arendse for the financial assistance rendered from iThemba LABS during the first year of my Master's degree study, and for his motivation.

- HySA Systems University of the Western Cape Centre for allowing me to use their facilities during the experimentation phase of my research work.

- My family for their support throughout my studies, especially, Uncle Godfrey Mwiinga for the sponsorship during my undergraduate studies.

- Above all, I wish to sincerely thank God for His providence and gift of life, without whose benediction I would not have attained this achievement.

The financial assistance of the National Research Foundation and CPUT towards this research is acknowledged. Opinions expressed in this thesis and the conclusions arrived at, are those of the author, and are not necessarily to be attributed to the National Research Foundation and CPUT.

DEDICATION

This work is dedicated to my late mother, my family, friends and all those who commit to pursue constructive undertakings that add value and enhance human life the world over.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

APPENDICES

DEFINITION OF TERMS / GLOSSARY

AFC	Alkaline Fuel Cell
BoP	Balance of plant
CHP	Combined heat and power
CMFC	Current Mode Feedback Control
DG	Distributed Generation
DMFC	Direct Methanol Fuel Cell
EA	Error Amplifier
Eq.	Equation
FC	Fuel Cell
FCT	Fuel Cell Technology
GM	Gain Margin
IBVM	Interleaved Boost Voltage Multiplier
ICFFB	Isolated Current Fed Full Bridge
MCFC	Molten Carbonate Fuel Cell
MCU	Microcontroller Unit
PAFC	Phosphoric Acid Fuel Cell
PCMFC	Peak Current Mode Feedback Control
PCU	Power Conditioning Unit
PEM	Proton Exchange Membrane
PEMFC	Proton Exchange Membrane Fuel Cell
PM	Phase Margin
RES	Renewable Energy Source
RET	Renewable Energy Technologies
SA	South Africa
SOFC	Solid Oxide Fuel Cell
SOC	State of charge

VMFC	Voltage Mode Feedback Control
Grid	Interconnected network of power lines used to deliver electricity from the generation stations to the consumer.
Load profile	A load profile is a variation of an electrical load over time for a particular consumer and this can be represented using a graph showing the electrical load versus time.

CHAPTER 1
INTRODUCTION

1.1 Background

The rapid increase in energy demand and the simultaneous slow increase in energy output, pose a challenge to global energy supplies. In addition, the use of non-renewable electric utilities pose further challenges as these impacts negatively on the environment (Chevron, 2013). Findings in Chevron (2013) also show that global energy supplies are insecure and unstable besides leading to concerns about the climate. The above propositions are supported in James et al. (2007), wherein, it is asserted that the insecurity and instability posed by global energy supplies, and the concern about climate change are the major factors for the drive towards use of renewable energy sources (RES) and renewable energy technologies (RET).

Of the currently existing renewable energy technologies, fuel cell (FC) technology is considered to be one of the better options due to its cleanliness, its modularity, its high efficiency and its non-intermittence compared to wind and solar energy sources (Vázquez-Blanco et al., 2009). According to Mushsin and Zehra (2009), the use of FC technologies has been implemented over a wide spread of applications such as residential combined heat and power (CHP), transportation and industrial to name but a few. To this end, Sammes and Boersma (1999) alludes that a fair amount of research has been carried out on the subject of FC technology.

1.1.1 Technical operation of a fuel cell (FC)

A fuel cell is an electro-chemical device that converts reactants into electricity, heat and water (Farooque & Maru, 2002). The type of reactants used depends on the design and type of a FC. The available reactants in use consist of hydrocarbons and oxidants. Each FC is designed to have its own specific operating range of temperatures. Although each type of FC is distinguished by its properties such as the material used for its construction, the size and the geometry, structurally any FC consists of an electrolyte and two electrodes – an anode and a cathode (Lepiller, 2010). Figure 1.1 shows a detailed diagram of the basic construction of a proton-conducting FC.

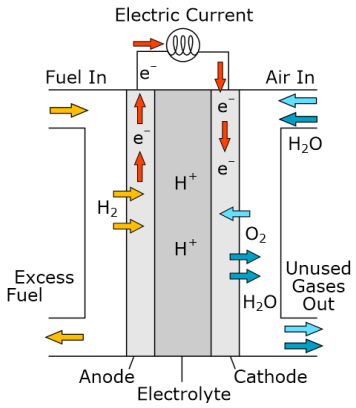


Figure 1.1: The schematic of a proton-conducting FC. (Adapted from Dervisoglu, 2012).

Figure 1.1 shows that as the fuel (hydrogen in this case) comes into contact with the anode, electrons are extracted to leave two Hydrogen ions ($H_2 - 2e^- = 2H^+$). These ions flow into the electrolyte. On the cathode side as air flows in, electrons are added to leave two Oxygen ions ($O_2 + 2e^- = 2O^-$) that flow into the electrolyte. The Hydrogen and Oxygen ions combine to generate water (H_2O). The creation of electrons at the Anode side that flow to the Cathode side to be annihilated constitutes the generation of electricity. This is the basic operation of a FC.

1.1.2 Types of fuel cell operation

There are two types of fuel cell operation dependent on the direction of flow of ions in the electrolyte or membrane. Figure 1.2 and Figure 1.3 show the electro-chemical reaction that takes place within the two types of fuel cells. The only difference there is, is the type of ions moving from one electrode to the other via the membrane, and this is dependent on the material the membrane is made of. Figure 1.2 shows the schematic for the operation of a Phosphoric Acid FC and PEM FC, where pure hydrogen is fed at the anode side while Oxygen is simultaneously fed at the cathode side

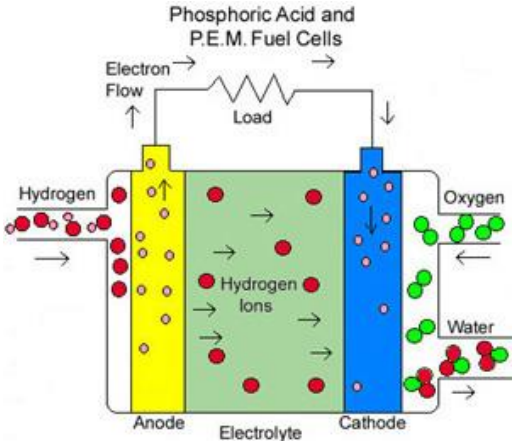


Figure 1.2: The schematic for the operation of a Phosphoric Acid FC and PEM FC. (Adapted from Smithsonian Institute, 2008)

During the combustion of the reactants, the molecular bond of Hydrogen and Oxygen are broken down. The Hydrogen ions move from the anode to the cathode via the electrolyte, while the Oxygen ions move from the cathode to the anode via the electrolyte. The two ions combine to produce water, whereas the Hydrogen electrons produce a current as they flow through the load and the conductor linking the two electrodes. These electrons become annihilated at the cathode to create Oxygen ions.

Figure 1.3 shows the schematic for the operation of a solid-oxide FC. The ion movement through the electrolyte is in the opposite manner to the flow shown in Figure 1.2. This is from the cathode to the anode and water is produced at the anode side of the FC. Thus, Oxygen ions move from the cathode to the anode via the electrolyte to produce water and electricity in a combustion reaction with Hydrogen.

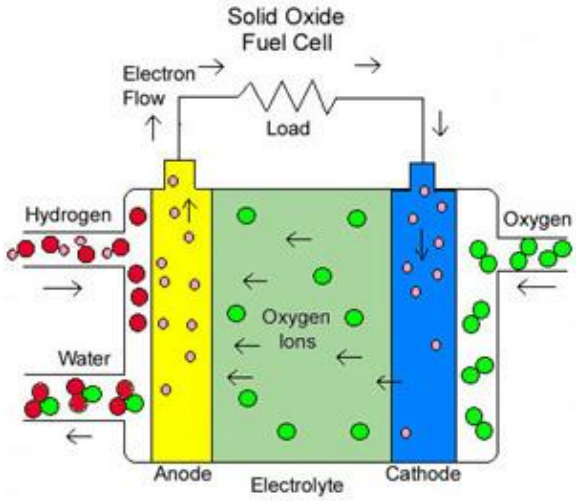


Figure 1.3:The schematic for the operation of a Solid Oxide FC
(Adapted from Smithsonian Institute, 2008)

1.1.3 Types of fuel cells

Generally, fuel cells are distinguished according to the chemical composition of the electrolyte and the fuel used (Kirubakaran et al., 2009). From the literature reviewed, there are about six major types of fuel cells available on the market today. These are the Polymer Electrolyte Membrane Fuel Cell (PEMFC), the Alkaline Fuel Cell (AFC), the Phosphoric Acid Fuel Cell (PAFC), the Molten Carbonate Fuel Cell (MCFC), the Direct Methanol Fuel Cell (DMFC) and the Solid Oxide Fuel Cell (SOFC). Furthermore, fuel cells are distinguished based on the characteristic of their operating temperatures. When distinguishing fuel cells based on the characteristic of their operating temperatures, the DMFC, the PEMFC, the AFC and the PAFC are classified as low temperature fuel cells with an operating temperature range of $50°C - 250°C$. While the MCFC and the SOFC are classified as high temperature fuel cells with an operating temperature range of $650°C - 1000°C$ (Kirubakaran et al, 2009).

1.1.4 FC power supply unit (PSU) design

In the design of a FC Power Supply Unit (FCPSU), first the type of the FC stack module must be selected, and then based on the stack specifications an appropriate power-conditioning unit (PCU) can also be selected and interfaced to the stack. The PCU is responsible for the conversion of the low unregulated direct current (DC) voltage produced by the FC stack to a regulated DC or alternating current (AC) voltage. Practically, a PCU is realised by using the direct current to direct current to alternating current (DC –DC – AC) concept. The DC – DC – AC concept is a combination of the direct current to direct current (DC – DC) converter and the direct current to alternating current (DC – AC) inverter. The DC – DC converter is usually directly coupled to the FC stack, whereas the DC – AC inverter can either be directly coupled to the FC stack or to the DC – DC converter. When a DC – DC converter is interfaced to a FC stack, it converts the low unregulated DC voltage of the stack to a high-regulated DC voltage. However, when the DC – AC inverter is interfaced to either a FC stack or a DC – DC converter, it produces an ac voltage from the DC input voltage. Both the regulated DC and AC voltage can be used for any dedicated load supply. Figure 1.4 shows the process flow diagram for a Ballard 250 kW PEMFC PSU plant. The PEMFC stack plant consists of the balance of plant (BoP), the controller and the DC – AC Inverter/DC – DC converter. The stack BoP is all auxiliary equipment that is required in order to ensure proper operation of the stack as a reliable and safe power source.

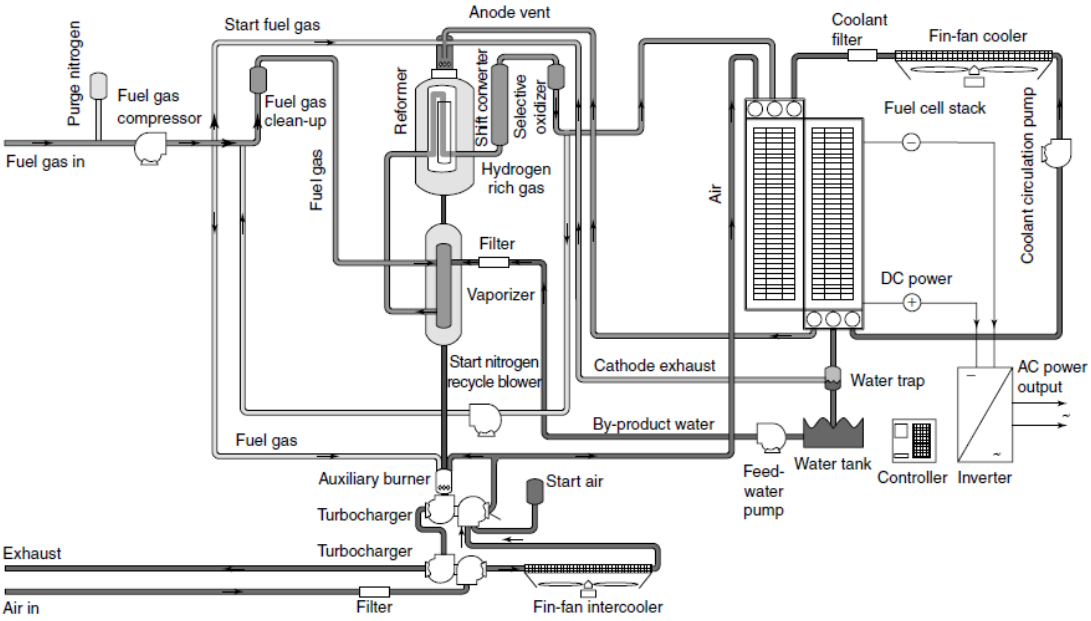


Figure 1.4: The process flow diagram for a Ballard 250 kW PEMFC PSU plant. (Adapted from J.Larminie & A.Dicks, 2003).

For the FCPSU design, an H – 1000 PEMFC stack module manufactured by Horizon Fuel Cell Technologies (HFCTs) is used. The H – 1000 PEMFC stack module is a low

power module with a maximum operating temperature of 65°C and uses pure hydrogen and oxygen to produce electricity and water, and it comes with a controller for the FC stack BoP. The schematic for the system setup of the H – 1000 PEMFC stack module with its auxiliaries is given in Appendix A. The schematic shows the inputs and outputs of the stack, the temperature sensor, the stack controller and the auxiliary power supply. In order to produce power from the combustion of hydrogen and oxygen, H_2 gas is continuously supplied to the stack from a Hydrogen cylinder and a blower continuously supplies Oxygen to the stack from the air. This process is monitored by the controller, which controls the power production and measures the stack temperature, current and voltage. During the combustion of hydrogen and oxygen, power and water are produced. The water is disposed from the stack through the purge valve, while the generated power is tapped from the stack through the positive and negative load terminals. For this work, a PCU is used as the load to the FC stack; therefore, it connects to the load terminals. Under abnormal conditions such as under-voltage or over-current, the controller shuts down the operation of the stack as a safety and protective measure (Horizon Fuel Cell Technologies, 2013).

The technical specification data for the H-1000 PEMFC stack module is given in Appendix B: H-1000 PEMFC stack technical specifications. The data include the FC stack power rating, the bias voltage and current, the recommended operating conditions and the system properties. From this data, different types of converters and inverters can be designed for the PCU of the FCPSU. In order to ensure reliable operation of the PCU, the design has to take into account the given FC stack low voltage shut down of 24 V, the over current shut down of 42 A and the over temperature shut down of 65°C.

Safety

Hydrogen is a highly flammable gas and this requires that safety precautions are observed and adhered to, strictly. Some standard safety precautions to be observed when using the H-1000 PEMFC stack include; a well-ventilated work place and the installation of hydrogen sensors. Besides these, other safety precautions include: avoid contact with exposed parts, ground all equipment in contact with the stack to minimize static discharge, all sources of ignition must be kept away from the FC stack, hydrogen leakage must be avoided, approved standards for hydrogen storage must be observed and the proper handling of compressed gas cylinders must be observed. Finally, the recommended system setup must be followed before operating the stack (Horizon Fuel Cell Technologies, 2013).

1.2 Statement of the research problem

Several fuel cells piled together are referred to as a stack. Individual voltages of each FC combine to form a stack voltage. A FC stack is designed to generate a voltage as a result of a chemical reaction, with water produced as a by-product. The problem is that, the voltage that is generated is unstable (unregulated), and so it cannot be used as it would damage appliances. It is then a requirement that this voltage is stabilised.

Besides the damage that would be caused to appliances by the unstable voltage, the other problem is that the FC stack itself can be damaged. When the stack voltage swings between no-load to full-load, the individual FC voltage falls significantly as the current density rises. The result is that a current ripple is produced within the stack. This ripple causes unwanted heating of the individual fuel cells and eventually reduces the life expectancy of the stack.

The fact that damage may occur to appliances or to the FC stack itself presents a challenge in the use of the technology for most applications. It is then required that the technology is made to be useful by alleviating these challenges.

The third problem is that the performance of the FC stack can be adversely affected by its slow response to load changes. This occurs when the load demands more power, which the FC stack, cannot provide instantly. That is so because the production of electricity from the combustion of H_2 and O_2 within the FC stack is purely a chemical reaction process that takes several time constants to complete (Abd et al., 2014). This creates a mismatch and imbalance in the output power of the FC stack and the power demand of the load.

In order to address these problems and therefore to make FC technology useful, the generated voltage must be stabilised. The design of a suitable power supply unit (PSU) is required in order to operate a FC stack at a fixed or stabilised output voltage within the linear region of the stack polarization curve.

1.3 Rationale and motivation for the research

The economy of South Africa (SA) faces the challenge of rapid increases in energy demand. According to SAinfo reporter (2012), the energy demand is projected to double by 2030. Due to a lack of adequate investment in the country's energy infrastructure in the past years, the energy demand is increasing faster than the power utility company can meet it (SAinfo reporter, 2012).

SAinfo reporter (2012), also reported that the power generation system of SA is heavily dependent on coal. However, due to an increase in the energy demand and the government's support for green energy, there is a need to diversify power generation to independent renewable energy sources (SAinfo reporter, 2012). This is expected to bring electricity supply and distribution into balance (SAinfo reporter, 2012). More than 3.4 million households are without electricity in SA (Carbon Trust Advisory, 2013), with approximately 1.3 million households located in rural communities (Carbon Trust Advisory, 2013). Despite the determined efforts by the SA government to improve power capacity and transmission lines, large areas in some parts of the country will still be off-grid in the near future (Carbon Trust Advisory, 2013).

The main goal of any power utility company in a competitive and challenging environment is to provide high quality and reliable electricity at cheap costs (Tanrioven & Alam, 2006). To achieve this goal, power utility companies support distributed generation (DG) of power (Tanrioven & Alam, 2006). DG is a process whereby power is generated from many power sources and these are connected directly to the distribution network or consumer point of control. This ensures lower environmental impacts with an improved security of supply (Thomas et al, 2001). Among the existing various DG techniques, fuel cells have generated greater interest due to their cleanliness, fast start-up characteristics, high efficiency and their capability to deliver power uninterrupted. This is not so in the case of wind and solar sources. The later have a major disadvantage in that the delivery of power happens only when the wind blows or when the sun shines (Kirubakaran et al, 2009). A recent report produced for Anglo American Platinum Ltd identified FC technology as a significant potential to overcome the challenge of providing clean, reliable and high quality electricity (Carbon Trust Advisory, 2013).

1.4 The Research Objectives and Aims

1.4.1 The research objective

The objective of the research is to design and develop a prototype circuit for a 1 kW PEMFC stack power supply unit (PSU). Some of the key design specifications of the unit will include a stable output voltage and low input current ripple, and it is intended to be a stand-alone system for application in areas where the power grid is absent.

1.4.2 The research aim

The aims of the research are intended to realise the objective and these are:

- Literature review of existing converter topologies used in PCUs for PEMFC PSUs.

- Determine the most appropriate and most cost effective converter topology for the PCU based on the selected FC stack specifications.
- Mathematical modelling, design, control and simulation of the preferred converter topologies for the PEMFC PCU.
- Based on the simulation results, investigate, analyse and determine the most appropriate converter topology, and then construct a circuit prototype thereof.
- Implement a controller for the circuit prototype.
- Test the circuit prototype under load transients in order to simulate different residential load profiles.

1.5 Research design and methodology

In order to achieve the aims of this project, a brief overview of the components of a fuel cell power supply unit (FC PSU) are studied and investigated, with focus on the DC – DC converter. A FC PSU consists of a power-conditioning unit (PCU), balance of plant (BoP) and a controller. The PCU can constitute a DC – DC converter only, a DC – AC inverter only or a combination of both.

A literature review of current converter topologies used for the design of FC PCUs is carried out to establish designs for simulations and experimental tests. Based on the literature review, the system requirements for the designs, the system specifications and the operating conditions of the selected FC stack, the performance characteristics of different designs is analysed using mathematical modelling and simulation. The simulation of the designs and controller analysis processes require the use of various software packages. These packages include MATLAB/Simulink and code composer studio (CCS).

Based on the data gathered and generated, the design showing better performance is adopted to develop a prototype circuit for the FC PCU. Then the prototype circuit will be investigated under varying power loads representing different load profiles.

1.6 Research significance

There are many challenges and concerns that relate to power supply globally, these are: the rapid increase in global energy demands, the high costs of connecting rural communities and remote places to an existing power grid, the need to mitigate climate change by use of green energy sources and resource depletion (Abdeen, 2008).

By integrating FC PSUs in the global power supply chain, some of the challenges and concerns involving the production and distribution of power can be minimised or overcome. A FC based power supply has low to zero emission of carbon, is cheaper

to install in rural and remote areas where connecting to an existing power grid is costly, has high efficiency and has high power quality. Research on a FC power supply is therefore vital, because the results would be used to improve the efficiency of the system, and to establish the feasibility of the technology for application in residences.

Based on the literature reviewed, at present, the indication is that FC power technology is used on a small scale to run automobiles, in telecoms power supply units, in industries and in various other power supply applications. The success of FC power technology would therefore benefit these areas of power application, and would further promote its use in other areas.

1.7 Thesis outline

The chapters in this thesis covers the current research on the converter topologies used for FC PCUs, the existing challenges and problems of the available converter topologies, the modelling, design, control and development of an experimental prototype circuit for the FC PCU.

Chapter 1: is an introduction to the thesis. It defines the statement of the research problem, the background to the research, the objectives, the aims and the goals of the research.

Chapter 2: deals with the literature review. The various converter topologies employed in FC PCUs applications are discussed. The comparison, performance characteristics and advantages of each topology are also discussed in depth.

Chapter 3: covers the mathematical modelling and power stage design of various converter topologies. Mathematical equations that are indicative of the converter performance characteristics for each respective converter topology are also derived.

Chapter 4: discusses the controller design and simulation of various converter topologies, and the relative analysis of the various converter simulation results.

Chapter 5: discusses the prototype circuit of the IBVM converter and the experimental measurements.

Chapter 6: concludes the research work and makes some recommendations for the future research work.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The literature reviewed covers both past and present research on PCUs used for PEMFC PSU applications. In the review, a discussion of the topologies and the various technicalities of PCUs are presented. The discussion also pinpoints the importance of an appropriate PCU in regulating the output voltage of a PEMFC stack. This is the objective of this research study.

2.2 Fuel cell technology

The use of FC technology became popular some time ago (Tanrioven & Alam, 2006), especially in residences (Takuya et al., 2007), in vehicular applications (Virgilio et al, 2013) and in utility power supply applications (Brooke, 2007) mainly due to its cleanliness. FC technology has attracted attention in the distributed generation sector because of the high-energy demands globally and because of the current high pollution levels (Shailendra et al., 2012). The features of FC Technology are high efficiency, cleanliness and high quality of power. These features make the technology a good candidate for some applications in industries and in remote places (Michael et al., 2001).

2.3 Power conditioning unit (PCU)

A PCU is an important part of FC stack based power supplies. Its function is to convert the unregulated low DC voltage of a FC stack into a regulated and higher DC voltage that is usable for various power applications (US Department of Energy, 2005). A PCU can be realised by means of a power inverter/converter, and the choice of the power inverter/converter topology depends on the characteristics and performance of a FC stack and the intended application. The performance of a FC stack is described by the polarisation curve of the individual FCs that make up a FC stack, which are the building blocks of a FC stack (Farooque & Maru, 2002). Figure 2.1 shows the polarisation curve for the stack voltage and current density of a typical low voltage and low-pressure fuel cell. In the figure, the actual “No loss” voltage is less than its standard theoretical value. The cell voltage decreases as the current density increases but with a rapid initial voltage decrease followed by a linear region and another rapid voltage decrease at higher currents. As the polarisation curve indicates, the output power of a FC stack is prone to variations; therefore, for any practical applications the stack voltage must be regulated at a desired value. A PCU is used to perform the required and necessary voltage regulation, voltage boost and in some cases voltage inversion of the FC stack output voltage. Ultimately, the use of a PCU is to overcome the negative characteristics

of a FC stack. These have been stated before as unstable stack output voltage, low voltage output and a slow dynamic response (Vázquez-Blanco et al., 2009).

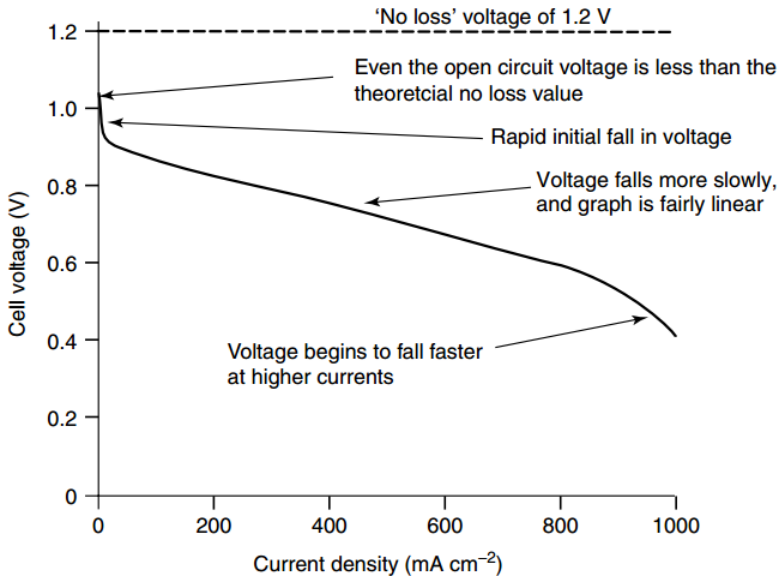


Figure 2.1: The polarisation curve for the cell voltage versus the current density of a typical low temperature and low pressure single fuel cell.

(Adapted from Larmine & Dicks, 2003).

Figure 2.2 shows a graph of voltage against current of a FC stack and a step-up converter used as a PCU. The graph illustrates how a converter regulates the unstable voltage of a FC stack to a stable voltage a little lower than the maximum FC stack voltage (J.Larminie & A.Dicks, 2003). The unstable stack voltage is fed to the step-up converter, where it is regulated to a predetermined level.

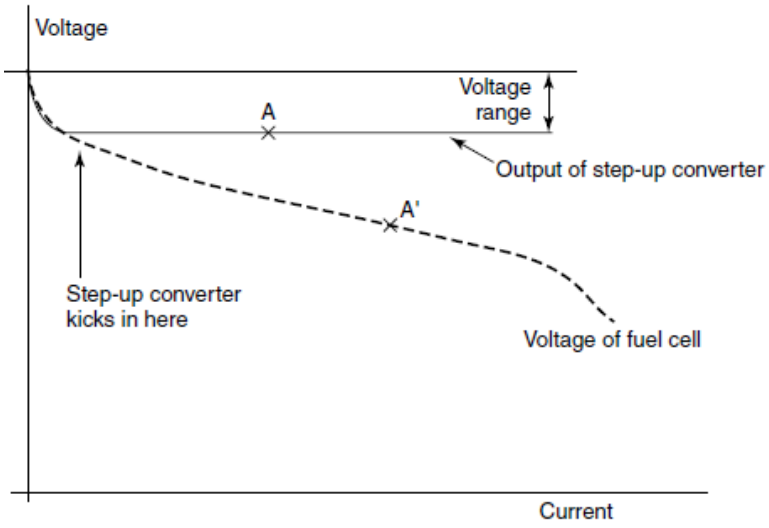


Figure 2.2: A graph of voltage against current of a FC and step-up converter.

(Adapted from Larmine & Dicks, 2003).

2.3.1 Power Converter topologies for FC PCUs

The commonly used converter topologies for PCUs in FC PSUs application are the single-stage and the multi-stage converter topologies (Yu et al., 2007). Figure 2.3 shows a block diagram of the FC PSU with a single stage converter topology PCU while Figure 2.4 shows a block diagram of the FC PSU with a multistage converter PCU. The single stage topology has one voltage conversion stage, DC – AC converter, which converts the low unregulated FC voltage directly to a higher regulated AC voltage. Usually, the DC – AC inverter output is coupled directly to a low frequency step-up transformer and then boosted to a high AC voltage (Vázquez et al., 2008). Single stage converter topologies offer a low component count as well as small losses (Shailendra et al, 2012). In contrast, the multi-stage topology has two stages, the DC – DC converter stage and the DC – AC inverter stage. The DC – DC converter boosts the stack output voltage to a higher regulated DC voltage, and isolates the low power circuits from the high power circuits. On the other hand, the DC – AC inverter cascaded to the output of the DC – DC converter inverts the high DC output voltage from the DC – DC converter to a useful AC voltage, depending on the voltage and frequency requirements of the load (220V at 50Hz or 120V at 60Hz). In some cases, the inverter output voltage may contain large switching harmonics that are hazardous to the load, therefore, an inductor capacitor (LC) filter must be connected intermediate between the inverter and the load to reject the harmonics and ensure a clean sinusoidal waveform for the load.

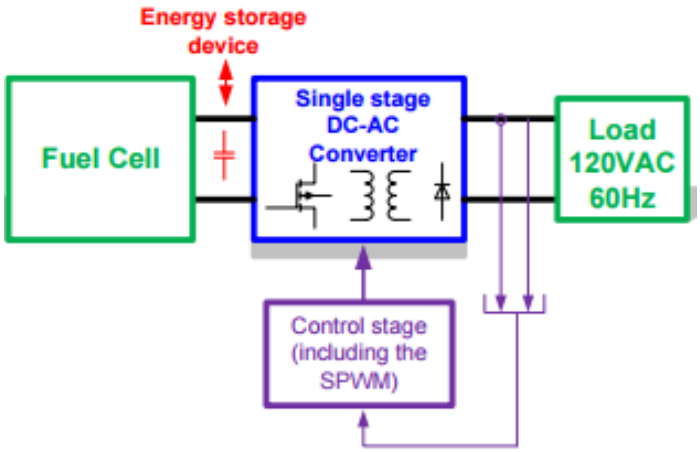


Figure 2.3: The block diagram for the FC PSU with a single stage power converter topology PCU.

(Adapted from Vázquez-Blanco et al., (2009).

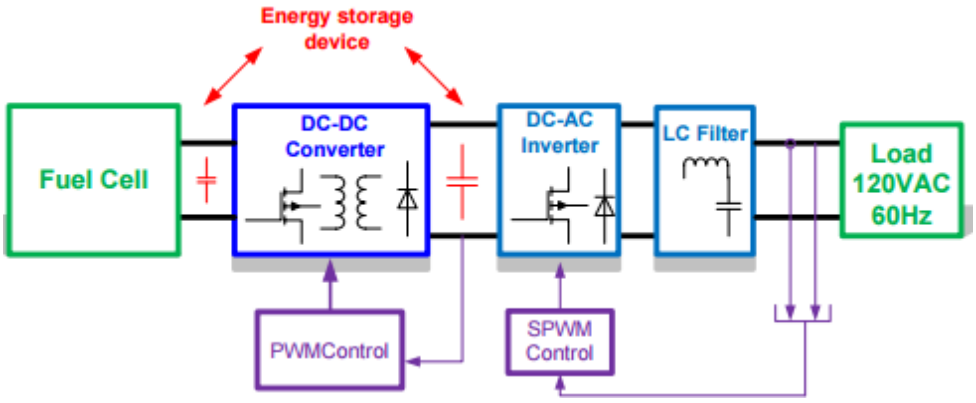


Figure 2.4: The block diagram of the FC PSU with a traditional multistage power converter topology PCU.

(Adapted from Vázquez-Blanco et al.,2009).

Figure 2.5 shows a block diagram of a FC stack PSU with a single stage inverter PCU and a voltage amplification stage. The inverter converts the unregulated and low FC stack output voltage to a regulated and low AC output voltage. The voltage amplification stage transforms the low AC voltage to a higher AC output voltage required for grid connection and load application. This topology has the disadvantage of high conduction and switching losses due to the large component count as that of Figure 2.4 (Miranda et al., 2006). However, it also offers the advantage of less power stress on the components in the power stage (Kong et al., 2004). In general, converter topologies with higher component counts will exhibit high conduction losses and switching losses and vice versa.

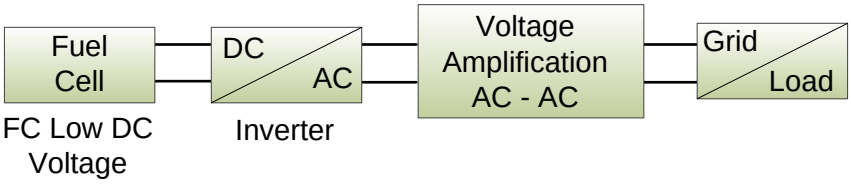


Figure 2.5: The block diagram of a FC PSU with a single stage inverter PCU and a voltage amplification stage.

(Adapted from Tanrioven & Alam, 2006).

PWM DC – DC Converter topologies can be classified into current fed (CF) and voltage fed (VF) converters. According to Changrong and Jih-Sheng (2007), the use of CF Converter topologies in PCUs for FC PSUs has been reported to reduce the input current ripple, which causes heating of the stack. Figure 2.6 a) shows a FC PCU with a VF converter, and b) shows a FC PCU with a CF converter. The VF converter has an input filter connected in parallel with the stack; the function of the input filter is to reject the input current ripple. On the other hand, the CF converter has an input inductor in series with the stack. The inductor acts as a current source and therefore reduces the input current ripple present in the stack.

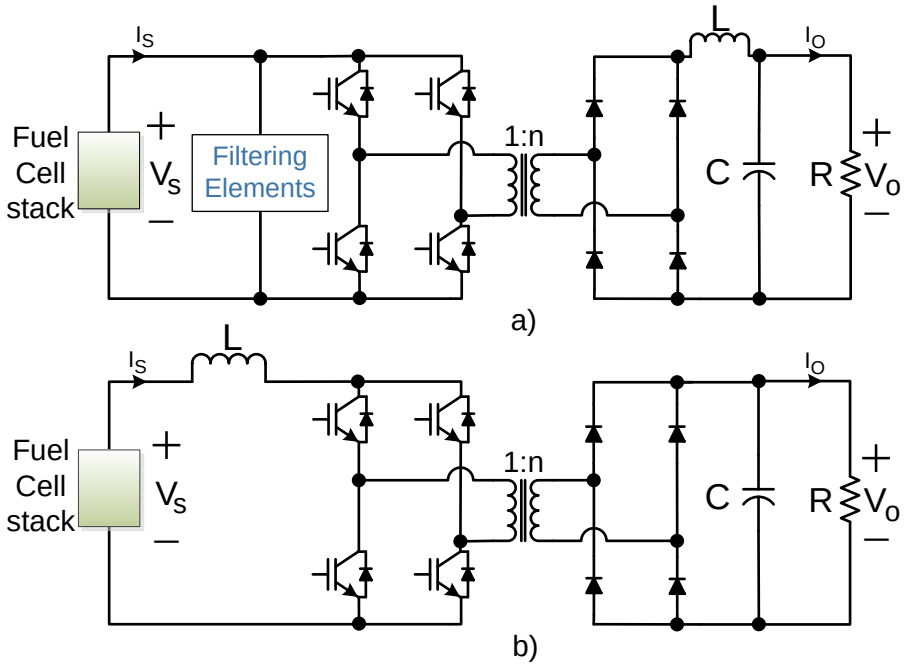


Figure 2.6: The FC PCU with VF and CF DC – DC power converter topologies.

a) VF full-bridge DC – DC converter topology and b) CF full-bridge DC – DC converter topology (Adapted from Palma, 2012).

Figure 2.7 shows a block diagram of the FC PCU with VF and CF converter topologies for grid applications. Both the VF DC – DC converter in a) and the CF DC – DC converter in b), have an input filter in parallel with the stack and a high frequency transformer intermediate between the switches and the rectifiers. The function of the input filter is to reject the input current ripple, while the function of the high frequency transformer is to transform the switched DC voltage to a higher DC voltage.

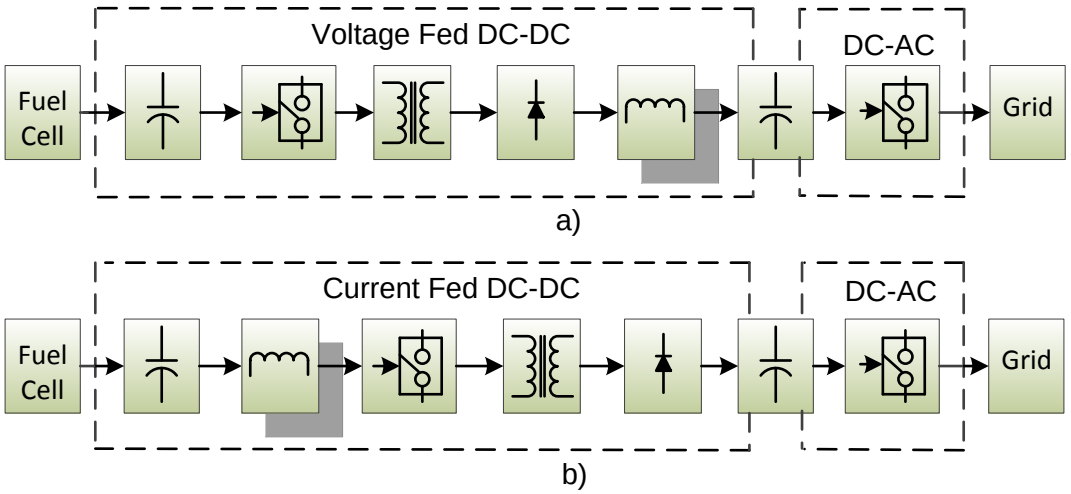


Figure 2.7: The block diagram of the FC PCU with VF and CF DC – DC power converter topologies for grid tied applications.

a) VF DC – DC converter topology and b) CF DC - DC converter topology (Adapted from Gert et al., 2002).

Figure 2.8 shows the DC – DC voltage fed interleaved full-bridge converter. The converter consists of two DC – DC VF full-bridge converters that are interleaved together. The converter inputs are connected in parallel with the stack and the outputs are connected in series. This topology offers smaller number of transformer turns and so offers a smaller ratio, a smaller input current ripple and a reduced component size. However, the topology has the disadvantage of high conduction losses due to its inherent high component count.

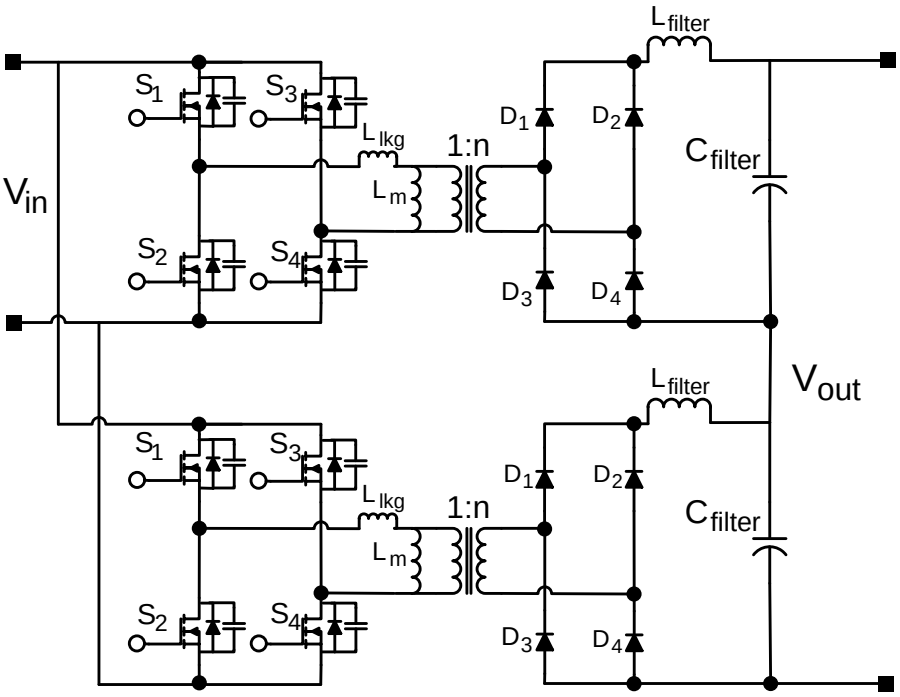


Figure 2.8: The DC – DC voltage fed interleaved full-bridge converter.
(Adapted from Young-Sang et al., 2012).

There are several types of CF and VF DC – DC converters available, but for high power applications the full bridge topology is preferred (Troy et al, 2002) because of its efficiency and cost (Jin et al, 2004). Whereas, the use of CF DC – DC converters and the interleaving of converters ensures low input current ripple (Troy et al., 2002).

2.3.2 PCU design consideration

The two most important criteria used in the design of converters/inverters for FC PCUs are voltage stability and current ripple reduction. The input current ripple must be kept to a minimum as high current ripple causes heating of the stack, which lowers the stack life expectancy and efficiency (Saijun & Xiaoyan, 2012). According to Gert et al. (2002), an input filter can be included in the converter design to reduce the input current ripple. Alternatively, a CF converter can be used instead of a VF converter (Yu et al., 2007, Palma, 2013).

Another important factor to consider in the design of converters/inverters for FC PCUs is the supply of a wide range of input voltages from FC stacks. This makes the PCU capable of maintaining a constant output voltage irrespective of the stack voltage variations and the load current variations (Maja et al., 2004).

2.4 Conclusion

This chapter focuses on FC technology as a possible renewable energy source that has the potential to meet energy demands at low costs with minimal impact on the environment. It covers some of the converter and inverter topologies that are recommended for use in FC PCU applications and those that are currently in use.

The chapter discusses the various possible topologies of DC – DC converter topologies that are available for use in the power conditioning of a FC stack output voltage. It also discusses the advantages and disadvantages imposed by each converter topology on the overall system efficiency, performance, cost and durability of the FC PSU. The effect of the input current ripple on the system's performance and durability is also highlighted.

Based on the literature review, it is evident that the suitable converter topology for use in a PCU of the FC PSU must be selected based on the power supply requirements of the load and the system specifications of the FC stack. This would ensure high efficiency and high system performance for the designed FC PSU.

The next chapter considers the modelling and design of PWM DC – DC converter topologies used in PEMFC PCUs.

CHAPTER 3
MODELLING and DESIGN of PWM CONVERTERS

3.1 Introduction

In this chapter, the circuits and operation of four PWM DC - DC converter topologies are presented. Based on the topologies, large-signal and small-signal equations are derived. Models and transfer functions of the power stage for each converter are also derived by using the circuit averaging technique. Figure 3.1 shows the simplified power stage of a converter, which consists of lumped elements such as capacitors, inductors, switches and diodes. According to control theory, small-signal models are linear and time invariant systems that are crucial in the design of a controller for a system. On the other hand, large-signal models are inherently non-linear and time variant.

The component and parameter equations that ensue from the modelling of each converter are used later to calculate the power stage components and parameters in the power stage design of the particular PWM converter.

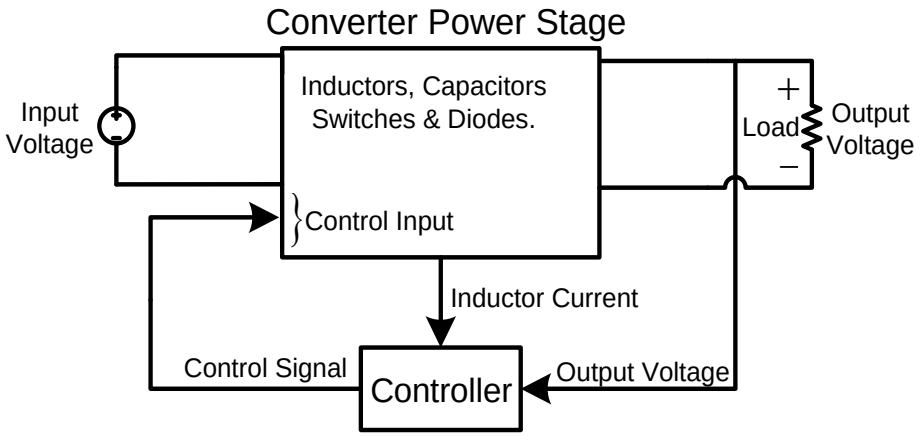


Figure 3.1: The simplified circuit of a PWM DC – DC converter.

The modelling to be carried out in this work is based on the works of Middlebrook and Cuk (1976), Vorpérian (1990), Ben-Yaakov and Adar (1994), Robert and Dragan (2001), Bryant and Kazimierczuk (2004), Haiping et al. (2004), Bryant and Kazimierczuk (2007), Kazimierczuk (2008), Rosas-Caro et al. (2010) and Matheepot et al. (2013). The four PWM DC – DC converter topologies to be modelled and designed in this section are the isolated current-fed full-bridge (ICFFB) converter, the boost converter, the sepic converter and the interleaved boost voltage multiplier (IBVM) converter.

3.2 ICFFB Converter

3.2.1 Modelling of the ICFFB converter

In this section, the circuit, the operation and the circuit averaging description of the ICFFB converter are presented. Based on the circuit averaging description of the converter over one switching period, the parameter and component equations are derived. A linearized model is also derived from which the small-signal input-to-output and control-to-output voltage transfer functions are derived. The transfer functions are used later in the design of a controller and in the simulation stage.

The ICCFB converter is an all-round power control topology that can be used for a wide range of power conversions (Martin et al., 2008). Some of its capability includes wide input voltage range, high power handling, high boosting ratio, versatile symmetry and isolation of the output from the input (O.Alavi & S.Dolatabadi, 2015).

Generally, there are two types of isolated full bridge converters, namely: the isolated voltage-fed full-bridge (IVFFB) converter and the isolated current-fed full-bridge (ICFFB) converter. In this work, the ICFFB converter is preferred for the FC stack power conditioning application, mainly due to its high voltage gain and low input current ripple characteristics.

3.2.2 Circuit topology

Figure 3.2 shows the circuit of the PWM ICFFB converter. The circuit consists of a DC input voltage V_I, four controllable MOSFET switches S_1, S_2, S_3 and S_4, a high frequency (HF) transformer, four high speed high-power switching diodes D_1, D_2, D_3 and D_4, an input inductor L, an output filter capacitor C, an output voltage V_O and a resistive load R.

The input inductor acts as a current source and the transformer boosts the input voltage to a higher DC output voltage. These features make the ICFFB converter compatible with the performance characteristics of a FC stack. The basic structure of the converter is derived from Robert and Dragan (2001). However, a full-bridge rectifier is used after the secondary winding of the transformer instead of a half bridge rectifier. The analysis of the operation of the ICFFB converter covered in this section is based on the work of Robert and Dragan (2001), Kong et al. (2004) and O.Alavi and S.Dolatabadi (2015).

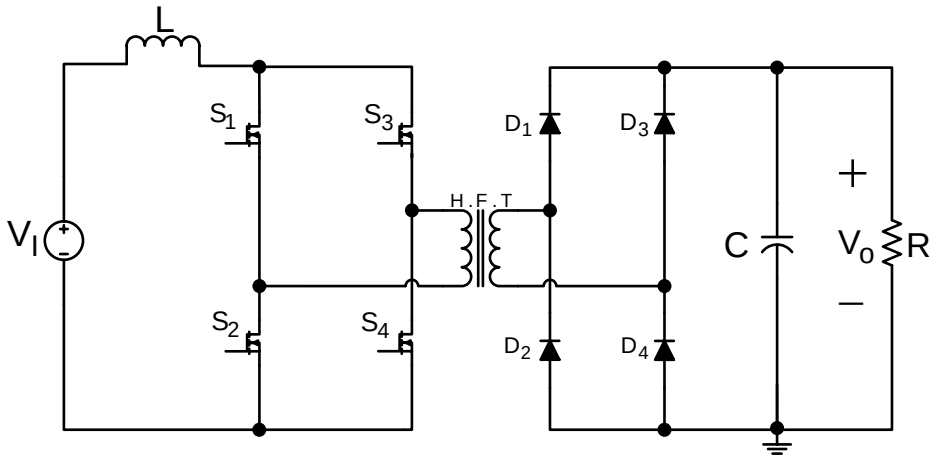


Figure 3.2: The circuit of the isolated PWM ICFFB converter.

Figure 3.3 shows the detailed circuit of the PWM ICFFB converter with series parasitic resistances of the components and an ideal transformer operating in continuous current mode (CCM). In the diagram r_L is the equivalent series resistance (ESR) of the input inductor, r_M is the series parasitic resistance of each MOSFET switch, n is the transformer turns ratio, V_F is the forward voltage drop across each conducting rectifier diode, r_F is the forward resistance of each conducting rectifier diode and r_C is the equivalent series resistance (ESR) of the capacitor. In the Figure, the full model of a rectifier diode is depicted as a voltage source in series with a forward resistor. The four models of the rectifier diode are inside the dotted lines.

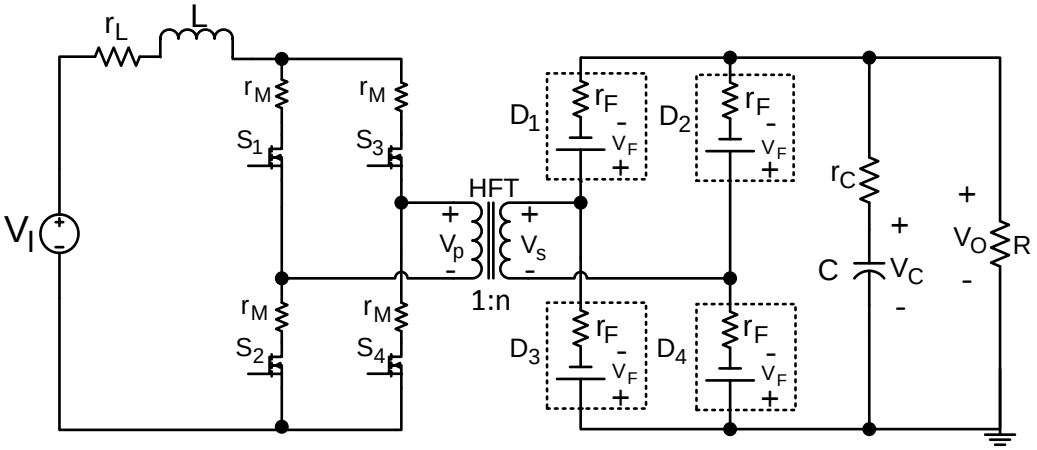


Figure 3.3: The detailed circuit of the PWM ICFFB converter.

3.2.3 Converter Steady State Analysis

Operation Principle of the Converter

In the analysis of the ICFFB converter circuit, it is assumed that the converter is operating in steady state with CCM. With CCM, the operation of the ICFFB converter over one switching period can be divided into four modes, where one switching cycle

of the converter is equal to T_s and T_{sL} is the switching period of the inductor current and the capacitor voltage.

The four switches of the converter are operated as pairs of S_1, S_4 and S_2, S_3. The switches turn on and off alternately at the switching frequency f_s $(f_s = 1/T_s)$, with the duty D greater than 50 % in order to warrant a switch overlap between the switch pairs. The two switch pairs are hard switched and operated by two gate signals that are $180°$ phase shifted. In Robert and Dragan (2001), it was observed that if the off-times of the switch pairs were equal, the average voltage of the transformer and the total volt-seconds applied to the magnetizing inductance of the transformer would be equal to zero over one switching period. Figure 3.4 shows some of the important current and voltage waveforms of the ICFFB converter over one switching period. Where the time interval $t_0 - t_4$ is equal to one operating period.

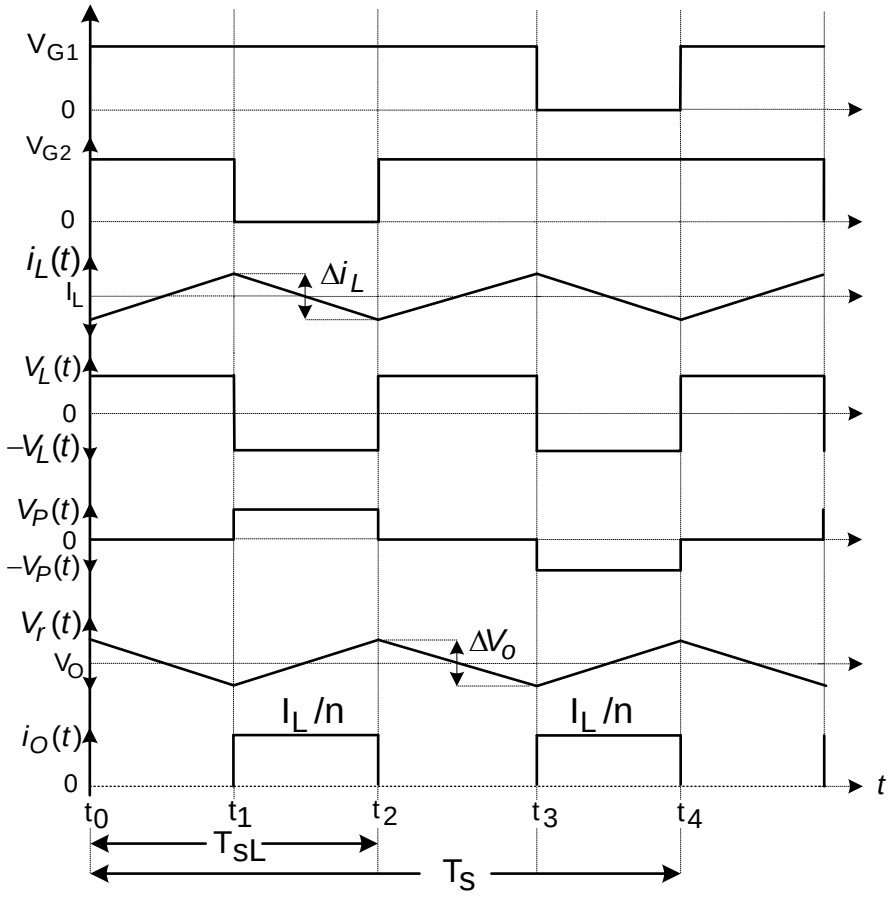


Figure 3.4: The current and voltage waveforms of the ICFFB converter during steady state switching.

Where V_{G1} and V_{G2} are gate signals for the MOSFETs, $i_L(t)$ is the instantaneous inductor current, I_L is the average inductor current, $i\Delta_L$ is the peak-to-peak inductor current ripple, $V_L(t)$ is the instantaneous inductor voltage, $V_P(t)$ is the instantaneous

voltage of the transformer primary winding, $V_r(t)$ is the output capacitor voltage ripple, ΔV_O is the peak-to-peak output voltage ripple and $i_O(t)$ is the instantaneous current of the transformer secondary winding.

Figure 3.5 to Figure 3.8 show the operation modes of the ICFFB converter. Solid lines mark the current conducting paths in the circuit of the converter for each mode, while broken lines mark the non-current conducting paths, and the arrow line marks the directions of the current flow.

Mode 1: $\left(t_0 - t_1 = \left(D - \frac{1}{2} \right) T_s \right)$

Figure 3.5 shows the equivalent circuit of the converter during mode 1. During this interval, all the four MOSFET switches S_1, S_2, S_3 and S_4 turn on and conduct the inductor current I_L and the inductor is charged up by the source. The current through the primary winding of the transformer is equal to zero. Meanwhile, on the secondary side of the transformer, the current through the secondary winding is zero, all the four diodes D_1, D_2, D_3 and D_4 turn off and the load current is supplied by the discharging capacitor. Since the primary winding of the transformer is shorted to ground, the voltage across the primary winding and the secondary winding is equal to zero. This mode ends when S_1 and S_4 turn off.

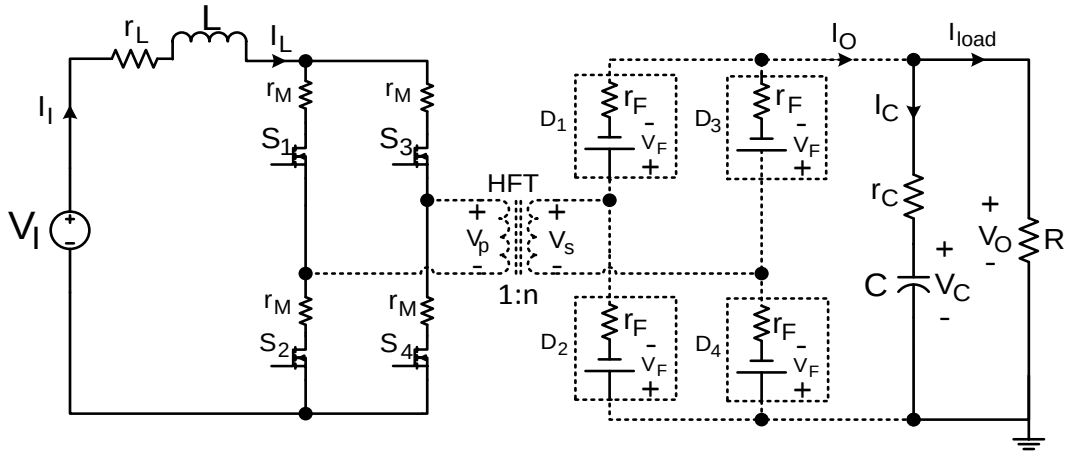


Figure 3.5: The equivalent circuit of the ICFFB converter during mode 1.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L\frac{di_L(t)}{dt} + r_L I_L + 2r_M I_L = V_I, \tag{3.1}$$

$$C\frac{dv_C(t)}{dt} = -I_{Load}, \tag{3.2}$$

$$I_{Load} = \frac{V_o}{R}. \tag{3.3}$$

Where I_I is the input current and is equal to I_L, I_O is the average current of the secondary winding side of the transformer, I_{Load} is the average load current, V_P is the average voltage across the primary winding side of the transformer, V_S is the average voltage across the secondary winding side of the transformer, V_C is the voltage across the capacitor, V_O is the output voltage, V_I is the input voltage and R is the load resistance.

Mode 2: $(t_1 - t_2 = (1-D)T_s)$

Figure 3.6 shows the equivalent circuit of the converter during mode 2. During this interval, switches S_1 and S_4 turn off, whereas S_2 and S_3 stay on. The inductor discharges current through S_2, S_3 and the primary winding of the transformer while energy is transferred to the load. On the secondary side of the transformer, the output current flows from the secondary winding to the load and capacitor via D_1, and then back to the secondary winding via D_4. During this interval, the capacitor is charged up. This mode ends when the switch pair of S_1 and S_4 turns on again.

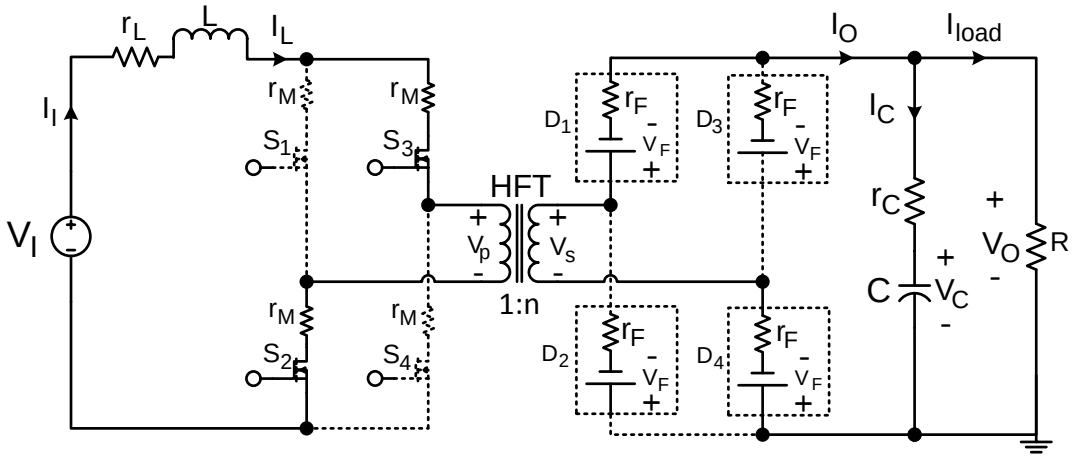


Figure 3.6: The equivalent circuit of the ICFFB converter during mode 2.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L\frac{di_L(t)}{dt} + r_L I_L = V_I - 2r_M I_L - V_P, \tag{3.4}$$

$$C\frac{dv_C(t)}{dt} = I_O - \frac{V_O}{R}, \tag{3.5}$$

where I_O is equal to $\frac{I_L}{n}$ and V_P is equal to $\frac{1}{n}(2r_F + I_O + 2V_F + V_O)$.

Mode 3: $\left(t_2 - t_3 = \left(D - \frac{1}{2} \right) T_s \right)$

Figure 3.7 shows the equivalent circuit of the converter during mode 3. All the four switches turn on again. This mode is similar to mode 1 and the corresponding differential equations are similar.

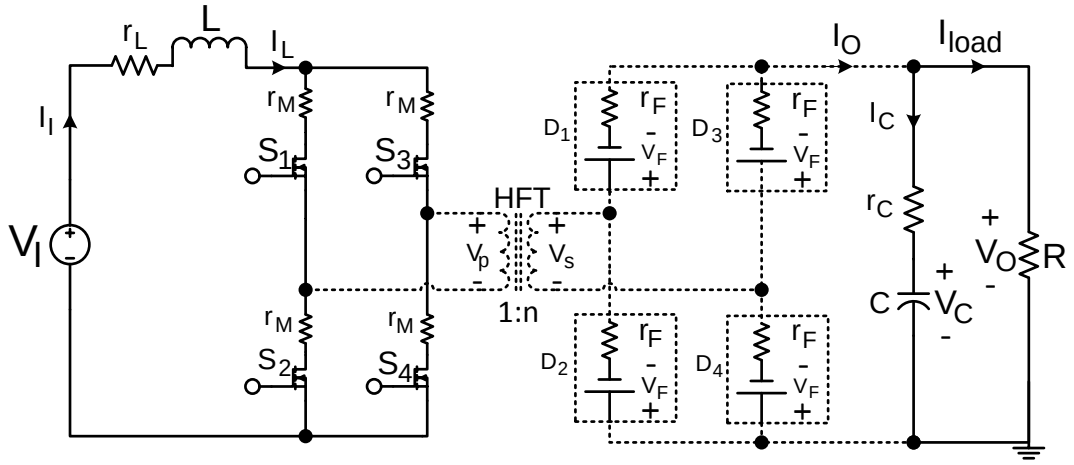


Figure 3.7: The equivalent circuit of the ICFFB converter during mode 3.

Mode 4: $\left(t_3 - t_4 = (1-D) T_s \right)$

Figure 3.8 shows the equivalent circuit of the converter during mode 4. During this interval, switches S_2 and S_3 turn off, whereas S_1 and S_4 stay on. The inductor discharges current through S_1, S_4 and the primary winding of the transformer while energy is transferred to the load. On the secondary side of the transformer, the output current flows from the secondary winding to the load and the capacitor via D_3, and then back to the secondary winding via D_2. The capacitor C is charged up. This mode ends when the switch pair of S_2 and S_3 turns on again.

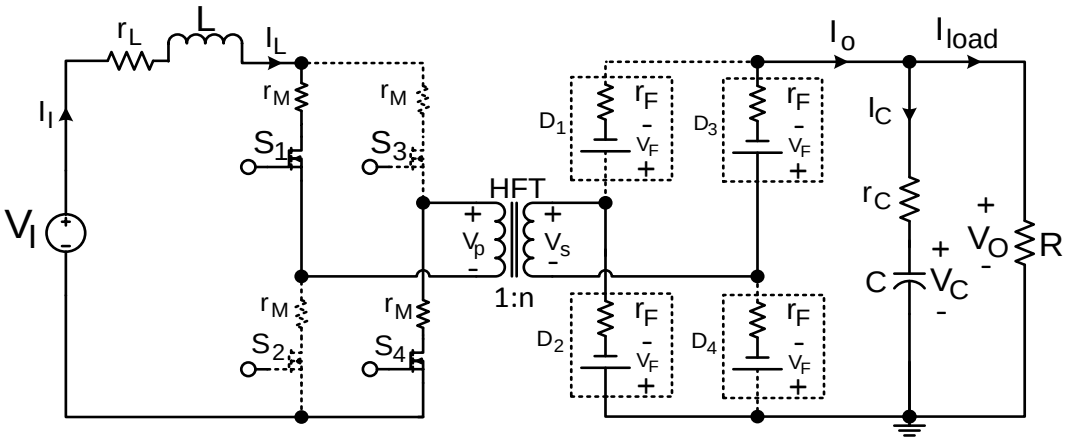


Figure 3.8: The equivalent circuit of ICFFB converter during mode 4.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L\frac{di_L(t)}{dt} + r_L I_L = V_I - 2r_M I_L + V_P, \tag{3.6}$$

$$C\frac{dv_C(t)}{dt} = I_O - \frac{V_O}{R}, \tag{3.7}$$

$$V_O = V_C + r_C C\frac{dv_C(t)}{dt}, \tag{3.8}$$

where V_P is equal to $-\frac{1}{n}\left(2r_F I_O + 2V_F + V_O\right)$.

Average inductor voltage

The average inductor voltage is found by taking the integral of the inductor instantaneous voltage over one switching cycle by using Eq. (3.1), (3.4) and (3.6), and it is given as

$$\begin{aligned}\left\langle V_L(t)\right\rangle &= \frac{1}{T_s}\int_0^{T_s} V_L(t)\,dt \\ &= \left(2\left(V_I - (r_L + 2r_M)I_L\right)\right)\left(D - \frac{1}{2}\right) + 2\left(V_I - (r_L + 2r_M)I_L - \frac{1}{n}\left(2r_F I_O + 2V_F + V_O\right)\right)D'.\end{aligned} \tag{3.9}$$

Where $\left\langle V_L(t)\right\rangle$ is the total inductor voltage over one switching cycle.

According to the inductor volt-second balance principle, when a converter is operating in steady state under CCM conditions, the net change in the inductor current during the charging interval is equal to the net change in the inductor current during the discharging interval over one switching cycle. Applying the inductor volt-second balance principle to the average inductor voltage will therefore yield a zero net volt-second balance. The inductor volt-second balance over one switching period is therefore given as

$$\begin{aligned}0 &= \frac{1}{T_s}\int_0^{T_s} V_L(t)\,dt \\ &= \left(2\left(V_I - (r_L + 2r_M)I_L\right)\right)\left(D - \frac{1}{2}\right) \\ &\quad + 2\left(V_I - (r_L + 2r_M)I_L - \frac{1}{n}\left(2r_F I_O + 2V_F + V_O\right)\right)D' \\ &= V_I - (r_L + 2r_M)I_L - \frac{1}{n}\left(4r_F\frac{I_L}{n} + 4V_F + 2V_O\right)D'.\end{aligned} \tag{3.10}$$

In Eq. (3.10) $\frac{I_L}{n}$ is substituted for I_O in order to solve for I_L, the result is given as

$$I_L = \frac{nV_I - 4V_F D' - 2V_O D'}{nr}, \tag{3.11}$$

where

$$r = \frac{n^2 (r_L + 2r_M) + 4D'r_F}{n^2}. \tag{3.12}$$

Figure 3.9 shows the equivalent DC circuit of the input section of the ICFFB converter constructed by from the inductor volt-second balance equation given by Eq. (3.10).

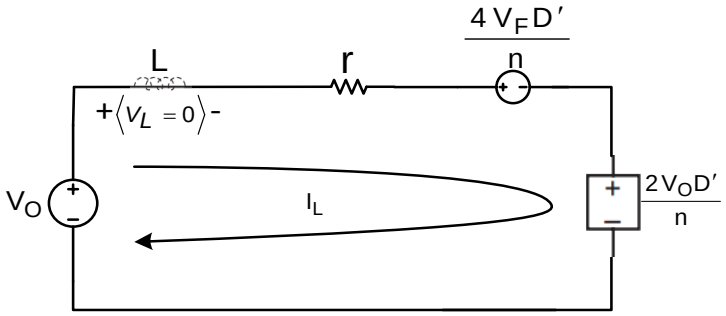


Figure 3.9: The equivalent DC circuit of the input section of the ICFFB converter.

Average capacitor current

The average capacitor current is found by taking the integral of the capacitor instantaneous current over one switching cycle using Eq. (3.2), (3.5) and (3.7), and it is given as

$$\begin{aligned} \langle I_C(t) \rangle &= \frac{1}{T_s} \int_0^{T_s} i_C(t)\,dt \\ &= 2\left(-\frac{V_O}{R}\right)\left(D - \frac{1}{2}\right) + 2\left(I_O - \frac{V_O}{R}\right)D' = 2I_O D' - \frac{V_O}{R}. \end{aligned} \tag{3.13}$$

Where $\langle I_C(t) \rangle$ is the total capacitor current over one switching cycle.

According to the capacitor charge-balance principle, when a converter is operating in steady state under CCM conditions, the net change in the capacitor voltage during the charging interval is equal to the net change in the capacitor voltage during the discharging interval over one switching cycle. Applying the capacitor charge-balance principle to the average capacitor current will therefore yield a zero net charge-balance. The capacitor charge-balance over one switching cycle is therefore given as

$$\begin{aligned} 0 &= \frac{1}{T_s} \int_0^{T_s} i_C(t)\,dt \\ &= 2\left(-\frac{V_O}{R}\right)\left(D - \frac{1}{2}\right) + 2\left(I_O - \frac{V_O}{R}\right)D' = 2I_O D' - \frac{V_O}{R}. \end{aligned} \tag{3.14}$$

Where

$$I_O = \frac{V_O}{2D'R}, \tag{3.15}$$

$$V_O = \frac{2I_L D'R}{n}. \tag{3.16}$$

Replacing I_L in Eq. (3.16) with the value of I_L found in eq. (3.11), and then solving for V_O yields

$$V_O = \frac{V_I}{\frac{2D'}{n}\left(1+\frac{2V_F}{V_O}+\frac{n^2 r}{4D'^2 R}\right)}. \qquad (3.17)$$

Figure 3.10 shows the equivalent DC circuit of the output section of the ICFFB converter constructed from the capacitor charge-balance equation.

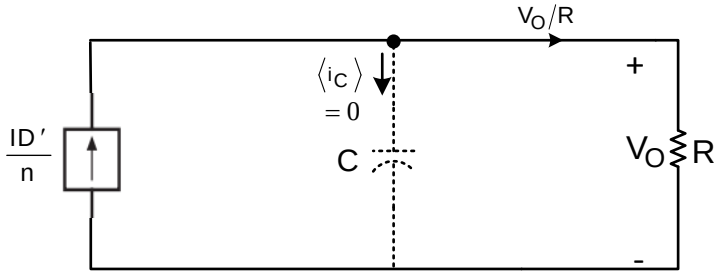


Figure 3.10: The equivalent DC circuit of the output section of the ICFFB converter.

Figure 3.11 shows the complete DC circuit of the ICFFB converter constructed from a combination of the inductor volt-second balance equation and the capacitor charge-balance equation.

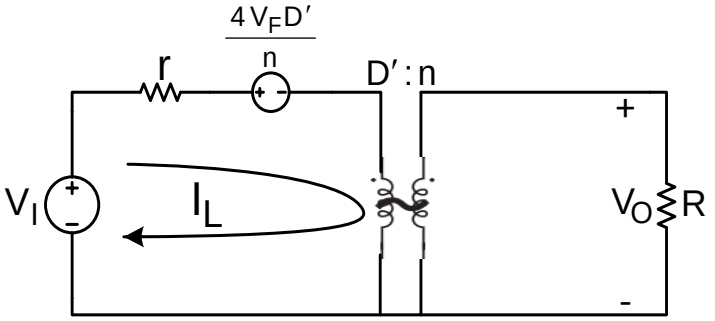


Figure 3.11: The complete DC circuit of the ICFFB converter.

DC Voltage transfer function

The DC voltage transfer function of the converter can be derived from Figure 3.11 or Eq. (3.17) and it given as

$$M(D) = \frac{V_O}{V_I} = \frac{V_I}{\frac{2D'}{n}\left(1+\frac{2V_F}{V_O}+\frac{n^2 r}{D'^2 R}\right)V_I} = \frac{n}{2D'\left(1+\frac{2V_F}{V_O}+\frac{n^2 r}{4D'^2 R}\right)} \qquad (3.18)$$

DC Current transfer function

The DC current transfer function of the converter is derived from Eq. (3.15) and (3.16) and it is given as

$$M(I) = \frac{I_O}{I_I} = \frac{D'}{n}. \tag{3.19}$$

The inductor current ripple

The peak-to-peak inductor current ripple Δi_L is the change in the inductor current during the charging interval or the discharging interval of the inductor. The change in the inductor current in any operating mode is proportional to the inductor current slope of that operating mode. The inductor current slope can be varied by varying the inductance of the inductor. The peak-to-peak inductor current ripple for the ICFFB converter is derived from Eq. (3.1) in mode 1 and it is expressed as

$$L\frac{di_L(t)}{dt} = V_I - (r_L + 2r_M)I_L \tag{3.20}$$

$$\Delta i_L = \frac{(V_I - (r_L + 2r_M)I_L)DT_S}{L} = \frac{(V_I - (r_L + 2r_M)I_L)D}{Lf_S}. \tag{3.21}$$

Substituting I_I with the value of I_I given by eq. (3.16) into eq. (3.21) yields

$$\Delta i_L = \frac{2V_I DD'R - nV_O D(r_L + 2r_M)}{2D'f_S LR}. \tag{3.22}$$

The minimum inductor value that is required to maintain the inductor current ripple within the desired range is derived from Eq. (3.22) by solving for L.

The capacitor voltage ripple

The peak-to-peak capacitor voltage ripple Δv_C is the change in the capacitor voltage during the charging interval or the discharging interval of the capacitor. The change in the capacitor voltage in any operating mode is proportional to the capacitor voltage slope of that operating mode. The voltage slope can be varied by varying the capacitance of the capacitor. The capacitor voltage ripple is derived from Eq. (3.2) in mode 1 and it is expressed as

$$C\frac{dv_C(t)}{dt} = \frac{V_O DT_S}{R}. \tag{3.23}$$

$$\Delta v_C = \frac{V_O DT_S}{RC} = \frac{V_O D_{max}}{R_{Lmin} C_{min} f_S}, \tag{3.24}$$

The minimum capacitor value that is required to maintain the capacitor voltage ripple within the desired range is derived from Eq. (3.24) by solving for C_{min}.

Converter Efficiency

The converter efficiency is derived by substituting Eq. (3.18) and (3.19) into eq. (3.25) and then solving for η as shown below

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{V_O D'}{V_I n} = M(D)\,\frac{D'}{n}. \tag{3.25}$$

Where η is the converter efficiency in Watts. The converter duty cycle D is derived from Eq. (3.25) and is given as

$$D = 1 - \frac{\eta V_I n}{V_O}. \tag{3.26}$$

3.2.4 Small Signal Modelling of the ICFFB Converter

According to Robert and Dragan (2001) and Czarlcowslci and Kazimierczuk (1992), the voltage and current waveforms of PWM converters consists of low frequency excitations (AC components or small AC variations) superimposed on steady state (DC) components of the waveforms. Fundamentally, each of the waveforms has a DC component, a low frequency AC component with its harmonics and a high frequency component of the converter switching frequency with its harmonics (Czarlcowslci & Kazimierczuk, 1992) .In the design of a converter controller, only linearized average DC components and low frequency AC components of the waveforms are considered. Therefore, based on the analysis of Robert and Dragan (2001) and Czarlcowslci and Kazimierczuk (1992), the averaged inductor and capacitor equations given by Eq. (3.10) and (3.13) are re-written as

$$\begin{aligned} L\frac{d\langle i_L(t)\rangle_{T_S}}{dt} &= \langle v_I(t)\rangle_{T_S} - (r_L + 2r_M)\langle I_L(t)\rangle_{T_S} \\ &- \frac{4}{n}\left(\frac{r_F\langle I_L(t)\rangle_{T_S}}{n} + V_F + \frac{\langle v_O(t)\rangle_{T_S}}{2}\right)d'(t), \end{aligned} \tag{3.27}$$

$$C\frac{d\langle v_c(t)\rangle_{T_S}}{dt} = 2\frac{d'(t)\langle I_L(t)\rangle_{T_S}}{n} - \frac{\langle v_O(t)\rangle_{T_S}}{R}. \tag{3.28}$$

The averaged inductor and capacitor equations given by Eq. (3.27) and (3.27) consist of the averaged voltage, the averaged current and the averaged duty cycle that contain DC components and low frequency AC components, which are expressed as

$$\langle v_I(t)\rangle_{T_S} = V_I + \hat{v}_I(t), \tag{3.29}$$

$$d'(t) = 1 - (D + \hat{d}(t)), \tag{3.30}$$

$$\langle i_L(t)\rangle_{T_S} = I_L + \hat{i}_L(t), \tag{3.31}$$

$$\langle v_O(t)\rangle_{T_S} = V_O + \hat{v}_O(t), \tag{3.32}$$

$$\langle v_c(t)\rangle = V_C + \hat{v}_C(t). \tag{3.33}$$

Equation (3.27) and (3.28) are non-linear due to the time variant quantities (small AC variations): $\hat{v}_I(t)$, $\hat{d}(t)$, $\hat{i}_L(t)$, $\hat{v}_O(t)$ and $\hat{v}_c(t)$. In Eq. (3.29) to (3.33), the small AC variations are superimposed on the DC components. The DC components are given as V_I, D, I_L, V_O and V_C.

The next step is to linearize Eq. (3.27), (3.28) and the equation of the output voltage at the DC operating point, and to construct the equivalent small signal model of the converter. In order to linearize the equations, we expand them by inserting the DC values and the small AC variations, thereafter; we multiply them out and discard all terms that contain only: DC quantities, AC quantities and the diode forward voltage drop. The residue of each equation is a linearized equation and consists of first order AC quantities containing a single AC quantity multiplied by a DC term. The linearized small signal equations that describe the AC small signal variations of the ICFFB converter are given as

$$L\frac{d\hat{i}_L(t)}{dt} = \hat{v}_I(t) - \hat{i}_L(t)(r_L + 3r_M - 2r_M D) - \frac{2}{n}\left(2\frac{\left(D' r_F \hat{i}_L(t) - I_L r_F \hat{d}(t)\right)}{n} + D'\hat{v}_O(t) - V_O\hat{d}(t)\right), \tag{3.34}$$

$$C\frac{d\hat{v}(t)}{dt} = -\frac{\hat{v}_O(t)}{R} - 2\frac{I_L\hat{d}(t)}{n} + 2\frac{D'\hat{i}_L(t)}{n}, \tag{3.35}$$

$$\hat{v}_O(t) = \hat{v}_c(t) + r_c C\frac{d\hat{v}_c(t)}{dt}. \tag{3.36}$$

The next step is to take the Laplace transform of Eq. (3.34) and (3.35), and the results are given as

$$sL\hat{i}_L(s) = \hat{v}_I(s) - r\hat{i}_L(s) + r_1 I_L\hat{d}(t) + \frac{2V_o\hat{d}(s)}{n} - \frac{2D'\hat{v}_O(s)}{n}, \tag{3.37}$$

$$sC\hat{v}_c(s) = -\frac{\hat{v}_O(s)}{R} - 2\frac{I_L\hat{d}(s)}{n} + 2\frac{D'\hat{i}_L(s)}{n}, \tag{3.38}$$

where r is equal to $\left(r_L + 3r_M - 2r_M D + \frac{4r_F D'}{n^2}\right)$ and r_1 is equal to $2r_M + \frac{4r_F}{n^2}$.

Figure 3.12 shows the equivalent small signal model of the ICFFB converter derived from the linearized inductor and capacitor small signal equations given by Eq. (3.34) and (3.35).

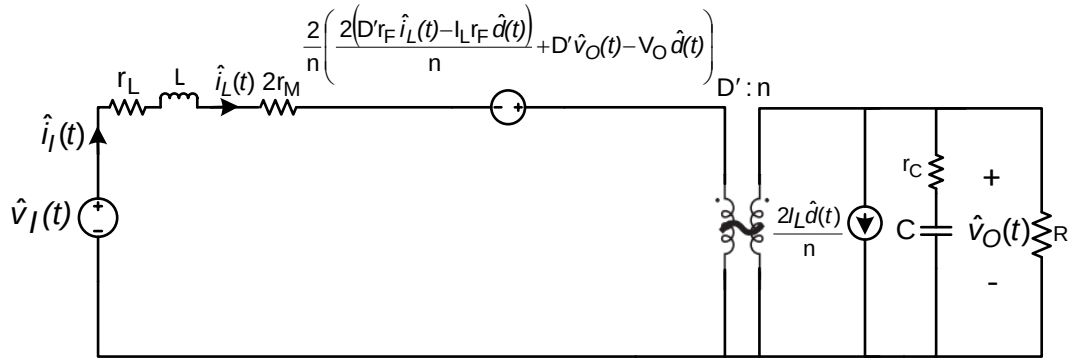


Figure 3.12: The equivalent small signal model of the ICFFB converter.

Open-loop Transfer Functions

Figure 3.12 represents the equivalent small signal model of the ICFFB converter as a system with two inputs and one output. The inputs and output of the system can be expressed in the Laplace domain as $\hat{v}_I(s)$, $\hat{d}(s)$ and $\hat{v}_O(s)$. Where $\hat{v}_O(s)$ is the small signal AC output voltage variation of the converter and it can be expressed as the superposition of compounds derived from the inputs as

$$\hat{v}_O(s) = G_{vOd}(s)\hat{d}(s) + G_{vOI}(s)\hat{v}_I(s). \tag{3.39}$$

The small signal open-loop control-to-output transfer function $G_{vOd}(s)$ is defined as

$$G_{vOd}(s) = \left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_I(s)=0}, \tag{3.40}$$

And the open-loop line-to-output transfer function $G_{vOI}(s)$ is defined as

$$G_{vOI}(s) = \left.\frac{\hat{v}_O(s)}{\hat{v}_I(s)}\right|_{\hat{d}(s)=0}. \tag{3.41}$$

In Eq. (3.27) solving for $\hat{i}_L(s)$ then substituting the result into Eq. (3.38) and then solving for $\hat{v}_O(s)$ yields the simplified small signal output voltage of the ICFFB converter which is expressed in the normalized form as

$$\hat{v}_O(s) = \frac{\left(2\left[n\hat{v}_I(s) + nr_1 I_L\hat{d}(s) + 2V_O\hat{d}(s)\right]D'R - 2n(sL+r)I_L\hat{d}(s)R\right)(1+sr_C C)}{n^2(sL+r)sRC + 4D'^2R(1+sr_c C)R + n^2(sL+r)(1+sr_c C)} \tag{3.42}$$

The small signal open-loop control-to-output transfer of the converter is derived from Eq. (3.40) and (3.42), and expressed in the standard form of a second order transfer function of a system as

$$G_{vOd}(s) = -G_{vO}\frac{\left(1+\frac{s}{\omega_{zn}}\right)\left(1-\frac{s}{\omega_{zp}}\right)}{1+\frac{s}{Q\omega_O}+\left(\frac{s}{\omega_O}\right)^2}, \tag{3.43}$$

The open-loop control-to-output transfer function of the ICFFB converter is therefore given as

$$G_{vOd}(s) = \left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_I(s)=0} = -\frac{V_O r_C}{D'(R+r_C)} \times \frac{\left(s+\frac{1}{Cr_C}\right)\left(s-\frac{1}{L}\left[\frac{4D'^2R}{n^2}+D'r_1-r\right]\right)}{s^2+\frac{s\left[C\left(n^2r(R+r_C)+4D'^2Rr_C\right)+n^2L\right]}{n^2LC(R+r_C)}+\frac{4D'^2R+n^2r}{n^2LC(R+r_C)}}. \tag{3.44}$$

The small signal open-loop line-to-output transfer function of the converter is derived from Eq. (3.41) and (3.42), and expressed in the standard form of a second order transfer function of a system as

$$G_{vOl}(s) = G_{vO}\frac{1+\frac{s}{\omega_{zn}}}{1+\frac{s}{Q\omega_O}+\left(\frac{s}{\omega_O}\right)^2} \tag{3.45}$$

The open-loop line-to-output transfer function of the ICFFB converter is therefore given as

$$G_{vOl}(s) = \left.\frac{\hat{v}_O(s)}{\hat{v}_I(s)}\right|_{\hat{d}(s)=0} = 2\frac{D'Rr_C}{nL(R+r_C)} \times \frac{s+\frac{1}{Cr_C}}{s^2+\frac{s\left[C\left(n^2r(R+r_C)+4D'^2Rr_C\right)+n^2L\right]}{n^2LC(R+r_C)}+\frac{4D'^2R+n^2r}{n^2LC(R+r_C)}}. \tag{3.46}$$

3.2.5 Design of the ICFFB Converter

Table 3.1 shows the converter design specifications. The parameter and component values of the converter power stage are determined by using the given design specifications, the steady state parameter and component equations that were derived in the converter steady state analysis section.

Table 3.1: The ICFFB converter design specifications

parameter	Value	Comments
Output power P_O	50 – 900 W	At full-load for P_I of 1 kW
Input voltage V_I	36 – 67 VDC	With Nominal Voltage of 52 VDC
Output voltage V_O	100 VDC	Galvanic isolation required
Efficiency target η	90 %	optimised at full-load
Input current ripple	$\leq$ 30 % of I_L	For load range 5.5-100 %
Output voltage ripple Δv_O	< 1 % of V_O	
Switching frequency f_s	$\cong$ 50 kHz	

DC voltage transfer function calculation

The maximum, nominal and minimum values of the DC voltage transfer function are calculated by using Eq. (3.18) and they are given as 2.8, 2 and 1.5.

Turns-ratio selection

The turns-ratio n is determined by using Eq. (3.26), with the assumption that the maximum duty cycle D_{max} is 0.45. The calculated maximum turns-ratio is 1.7, but a value of 1.6 was selected. With this value of n, the duty cycle can be varied above or below its nominal value in proportion to the input voltage range.

Duty cycle

The maximum, nominal and minimum values of the duty cycle are determined by using Eq. (3.26) and they are given as 0.49, 0.28 and 0.04.

Selection of Capacitor, Inductor and load Resistor

The minimum value of the capacitor which is required to achieve the specified output voltage ripple is determined by using Eq. (3.24) and it is given as $173.39\,\mu F$. While the maximum value of the required capacitor ESR is given as $9\ m\Omega$.

The minimum value of the inductor which is required in order to achieve an inductor current ripple equal to 30 % of the minimum input current, and to keep the converter operation in CCM is determined by using eq. (3.22), and it is given as $47.287\,\mu H$.

The required range of the load resistor is determined by using eq. (3.25) and it is given as $11.11\ \Omega$ – $200\ \Omega$.

3.3 Boost converter

3.3.1 Modelling of the boost Converter

In this section, the circuit, the operation and the circuit averaging description of a boost converter are presented. Based on the circuit averaging description of the converter over one switching period, the parameter and component equations are derived. A linearized small signal model is also derived from which the small signal input-to-output and control-to-output voltage transfer functions are derived. The transfer functions are used later in the design of a controller and in the simulation stage.

3.3.2 Circuit topology

Figure 3.13 shows the circuit of the PWM boost converter without parasitic resistances. The circuit consists of a DC input voltage V_I, one controllable MOSFET switch S, one high-speed high power diode D_1, an input inductor L, an output filter capacitor C and a resistive load R. Further, the circuit consists of the input current I_I, the inductor voltage V_L, the inductor current I_L, the diode current I_D, the capacitor current I_C, the load current I_{Load} and the output voltage V_O. The analysis of the boost converter covered in this section is based on the works of (Robert & Dragan, 2001) and (Kazimierczuk, 2008).

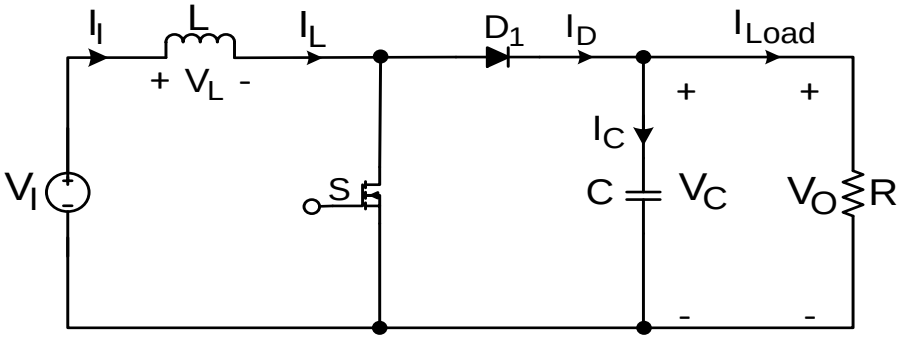


Figure 3.13: The circuit of the PWM boost converter.

Figure 3.14 shows the detailed circuit of a non-ideal PWM boost converter with the series parasitic resistances of the components. In the diagram r_L is the equivalent series resistance (ESR) of the input inductor, r_M is MOSFET parasitic resistance when conducting, V_F is the forward voltage drop across the diode when conducting, r_F is the forward resistance of the diode when conducting and r_C is the equivalent series resistance (ESR) of the capacitor. In the circuit, the full model of the rectifier diode is depicted as a voltage source in series with a forward resistor enclosed inside dotted lines.

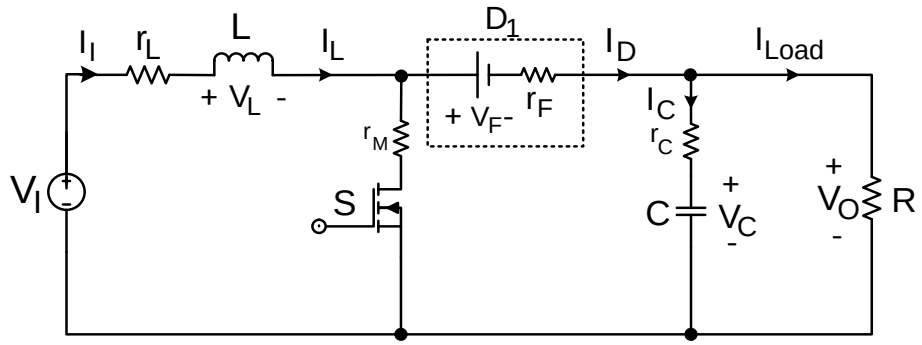


Figure 3.14: The detailed circuit of the PWM boost converter.

3.3.3 Converter Steady State Analysis

Operation Principle of the Converter

In the analysis of the boost converter circuit, it is assumed that the converter is operating in steady state with CCM. With CCM, the operation of the boost converter over one switching period can be divided into two modes, where one switching cycle is equal to T_s. The MOSFET switch is hard switched by a gate signal at the switching frequency $f_s = (1/T_s)$, with a duty cycle D. Figure 3.15 shows some of the important switching waveforms of the converter over one switching period. Where the time intervals DT_s and $D'T_s$ are equal to one operating period.

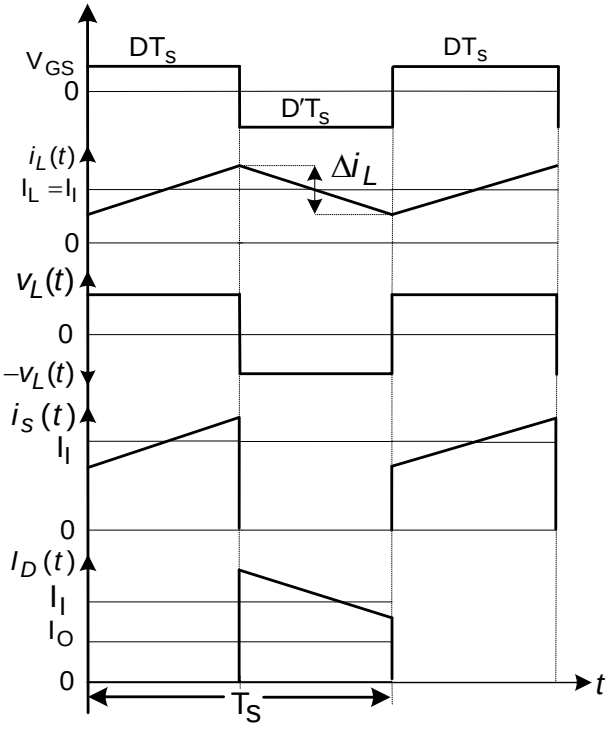


Figure 3.15: The current and voltage waveforms of the boost converter during steady state switching.

Where V_{GS} is the gate signal for the MOSFET, $i_L(t)$ is the instantaneous inductor current, Δi_L is the peak-to-peak inductor current ripple, I_L is the average inductor current, $V_L(t)$ is the average inductor voltage, $i_S(t)$ is the MOSFET instantaneous current, I_I is the average input current, $I_D(t)$ is the diode instantaneous current, DT_S is the switch on-time and $D'T_S$ is the switch off-time.

Figure 3.16 and Figure 3.17 show the operation modes of the boost converter.

Mode 1: DT_s

Figure 3.16 shows the equivalent circuit of the converter during mode1. During this interval the switch S turn on and conducts the inductor current I_L, the inductor is charged up by the source, the diode is reverse biased and the capacitor provides power to the load resistor. This mode ends when the switch turn off.

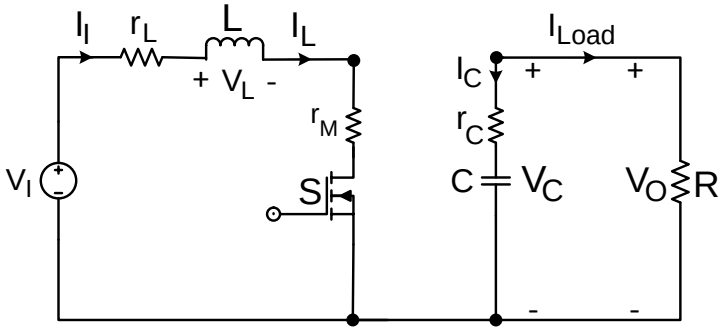


Figure 3.16: The equivalent circuit of the boost converter during mode 1.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L\frac{di_L(t)}{dt} = V_I - r_L I_L - r_M I_L, \tag{3.47}$$

$$C\frac{dv_C(t)}{dt} = -\frac{V_O}{R}, \tag{3.48}$$

$$V_O = V_C + r_C I_{Load} = V_C + r_C \frac{V_O}{R}. \tag{3.49}$$

Mode 2: $D'T_s$

Figure 3.17 shows the equivalent circuit of the boost converter during mode 2. During this interval, the switch turn off and the diode is forward biased and conducts the inductor current I_L. While the inductor discharges current into the output capacitor and the load resistor via the diode.

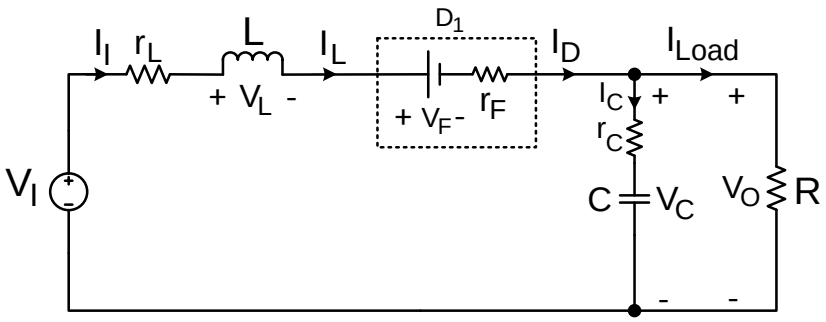


Figure 3.17: The equivalent circuit of the boost converter during mode 2.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L\frac{di_L(t)}{dt} = V_I - r_L I_L - r_F I_D - V_F - V_O, \tag{3.50}$$

$$C\frac{dv_C(t)}{dt} = I_D - I_{Load} = I_L - \frac{V_O}{R}, \tag{3.51}$$

$$V_O = V_C + r_C I_C = V_C + r_C C\frac{dv_C(t)}{dt}. \tag{3.52}$$

Average inductor voltage

The average inductor voltage is found by taking the integral of the inductor instantaneous voltage over one switching cycle using Eq. (3.47) and (3.50), and it is given as

$$\begin{aligned}\langle v_L(t)\rangle &= \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt,\\ &= D\left(V_I - r_L I_L - r_M I_L\right) + D'\left(V_I - r_L I_L - r_F I_L - V_F - V_O\right).\end{aligned} \tag{3.53}$$

Applying the inductor volt-second balance principle to Eq. (3.53) yields

$$\begin{aligned}0 &= \frac{1}{T_s}\int_0^{T_s} V_L(t)\,dt\\ &= D\left(V_I - r_L I_L - r_M I_L\right) + D'\left(V_I - r_L I_L - r_F I_D - V_F - V_O\right)\\ &= V_I - \left(Dr_M + r_L + D'r_F\right)I_L - D'V_F - D'V_O\\ &= V_I - rI_L - D'V_F - D'V_O.\end{aligned} \tag{3.54}$$

Where

$$r = Dr_M + r_L + D'r_F. \tag{3.55}$$

Figure 3.18 shows the equivalent DC circuit of the input section of the boost converter constructed from the inductor volt-second balance equation given by Eq. (3.54).

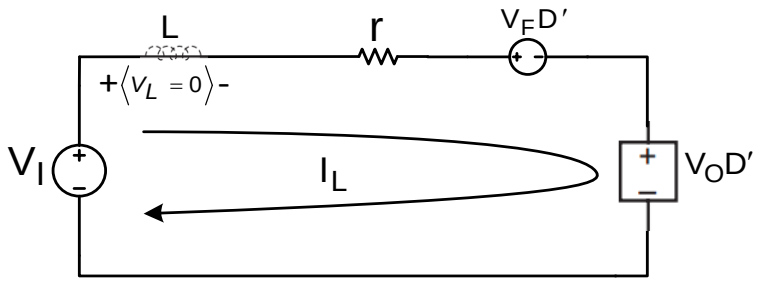


Figure 3.18: The equivalent DC circuit of the input section of the boost converter.

Average capacitor current

The average capacitor current is found by taking the integral of the capacitor instantaneous current over one switching cycle using Eq. (3.48) and (3.51), and it is given as

$$\langle I_C(t) \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t) dt = D\left(-\frac{V_O}{R} \right) + D'\left(I_L - \frac{V_O}{R} \right). \qquad (3.56)$$

Applying the capacitor charge-balance principle to eq. (3.56) yields

$$0 = \frac{1}{T_s} \int_0^{T_s} I_C(t) d = D\left(-\frac{V_O}{R} \right) + D'\left(I_L - \frac{V_O}{R} \right) = I_L D' - \frac{V_O}{R}. \qquad (3.57)$$

The output voltage is determined by replacing I_L in Eq. (3.57) with the value of I_L found in Eq. (3.54) and then solving for V_O which is given as

$$V_O = \frac{V_I}{D'\left(1 + \frac{V_F}{V_O} + \frac{r}{D'^2 R} \right)}. \qquad (3.58)$$

Figure 3.19 shows the equivalent DC circuit of the output section of the boost converter constructed from the capacitor charge-balance equation given by Eq. (3.57).

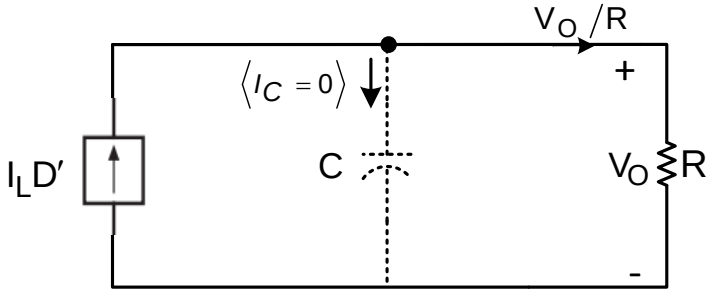


Figure 3.19: The equivalent DC circuit of the output section of the boost converter.

Figure 3.20 shows the complete DC circuit of the boost converter derived from the inductor volt-seconds balance equation and the capacitor charge-balance equation.

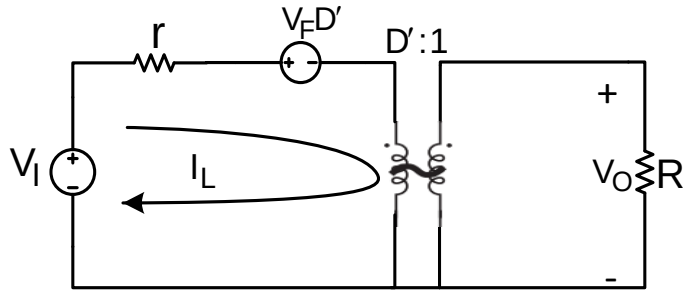


Figure 3.20: The complete DC circuit of the boost converter.

DC Voltage transfer function

The DC voltage transfer function of the converter can be derived from Figure 3.20 or Eq. (3.58) and it is expressed as

$$M(D) = \frac{V_O}{V_I}$$

$$= \frac{V_I}{D'\left(1+\frac{V_F}{V_O}+\frac{r}{D'^2 R}\right)V_I} = \frac{1}{D'\left(1+\frac{V_F}{V_O}+\frac{r}{D'^2 R}\right)}. \tag{3.59}$$

DC Current transfer function

The DC current transfer function of the converter is derived from Eq. (3.57) and (3.58) and it expressed as

$$M(I) = \frac{I_O}{I_I} = (1-D) = D'. \tag{3.60}$$

The inductor current ripple

The peak-to-peak inductor current ripple Δi_L is the change in the inductor current during the charging interval or the discharging interval of the inductor. It is derived from Eq. (3.47) in mode 1 and expressed as

$$L\frac{d i_L(t)}{dt} = V_I - r_L I_L - r_M I_L, \tag{3.61}$$

$$\Delta i_L = \frac{\left[V_I - r_L I_L - r_M I_L\right]DT_S}{L} = \frac{\left[D'^2 V_O R - (r_L + r_M)V_O\right]D}{D' f_S L R}. \tag{3.62}$$

The minimum inductor value that is required in order to maintain the inductor current ripple within the desired range is derived from Eq. (3.62) and expressed as

$$L_{min} \geq \frac{\left[D'^2_{min} V_O R_{max} - (r_L + r_M)V_O\right]D_{min}}{D'_{min} f_S \Delta i_L(max) R_{max}}. \tag{3.63}$$

Where D_{min} is minimum duty cycle during mode 1, D'_{min} is minimum duty cycle during mode 2, R_{max} is the maximum load resistor and $\Delta i_L(max)$ is the maximum peak-to-peak inductor current ripple.

The capacitor voltage ripple

The peak-to-peak capacitor voltage ripple Δv_C is the change in the capacitor voltage during the charging interval or the discharging interval of the capacitor. It is derived from Eq. (3.48) and expressed as

$$C\frac{dv_C(t)}{dt} = -\frac{V_o}{R}, \tag{3.64}$$

$$\Delta v_C(t) = \frac{V_o DT}{RC} = \frac{V_o D}{f_s RC}, \tag{3.65}$$

where Δv_C is the peak-to-peak capacitor voltage ripple during mode 1.

The minimum capacitor value that is required to maintain the output voltage ripple within the desired range is derived from Eq. (3.65) and expressed as

$$C_{min} \geq \frac{V_O D_{max}}{f_s R_{min}\, \Delta v_C(max)}. \tag{3.66}$$

Converter Efficiency

The converter efficiency is derived by equating Eq. (3.59) and (3.60) and then solving for η as shown below

$$\begin{aligned}\eta &= \frac{P_O}{P_i} = \frac{V_O I_O}{V_I I_I} = \frac{V_O D'}{V_I} \\ &= M(D)\, D' \\ &= \frac{1}{\left(1 + \frac{V_F}{V_O} + \frac{r}{D'^2 R}\right)}.\end{aligned} \tag{3.67}$$

The converter duty cycle is derived from Eq. (3.67) and it is given as

$$\begin{aligned}D &= \frac{M(D) - \eta}{M(D)} \\ &= 1 - \frac{\eta}{M(D)} = 1 - \frac{\eta V_I}{V_O}.\end{aligned} \tag{3.68}$$

3.3.4 Small Signal Modelling of the Boost Converter

In order to perform the small signal analysis of the boost converter, the same approach that was taken for the small signal analysis of the ICFFB converter is considered. The nonlinear averaged inductor and capacitor equations are re-written as

$$\mathrm{L}\frac{\mathrm{d}\left\langle i_L(t)\right\rangle_{T_S}}{\mathrm{dt}} = \left\langle \mathrm{v_I(t)}\right\rangle_{\mathrm{T_S}} - \mathrm{r}\left\langle \mathrm{I_L(t)}\right\rangle_{\mathrm{T_S}} - \left(\mathrm{V_F} + \left\langle v_O(t)\right\rangle_{T_S}\right) d'(t), \tag{3.69}$$

$$\mathrm{C}\frac{\mathrm{d}\left\langle v_C(t)\right\rangle_{\mathrm{T_S}}}{\mathrm{dt}} = d'(t)\left\langle \mathrm{I_L(t)}\right\rangle_{\mathrm{T_S}} - \frac{\left\langle v_O(t)\right\rangle_{\mathrm{T_S}}}{\mathrm{R}}. \tag{3.70}$$

The next step is to perturb the above equations in order to get linearized equations that describe the AC small signal variations of the boost converter. The linearized equations are therefore given as

$$\mathrm{L}\frac{\mathrm{d}\hat{i}_L(t)}{\mathrm{dt}} = \hat{v}_I(t) - \mathrm{r}\,\hat{i}_L(t) - \mathrm{D}'\hat{v}_O(t) + \mathrm{V_O}\,\hat{d}(t), \tag{3.71}$$

$$\mathrm{C}\frac{\mathrm{d}\hat{v}(t)}{\mathrm{dt}} = -\frac{\hat{v}_O(t)}{\mathrm{R}} - \mathrm{I_L}\,\hat{d}(t) + \mathrm{D}'\hat{i}_L(t) \tag{3.72}$$

The final step is to take the Laplace transform of Eq. (3.71) and (3.72), and the results are given as

$$\mathrm{sL}\hat{i}_L(s) = \hat{v}_I(s) - \mathrm{r}\,\hat{i}_L(s) - \mathrm{D}'\hat{v}_O(s) + \mathrm{V_O}\,\hat{d}(s), \tag{3.73}$$

$$\mathrm{sC}\hat{v}(s) = -\frac{\hat{v}_O(s)}{\mathrm{R}} - \mathrm{I_L}\,\hat{d}(s) + \mathrm{D}'\hat{i}_L(s), \tag{3.74}$$

Figure 3.21 shows the equivalent small signal model of the boost converter derived from the linearized small signal equations of the inductor and capacitor.

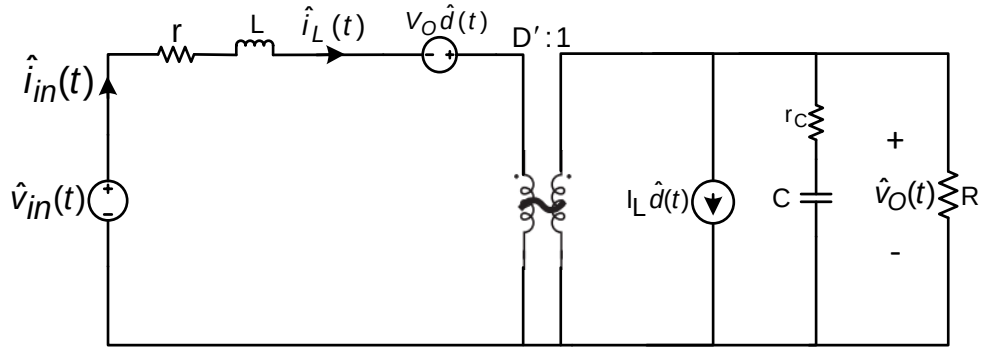


Figure 3.21: The equivalent small signal circuit model of the boost converter.

Open-loop Transfer Functions

The small signal output voltage of the boost converter can be derived from Eq. (3.713) and (3.724) or from Figure 3.21, and it is given as

$$\hat{v}_O(s) = \frac{\left(\frac{\hat{v}_I(s)}{\hat{d}(s)}D'R + V_O D'R - \frac{V_O(sL+r)}{D'}\right)\frac{\hat{d}(s)(1+sr_C C)}{LC(r_C+R)}}{s^2 + s\frac{C\left[r(R+r_C)+D'^2 r_C R\right]+L}{LC(r_C+R)} + \frac{r+D'^2 R}{LC(r_C+R)}} \tag{3.75}$$

The converter small signal open-loop control-to-output and line-to-output transfer functions are derived from Eq. (3.75) and they are given as

$$G_{v_O d(s)} = \frac{\hat{v}_O(s)}{\hat{d}(s)}\bigg|_{\hat{v}_I(s)=0} = -\frac{V_O r_C}{D'(r_C+R)} \times \frac{\left(s+\frac{1}{Cr_C}\right)\left(s-\frac{1}{L}\left[D'^2 R - r\right]\right)}{s^2 + s\frac{C\left[r(R+r_C)+D'^2 r_C R\right]+L}{LC(r_C+R)} + \frac{r+D'^2 R}{LC(r_C+R)}}, \tag{3.76}$$

$$G_{v_O I(s)} = \frac{\hat{v}_O(s)}{\hat{v}_I(s)}\bigg|_{\hat{d}(s)=0} = \frac{D'Rr_C}{L(r_C+R)} \times \frac{s+\frac{1}{Cr_C}}{s^2 + s\frac{C\left[r(R+r_C)+D'^2 r_C R\right]+L}{LC(r_C+R)} + \frac{r+D'^2 R}{LC(r_C+R)}}. \tag{3.77}$$

3.3.5 Design of the Boost Converter

Table 3.2 shows the converter design specifications. The parameter and component values of the converter power stage are determined by using the given design specifications, the steady state parameter and component equations that were derived in the steady state analysis section.

Table 3.2: The boost converter design specifications

parameter	Value	Comments
Output power P_O	50 – 900 W	At full-load for P_I of 1 kW
Input voltage V_I	36 – 67 VDC	Nominal Voltage: 52 VDC
Output voltage V_O	100 VDC	Galvanic isolation required
Efficiency target η	90 %	optimised at full-load
Input current ripple	$\leq$ 30 % of I_L	For load range 5.5-100 %
Output voltage ripple Δv_O	< 1 % of V_O	
Switching frequency f_s	$\cong$ 50 kHz	

DC voltage transfer function calculation

The maximum, nominal and minimum values of the DC voltage transfer function are calculated by using Eq. (3.68) and they are given as 2.8, 2 and 1.5.

Duty cycle

The maximum, nominal and minimum values of the duty cycle are determined by using Eq. (3.68) and they are given as 0.679, 0.55 and 0.4.

Selection of Capacitor, Inductor and Resistor

The minimum value of the capacitor, which is required to achieve the specified output voltage ripple, is determined by using Eq. (3.66) and it is given as $244.82\,\mu F$.

The minimum value of the inductor which is required to achieve an inductor current ripple equal to 30% of the minimum input current, and to keep the converter operation in CCM is determined by using Eq. (3.63), and it is given as $287.91\,\mu H$.

The required range of the load resistor is calculated by using Eq. (3.67), and it is given as 11.11 Ω – 200 Ω.

3.4 Sepic converter

3.4.1 Modelling of the sepic converter

In this section, the circuit, the operation and the circuit averaging description of a sepic converter are presented. Based on the circuit averaging description of the converter over one switching period, the parameter and component equations are derived. Linearized equations are also derived from which the small signal input-to-output and control-to-output voltage transfer functions are derived. The transfer functions are used later in the design of a controller and in the simulation stage.

The sepic converter is a fourth order system and that makes it difficult to control, however, because of its non-pulsating input current characteristic, it is widely used in battery powered applications where the input voltage to a load has to be stepped-up or stepped down depending on the state of charge (SOC) of the battery (Ray, 2006). In spite of the converter's popular use in battery-powered applications, there is lack of proper documentation of the topology (Ray, 2006). In this work, a full model of a sepic converter based on the work of Vorpérian is presented.

3.4.2 Circuit topology

Figure 3.22 shows the circuit of the PWM sepic converter. The circuit consists of an input voltage V_I, one controllable MOSFET switch S, one high speed high-power switching diode D_1, two input inductors L_1 and L_2, two capacitors C_1 and C_2 and a resistive load R. Further, the circuit consists of the input current I_I, the inductors voltages V_{L1} and V_{L2}, the inductors currents I_{L1} and I_{L2}, the capacitors voltages V_{C1} and V_{C2}, the capacitors currents I_{C1} and I_{C2}, the load current I_{Load} and the output voltage V_O. The analysis of the operation of the sepic converter covered in this section is based on the work of Robert and Dragan (2001), Vatché (2004) and Geethalakshmi and Sreeram (2014).

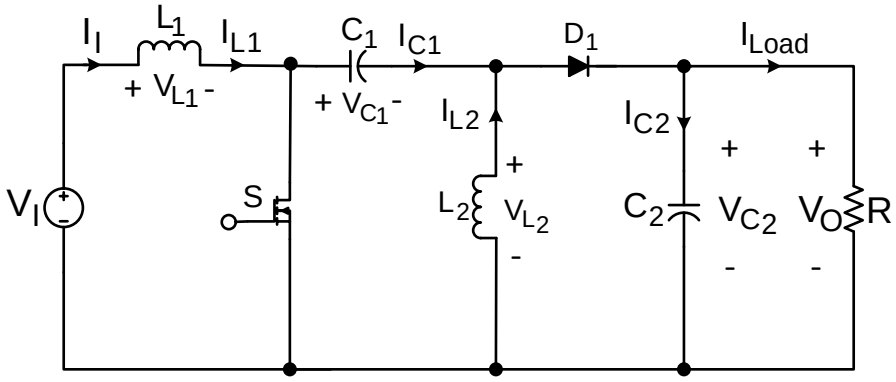


Figure 3.22: The circuit of the PWM sepic converter.

3.4.3 Converter steady state analysis

In the analysis of the sepic converter, it is assumed that the converter is operating in steady state with CCM. With CCM, the operation of the sepic converter over one switching period is divided into two modes, where one switching cycle is equal to T_S. The switch repeatedly turn on and off at the switching frequency $f_s(f_s = 1/T_s)$, with the duty cycle D. Figure 3.23 shows some of the important switching waveforms of the converter over one switching period. The time intervals DT_s and $D'T_s$ are equal to one operating period.

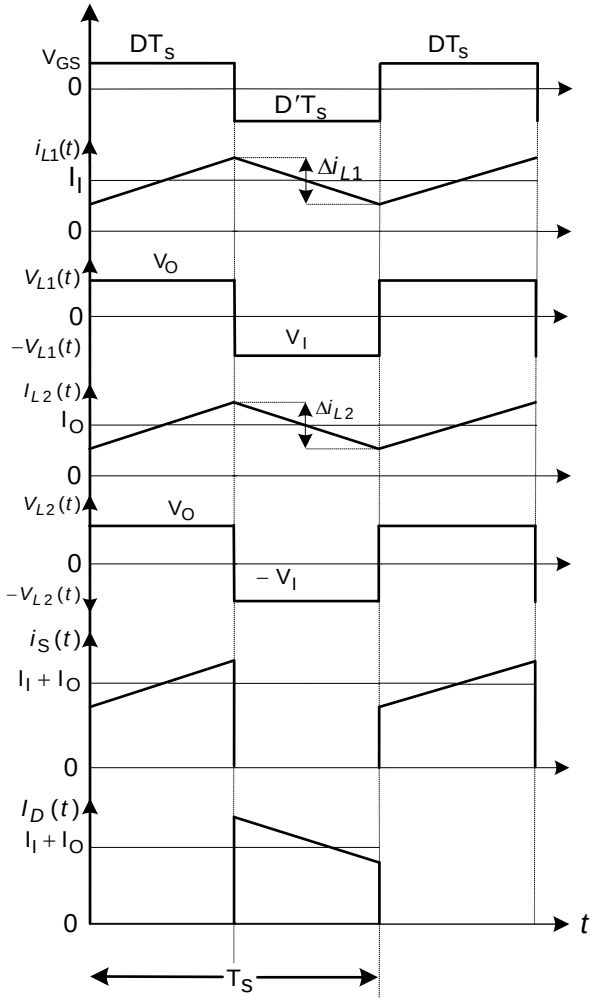


Figure 3.23: The current and voltage waveforms of the sepic converter during steady state switching.

Where V_{GS} is the gate signal for the MOSFET, $i_{L1}(t)$ and $i_{L2}(t)$ are the inductors instantaneous current, $\Delta i_{L1}(t)$ and $\Delta i_{L2}(t)$ are the inductors peak-to-peak current ripple, I_O is the average output current and it equal to I_{Load}, $V_{L1}(t)$ and $V_{L2}(t)$ are the average inductors voltage, $i_S(t)$ is the MOSFET instantaneous current, I_I is the average input current, $I_D(t)$ is the diode instantaneous current, DT_S is the switch on-time and $D'T_S$ is the switch off-time.

Mode 1: DT_s

Figure 3.24 shows the equivalent circuit of the sepic converter during mode 1. The circuit includes the inductors ESRs r_{L1} and r_{L2}, the capacitors ESRs r_{C1} and r_{C2} and the MOSFET series resistance r_M. During this time interval, the switch turn on and conduct the input current, both inductors are charging up, C_1 discharges through L_2 and C_2 provides power to the load. According to Ray (2006), the fact that both inductors are uncoupled from the load at this interval leads to difficult control characteristics. This interval ends when the switch turn off.

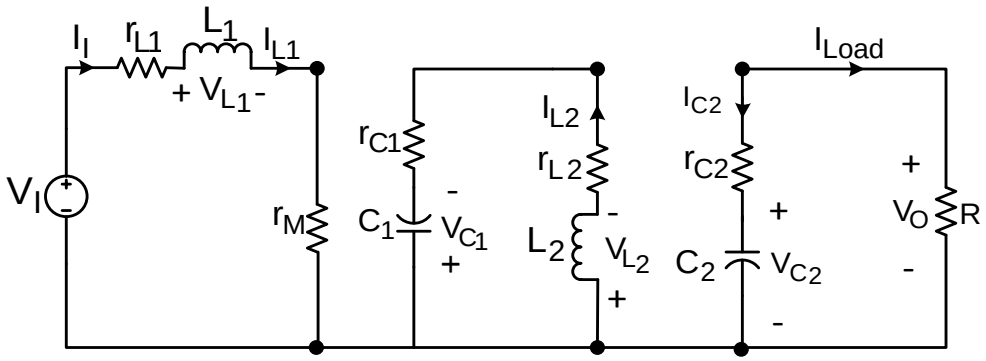


Figure 3.24: The equivalent circuit of the sepic converter during mode 1.

The differential equations that describe the dynamics of the converter during this mode of operation are expressed as

$$L_1 \frac{di_{L_1}(t)}{dt} = V_I - I_{L_1}\left(r_{L_1} + r_M\right), \tag{3.78}$$

$$C_1 \frac{dv_{C_1}(t)}{dt} = -I_{L_2}, \tag{3.79}$$

$$L_2 \frac{di_{L_2}(t)}{dt} = V_{C_1} - I_{L_2}\left(r_{L_2} + r_{C_1}\right), \tag{3.80}$$

$$C_2 \frac{dv_{C_2}(t)}{dt} = -\frac{V_O}{R} \tag{3.81}$$

Mode 2: $D'T_s$

Figure 3.25 shows the equivalent circuit of the sepic converter during mode 2. During this time interval, the switch turn off, and both inductors provide current to the load, I_{L1} charges C_1 and C_2 is charged up by the current from both inductors. This mode ends when the switch turn on.

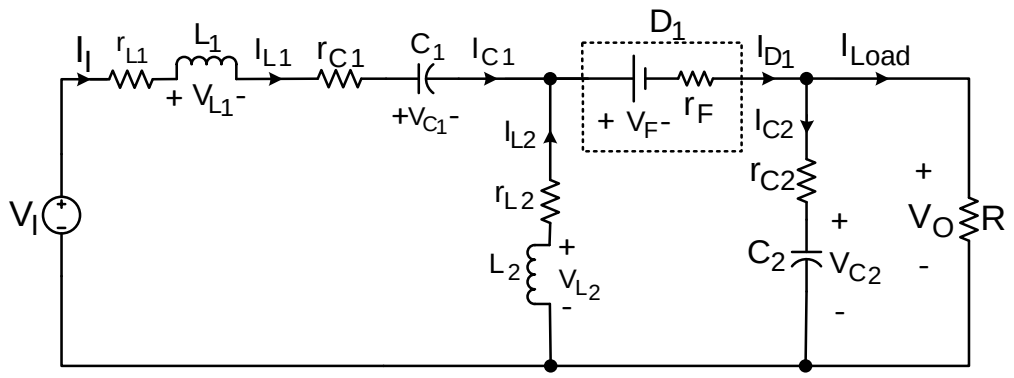


Figure 3.25: The equivalent circuit of the sepic converter during mode 2.

The differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L_1 \frac{di_{L_1}(t)}{dt} = V_I - I_{L_1}\left(r_{L_1} + r_{C_1}\right) - V_{C_1} - r_F\left(I_{L_1} + I_{L_2}\right) - V_{D_1} - V_O, \tag{3.82}$$

$$C_1 \frac{dv_{C_1}(t)}{dt} = I_{L_1}, \tag{3.83}$$

$$L_2 \frac{di_{L_2}(t)}{dt} = -V_O - I_{L_1} r_F - I_{L_2}\left(r_{L_2} + r_F\right), \tag{3.84}$$

$$C_2 \frac{dv_{C_2}(t)}{dt} = I_{L_1} + I_{L_2} - \frac{V_O}{R}. \tag{3.85}$$

Average capacitor current for C_1

The average capacitor current for C_1 is found by taking the integral of the instantaneous current through C_1 over one switching cycle and it is given as

$$\begin{aligned} \left\langle i_{C_1}(t)\right\rangle &= \frac{1}{T_s}\int_0^{T_s} i_{C_1}(t)dt = 0, \\ \left\langle i_{C_1}(t)\right\rangle &= \frac{1}{T_s}\left[\int_0^{DT_S} i_{C1}(t)dt + \int_{DT_S}^{T_S} i_{C_1}(t)dt\right] = 0 \\ \left\langle i_{C_1}(t)\right\rangle &= D'I_{L_1} - DI_{L_2} = 0. \end{aligned} \tag{3.86}$$

I_{L_1} is derived from Eq. (3.86) and it is given as

$$I_{L_1} = \frac{D}{D'} I_{L_2}. \tag{3.87}$$

Average capacitor current for C_2

The average capacitor current for C_2 is found by taking the integral of the instantaneous current through C_2 over one switching cycle and it is given as

$$\left\langle i_{C2}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} I_{C2}(t)\,dt = 0,$$

$$\left\langle i_{C2}(t)\right\rangle = \frac{1}{T_s}\left[\int_0^{DT_s} I_{C2}(t)\,dt + \int_{DT_s}^{T_s} I_{C2}(t)\,dt\right] \tag{3.88}$$

$$\left\langle i_{C2}(t)\right\rangle = D'I_{L1} + D'I_{L2} + \frac{V_O}{R} = 0.$$

I_{L1} is derived from Eq. (3.88) and it is expressed as

$$I_{L1} = \frac{V_O}{D'R} - I_{L2}\,. \tag{3.89}$$

I_{L2} is derived by equating Eq. (3.87) to (3.89) and then solving for I_{L2} as shown below

$$\frac{D}{D'}I_{L2} = \frac{V_O}{D'R} - I_{L2}\,,$$
$$I_{L2} = \frac{V_O}{R}. \tag{3.90}$$

I_{L1} can also be derived by substituting the value of I_{L2} found in Eq. (3.90) into Eq. (3.87) or (3.89) and it is given as

$$I_{L1} = \frac{D}{D'}I_{L2}\,,$$
$$I_{L1} = \frac{V_O D}{D'R}. \tag{3.91}$$

Average inductor voltage for L_1

The average inductor voltage across L_1 is found by taking the integral of the inductor instantaneous voltage over one switching cycle by using Eq. (3.92) and it is expressed as

$$\left\langle v_{L1}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} V_L(t)\,dt = 0,$$

$$\left\langle v_{L1}(t)\right\rangle = \frac{1}{T_s}\left[\int_0^{DT_s} V_{L1}(t)\,dt + \int_{DT_s}^{T_s} V_{L1}(t)\,dt\right] = 0,$$

$$0 = \frac{V_I}{D'} - \frac{V_O D^2 r_M}{RD'^2} - \frac{V_O D r_{L1}}{RD'^2} - \frac{V_O D r_{C1}}{RD'} - \frac{V_O r_F}{RD'} - V_F \tag{3.92}$$
$$- V_O - V_{C1}\,.$$

The voltage across C_1, V_{C1}, is derived from Eq. (3.92) and it expressed as

$$V_{C_1} = \frac{V_I}{D'} - V_O\left(\frac{D^2 r_M}{RD'^2} - \frac{Dr_{L_1}}{RD'^2} - \frac{Dr_{C_1} + r_F}{RD'} - 1\right) - V_F . \tag{3.93}$$

Average inductor voltage for L_2

The average voltage across L_2 is found by taking the integral of the inductor instantaneous voltage over one switching cycle and it is expressed as

$$\begin{aligned}
&\left\langle v_{L_2}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} V_{L1}(t)\,dt = 0,\\
&\left\langle v_{L_2}(t)\right\rangle = \frac{1}{T_s}\left[\int_0^{DT_s} V_{L_2}(t)\,dt + \int_{DT_s}^{T_s} V_{L_2}(t)\,dt\right] = 0\\
&\left\langle v_{L_2}(t)\right\rangle = DV_{C_1} - (V_O + V_F)D' - I_{L_2}\left(D'r_F + Dr_{C_1} + r_{L_2}\right)\\
&- D'I_{L_1}r_F = 0,\\
&\left\langle v_{L_2}(t)\right\rangle = DV_{C_1} - \frac{V_O r_F}{R} - \frac{V_O r_{L_2}}{R} - \frac{V_O Dr_{C_1}}{R} - V_O D'\\
&- V_F D' = 0.
\end{aligned} \tag{3.94}$$

The voltage across C_2, V_{C2}, is derived from Eq. (3.94) and it is expressed as

$$V_{C_1} = \frac{V_O r_F}{RD} + \frac{V_O r_{L_2}}{RD} + \frac{V_O Dr_{C_1}}{R} + \frac{V_O D'}{D} + \frac{V_F D'}{D}. \tag{3.95}$$

DC Voltage transfer function

The DC voltage transfer function of the sepic converter is derived from Eq. (3.93) and (3.95). First, Eq. (3.95) is equated to Eq. (3.93) and then solving for V_O as shown below.

$$\begin{aligned}
&\frac{V_O r_F}{RD} + \frac{V_O r_{L_2}}{RD} + \frac{V_O Dr_{C_1}}{R} + \frac{V_O D'}{D} + \frac{V_F D'_F}{D} = \frac{V_I}{D'}\\
&- \frac{V_O D^2 r_M}{RD'^2} - \frac{V_O Dr_{L_1}}{RD'^2} - \frac{V_O Dr_{C_1}}{RD'} - \frac{V_O r_F}{RD'} - V_F - V_O,\\
&V_O = \frac{V_I D}{D'\left(1 + \frac{V_F}{V_O} + \frac{r_{C_1}D + r_F D}{RD'} + \frac{r_{L_1}D^2 + D^3 r_M}{RD'^2} + \frac{r_{L_2}}{R} + r_F\right)}.
\end{aligned} \tag{3.96}$$

The DC voltage transfer function of the converter is derived from Eq. (3.96) and it is expressed as

$$M(D) = \frac{D}{D'\left(1 + \frac{V_F}{V_O} + \frac{r_{C_1}D + r_F D}{RD'} + \frac{r_{L_1}D^2 + D^3 r_M}{RD'^2} + \frac{r_{L_2}}{R} + r_F\right)}. \tag{3.97}$$

DC Current transfer function

The DC current transfer function of the converter is equivalent to the inverse of the converter lossless voltage transfer function given by Eq. (3.98)

$$M(D) = \frac{V_O}{V_I} = \frac{D}{D'}. \tag{3.98}$$

The DC current transfer function is derived from eq. (3.98) and it is given as

$$M(I) = \frac{I_O}{I_I} = \frac{V_I}{V_O} = \frac{D'}{D}. \tag{3.99}$$

The inductor current ripple

The peak-to-peak inductor current ripple for L_1, Δi_{L1}, can be derived from either Eq. (3.78) or (3.82) and it is given as

$$\begin{aligned} \Delta i_{L1} &= \Delta i_{L1}(DT_s) - \Delta i_{L1}(0), \\ \Delta i_{L1} &= \frac{\left[D'V_I R - V_O D\left(r_{L1} + r_M\right)\right]D}{D'L_1 R f_s}. \end{aligned} \tag{3.100}$$

The peak-to-peak current ripple for L_2, ΔiL_2, is derived from Eq. (3.84) and it is given as

$$\begin{aligned} \Delta i_{L2} &= \Delta i_{L2}(DT_s) - \Delta i_{L1}(T_s), \\ &= \frac{\left[V_O\left(1 + \frac{r_F}{D'R}\right) + V_F\right]D'}{L_2 f_s}. \end{aligned} \tag{3.101}$$

The capacitor voltage ripple

The peak-to-peak voltage ripple for C_1, Δv_{C1}, is derived from Eq. (3.83) and it is expressed as

$$\begin{aligned} \Delta v_{C1} &= \Delta v_{C1}(T_s) - \Delta v_{C1}(DT_s), \\ \Delta v_{C1} &= \frac{DV_O}{RC_1 f_s}. \end{aligned} \tag{3.102}$$

The peak-to-peak voltage ripple for C_2 , Δv_{C2} , is derived from Eq. (3.85) and it is expressed as

$$\begin{aligned} \Delta v_{C2} &= \Delta v_{C2}(T_s) - \Delta v_{C2}(DT_s), \\ \Delta v_{C2} &= \frac{DV_O}{RC_2 f_s}. \end{aligned} \tag{3.103}$$

Converter Efficiency

The converter efficiency is derived from Eqs. (3.98) and (3.99), and it is expressed as

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{V_O D'}{V_I D},$$

$$= \frac{1}{\left(1 + \frac{V_F}{V_O} + \frac{Dr_{C_1}}{D'R} + \frac{r_{L_2}}{R} + r_F + \frac{Dr_F}{D'R} + \frac{D^2 r_{L_1}}{D'^2 R} + \frac{D^3 r_M}{D'^2 R}\right)}. \quad (3.104)$$

3.4.4 Small Signal Modelling of Sepic Converter

According to Ray (2006), the best approach to model both the small signal and large signal characteristics of the sepic converter is by employing the PWM switch model. The PWM switch model represents the switching network of a converter, and fully models the non-linearity of PWM switching converters (Ray, 2006). First, a bit of circuit manipulations are required to disclose the position of the PWM switch model within the converter circuit. Once the PWM switch model is located, its average voltages and currents are determined and linearized. Thereafter, the required voltages and currents of the converter can be determined. Figure 3.26 shows the PWM switch model and its invariant terminal characteristics based on the work of Vatché (2004). The switch has three terminals a, p and c, which are identified as active, passive and common. The common terminal carries the total switched inductive current in the converter, the voltage $V_{ap}(t)$ in all converters is DC, while $V_{CP}(t)$ is pulsating. The PWM switch model can be used to represent a two-switch switch network in any switching converter such as the boost, buck, sepic and many others. In the modelling of a switching converter using the PWM switch model, the switching network is treated as the only non-linear part of the converter. So by simply replacing the switch network of a converter with the PWM switch model, a linearized small signal model and large signal model of the converter can be obtained, and various transfer functions of the converter can also be derived.

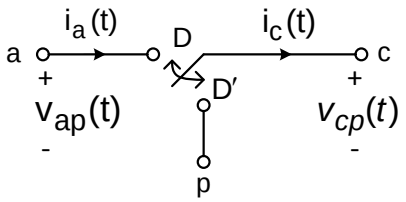


Figure 3.26: The PWM switch model and its invariant terminal characteristics.

The invariant equations that describe the dynamics of the terminal currents and port voltages of the PWM switch shown in Figure 3.26 are given as

$$\begin{aligned} i_a(t) &= d(t)\, i_c(t), \\ v_{cp}(t) &= d(t)\, v_{ap}(t). \end{aligned} \tag{3.105}$$

Averaging Eq. (3.105) yields

$$\begin{aligned} I_a &= D I_c, \\ V_{cp} &= D V_{ap}. \end{aligned} \tag{3.106}$$

In order to obtain the averaged linearized small signal equations of the PWM switch model, Eq. (3.106) is perturbed and expressed as

$$\begin{aligned} \hat{i}_a &= D\hat{i}_c + I_c \hat{d}, \\ \hat{v}_{cp} &= D\hat{v}_{ap} + V_{ap} \hat{d}. \end{aligned} \tag{3.107}$$

Figure 3.27 shows the linearized average PWM switch model with the dependent current and voltages sources constructed from Eq. (3.107).

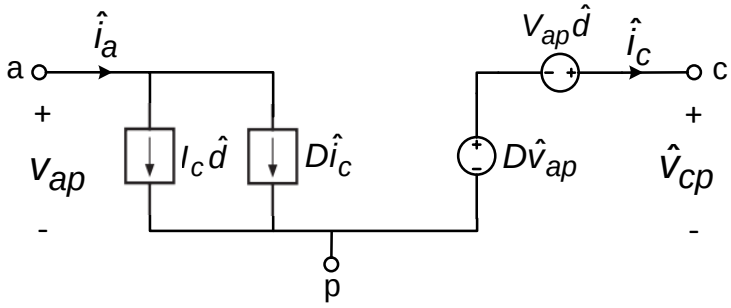


Figure 3.27: The linearized average PWM switch model with the dependent current and voltage sources.

In Figure 3.27, the dependent current source $D\hat{i}_c$ and the dependent voltage source $D\hat{v}_{ap}$ are transformed into a 1:D transformer. Figure 3.28 shows the resulting linearized average PMW switch model with the dependent sources replaced with a 1:D transformer. All the terms driven by the control input $\hat{d}$ such as $\hat{d}\left(V_{ap}/D\right)$ are moved to the left side of the transformer.

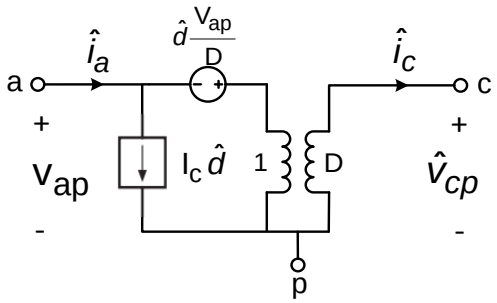


Figure 3.28: The linearized average PWM switch model with the dependent sources replaced with a 1:D transformer.

In Figure 3.26 to Figure 3.28, the parasitic elements of the PWM switch are neglected. However, in practical switches the presence of parasitic elements affects the average port voltages of the switch; therefore, these must be accounted for in the PWM switch model (Vatché, 2004). Figure 3.29 shows the DC and small signal PWM switch model with parasitic elements.

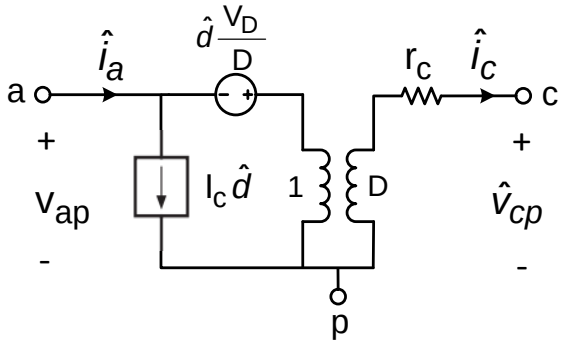


Figure 3.29: The DC and small signal PWM switch model with parasitic elements.

Where $\hat{v}_{cp}$, r_c and V_D are expressed as

$$\begin{aligned} \hat{v}_{cp} &= D\hat{v}_{ap} + V_D\,\hat{d} - \hat{i}\,r_c, \\ V_D &= V_{ap} + I_c\left[r_e\left(D - D'\right) + r_F - r_M\right], \\ r_c &= DD'r_e + Dr_M + D'r_F. \end{aligned} \tag{3.108}$$

Where r_e is a high frequency resistance that appears across ports a and p, r_M and r_F are the on-resistance of the active and passive terminals of the PWM switch.

Figure 3.30 shows the equivalent circuit of the sepic converter with the switch network disclosed. The switch network comprises of the active switch (MOSFET) and the passive switch (Diode). The circuit is obtained by manipulating Figure 3.22 as follows: D_1 is moved to the bottom part of the converter and the bottom terminal of L_2 is moved further left to the negative terminal of the source. This procedure discloses the PWM switch model of the converter with its three ports: active, passive and common.

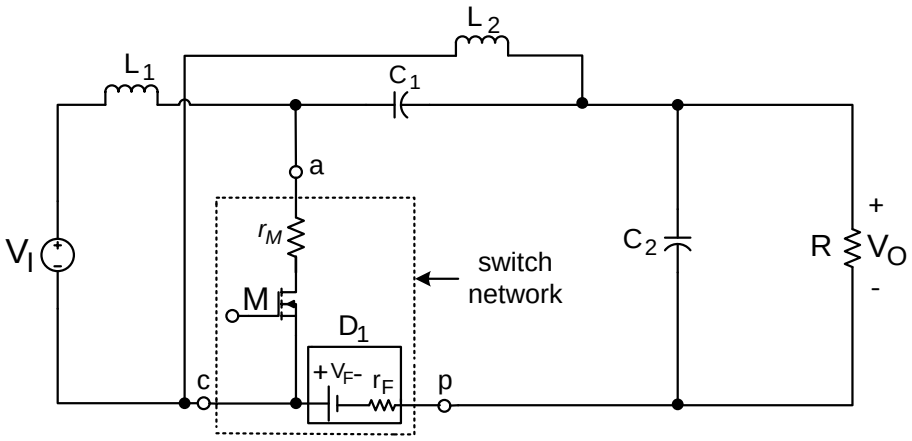


Figure 3.30: The equivalent circuit of the sepic converter with the switch network disclosed.

Figure 3.31 shows the equivalent circuit of sepic converter with the switch network replaced with PWM switch model. Both the large and small signal transfer functions of the converter can be derived from the circuit.

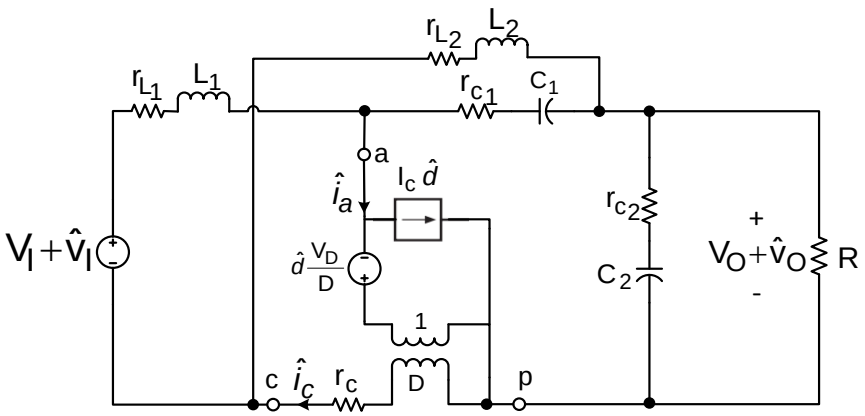


Figure 3.31: The equivalent circuit of the sepic converter with the switch network replaced with the PWM switch model.

Open-loop Transfer Functions

The transfer functions that will be considered are the small signal open-loop control-to-output transfer function and the small signal open-loop line-to-output transfer function. Figure 3.32 shows the equivalent circuit of the sepic converter with all DC sources, $\hat{v}_{in}$ and $\hat{d}$ set to zero. In order to find the transfer functions, first the denominator D(s) of the transfer functions is determined, and then the numerators of each transfer function are determined. To start with, all DC sources, $\hat{v}_I$ and $\hat{d}$ in Figure 3.31 are set to zero. This leads to Figure 3.32 from which D(s) is determined. The small signal open-loop transfer functions are expressed as

$$G_{v_O d(s)} = \frac{\hat{v}_O(s)}{\hat{d}(s)} = K_D \frac{N_d(s)}{D(s)}\bigg|_{\hat{v}_I(s)=0}, \qquad (3.109)$$

$$G_{vOI(s)} = \frac{\hat{v}_O(s)}{\hat{v}_I(s)} = M\frac{N_I(s)}{D(s)}\Big|_{\hat{d}(s)=0}. \tag{3.110}$$

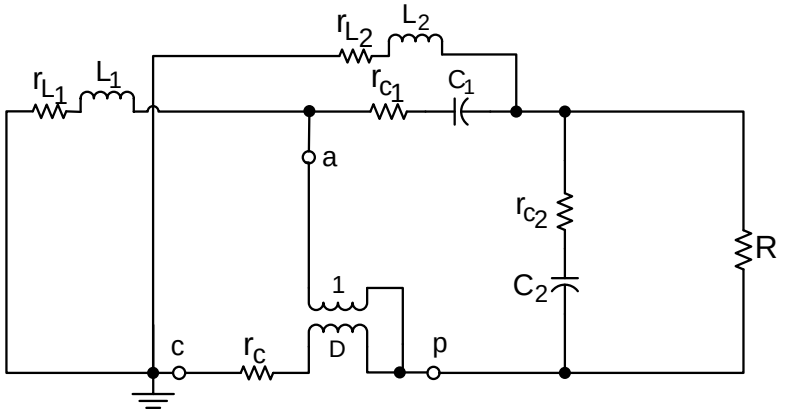


Figure 3.32: The equivalent circuit of the sepic converter with all DC sources, $\hat{v}_{in}$ and $\hat{d}$ set to zero.

Determination of the denominator D(s)

The denominator D(s) is a fourth order polynomial and it is expressed as

$$D(s) = 1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4. \tag{3.111}$$

The coefficients $a_1 - a_4$ in Eq. (3.111) are equal to the resistance and reactance seen looking from ports (1) to (4) of the reference circuit given in Figure 3.33. The reference circuit is derived by replacing the inductors and capacitors in Figure 3.32 with short circuits and open circuits. Simplifying Eq. (3.111) yields

$$D(s) = \left(1 + \frac{s}{w_{o1}Q_1} + \frac{s^2}{w_{o1}^2}\right)\left(1 + \frac{s}{w_{o2}Q_2} + \frac{s^2}{w_{o2}^2}\right). \tag{3.112}$$

Assuming a moderate to high Q-factor Q, and properly separated resonances, Eq. (3.112) is expanded and equated to Eq. (3.111) to get

$$a_1 \cong \frac{1}{w_{o1}Q_1}, \tag{3.113}$$

$$a_2 \cong \frac{1}{w_{01}^2} \tag{3.114}$$

$$a_3 \cong \frac{1}{w_{o1}Q_1 w_{o2}^2} + \frac{1}{w_{o2}Q_2 w_{o1}^2} \tag{3.115}$$

$$a_4 \cong \frac{1}{w_{o1}^2 w_{o2}^2} \tag{3.116}$$

The coefficients $a_1 - a_4$ are determined by applying the N-Extra Element Theorem (NEET) to Figure 3.33, whereby the resistance and reactance seen from each port is determined. Figure 3.33 shows the reference circuit for determining the coefficients of D(s) with normal port conditions. The circuit shows that the resistor r_C has been moved to the active terminal and multiplied by the term $(D^2)^{-1}$. Vatché (2004), covers a detailed description of the N-Extra Element Theorem.

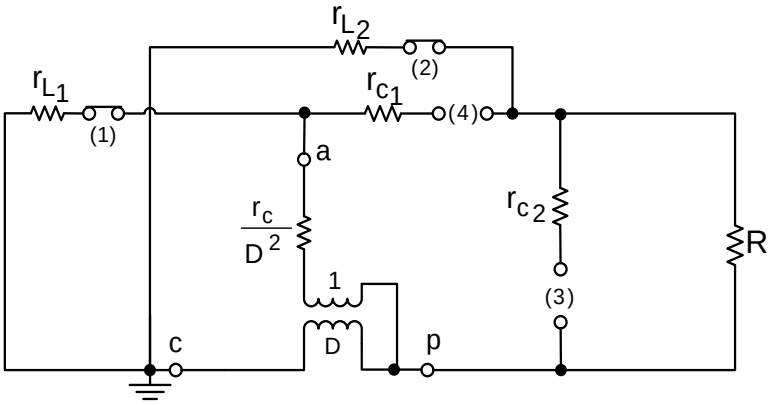


Figure 3.33: The reference circuit for determining the coefficients of D(s) with normal port conditions.

The coefficients of D(s) are determined by applying the NEET to the reference circuit given in Figure 3.33 and they are given as

$$a_1 = \left(L_1 \left(\frac{D}{D'} \right)^2 + L_2 \right) \frac{1}{R}, \tag{3.117}$$

$$a_2 \cong L_1 \left(C_1 + \left(\frac{D}{D'} \right)^2 C_2 \right) + L_2 \left(C_1 + C_2 \right), \tag{3.118}$$

$$a_3 \cong \frac{L_1 L_2 C_1}{R D'^2}, \tag{3.119}$$

$$a_4 \cong \frac{L_1 L_2 C_1 C_2}{D'^2}. \tag{3.120}$$

The resonances frequencies and the Q-factors are expressed as

$$w_{o1} \cong \frac{1}{\sqrt{L_1 \left(C_2 \left(\frac{D}{D'} \right)^2 + C_1 \right) + L_2 \left(C_1 + C_2 \right)}}, \tag{3.121}$$

$$Q_1 \cong \frac{R}{w_{o1} \left(L_1 \left(\frac{D}{D'} \right)^2 + L_2 \right)}, \tag{3.122}$$

$$w_{o2} \cong \sqrt{\frac{1}{L_2 \frac{C_1}{D^2} // \frac{C_2}{D'^2}} + \frac{1}{L_1 C_1 // C_2}}, \tag{3.123}$$

$$Q_2 \cong \frac{R}{w_{o2}(L_1 + L_2)\frac{C_1}{C_2}\left(\frac{w_{o1}}{w_{o2}}\right)^2}. \tag{3.124}$$

Determination of the small-signal open-loop line-to-output transfer function

In the expression of the line-to-output transfer function given by Eq. (3.110), the terms M and D(s) have already been found, while the term $N_{in}(s)$ will be determined next. The term M relates to the lossless DC voltage transfer function given by Eq. (3.98). On the other hand, the term $N_{in}(s)$ relates to the null conditions of $\hat{v}_O(s)$ to the stimulation of $\hat{v}_I(s)$ and it is expressed as a factor of $N_1(s)$ and $N_2(s)$. Where $N_1(s)$ corresponds to the first null condition and $N_2(s)$ corresponds to the second null condition. Figure 3.34 shows the equivalent circuit of the sepic converter used to determine the line-to-output transfer function. The control term $\hat{d}(s)$ is set to zero.

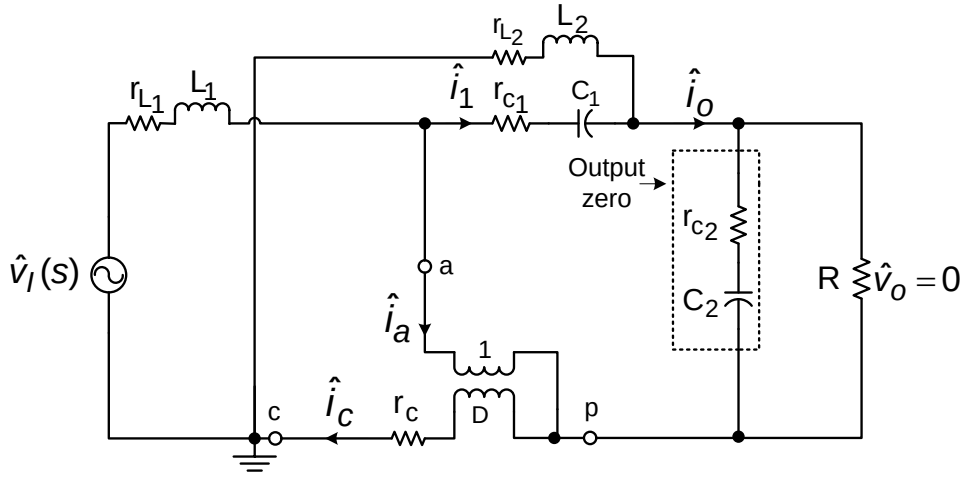


Figure 3.34: The equivalent circuit of the sepic converter used to determine the line-to-output transfer function.

The first null condition of $\hat{v}_O(s)$ is given by the output zero when it shorts, so that the first factor of $N_{in}(s)$ is expressed as

$$N_{in}(s) = (1 + sr_{C2}C_2)N_2(s). \tag{3.125}$$

The second null condition of $\hat{v}_O(s)$, $N_2(s)$ is given when $\hat{i}_o$ is equal to zero so that $\hat{i}_1$ flows through the first impedance branch of $(r_{C1} + 1/sC_1)$ and the second impedance branch of $(r_{L2} + sL_2)$. With $\hat{v}_O(s)$ at null, it follows that both $\hat{i}_a$ and

$\hat{i}_c$ are zero, therefore, the voltage across the first and the second impedance branch can be expressed as

$$\hat{v}_{ap} = \hat{i}_1\left(r_{C1} + 1/sC_1\right), \tag{3.126}$$

$$\hat{v}_{cp} = -\hat{i}_1\left(r_{L2} + sL_2\right). \tag{3.127}$$

Equation (3.127) is expressed in terms of Eq. (3.126) as $\hat{v}_{cp} = D\hat{v}_{ap}$ and yields

$$\begin{aligned} \hat{i}_1\left(r_{C1} + 1/sC_1\right)D &= -\hat{i}_1\left(r_{L2} + sL_2\right), \\ 1 + sC_1\left(Dr_{C1} + r_{L2}\right) + s^2L_2C_1 &= 0, \\ \therefore N_2(s) &= 1 + sC_1\left(Dr_{C1} + r_{L2}\right) + s^2L_2C_1. \end{aligned} \tag{3.128}$$

Finally, the line-to-output transfer function is determined by substituting the numerator term into Eq. (3.110) and it is given as

$$G_{v_o l(s)} = \frac{D}{D'} \frac{\left(1 + sr_{C2}C_2\right)\left(1 + sC_1\left(Dr_{C1} + r_{L2}\right) + s^2L_2C_1\right)}{\left(1 + \dfrac{s}{w_{O1}Q_1} + \dfrac{s^2}{w_{O1}^2}\right)\left(1 + \dfrac{s}{w_{O2}Q_2} + \dfrac{s^2}{w_{O2}^2}\right)}. \tag{3.129}$$

Determination of the small-signal open-loop control-to-output transfer function

In the control-to-output transfer function given by Eq. (3.109), the term $D(s)$ has already been found, while the terms K_D and $N_d(s)$ are determined next. Figure 3.35 shows the equivalent circuit of the sepic converter used to determine the control-to-output transfer function. The source $\hat{v}_I(s)$ is set to zero. The term K_D is derived from the expression of the DC voltage transfer function of the converter as shown below

$$\begin{aligned} K_D &= \frac{dV_O}{dD} \\ &= V_I \frac{d}{dD}\left(\frac{D}{1-D}\right) = \frac{1}{D'^2}. \end{aligned} \tag{3.130}$$

The term $N_d(s)$ relates to the null conditions of $\hat{v}_O(s)$ to the stimulations of the sources $\left(V_D/D\right)\hat{d}$ and $I_c\,\hat{d}$. The first null condition is given by the output zero, therefore, $N_d(s)$ is expressed in terms of the output zero as its first factor as

$$N_d(s) = \left(1 + sr_{C2}C_2\right)N_2(s), \tag{3.131}$$

where $\left(1 + sr_{C2}C_2\right)$ is the output zero.

The term $N_2(s)$ corresponds to the second null condition when $\hat{i}_0(s)$ is equal to zero. With $\hat{i}_0(s)$ equal to zero, applying Kirchhoff current law (KCL) at node "C" and at node "P" yields

$$\hat{i}_C(s) = \hat{i}_1 + \hat{i}, \tag{3.132}$$

$$\hat{i}_C\hat{d} = D\hat{i}_C - \hat{i}_C = -D'\hat{i}_C. \tag{3.133}$$

With some manipulation of Eq. (3.132) and (3.133), the second factor of the control-to-output numerator is determined and expressed as

$$1 - sL_1\left(\frac{D}{D'}\right)^2 + s^2C_1(L_1 + L_2) - s^3\frac{L_1L_2C_1}{R}\left(\frac{D}{D'}\right)^2. \tag{3.134}$$

Substituting Eq. (3.134) and (3.130) into Eq. (3.109) yields the control-to-output transfer function of the sepic converter. The numerator term given by Eq. (3.134) is characterised by a real right half plane zero (RHPZ) and a pair of complex conjugate zeroes.

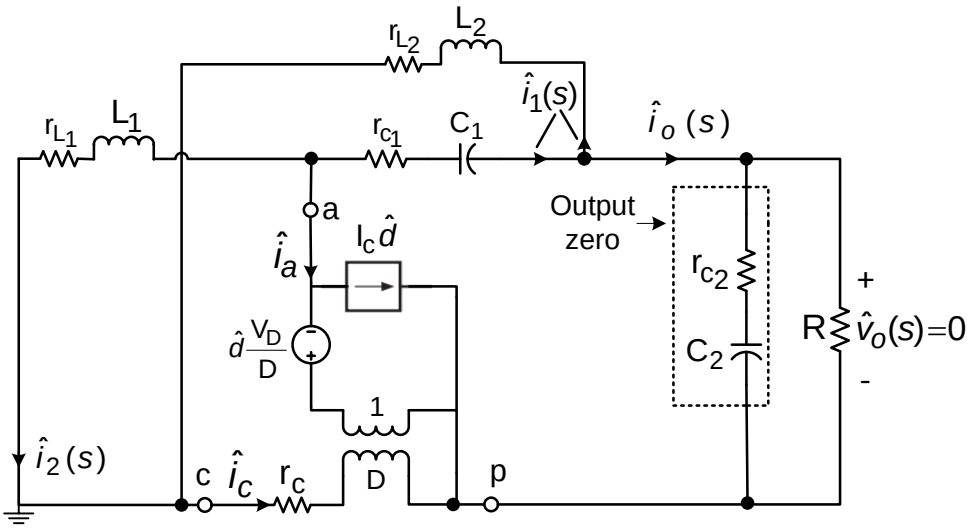


Figure 3.35: The equivalent circuit of the sepic converter used to determine the control-to-output transfer function.

3.4.5 Design of the Sepic Converter

Table 3.3 shows the converter design specifications. The parameter and component values of the converter power stage are determined by using the converter design specifications, the steady state parameter and component equations that were derived in the converter steady state analysis section.

Table 3.3: The sepic converter design specifications

parameter	Value	Comments
Output power P_O	50 – 900 W	At full-load for P_I of 1 kW
Input voltage V_I	36 – 67 VDC	Nominal Voltage: 52 VDC
Output voltage V_O	100 VDC	Galvanic isolation required
Efficiency target η	90 %	optimised at full-load
Input current ripple	$\leq$ 30 % of I_L	For load range 5.5-100 %
Output voltage ripple Δv_O	< 1 % of V_O	
Switching frequency f_s	$\cong$ 50 kHz	

DC voltage transfer function calculation

The maximum, nominal and minimum values of the DC voltage transfer function are calculated by using Eq. (3.98), and they are given as 2.78, 1.92 and 1.49.

Duty cycle

The maximum, nominal and minimum values of the duty cycle are determined by using Eq. (3.104) and they are given as 0.7553, 0.6812 and 0.6238.

Selection of Capacitor, Inductor and Resistor

The values of the capacitors are calculated using Eq. (3.102) and (3.103), and the values of the inductors are calculated using Eq. (3.100) and (3.101). While the range of the load resistor is determined by using the specified design output voltage, minimum and maximum converter output power. Table 3.4 shows a summary of the calculated component list for the sepic converter design.

Table 3.4: The component list for the power stage design of the sepic converter

Component	Value	Unit
C_1	135.914	µF
C_2	543.65	µF
L_1	100.65	µH
L_2	100.65	µH
R	11.11 – 200	Ω

3.5 IBVM Converter

3.5.1 Modelling of the IBVM converter

In this section, the circuit, the operation and the circuit averaging description of the interleaved boost voltage multiplier (IBVM) converter are presented. Based on the circuit averaging description of the converter over one switching period, the parameter and component equations are derived. Linearized equations are also derived from which the small signal control-to-output voltage transfer functions are derived. The transfer functions are used later in the design of a controller and in the simulation stage.

The interleaving feature of the IBVM converter has advantages of small current ripple, and offers high voltage gain at low duty cycles (An-Yeol et al, 2013). Further, according to Eliana et al. (2010), C.A.Ramos-Paja and E. Arango (2011), interleaving reduces the output voltage ripple and leads to a reduction in size, weight and volume of the circuit inductors and capacitors. These characteristics make the IBVM converter attractive for fuel cell power conditioning applications, where the key design objectives are low current ripple and high output voltage.

3.5.2 The circuit topology

S.Kamtip and Bhumkittipich (2011), J. S. Anu et al. (2012), Omar et al. (2012) and many others discuss interleaving of boost converters. The IBVM converter considered herein, is derived from a combination of the interleaved boost converter and the voltage multiplier boost converter (Rosas-Caro et al.,2010; Rosas-Caro et al.,2011).

Figure 3.36 shows the circuit of the PWM IBVM converter. The circuit consists of a DC input voltage V_I, an inner and outer boost leg, two input inductors L_1 and L_2, three capacitors C_1, C_2 and C_3, two controllable switches S_1 and S_2, four high speed high-power diodes D_1, D_2, D_3 and D_4, an output voltage V_O and a load resistor R.

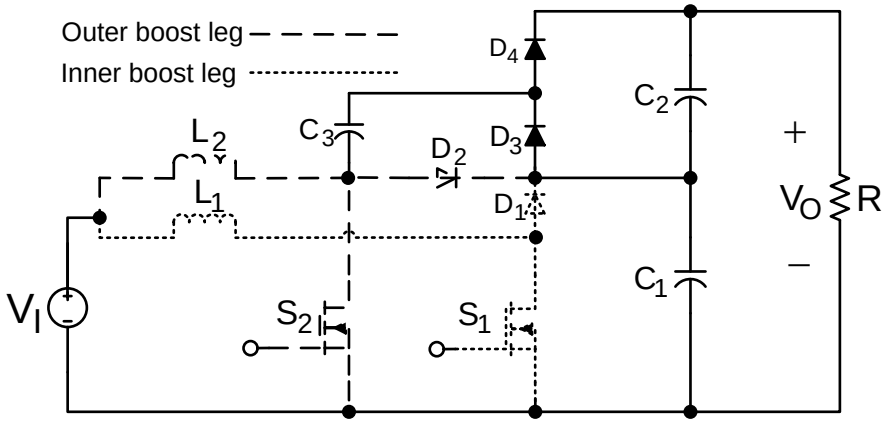


Figure 3.36: The circuit of the PWM IBVM converter.

3.5.3 Converter steady state analysis

Operation principle of the converter

In the analysis of the IBVM converter circuit, it is assumed that the converter is operating in steady state with CCM. In CCM, the operation of the converter over one switching period can be divided into four modes, where one switching cycle is equal to T_S. The switches repeatedly turn on and off at the switching frequency of $f_S (f_S = 1/T_S)$. The two switches are hard switched and operated by two gate signals that are $180°$ phase shifted.

Figure 3.37 and Figure 3.38 show some of the important current and voltage waveforms of the converter over one switching period. The switching time interval $t_0 - t_4$ is equal to one switching period and consist of four operating modes. V_{GS1} and V_{GS2} are the switch gate signals, $i_{L1}(t)$ and $i_{L2}(t)$ are the inductors instantaneous currents, I_{L1} and I_{L2} are the inductors average currents, Δi_{L1} and Δi_{L2} are the peak-to-peak inductors current ripple, $i_{D1}(t)$ and $i_{D2}(t)$ are the diodes instantaneous current, $V_{D1}(t)$ and $V_{D2}(t)$ are the diodes voltage, $i_{C1}(t)$, $I_{C2}(t)$ and $I_{C3}(t)$ are the capacitors instantaneous current, $v_{C1}(t)$, $v_{C2}(t)$ and $v_{C3}(t)$ are the capacitors instantaneous voltage, V_{C1}, V_{C2} and V_{C3} are the capacitors average voltage and Δv_{C1}, Δv_{C2} and Δv_{C3} are the peak-to-peak capacitors voltage ripple.

Figure 3.37 shows the equivalent current and voltage waveforms of the converter with duty cycle D greater than 50 % in order to warrant a switch overlap between the switches. On the other hand, Figure 3.38 shows the equivalent current and voltage waveforms of the converter with a duty cycle less than 50 %, which does not warrant a switch overlap between the switches. Since operating the converter at duty cycles above or below 50 % yields different current and voltage waveforms, it becomes a requirement to consider both scenarios in the modelling of the converter for controller design purpose. However, the modelling that will be done in this work will only consider converter operation at duty cycle values equal or greater than 50 %. Therefore, Figure 3.37 is used for the analysis of the converter.

The output voltage of the converter is found by applying the voltage balance principle of the diode-capacitor combination at the output node, so that the voltage across each capacitor is approximated as V_O/N and then the output voltage is approximated as $(N \times V_O)/N$. Where N represents the number of capacitors connected in series at the

output node. Fundamentally, the output voltage is equal to the sum of the individual voltages measured across each capacitor at the output node.

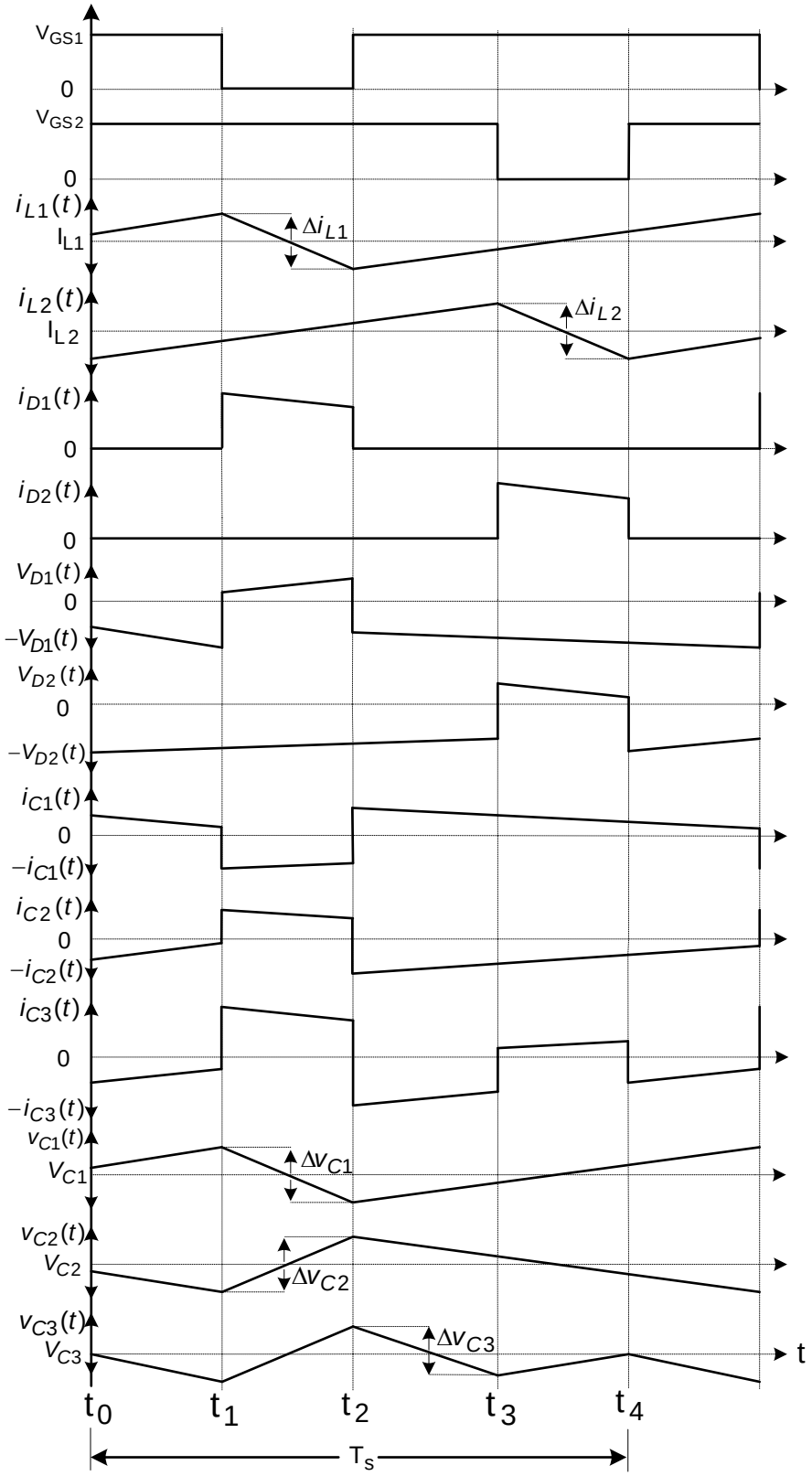


Figure 3.37: The current and voltage waveforms of the IBVM converter during steady state switching.

These waveforms are only applicable for D > 0.5

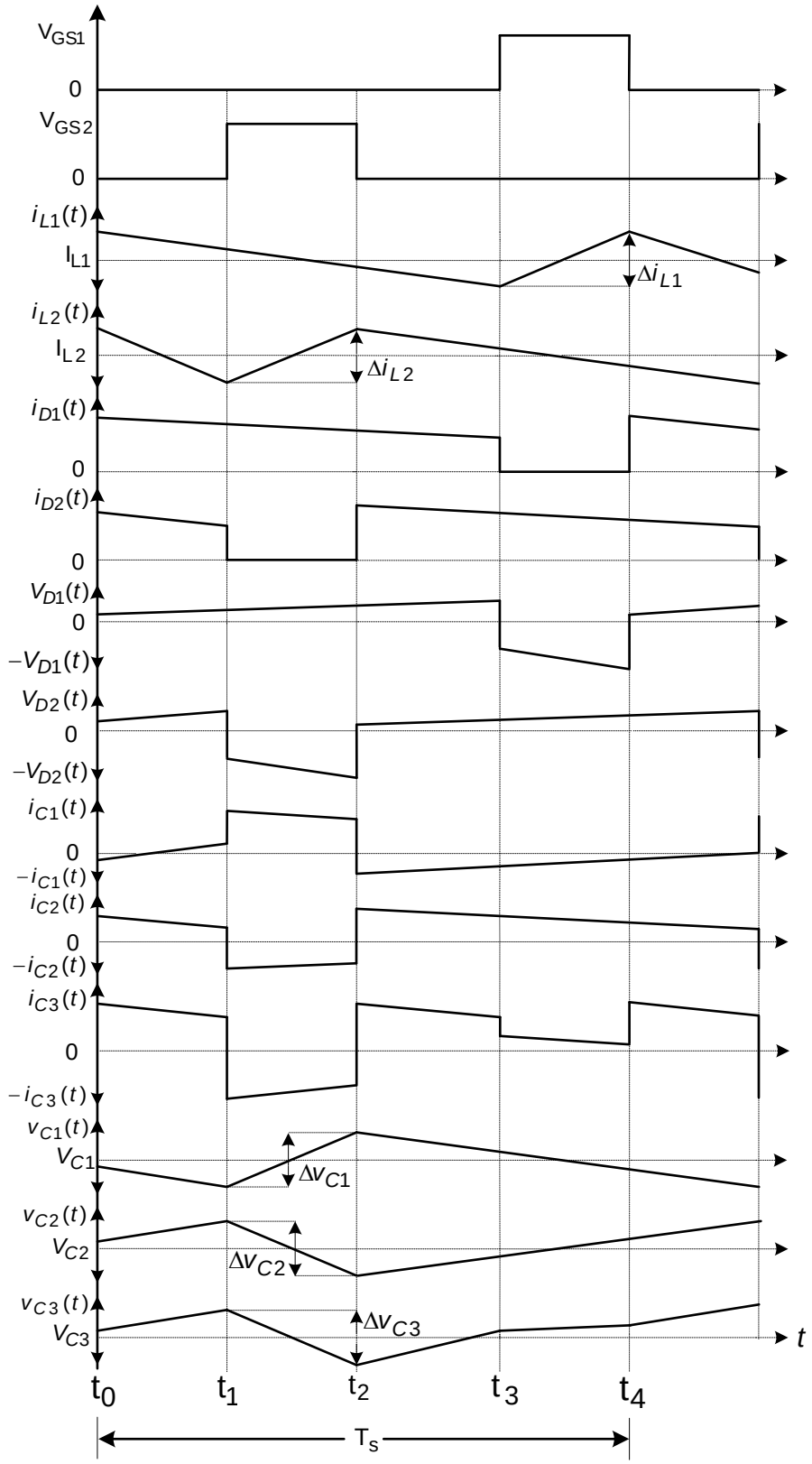


Figure 3.38: The current and voltage waveforms of the IBVM converter during steady state switching.

These waveforms are only applicable for D < 0.5.

Mode 1 ($t_0 - t_1$): $D - 0.5$

Figure 4.39 shows the equivalent circuit of the converter during mode 1. During this mode of operation, both switches S_1 and S_2 turn on and conduct the input current I_I, while the diodes D_1, D_2 and D_4 are reverse biased and D_3 is forward biased. Both L_1 and L_2 are charged up from the source. If the voltage across C_1 is lower than that across C_3, then D_3 is forward biased, allowing C_3 to discharge current into C_1 until the voltage level of C_1 is clamped to that of C_3. This action allows the voltage in all capacitors to be clamped to the same level over one switching period; hence, it provides a voltage self-balancing feature for all capacitors. The output voltage is equal to the sum of the voltage across C_2 and C_3, therefore both capacitors provide power to the load R. This mode ends when S_1 turn off.

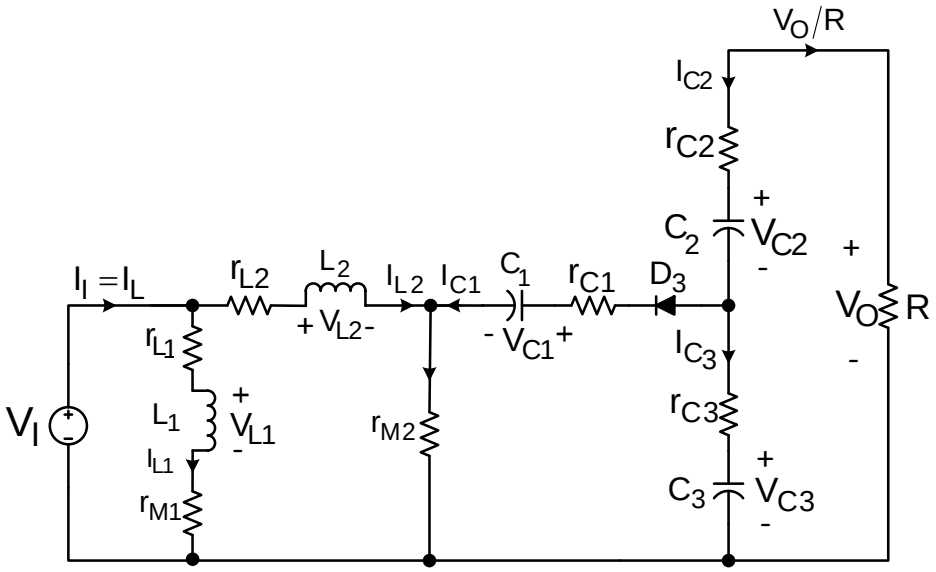


Figure 3.39: The circuit of the IBVM converter during mode 1.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$L_1 \frac{di_{L1}(t)}{dt} = V_I - I_{L1}(r_{L1} + r_{M1}), \tag{3.135}$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_I - r_{L2} I_{L2} - \left(C_1 \frac{dv_{C1}(t)}{dt} + I_{L2} \right) r_{M2}, \tag{3.136}$$

$$C_1 \frac{dv_{C1}(t)}{dt} = -C_3 \frac{dv_{C3}(t)}{dt} + C_2 \frac{dv_{C2}(t)}{dt}, \tag{3.137}$$

$$C_2 \frac{dv_{C2}(t)}{dt} = -\frac{V_O}{R}, \tag{3.138}$$

$$C_3 \frac{dv_{C3}(t)}{dt} = -C_1 \frac{dv_{C1}(t)}{dt} + C_2 \frac{dv_{C2}(t)}{dt}, \tag{3.139}$$

$$C_{eq}\frac{dv_{eq}(t)}{dt} = -\frac{2V_O}{R}. \tag{3.140}$$

Where r_{M1} and r_{M2} are the series resistance of the switches, r_{L1} and r_{L2} are the series resistance of the inductors, r_{C1}, r_{C2} and r_{C3} are the series resistance of the capacitors and C_{eq} is the parallel equivalent capacitance of the series connected capacitors at the output node.

Mode 2 ($t_1 - t_2$): D'

Figure 3.40 shows the equivalent circuit of the converter during mode 2. During this mode of operation, S_1 turns off whereas S_2 stays on and conducts both I_{L2} and I_{C1}, while D_2 and D_4 are reverse biased and D_1 and D_3 are forward biased. L_1 discharges current through C_3 while L_2 is charged up from the source. Similarly to mode 1, If the voltage across C_1 is lower than that of C_3, then D_3 is forward biased allowing C_3 to discharge current into C_1 until the voltage level of C_1 is clamped to that of C_3. The output voltage is equal to the sum of the voltage across C_2 and C_3. This mode ends when S_1 turns on again.

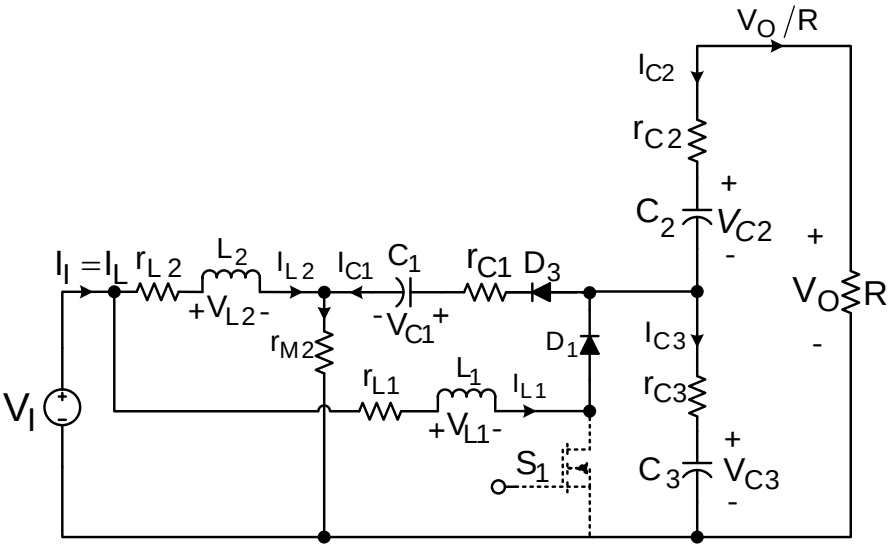


Figure 3.40: The circuit of the IBVM converter during mode 2.

The corresponding differential equations that describe the dynamics of the converter during this mode of operation are given as

$$\begin{aligned} L_1\frac{di_{L1}(t)}{dt} &= V_I - I_{L1}\left(r_{L1} + r_F\right) - V_F \\ &- r_{C_3}C_3\frac{dv_{C3}(t)}{dt} - V_{C3,} \end{aligned} \tag{3.141}$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_I - r_{L2} I_{L2} - \left(C_1 \frac{dv_{C1}(t)}{dt} + I_{L2} \right) r_{M2}, \tag{3.142}$$

$$V_O = r_{C2} C_2 \frac{dv_{C2}(t)}{dt} + r_{C_3} C_3 \frac{dv_{C3}(t)}{dt} + V_{C2} + V_{C3}, \tag{3.143}$$

$$C_1 \frac{dv_{C1}(t)}{dt} = I_{L2} - C_3 \frac{dv_{C3}(t)}{dt} - \frac{V_O}{R}, \tag{3.144}$$

$$C_2 \frac{dv_{C2}(t)}{dt} = -\frac{V_O}{R}, \tag{3.145}$$

$$C_3 \frac{dv_{C3}(t)}{dt} = I_{L2} - C_1 \frac{dv_{C1}(t)}{dt} - \frac{V_O}{R}, \tag{3.146}$$

$$C_{eq} \frac{dv_{eq}(t)}{dt} = -\frac{2V_O}{R} + I_{L1}. \tag{3.147}$$

Where r_F is the series resistance of each diode and V_F is the forward voltage drop across each diode.

Mode 3 ($t_2 - t_3$): $D - 0.5$

Figure 3.41 shows the equivalent circuit of the converter during mode 3. All two switches turn on again. This mode is similar to mode 1 and the corresponding differential equations are similar. This mode ends when S_2 turns off.

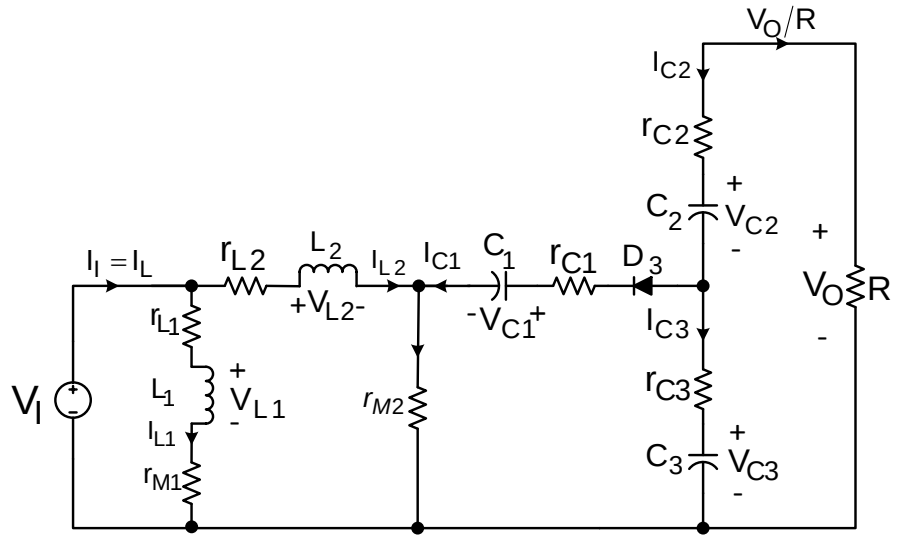


Figure 3.41: The equivalent circuit of the IBVM converter during mode 3.

Mode 4 ($t_3 - t_4$): D'

Figure 3.42 shows the equivalent circuit of the converter during mode 4. During this interval, S_1 stays on and S_2 turns off and the diodes D_1 and D_3 are reverse biased, while D_2 and D_4 are forward biased. L_1 is charged up from the source while L_2 discharges current into C_3. If the voltage across C_2 is lower than that across C_1, then

D_4 is forward biased allowing C_1 to discharge current into C_2 until the voltage level of C_2 is clamped to that of C_1. This mode ends when S_2 turns on again.

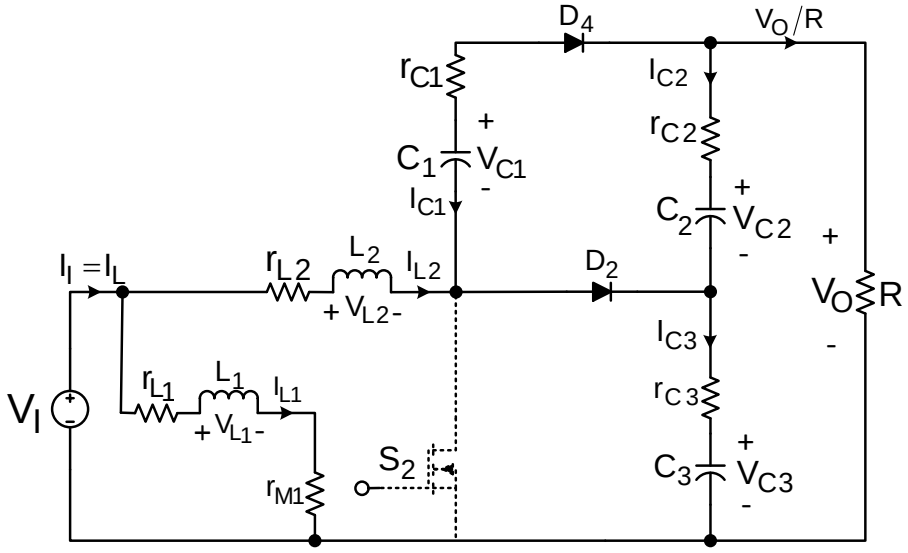


Figure 3.42: The circuit of the IBVM converter during mode 4.

$$L_1 \frac{di_{L1}(t)}{dt} = V_I - I_{L1}(r_{L1} + r_{M1}), \tag{3.148}$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_I - r_{L2} I_{L2} - V_F - \left(C_1 \frac{dv_{C1}(t)}{dt} + I_{L2} \right) r_F - r_{C_3} C_3 \frac{dv_{C3}(t)}{dt} - V_{C3}, \tag{3.149}$$

$$C_1 \frac{dv_{C1}(t)}{dt} = -C_2 \frac{dv_{C2}(t)}{dt} - \frac{V_O}{R}, \tag{3.150}$$

$$C_2 \frac{dv_{C2}(t)}{dt} = -C_1 \frac{dv_{C1}(t)}{dt} - \frac{V_O}{R}, \tag{3.151}$$

$$C_3 \frac{dv_{C3}(t)}{dt} = I_{L2} + C_1 \frac{dv_{C1}(t)}{dt} + C_2 \frac{dv_{C2}(t)}{dt}, \tag{3.152}$$

$$C_{eq} \frac{dv_{eq}(t)}{dt} = -\frac{2V_O}{R} + I_{L2} \tag{3.153}$$

Average inductors voltage

The average inductors voltage is found by taking the integral of the inductors instantaneous voltage over one switching cycle by using Eq. (3.135), (3.141), (3.136), (3.142), (3.148) and (3.149), and they are expressed as

$$\langle v_{L1}(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_{L1}(t) dt = V_I - r I_{L1} - V_F D - \frac{V_O D'}{2}, \tag{3.154}$$

$$\begin{aligned}\left\langle v_{L2}(t)\right\rangle &= \frac{1}{T_s}\int_0^{T_s} v_{L2}(t)\,dt,\\ &= V_I - r_2 I_{L2} - V_F D' - \frac{V_O r_{M2}}{R} - \frac{V_O D'}{2}.\end{aligned} \tag{3.155}$$

Where

$$r = r_{L1} + r_F D' + r_{M1} D, \tag{3.156}$$

$$r_2 = r_{L2} + r_{M2} D. \tag{3.157}$$

Average capacitor current

The average capacitor current of each capacitor and the equivalent capacitor current through the output node is found by taking the integral of the capacitors instantaneous current and the equivalent capacitor instantaneous current over one switching cycle. using Eq. (3.137), (3.138), (3.139), (3.140), (3.144), (3.145), (3.146), (3.147) ,(3.150), (3.151), (3.152) and (3.153), and they are expressed as

$$\left\langle i_{C1}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} i_{C1}(t)\,dt = Ir_{M2} D - I_{L2} + I_F D', \tag{3.158}$$

$$\left\langle i_{C2}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} i_{C2}(t)\,dt = -\frac{V_O}{R} - C_1 \frac{dv_{C_1}(t) D'}{dt}, \tag{3.159}$$

$$\begin{aligned}\left\langle i_{C3}(t)\right\rangle &= \frac{1}{T_s}\int_0^{T_s} i_{C3}(t)\,dt,\\ &= C_2 \frac{dv_{c2}(t)}{dt} - C_1 \frac{dv_{c1}(t) D}{dt} + I_{L1} D' + I_F D',\end{aligned} \tag{3.160}$$

$$\left\langle i_{Ceq}(t)\right\rangle = \frac{1}{T_s}\int_0^{T_s} i_{Ceq}(t)\,dt = I_L D' - \frac{2V_O}{R}. \tag{3.161}$$

Where

$$Ir_{M2} = \frac{V_O}{RD} + I_{L2}, \tag{3.162}$$

$$I_F = I_{L2} - \frac{V_O}{RD'}, \tag{3.163}$$

$$I_L = \frac{2V_O}{RD'}. \tag{3.164}$$

DC Voltage transfer function

The IBVM converter consists of two legs of boost converters interleaved together, and any boost leg can be used to derive the DC voltage transfer function of the IBVM

converter. Two DC voltage transfer functions are derived from the two boost legs using Eq. (3.161), (3.155) and (3.154), and they are expressed as

$$M(D_1) = \frac{V_O}{V_I} = \frac{2}{D'\left(1 + \frac{2r}{RD'^2} + \frac{2V_F}{V_O}\right)}, \tag{3.165}$$

$$M(D_2) = \frac{V_O}{V_I} = \frac{2}{D'\left(1 + \frac{2r_2}{RD'^2} + \frac{2r_{M2}}{RD'} + \frac{V_F}{2V_O}\right)}. \tag{3.166}$$

Where $M(D_1)$ is the DC voltage transfer function derived with respect to the inner boost leg of the converter and $M(D_2)$ is derived with respect to the outer boost leg. Eq. (3.165) and (3.166) will yield the same results for lossless conditions, but for non-lossless conditions, there will be a negligible difference.

DC Current transfer function

The DC current transfer function of the converter is equivalent to the inverse of the lossless DC voltage transfer function and it can be derived from Eq. (3.165) or (3.166), assuming lossless conditions, and it is expressed as

$$M(I) = \frac{I_O}{I_I} = \frac{I_O}{I_L} = \frac{D'}{2}. \tag{3.167}$$

The inductors current ripple

The peak-to-peak inductors current ripple ΔiL_1 and ΔiL_2 are derived from Eq. (3.135) and (3.136), and they are expressed as

$$\Delta iL_1 = \frac{V_O\left(D'^2R - 2\left(r_{L1} + r_{M1}\right)\right)D}{2D'RL_1 f_s}, \tag{3.168}$$

$$\Delta iL_2 = \frac{V_O\left(DD'^2R - 2\left(r_{L2} + r_{M2}\right)D - 2D'r_{M2}\right)}{2D'RL_2 f_s}. \tag{3.169}$$

Where ΔiL_1 and ΔiL_2 are the peak-to-peak current ripple of L_1 and L_2. The minimum inductance required for each inductor in order to maintain the inductor current ripple within the desired range is determined by using Eq. (3.168) and (3.169). The reviewed literature recommends setting the inductor current ripple to double the average input current in order to guarantee good converter control dynamics.

The output capacitor voltage ripple

Given that the capacitance and the voltage across all capacitors are equal, the capacitor voltage ripple across the equivalent capacitance at the output node is derived by first determining the voltage ripple across C_2 using Eq. (3.138). The voltage ripple across C_2, Δv_{C2}, and the voltage across its series resistance V_{rC2} are expressed as

$$\Delta v_{C2} = \frac{V_O D}{2 C_2 R f_s}, \tag{3.170}$$

$$V_{rC2} = r_{C2} I_{C2}. \tag{3.171}$$

Where

$$I_{C2} = \frac{I_O}{1-D}. \tag{3.172}$$

Since the output voltage is measured across C_2 and C_3, it follows that the output voltage ripple across the equivalent output capacitor is a sum of the voltage ripple across C_2 and C_3, and it is expressed as

$$\Delta v_O = 2\Delta v_{C2} + 2 r C_2 I_{C2}. \tag{3.173}$$

The minimum value of C_2 required to maintain the voltage ripple across C_2 within the desired range is determined using Eq. (3.170). Based on the assumption that the capacitance for all the capacitors are equal, the required capacitance for C_1 and C_3 is determined using Eq. (3.170).

Converter Efficiency

The converter efficiency is derived by substituting Eq. (3.165) and (3.167) or (3.166) and (3.167) into (3.174) and then solving for η as shown below

$$\eta = \frac{P_O}{P_I} = \frac{V_O I_O}{V_I I_I} = \frac{V_O D'}{2 V_I} = M(D)\frac{D'}{2}, \tag{3.174}$$

The converter efficiency can also be expressed in terms of the DC voltage transfer function of the inner and outer boost legs by replacing $M(D)$ in Eq. (3.174) with Eq. (3.165) or (3.166) to get

$$\eta M(D_1) = \frac{1}{\left(\frac{2r}{RD'^2} + \frac{2V_F}{V_O} + 1\right)}, \tag{3.175}$$

$$\eta M(D_2) = \frac{1}{\left(1 + \frac{2r_2}{RD'^2} + \frac{2r_{M2}}{RD'} + \frac{V_F}{2V_O}\right)}, \tag{3.176}$$

where $\eta M(D_1)$ is the converter efficiency expressed in terms of the DC voltage transfer of the inner boost leg and $\eta M(D_2)$ is the converter efficiency expressed in terms of the DC voltage transfer of the outer boost leg.

3.5.4 Small Signal modelling of the IBVM Converter

In order to perform the small signal analysis of the IBVM converter, the same approach that was taken for the small signal analysis of the ICFFB converter is considered. The non-linear averaged inductor equations and equivalent capacitor equations are re-written as

$$L_1 \frac{d\langle i_{L1}(t)\rangle_{T_s}}{dt} = \langle v_I(t)\rangle_{T_s} - r\langle I_{L1}(t)\rangle_{T_s} - V_F d'(t) - \frac{\langle v_O(t)\rangle_{T_s} d'(t)}{2}, \tag{3.177}$$

$$L_2 \frac{d\langle i_{L2}(t)\rangle_{T_s}}{dt} = \langle V_I(t)\rangle_{T_s} - r_2\langle I_{L2}(t)\rangle_{T_s} - V_F d'(t) - \langle v_O(t)\rangle_{T_s}\left(\frac{r_{M2}}{R} + \frac{d'(t)}{2}\right), \tag{3.178}$$

$$C_{eq} \frac{d\langle v_{Ceq}(t)\rangle_{T_s}}{dt} = d'(t)\langle I_{L2}(t)\rangle_{T_s} - \frac{2\langle v_O(t)\rangle_{T_s}}{R}. \tag{3.179}$$

The next step is to perturb the above equations in order to get linearized equations, which describe the AC small signal variations of the IBVM converter. The linearized equations are therefore given as

$$L_1 \frac{d\hat{i}_{L1}(t)}{dt} = \hat{v}_I(t) - r\hat{i}_{L1}(t) - \frac{D'\hat{v}_O(t) - V_O\hat{d}(t)}{2}, \tag{3.180}$$

$$L_2 \frac{d\hat{i}_{L2}(t)}{dt} = \hat{v}_I(t) - r_2\hat{i}_{L2}(t) - \frac{\hat{v}_O(t)r_{M2}}{R} - \frac{\hat{v}_O(t)D'}{2} + \frac{V_O\hat{d}(t)}{2}, \tag{3.181}$$

$$C_{eq} \frac{\hat{v}_{Ceq}(t)}{dt} = -\frac{2\hat{v}_O(t)}{R} - I_{L2}\hat{d}(t) + D\hat{i}_{L2}(t). \tag{3.182}$$

The final step is to take the Laplace transform of Eq. (3.179), (3.180) and (3.181), and the results are given as

$$sL_1\hat{i}_{L1}(s) = \hat{v}_I(s) - r\hat{i}_{L1}(s) - \frac{D'\hat{v}_O(s) - V_O\hat{d}(s)}{2}, \tag{3.183}$$

$$sL_2\hat{i}_{L2}(s)=\hat{v}_I(s)-r_2\hat{i}_{L2}(s)-\frac{\hat{v}_O(s)r_{M2}}{R}$$
$$-\frac{\hat{v}_O(s)D'}{2}+\frac{V_O\hat{d}(s)}{2}, \tag{3.184}$$

$$sC_{eq}\hat{v}_{Ceq}(s)=-\frac{2\hat{v}_O(s)}{R}-I_{L2}\hat{d}(s)+D\hat{i}_{L2}(s). \tag{3.185}$$

Converter Open-loop Transfer Functions

The small signal output voltage of the IBVM converter can be derived from a combination of Eq. (3.183) and (3.185) via the inner boost leg, or Eq. (3.184) and (3.185) via the outer boost leg. Two expressions of the small signal output voltage were derived and they are given as

$$\hat{v}_O(s)(L_1)=\frac{\begin{pmatrix}2\hat{v}_i(s)D'R+V_OD'R\hat{d}(s)\\-\frac{2V_O\hat{d}(s)(sL+r)}{D'}\end{pmatrix}\times\frac{(1+srC_{eq})}{L_1C_{eq}(R+2r_{Ceq})}}{s^2+s\frac{C_{eq}\left(r(R+r_{Ceq})+D'^2Rr_{Ceq}\right)+2L_1}{L_1C_{eq}(R+2r_{Ceq})}+\frac{2r+D'^2R}{L_1C_{eq}(R+2r_{Ceq})}}. \tag{3.186}$$

$$\hat{v}_O(s)(L_2)=\begin{pmatrix}2\hat{v}_I(s)D'R+V_OD'R\hat{d}(s)\\-\frac{2V_O\hat{d}(s)(sL_2+r_2)}{D'}\end{pmatrix}\times\frac{(1+srC_{eq})}{L_2C_{eq}(R+2r_{Ceq})}$$
$$\div\begin{pmatrix}s^2+s\frac{C_{eq}\left(r_2(R+r_{Ceq})+D'r_{Ceq}(D'R+2r_{M2})\right)+2L_2}{L_2C_{eq}(R+2r_{Ceq})}\\+\frac{2(r_2+D'r_{M2})+D'^2R}{L_2C_{eq}(R+2r_{Ceq})}\end{pmatrix}. \tag{3.187}$$

Where $\hat{v}_O(s)(L_1)$ is the converter small signal output voltage derived with respect to the inner boost leg of the converter, while $\hat{v}_O(s)(L_2)$ is the converter small signal output voltage derived with respect to the outer boost leg of the converter.

The converter small signal control-to-output transfer function can be derived from Eq. (3.186) or (3.187). Two expressions of the small signal control-to-output transfer functions were derived and they are given as

$$G_{v_O d_1}(s) = \left.\frac{\hat{v}_O}{\hat{d}_1(s)}\right|_{\hat{v}_I(s)=0}$$

$$= -\frac{2V_O r_{Ceq}\left(s+\frac{1}{r_{Ceq}C_{eq}}\right)\left(s-\frac{1}{L_1}\left[\frac{D'^2R}{2}-r\right]\right)}{D'(R+2r_{Ceq})} \div \left(s^2 + s\frac{C_{eq}\left(r\left(R+r_{Ceq}\right)+D'^2Rr_{Ceq}\right)+2L_1}{L_1C_{eq}(R+2r_{Ceq})} + \frac{2r+D'^2R}{L_1C_{eq}(R+2r_{Ceq})}\right), \quad (3.188)$$

$$G_{v_O d_2}(s) = \left.\frac{\hat{v}_O}{\hat{d}_2(s)}\right|_{\hat{v}_I(s)=0}$$

$$= -\frac{2V_O r_{Ceq}\left(s+\frac{1}{r_{Ceq}C_{eq}}\right)\left(s-\frac{1}{L_2}\left[\frac{D'^2R}{2}-r_2\right]\right)}{D'(R+2r_{Ceq})} \div \left(s^2 + s\frac{C_{eq}\left(r_2\left(R+r_{Ceq}\right)+D'r_{Ceq}\left(D'R+2r_{M2}\right)\right)+2L_2}{L_2C_{eq}(R+2r_{Ceq})} + \frac{2\left(r_2+D'r_{M2}\right)+D'^2R}{L_2C_{eq}(R+2r_{Ceq})}\right). \quad (3.189)$$

Where $G_{v_O d_1}(s)$ is the small signal control-to-output transfer function derived with respect to the inner converter boost leg, while $G_{v_O d_2}(s)$ is the small signal control-to-output transfer function derived with respect to the outer converter boost leg.

3.5.5 Design of the IBVM Converter

Table 3.5 shows the design specifications of the IBVM converter. The parameter and component values of the converter power stage are determined by using the given design specifications, the steady state parameter and component equations that were derived in the converter steady state analysis section.

Table 3.5: The IBVM converter design specifications

parameter	Value	Comments
Output power P_O	50 – 900 W	At full-load for P_I of 1 kW
Input voltage V_I	36 – 67 VDC	Nominal Voltage: 52 VDC
Output voltage V_O	200 VDC	Galvanic isolation required
Efficiency target η	90 %	optimised at full-load
Input current ripple	$\leq$ 30 % of I_L	For load range 5.5-100 %
Output voltage ripple Δv_O	< 1 % of V_O	
Switching frequency f_s	$\cong$ 50 kHz	

DC voltage transfer function calculation

The maximum, nominal and minimum values of the DC voltage transfer function are calculated using Eq. (3.165) and (3.166), and they are given as 5.56, 3.85 and 2.99.

Duty cycle

The maximum, nominal and minimum values of the duty cycle are determined using Eq. (3.175) and (3.176), and they are given as 0.676, 0.532 and 0.398.

Selection of Capacitor, Inductor and load Resistor

The values for the capacitors are calculated using Eq. (3.170) and the values for the inductors are calculated using Eq. (3.168) and (3.169). While the minimum and maximum values of the load resistor required to achieve the specified minimum and maximum output power can be calculated using Eq. (3.175) or (3.176). Table 3.6 shows a list of the component values for the converter power stage design.

Table 3.6: The component list for the power stage design of IBVM converter

Component	Value	Unit
C_1, C_2 & C_3	244.82	µF
r_{C1}, r_{C2} & r_{C3}	17.8	mΩ
L_1 & L_2	288 & 287.31	µH
R_{min} & R_{max}	44.44 & 400	Ω

3.6 Conclusion

Table 3.7 shows a summary of the converter topologies. The table directly compares the performance characteristics of the converter topologies. As shown in the table, the

ICFFB converter offers: isolation of the input voltage from the output voltage, very high power handling capability, high component count, high voltage boost ratio and no input current ripple and input voltage ripple cancellation. On the other hand, the IBVM converter offers: very high voltage boost ratio, input current ripple and input voltage ripple cancellation, high component count and high power handling capability. While the boost converter and the sepic converter offer: low voltage boost ratio, no input current ripple and input voltage ripple cancellation, low and medium component count respectively. A comparison of the performance characteristics of the converter topologies, shows that the IBVM converter is more favourable for the design of a PEMFC PCU compared to the other topologies.

Table 3.7: A summary of the converter topologies

Performance characteristic index	Converter Topology			
	ICFFB	Boost	Sepic	IBVM
Voltage boost ratio	High	Low	Low	Very high
Input current ripple cancellation	Nil	Nil	Nil	High
Input voltage ripple cancellation	Nil	Nil	Nil	High
Component count	High	Low	Medium	High
Control complexity	Medium	Low	High	Medium
Isolation of output from input	Yes	Nil	Nil	Nil
Power handling capability	Very High	Low	Low	High
Efficiency	$\frac{V_O D'}{V_I n}$	$\frac{V_O D'}{V_I}$	$\frac{V_O D'}{V_I D}$	$\frac{V_O D'}{2V_I}$

CHAPTER 4

CONVERTER CONTROL, SIMULATION RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, the design of controllers, the simulation results of the open-loop and the closed-loop models and the discussion of the simulation results for the four converter topologies discussed in chapter 3 are presented.

The simulation of the converter models was done in order to verify the circuit modelling and the converter designs carried out in chapter 3. MATLAB/Simulink 2014a student version software was used for simulation.

4.2 Converter Control

In principle, the essence of converter control is to maintain the output voltage of a converter at a fixed and desired voltage level when system conditions such as input voltage and load current change. In this section, the term feedback is used interchangeably with closed-loop.

Figure 4.1 shows the simplified circuit of a PWM DC – DC converter with current mode feedback control (CMFC). The feedback network samples and attenuates the output voltage $V_O(t)$ and feeds it to the controller, which then produces a control voltage for the modulator. $V_O(t)$ entirely relies on the duty cycle $d(t)$, the load current $i_{Load}(t)$ and the input voltage $V_I(t)$. According to Robert and Dragan (2001), Kittipeerachon and Bunlaksananusorn (2004), and Mark (2007), in the design of regulated converters, invariably the objective is to keep the output voltage of a converter constant at a desired level in spite of variations in the input voltage and load current. The above converter design constraints can be overcome by using a compensated feedback circuit as the controller, where the output voltage is made to conform to its reference.

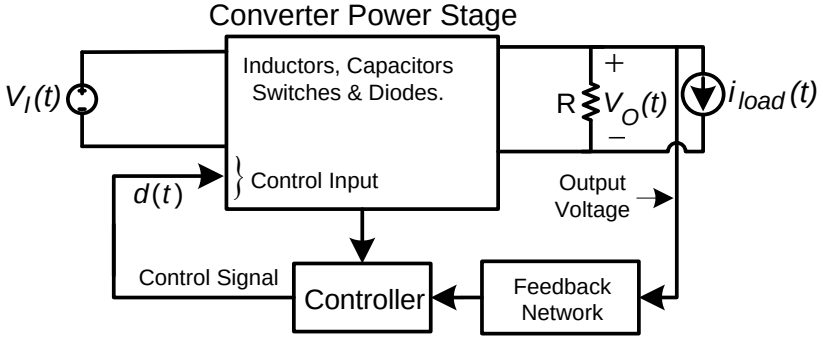


Figure 4.1: The simplified circuit of a PWM DC – DC converter with CMFC.

The function of a compensated feedback circuit is to maintain the output voltage at a fixed and desired level in spite of variations in the input voltage and load current. This uses negative feedback control. Negative feedback control can be realised by using voltage mode feedback control (VMFC) or current mode feedback control (CMFC). VMFC is ideal for simpler topologies such as the boost converter and the isolated current full-bridge converter, while CMFC is ideal for both simpler and complex topologies such as the sepic converter and the IBVM converter.

Dixon (1983), discusses the design of compensated circuits for VMFC and CMFC. Middlebrook (1987), Middlebrook (1989), Kazimierczuk (2000) and Bryant and Kazimierczuk (2005), state that the knowledge and understanding of the frequency response of the open-loop system of the converter power stage is required when designing compensated feedback circuits. The frequency response of the open-loop system of a converter power stage is determined by plotting bode-plots of the converter small-signal transfer functions. Small signal converter transfer functions are crucial in the design of a converter controller, and they are vital in predicting the stability and transient response of the converter system with feedback control (Robert & Dragan, 2001).

4.2.1 Open-loop control

According to Kittipeerachon and Bunlaksananusorn (2004), the distinguishing characteristic of an open-loop control system is its inability to compensate for any variations in the input variables of the system. The output voltage of a converter is simply commanded by the duty cycle; as a result, the open-loop control circuit does not correct for any variations and has no capability to keep the output voltage constant when variations arise. As result, any variations in the input voltage and load current will cause the converter output voltage to deviate from the reference value.

Figure 4.2 shows the block diagram of a PWM DC – DC converter with open-loop control. The block diagram comprises of the open-loop control circuit, the converter power stage, three inputs and an output-controlled variable. The open-loop control circuit consists of two inputs $V_{control}(t)$ and $V_{sawtooth}(t)$ and an output $d(t)$. The two inputs are fed to the pulse-width modulator block, where a PWM signal with duty cycle $d(t)$ is produced and then fed to the gate driver block. The gate driver block amplifies the PWM signal to higher voltage. The converter power stage block consists of a control input, variations in $v_I(t)$ and $i_{load}(t)$ and an output voltage $v_O(t)$. The output voltage is a function of the duty cycle, the input voltage and the load current.

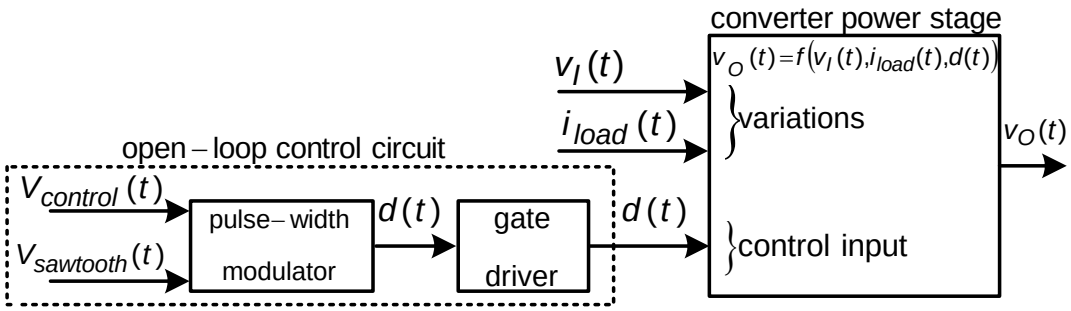


Figure 4.2: The block diagram of a PWM DC – DC converter with open-loop control

Figure 4.3 shows the input and out voltage waveforms of the pulse-width modulator. The pulse-width modulator produces a PWM signal with duty cycle $d(t)$ by comparing its two inputs $V_{control}(t)$ and $V_{sawtooth}(t)$. When the control voltage is greater than the sawtooth voltage, the pulse-width modulator outputs a high signal and vice versa. Therefore, the duty cycle and frequency of the PWM signal can be increased or decreased by varying the control and sawtooth voltage. In the diagram, DT_s denotes the time interval when the PWM signal is high, while $D'T_s$ denotes the time interval when the PWM signal is low.

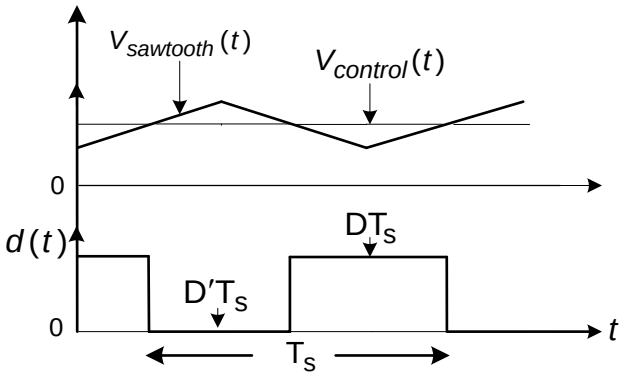


Figure 4.3: The input and output voltage waveforms of the pulse-width modulator.

4.2.2 Feedback control (Closed-loop control)

Feedback control is defined as the ability of a system to keep the controlled variable constant, with the capability to compensate for any variations in the input variables (Norman, CONTROLS SYSTEMS ENGINEERING). In converter control applications, feedback control can be classified into voltage mode feedback control (VMFC) and current mode feedback control (CMFC).

According to Hangseok (2011), the disadvantages of open-loop control such as sensitivity to variations and incompetence to correct for these variations can be solved by using negative feedback control. Here, a compensated feedback circuit

automatically adjusts the duty cycle in order to obtain an output voltage proportional to the output voltage reference. The control method involves comparing the measured converter output voltage to the output voltage reference in order to generate an error (difference) voltage, which is then used to influence the actual value of the converter output voltage. Invariably, PWM DC – DC converters require negative feedback control in order to regulate the output voltage to that of the output voltage reference. Negative feedback control reduces the error voltage between the converter output voltage and the output voltage reference. This mechanism keeps the converter output voltage constant in spite of variations.

4.2.3 Voltage mode feedback control

With VMFC, the converter output voltage is sampled by a feedback network and then fed to a compensated voltage error amplifier (EA). The compensated EA compares the sampled converter output voltage to a fixed output voltage reference, and then produces an error voltage proportional to the difference between the output voltage reference and the actual measured converter output voltage. The error voltage is fed to a pulse-width modulator as the control signal, where it is then used to produce a PWM signal for the switching devices. Figure 4.4 shows a compensated type III EA, which is also known as Integral-double lead controller. The EA consists of an output voltage reference V_{OR}, the converter output voltage feedback V_{OF}, a feedback impedance Z_f, an input impedance Z_i and an output control voltage (error voltage) V_c. h_{11} is the h-parameter of the resistive feedback network. The EA subtracts V_{OF} from V_{OR} in order to produce a control voltage V_C, which is then fed to the pulse-width modulator. An in depth study and design procedure of the type III voltage EA is covered by Kazimierczuk (2008) and many others.

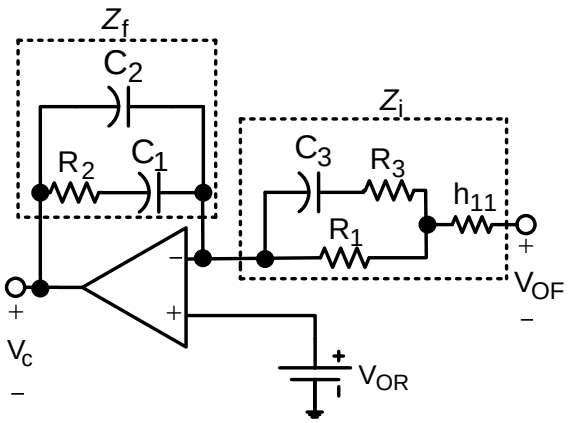


Figure 4.4: Compensated type III Voltage Error Amplifier

Figure 4.5 shows the block diagram of a PWM DC – DC converter with compensated VMFC. The block diagram consists of an output voltage reference V_{OR}, an output

voltage feedback V_{OF}, an error voltage $V_e(s)$, a control voltage $V_C(s)$, a resistive feedback network gain β, an EA gain $G_c(s)$, a pulse-width modulator gain $G_m(s)$, a gate driver gain $G_d(s)$ and the converter power stage with three inputs and an output. Compensation of the EA reduces the error voltage, stabilises the closed-loop gain $G_{cl}(s)$, ensures fast response to variations and ensures sufficient gain margin (GM) and phase margin (PM).

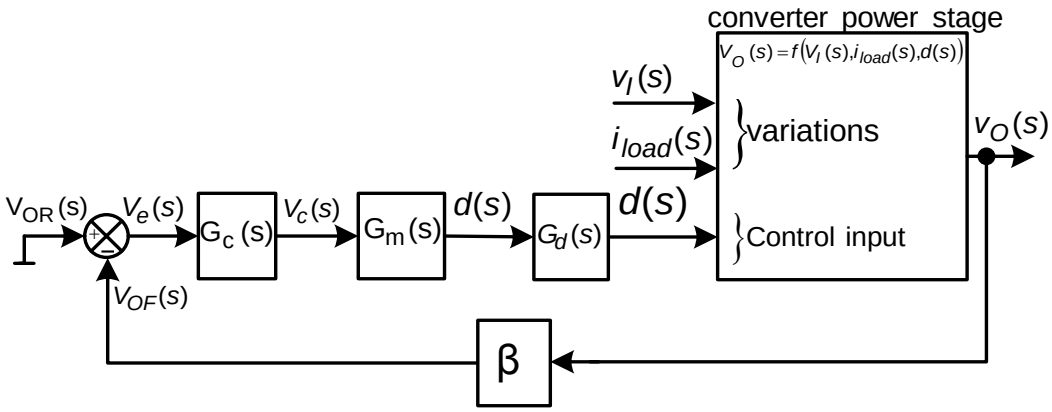


Figure 4.5: The block diagram of a PWM DC – DC converter with compensated VMFC.

Figure 4.6 shows the equivalent small-signal block diagram of a PWM DC – DC converter with VMFC. Several small signal transfer function expressions are derived from the diagram. The diagram depicts a converter as a system with three independent sources $\hat{v}_I(s)$, $\hat{v}_{OR}(s)$ and $\hat{i}_{load}(s)$ and a single output $\hat{v}_O(s)$. The signals with the hat ($\wedge$) symbol represent the AC component of the signals. $\hat{v}_I(s)$ is the low frequency voltage ripple variation and fluctuations of the input supply voltage. The converter small signal forward path voltage gain A, is determined by assuming that $\hat{v}_O(s)$ is constant and then setting $\hat{v}_{OR}(s)$ to zero, and it is given as

$$A \equiv \frac{\hat{v}_O(s)}{\hat{v}_e(s)} = G_c(s)G_m(s)G_d(s)G_{vOd}(s). \qquad (4.1)$$

The loop gain $T(s)$, which is the total gain around the negative feedback loop, is given as

$$T(s) = \frac{\hat{v}_O(s)}{\hat{v}_{OF}(s)} = \beta A = \beta G_c(s)G_m(s)G_d(s)G_{vOd}(s). \qquad (4.2)$$

The AC variations of the converter output voltage is given as

$$\hat{v}_O(s) = v_{OR}(s)\frac{A}{1+T(s)} + \hat{v}_I(s)\frac{G_{vOI}(s)}{1+T(s)} + \hat{i}_{load}(s)\frac{Z_O(s)}{1+T(s)}. \qquad (4.3)$$

Equation (4.3) indicates that feedback reduces the line-to-output transfer function $G_{vOI}(s)$, and the control-to-output transfer function $G_{vOd}(s)$ by a factor of $1/(1+T(s))$

. Assuming a very large loop gain, the reference-to-output transfer function is expressed as

$$G_{v_O R}(s) = \frac{\hat{v}_O(s)}{v_{OR}(s)} = \frac{1}{\beta}. \tag{4.4}$$

Analysing Eq. (4.4) shows that the reference-to-output transfer function is independent of the converter forward path gains, therefore below the crossover frequency f_c, the loop gain has a large magnitude and the reference tracks the output very well. The cross over frequency is defined as the frequency where the gain margin (GM) of a system is equal to one or $0\,dB$. The control voltage-to-duty cycle transfer function of the pulse-width modulator is given as

$$G_m(s) = \frac{1}{V_{Tm}}. \tag{4.5}$$

Where V_{Tm} is the amplitude of the sawtooth voltage. The transfer function of the compensated error amplifier is given as

$$G_c(s) = \frac{Z_f(s)}{Z_i(s)}. \tag{4.6}$$

The transfer functions derived from a converter without feedback control are referred to as open-loop transfer functions. On the other hand, transfer functions derived from a converter with feedback control are referred to as closed-loop transfer functions. The closed-loop transfer functions of a converter with VMFC are derived from Eq. (4.3), by setting only one independent source active at a time and the rest to zero.

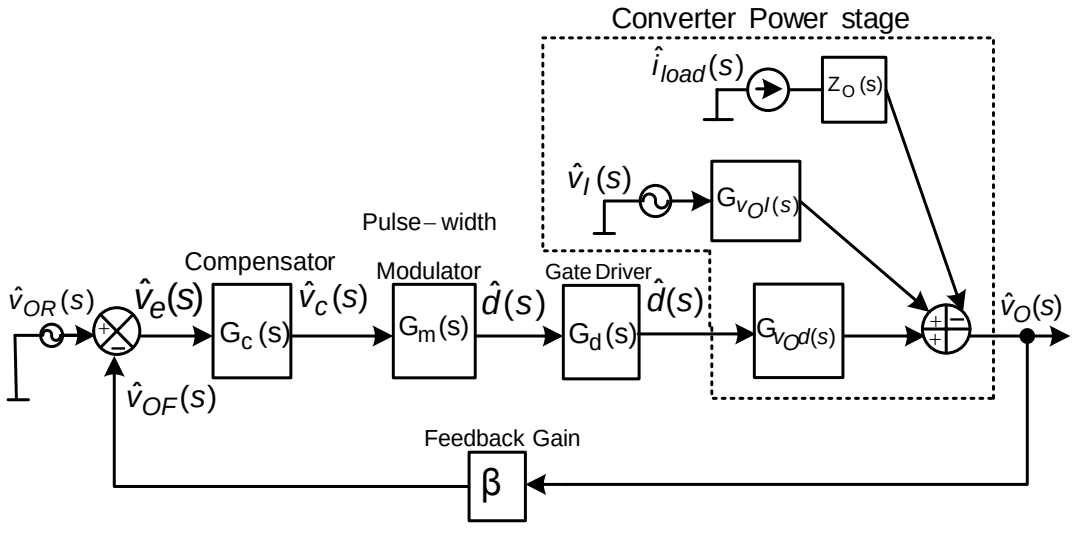


Figure 4.6: The equivalent small-small signal block diagram model of a PWM DC – DC converter with VMFC.

4.2.4 Current mode feedback control

Current mode feedback control (CMFC) consists of a current loop and a voltage loop. The current loop controls the inductor current of a converter and adjusts the duty cycle in proportion to the inductor current variation, while the voltage loop controls the output voltage of a converter and sets a reference voltage for the current loop that is proportion to the output voltage variation.

Currently, there are many forms of CMFC. In this work, peak current mode feedback control (PCMFC) is considered for the control of a sepic converter and IBVM converter. The PCMFC that will be covered herein is based on the work of Ridley (1990), Ridley (1991), Ridley (1999), Robert and Dragan (2001), Vatché (2004) and Andrea (2011).

In the reviewed literature, it is widely reported that the current loop in PCMFC is inherently unstable for duty cycle values greater than 0.5 due to sub-harmonic oscillations. In order to stabilise the current loop, an external ramp voltage is added to the inductor current and the sum is subtracted from the control voltage of the modulator, thereby damping the oscillations and compensating the current loop (Tan & Middlebrook, 1995; Vatché, 2004; Kazimierczuk, 2008). Compensation of the current loop is also recommended for duty cycle values less than 0.5 due to noise signals prevalent in switch mode converters (Andrea, 2011). Figure 4.7 shows the block diagram of the invariant model of the current controlled PWM (CC-PWM) switch with external ramp for compensation developed by Vatché Vorpérian. The model consists of a clock, an S-R latch, a PWM switch, a comparator, a ramp voltage V_{ramp}, a compensated control voltage v_c, a voltage sensor R_i, a pulsating terminal voltage $v_{cp}(t)$ and a steady DC terminal voltage $v_{ap}(t)$. The invariant model of the CC-PWM switch can be used to replace the switching elements of any switching converter using PCMFC. A clock with a constant period T_s repeatedly sets the S-R latch to initiate the on-time of the converter switch. R_i measures the inductor current and converts it into a voltage signal, and V_{ramp} compensates for the sub-harmonic oscillations of the current loop. Whenever the sum of R_i and V_{ramp} is greater than V_c, the comparator resets the S-R latch. Figure 4.8 shows the invariant waveforms of the CC-PWM switch model (Vatché, 2004). Where S_n is the positive slope of the inductor current during DT_s, S_f is the negative slope of the inductor current during $D'T_s$, S_e is the slope of the external ramp, I_c is the current of the common terminal and v_c is the compensated control voltage of the voltage loop.

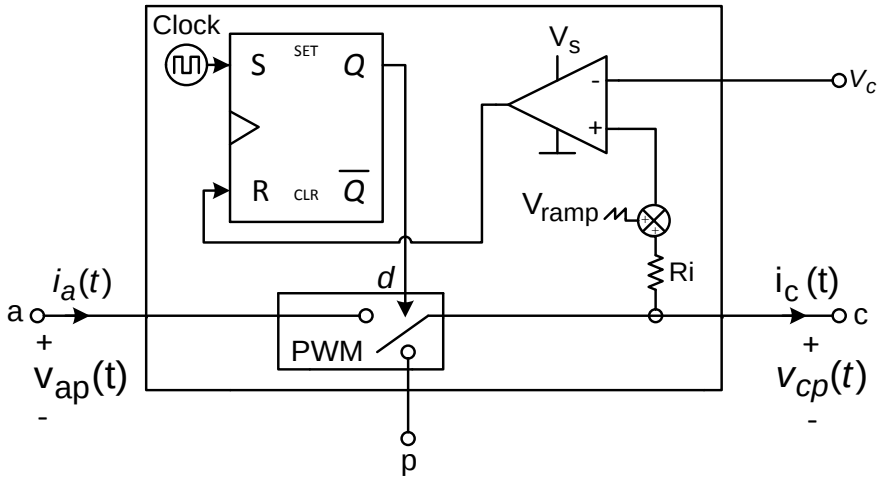


Figure 4.7: The block diagram of the invariant model of the CC-PWM Switch with external ramp compensation for stability.

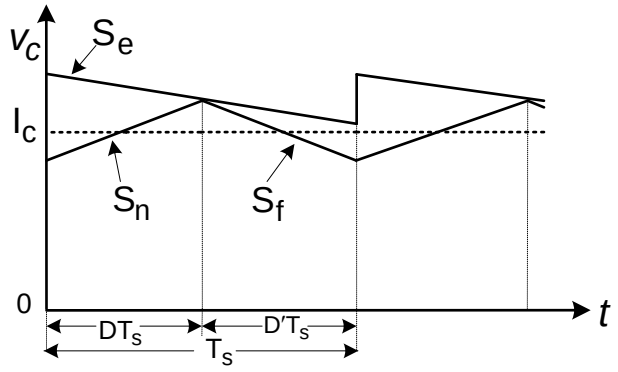


Figure 4.8: The invariant current and voltage waveforms of the CC-PWM Switch model with external ramp compensation for stability.

The equations that describe the waveforms of the CC-PWM switch model in Figure 4.8 are given as

$$S_n = \frac{V_{ac} R_i}{L} = \frac{V_{ap} D' R_i}{L}, \tag{4.7}$$

$$S_f = \frac{V_{cp} R_i}{L}, \tag{4.8}$$

$$V_c = I_c R_i + = \frac{S_f D' T_s}{2} + S_e D T_s, \tag{4.9}$$

where L is the effective inductance of the converter that determines the slew rate of the current slope.

Figure 4.9 shows the average large signal model of the CC-PWM switch model with external ramp compensation. The figure corresponds to the effect of the control law on the average quantities of Eq. (4.9) and the invariant equations of the PWM switch given in chapter 3.

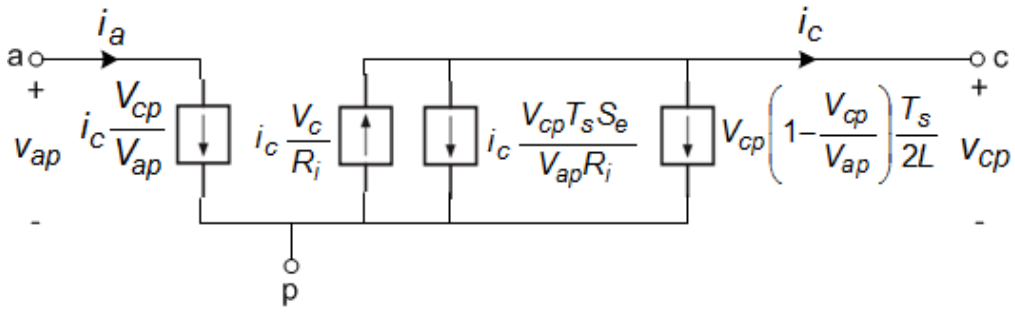


Figure 4.9: The average large signal model of the CC-PWM Switch model with eternal ramp compensation.

Figure 4.10 shows the small-signal model of the CC-PWM switch model with external ramp compensation. The small-signal model of the CC-PWM switch model is obtained by perturbing the large-signal average equations given in Figure 4.9. It is noteworthy to remember that C_s is used to model the sub-harmonic oscillations of the current loop. The small-signal model of the CC-PWM switch is used for linear controller design and stability analysis of PWM DC – DC converters with PCMFC.

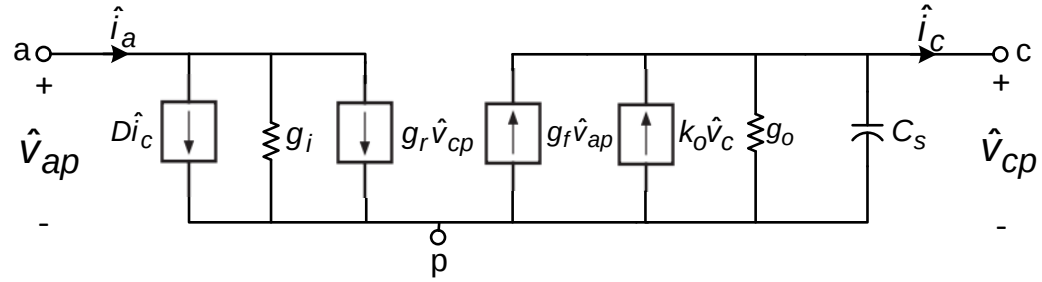


Figure 4.10: The small-signal model of the CC-PWM Switch model with external ramp compensation.

The presence of an S-R latch in the CC-PWM switch model introduces a sample and hold effect in the control loop, which results into an open loop sampling gain $H_e(s)$, common to the denominator of the small-signal dynamics of all PWM DC – DC converters operating in CCM with PCMFC. The modelling of $H_e(s)$ is thoroughly discussed by Middlebrook (1989), Ridley (1990) and Vatché (2004) and it given as

$$H_e(s) = 1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{{\omega_n}^2}, \qquad (4.10)$$

where Q_n is equal to $1/\pi\left[D'\left(S_e/S_n\right)+1/2-2\right]$, ω_n is equal to $\omega_s/2$ and ω_s is the angular frequency of the converter switching frequency. For design purposes, it is noteworthy to remember that Eq. (4.10) is only accurately modelled for frequencies up to half the converter's switching frequency.

In order to design a peak current mode feedback (PCMF) controller, first the small-signal control-to-output transfer function $\hat{v}_O / \hat{v}_c$ must be determined by performing the necessary circuit manipulation as described by Vatché (2004).

In summary, the design of compensated feedback control circuits, performance analysis and stability analysis of PWM DC – DC converters is dependent on the average linearised low-frequency small-signal models of converters and controllers. First, a knowledge and understanding of the frequency response characteristics of the open-loop system of the converter power stage is required. Here, the two major points to consider are the gain and the phase of the converter open-loop system. Once these have been determined, an appropriate compensator circuit can be selected in order to fine-tune the gain margin (GM) and the phase margin (PM) of the closed-loop system to ensure stability.

4.3 Control and Simulation of the ICFFB Converter

4.3.1 Control of the ICFFB Converter

Figure 4.11 shows the circuit of the ICFFB converter with open-loop control. The circuit consists of the power stage, the MOSFET gate drivers and the pulse-width modulator. The open-loop control of the converter is achieved by means of the open-loop control circuit, which consists of the pulse width modulator.

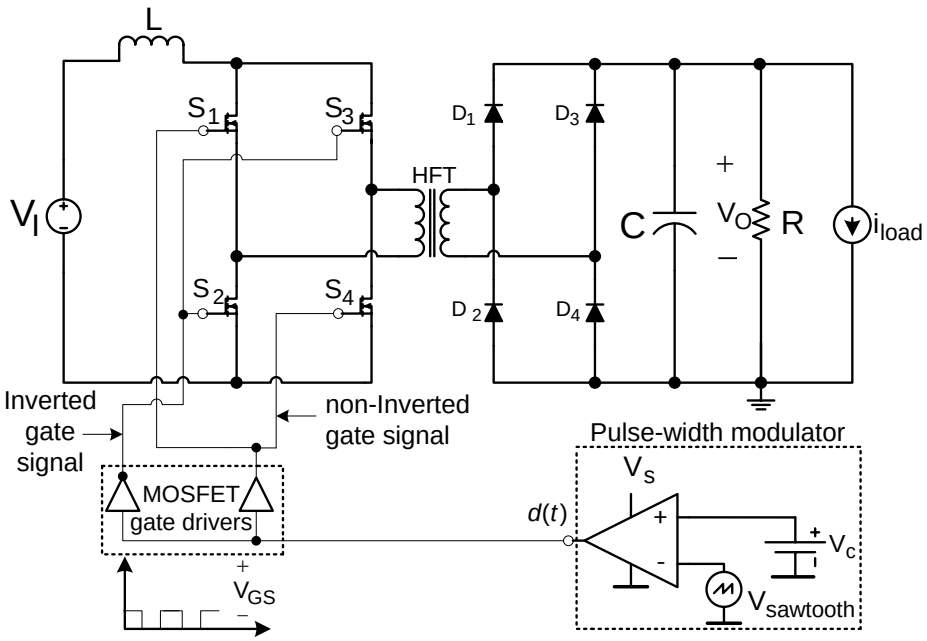


Figure 4.11: The circuit of the ICFFB converter with open-loop control.

Figure 4.12 shows the circuit of the ICFFB converter with VMFC. The circuit consists of a resistive feedback network (FN) with resistors R_A and R_B, a compensated EA voltage mode controller, a pulse-width modulator, the gate drivers and the power stage.

The pulse-width modulator compares V_c to $V_{sawtooth}$ and then produces a PWM signal with duty cycle $d(t)$ and the gate drivers amplify $d(t)$ to a higher V_{GS} amplitude, which is then used to control the switching of the MOSFETs.

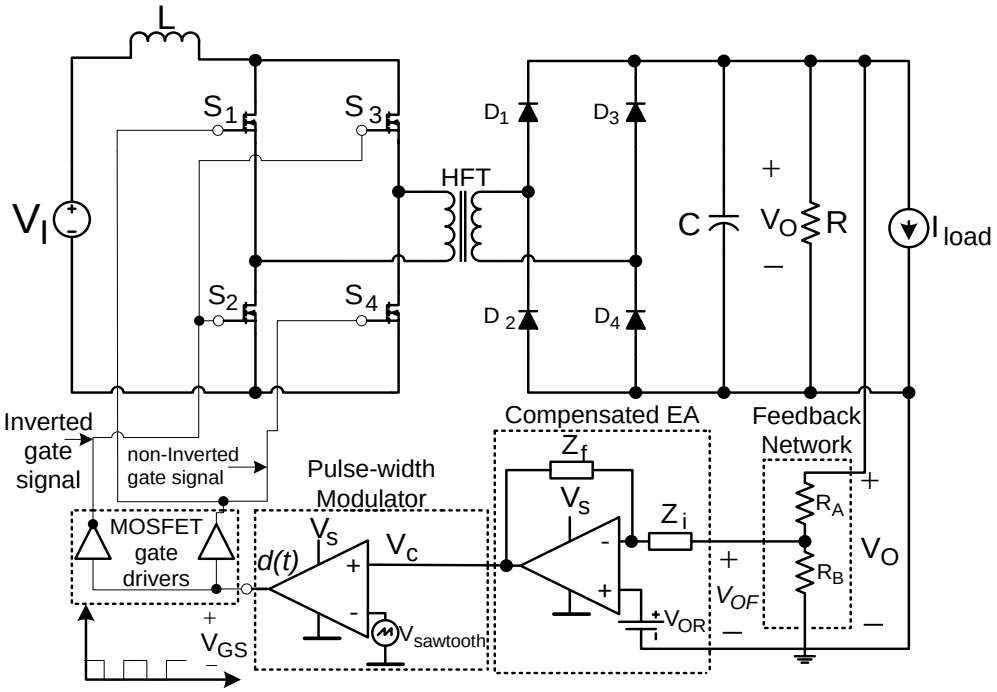


Figure 4.12: The circuit of the ICFFB converter with VMFC.

Table 4.1 shows the parameter and component values for the feedback network, pulse-width modulator and compensated EA of the designed ICFFB converter. A MATLAB code was used to calculate the parameter and component values of the voltage controller and to generate bode-plots of the transfer functions (See Appendix C1: Code for the design of the ICFFB converter controller). The compensated EA was used for the design of a type III voltage mode controller. Kazimierczuk (2008) covers an in-depth discussion of the controller design procedure.

Table 4.1: The parameter and component values for the feedback network, the pulse-width modulator and the compensated EA of the designed ICFFB converter.

Parameter & component list for EA, Voltage FN and Pulse width Modulator		
Component /parameter	Value	comments
V_{tm}	2.5 V	Sawtooth amplitude
V_{OR}	2.5 V	Output voltage reference
R_A, R_B, R_1 ,R_2, R_3	$39\,k\Omega, 1k\Omega, 1.2M\Omega,$ $282.78\,k\Omega,\ 325.64\,k\Omega$	Resistor values for the voltage FN and EA
C_1, C_2, C_3	$12.2\ nF, 3.31\ nF, 2.25\ nF$	Capacitor values for the EA.

4.3.2 Simulation of the ICFFB Converter

Figure 4.13 shows the simulation model of the ICFFB converter with open-loop control in Simulink environment. The model consists of a FC stack, an inductor L and its series resistance r_L, four MOSFET switches $M_1 - M_4$ and two PWM blocks, a high frequency transformer, four diodes $D_1 - D_4$, a capacitor C and its series resistance r_C, a variable load resistor and a scope. The FC block provides power to the converter and the high frequency transformer provides galvanic isolation of the output stage from the input stage and steps-up the input voltage. The variable load resistor ranges between R_{min} (full-load) to R_{max} (minimum-load). The power stage component and parameter values calculated in the design stage of chapter 3 were used for the simulation.

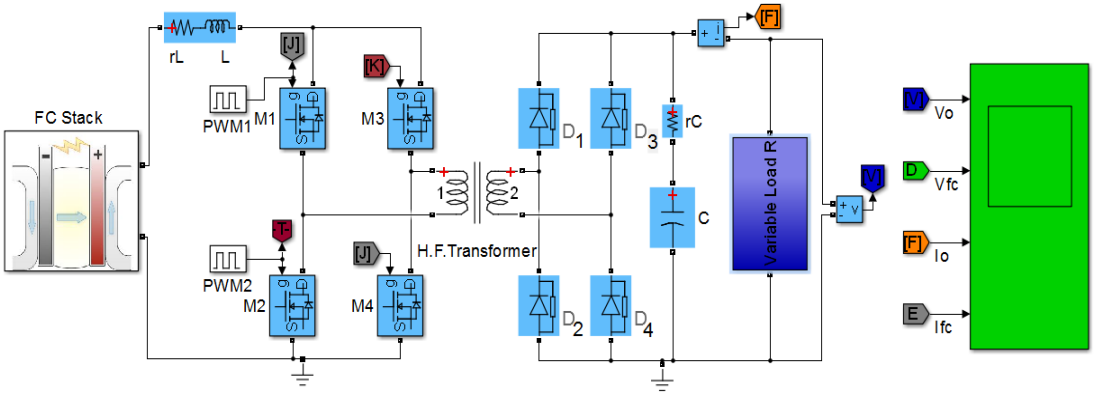


Figure 4.13: The simulation model of the ICFFB converter with open-loop control.

Figure 4.14 shows the bode-plot of the magnitude and the phase of the control-to-output transfer function of the ICFFB converter power stage with open-loop control. The plot indicates a gain margin (GM) of 23.8 dB at a frequency of 4.18 kHz and a phase margin (PM) of $-39°$ at a cross over frequency (f_c) of 20.5 kHz, with a total phase of $-219°$. In the analysis of system stability for PWM DC – DC converters, a system is deemed stable if the total phase of the open-loop control-to-output power stage transfer function is less than $-180°$ at f_c. Since the total phase of the control-to-output power stage transfer function of the ICFFB converter exceeds $-180°$ at f_c, the system is considered unstable, therefore without compensation of the feedback loop, the system would still be unstable even with feedback control. In order to ensure stability, a compensated feedback controller must be integrated into the system, as it will be shown later.

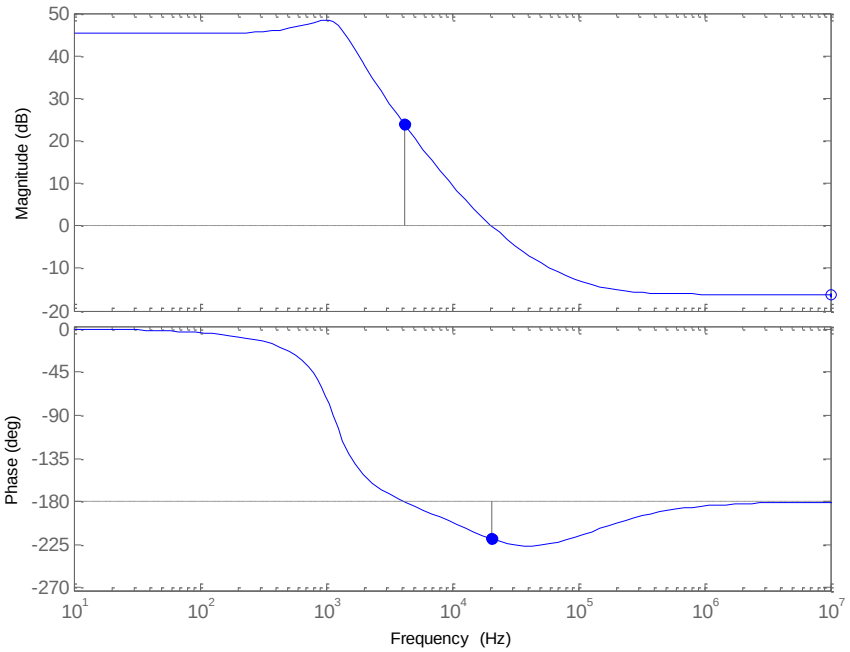


Figure 4.14: The bode-plot of the magnitude and the phase of the control-to-output transfer function of the ICFFB converter power stage with open-loop control.

Figure 4.15 shows the waveforms of the output voltage and the output current of the ICFFB converter and the FC stack at full-load with open-loop control. In the figure, V_O is the converter output voltage, V_{FC} is the FC stack output voltage, I_O is the converter output current and I_{FC} is the FC stack output current. V_O and I_O steadily increase after start-up, and reach their mean value of 89.8 V and 8.08 A in 4.5 ms. On the other hand, V_{FC} sharply drops after start-up, and then steadily increases and reaches its mean value of 37.6 V in 4.5 ms. While I_{FC} overshoots at start-up, and then steadily decreases and reaches its mean value of 26.4 A in 2.2 ms.

Figure 4.16 shows the waveforms corresponding to the output voltage and the output current of the ICFFB converter and the FC stack at minimum-load with open-loop control. V_O and I_O steadily increase after start-up, and reach their mean value of 89.99 V and 0.45 A in 15.5 ms and 13 ms respectively. On the other hand, V_{FC} sharply drops after start-up, and then steadily increases and reaches its mean value of 56 V in 6 ms. While I_{FC} overshoots at start-up, and then steadily decreases and reaches its mean value of 1.03 A in 5 ms.

Results in Figure 4.15 and Figure 4.16 show that V_O and I_O do not match the specified design values given in Table 3.1. This validates the discussed characteristic behaviour of open-loop control, whereby the controlled variable does not match its reference.

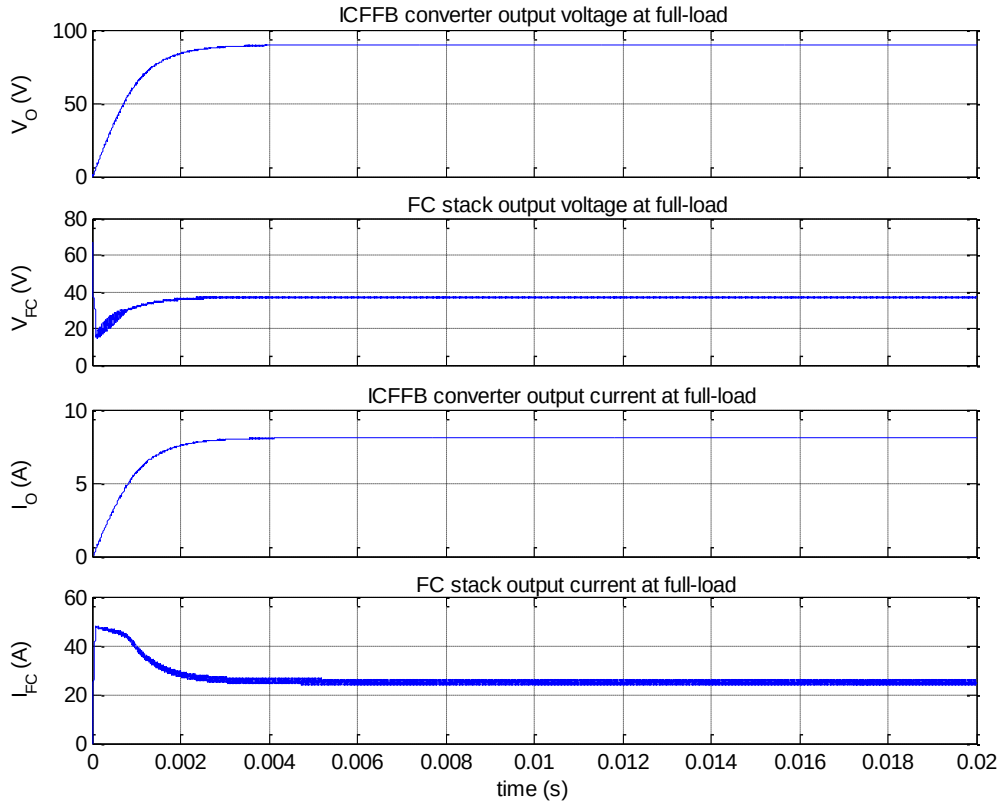


Figure 4.15: The waveforms of the output voltage and the output current of the ICFFB converter and the FC stack at full-load with open-loop control.

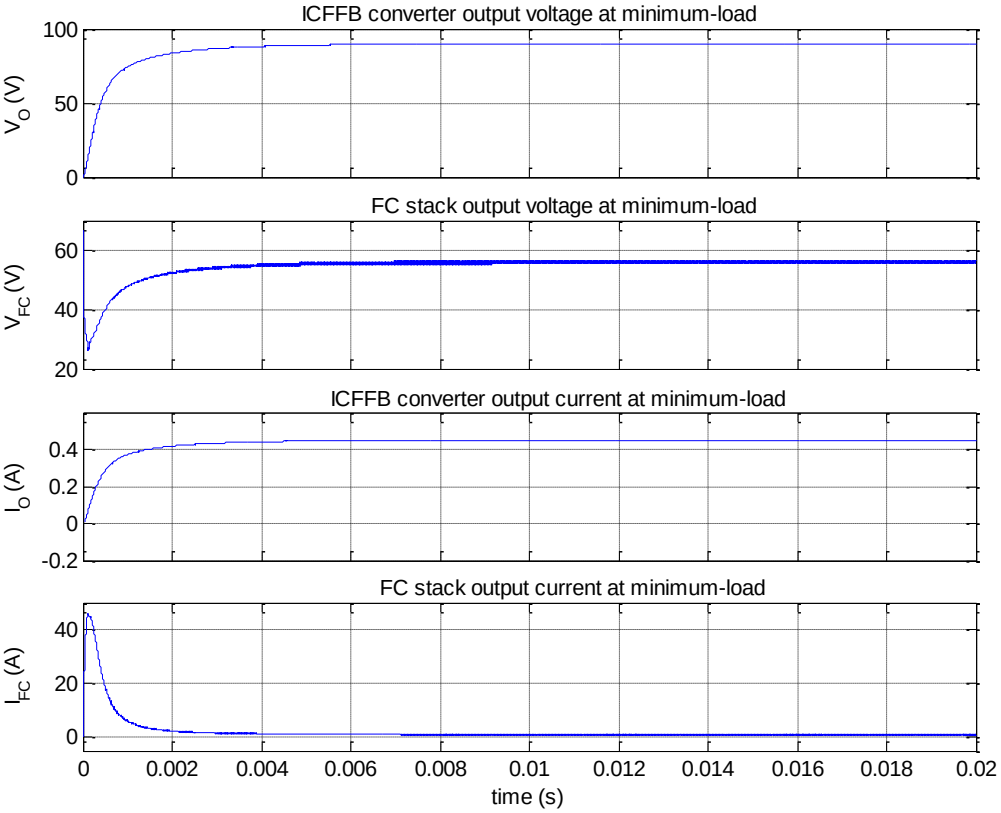


Figure 4.16: The waveforms of the output voltage and the output current of the ICFFB converter and the FC stack at minimum-load with open-loop control.

Figure 4.17 shows the waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at full-load with open-loop control. The converter has a peak-to-peak output voltage ripple (ΔV_O) of 0.4 V and a peak-to-peak output current ripple (ΔI_O) of 0.3 A. While the FC stack has a peak-to-peak output voltage ripple (ΔV_{FC}) of 1 V and a peak-to-peak output current ripple (ΔI_{FC}) of 2.4 A.

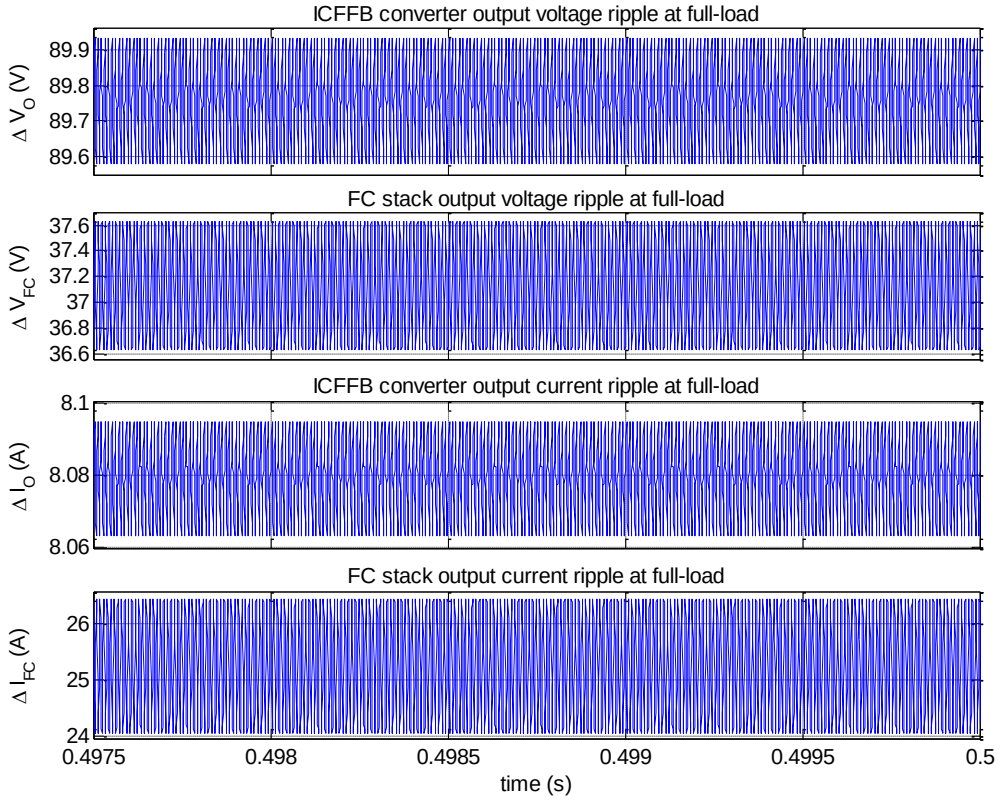


Figure 4.17: The waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at full-load with open-loop control.

Figure 4.18 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at minimum-load with open-loop control. The converter has a ΔV_O of 6 mV and a ΔI_O of 1.1 mA. While the FC stack has a ΔV_{FC} of 1.3 V and a ΔI_{FC} of 0.31 A.

The results in Figure 4.17 and Figure 4.18 show that ΔV_O, ΔI_O and ΔI_{FC} are greater at full-load than at minimum-load. While ΔV_{FC} is greater at minimum-load than at full-load.

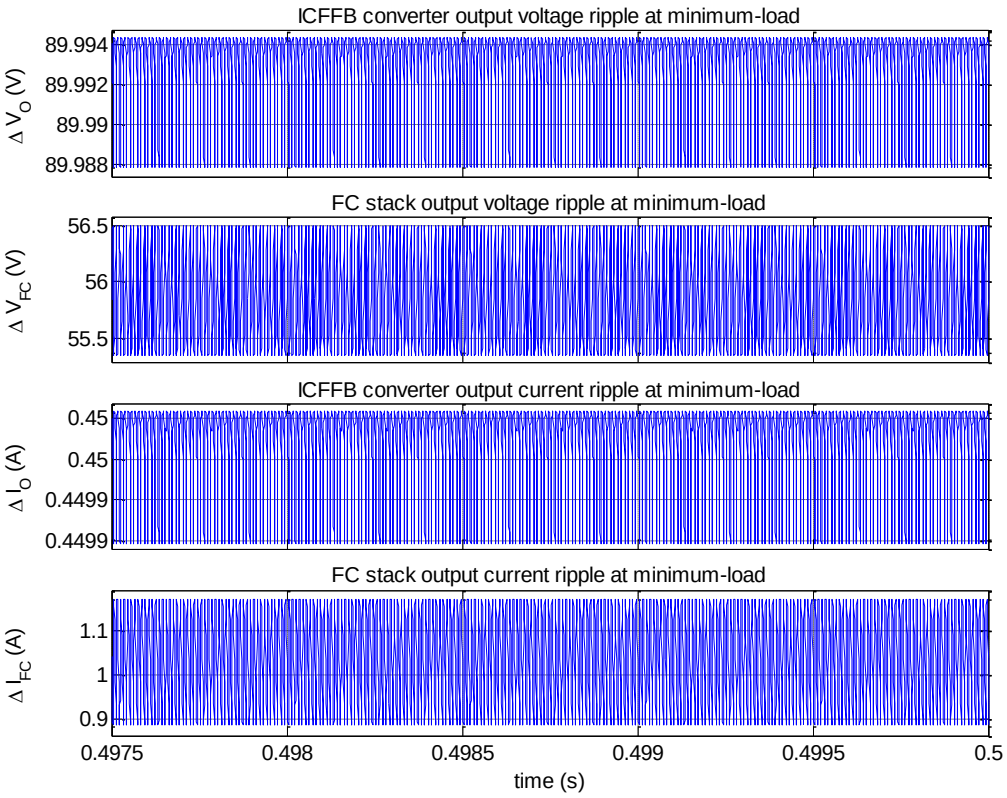


Figure 4.18: The waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at minimum-load with open-loop control.

Figure 4.19 shows the simulation model of the ICFFB converter with VMFC in Simulink environment. The model consists of the power stage and the feedback loop. The feedback loop comprises of a feedback network block, a controller transfer function block, a limiter block and a PWM block.

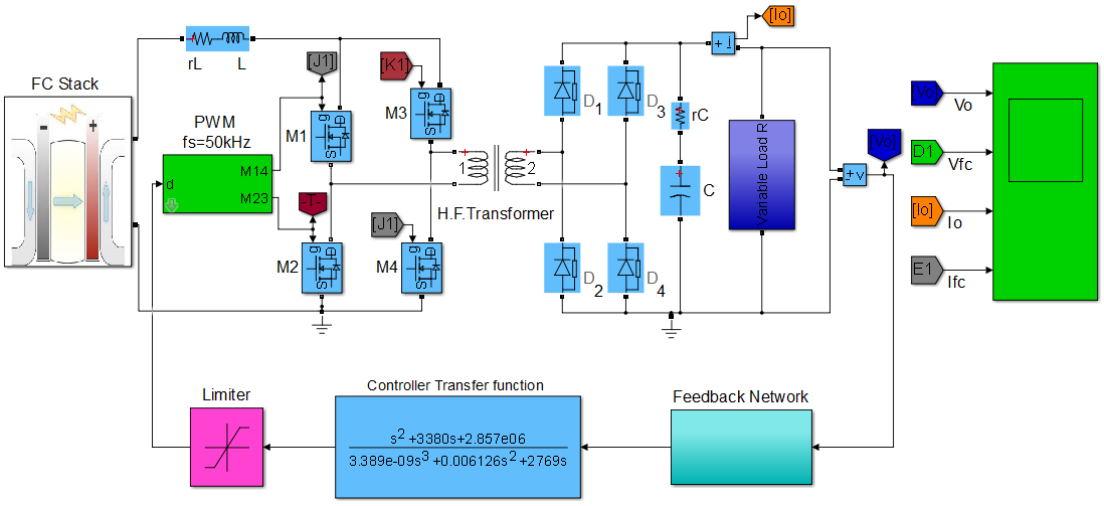


Figure 4.19: The simulation model of the ICFFB converter with VMFC.

Figure 4.20 shows the bode-plot of the magnitude and the phase of the voltage transfer function of the designed and compensated type III EA for the ICFFB converter controller with two zero-pole pairs. The controller has zero-pole pairs at 269 Hz and 143.86 kHz,

and a high cross over frequency at 6.22 kHz with a total PM of $80.1°$. The high cross over frequency ensures a wider bandwidth and faster transient response for the closed-loop control of the system.

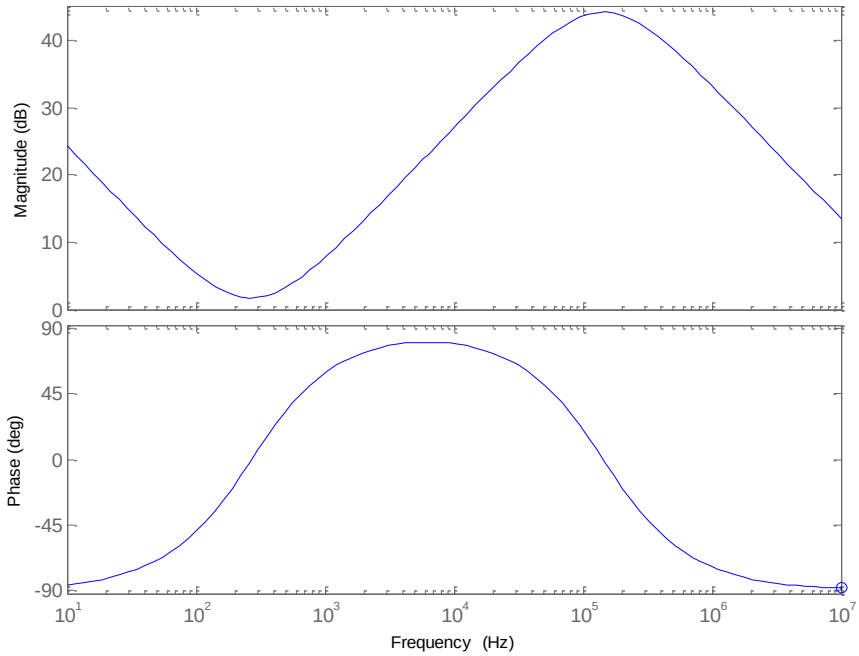


Figure 4.20: The bode-plot of the magnitude and the phase of the voltage transfer function of the designed and compensated type III EA for the ICFFB converter controller with two zero-pole pairs.

Figure 4.21 shows the bode-plot of the magnitude and the phase of the loop gain (T) for the ICFFB converter. The system has a GM of – 8.99 dB at a cross over frequency of 60.1 kHz and a PM of $70°$ at a frequency of 6.22 kHz.

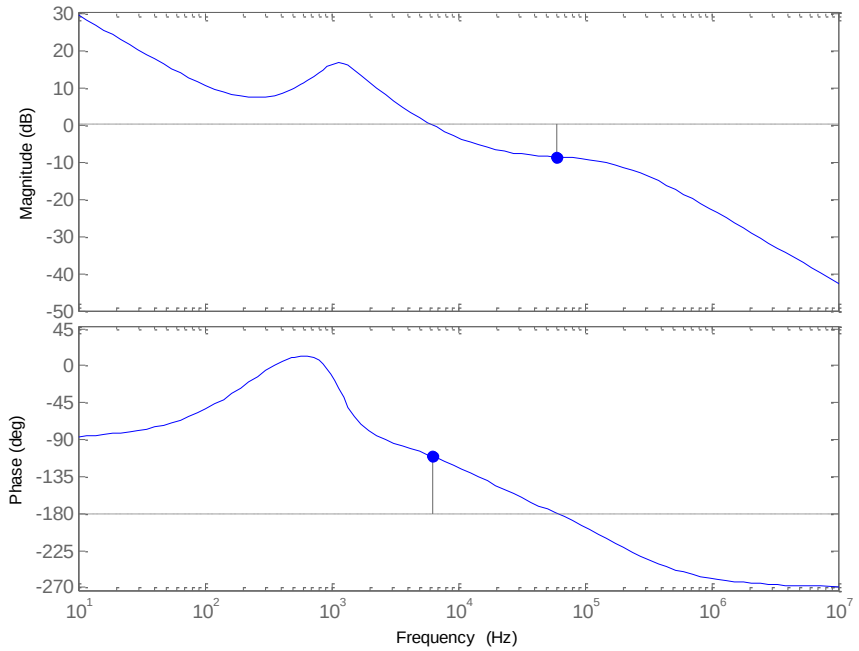


Figure 4.21: The bode-plot of the magnitude and the phase of the loop gain (T) for the ICFFB converter.

Figure 4.22 shows the waveforms of the output voltage and the output current of the ICFFB converter and the FC stack at full-load with VMFC. V_O and I_O steadily increase after start-up, and reach their mean value of 100 V and 9 A in 5.4 ms. On the other hand, V_{FC} drops sharply after start-up, and then steadily increases and develops spikes between 0.44 ms and 0.75 ms, then reaches its mean value of 62 V in 1.5 ms. While I_{FC} overshoots at start-up, and then steadily decreases and develops spikes between 0.44 ms and 0.75 ms, then reaches its mean value of 17 A in 1.7 ms.

Figure 4.23 shows the waveforms corresponding to the output voltage and the output current of the ICFFB converter and the FC stack at minimum-load with VMFC. V_O and I_O steadily increase after start-up, and then slightly overshoot and reach their mean value of 100 V and 0.5 A in 6 ms. On the other hand, V_{FC} sharply drops after start-up, and then steadily increases and develops spikes between 0.2 ms and 1.2 ms and reaches its mean value of 66.7 V in 3.2 ms. While I_{FC} overshoots at start-up, and then steadily decreases and develops spikes between 0.44 ms and 0.75 ms and reaches its mean value of value 0.75 A in 3 ms .

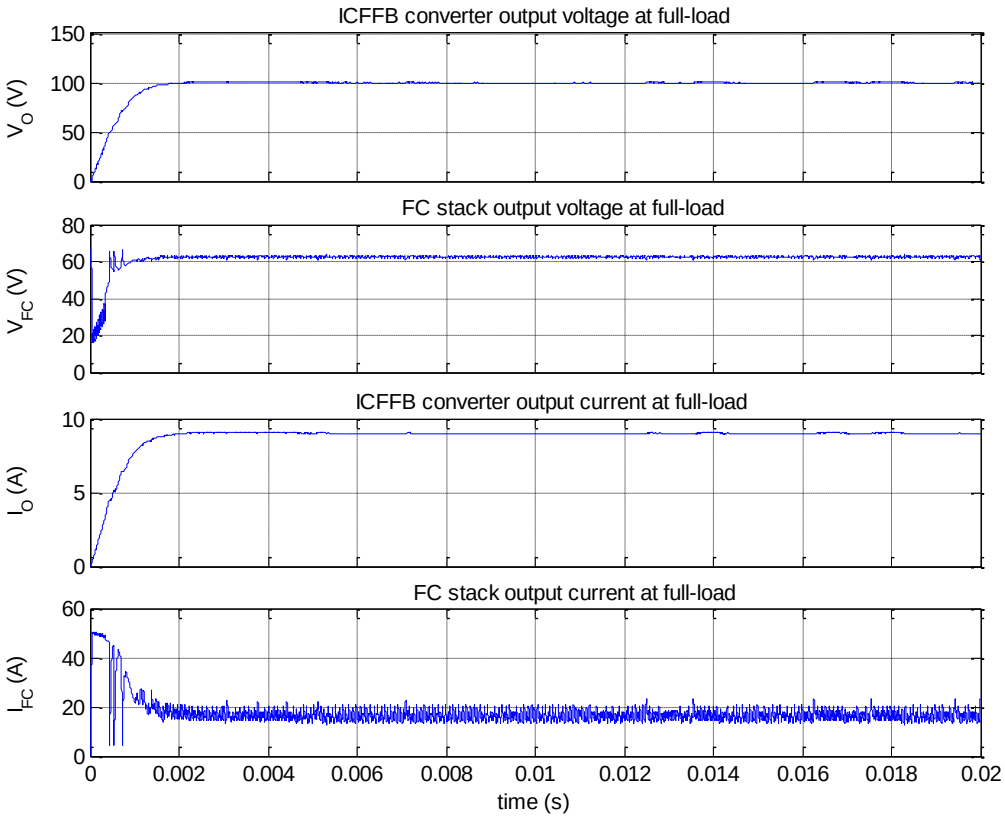


Figure 4.22: The waveforms of the output voltage and the output current of the ICFFB converter and the FC stack with VMFC at full-load.

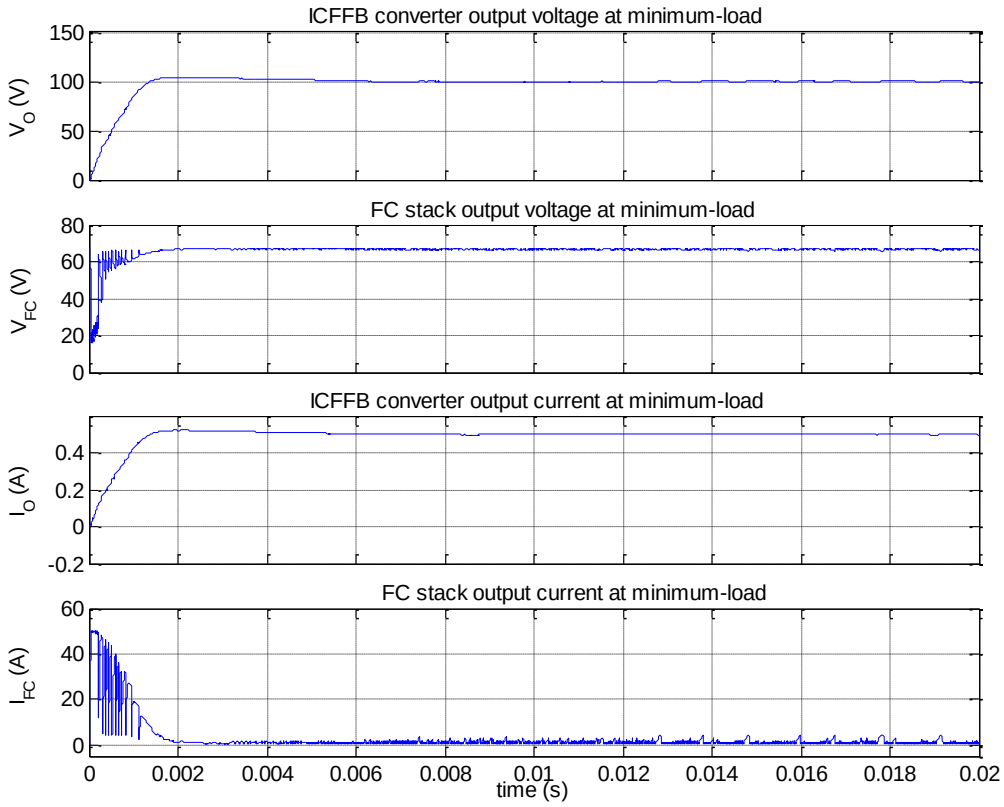


Figure 4.23: The waveforms of the output voltage and the output current of the ICFFB converter and the FC stack with VMFC at minimum-load.

The results in Figure 4.22 and Figure 4.23 show that the mean value of V_O and I_O match the specified design values given in Table 3.1. This validates the discussed characteristic behaviour of feedback control, whereby a system matches the controlled variable to its reference in spite of variations.

Figure 4.24 shows the waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at full-load with VMFC. The converter has a ΔV_O of 0.4 V and a ΔI_O of 39 mA. While the FC stack has a ΔV_{FC} of 1.5 V and a ΔI_{FC} of 5.9 A.

Figure 4.25 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack at minimum-load with VMFC. The converter has a ΔV_O of 2 mV and a ΔI_O of 0.1 mA. While the FC stack has a ΔV_{FC} of 0.5 V and a ΔI_{FC} of 1.7 A.

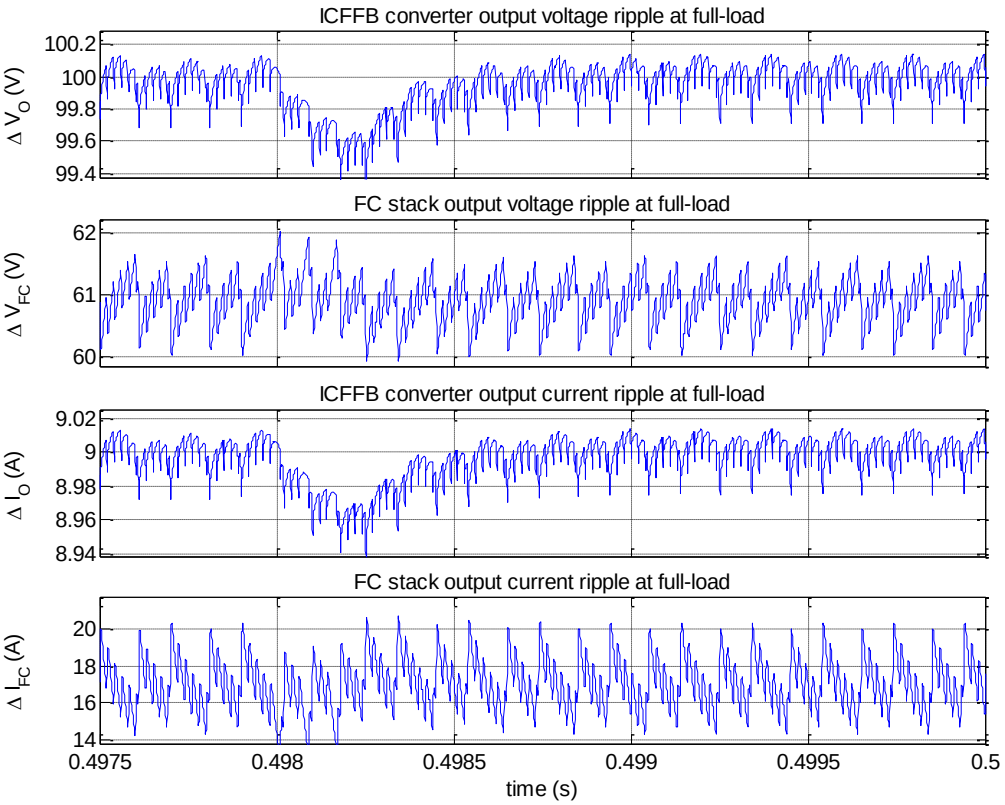


Figure 4.24: The waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack with VMFC at full-load.

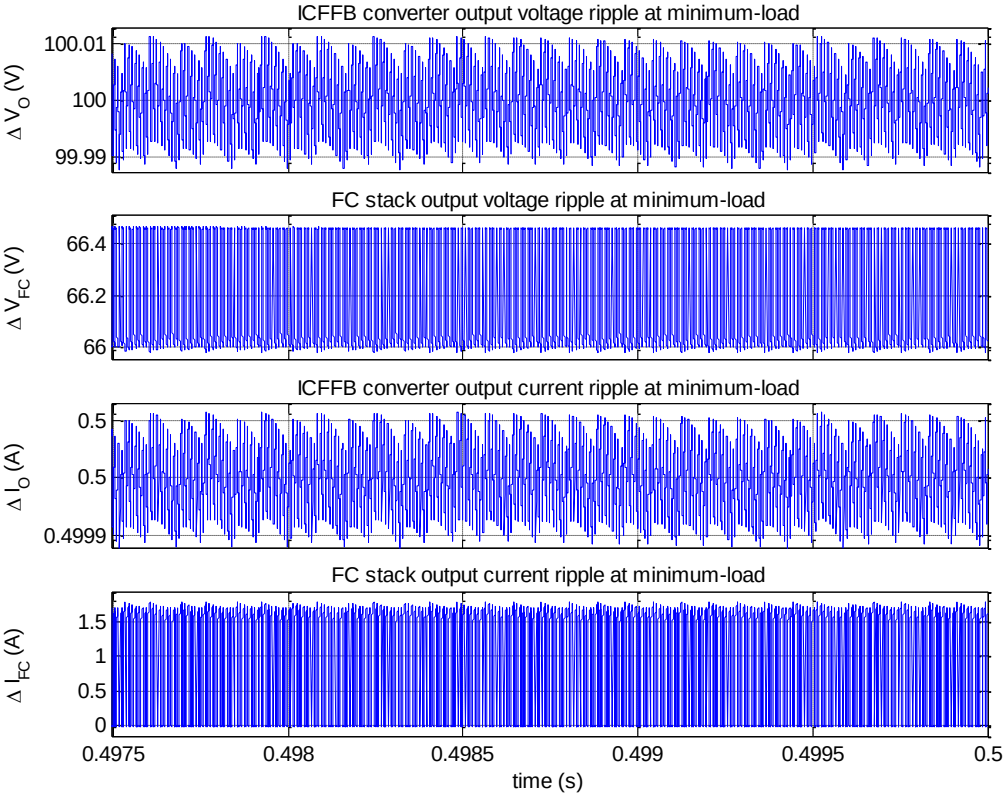


Figure 4.25: The waveforms of the output voltage ripple and the output current ripple of the ICFFB converter and the FC stack with VMFC at minimum-load.

The results in Figure 4.24 and Figure 4.25 indicate that ΔV_O and ΔI_O reduces with VMFC, while ΔV_{FC} increases. On the other hand, ΔI_{FC} increases at full-load and reduces at minimum-load with VMFC.

Figure 4.26 shows the waveforms of the output voltage and the output current of the ICFFB converter and the FC stack in response to load transients. The output voltage and the output current of the converter and the stack stabilise shortly after start-up. Then at 0.25 s, a load transient is introduced by increasing the load resistance, as a result: V_{FC} increases while its ripple content reduces, I_{FC} decreases and develops spikes between 0.25 s and 0.375 s, V_O overshoots and then stabilises again at 100 V and I_O decreases. Another load transient is introduced at 0.45 s, as a result: V_{FC} slightly increases, I_{FC} decreases again and retains high ripple content, V_O overshoots and then stabilises again at 100 V and I_O decreases again.

The results in Figure 4.26 indicate that V_O is stable and remains stable regardless of load transients arising from variations in the load resistance. This is proof that the modelling of the ICFFB converter is valid and that the designed controller works.

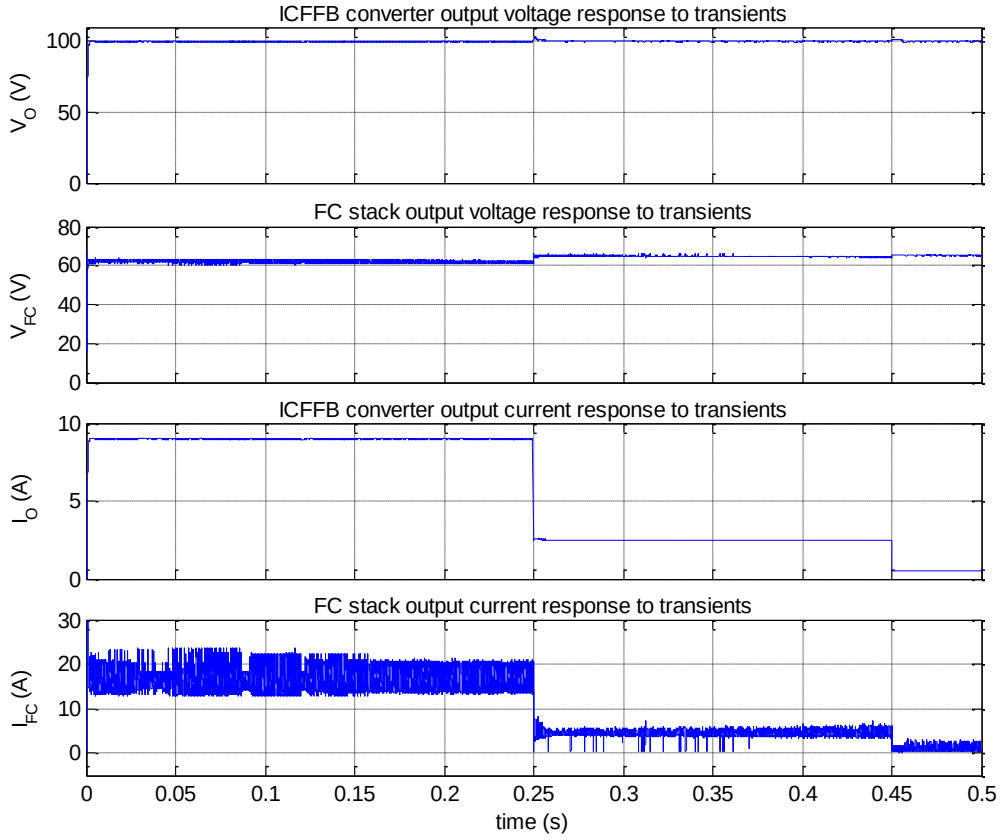


Figure 4.26: The waveforms of the output voltage and the output current of the ICFFB converter and the FC stack in response to load transients.

4.4 Control and Simulation of the Boost Converter

4.4.1 Control of the Boost Converter

Figure 4.27 shows the circuit of the boost converter with open-loop control. The circuit consists of the power stage, the MOSFET gate driver and the pulse width modulator.

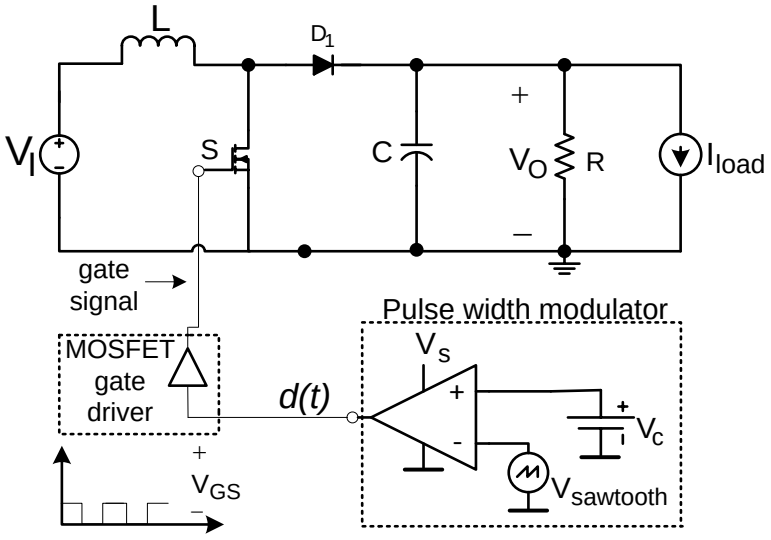


Figure 4.27: The circuit of the boost converter with open-loop control.

Figure 4.28 shows the circuit of the boost converter with VMFC. The circuit consists of the power stage, the feedback network, the pulse-width modulator and the MOSFET gate driver. The functional description of the feedback network, pulse-width modulator and gate driver is similar to that given for the ICFFB converter.

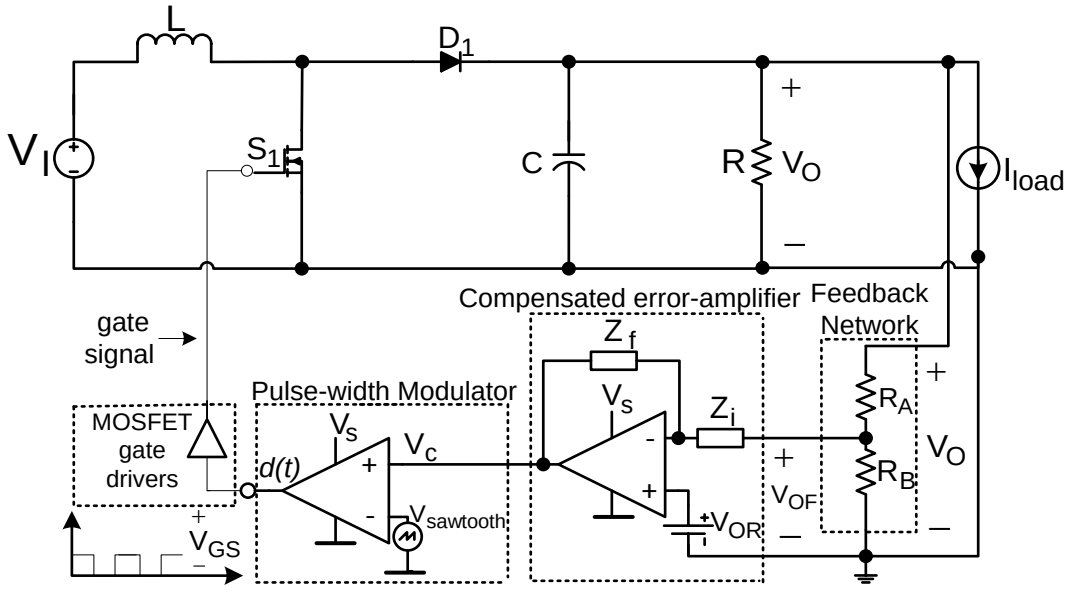


Figure 4.28: The circuit of the boost converter with VMFC.

Table 4.2 shows the parameter and component values for the feedback network, the pulse-width modulator and the compensated EA of the designed boost converter. A

MATLAB code was used to calculate the parameter and component values of the voltage controller and to generate bode-plots of the transfer functions (See Appendix C2: Code for the design of the boost converter controller). The compensated EA was used for the design of a type III voltage controller.

Table 4.2: The parameter and component values for the feedback network, the pulse-width modulator and the compensated EA of the designed boost converter.

Parameter & component list for EA, Voltage FN and Pulse width Modulator		
Component /parameter	Value	comments
V_{tm}	2.5 V	Sawtooth amplitude
V_{OR}	2.5 V	Output voltage reference
R_A, R_B, R_1, R_2, R_3	39 kΩ, 1kΩ, 3.5 MΩ, 3.5 MΩ, 7.66 MΩ	Resistor values for the voltage FN and EA
C_1, C_2, C_3	2.01 nF, 13.16 nF, 801.77 pF	Capacitor values for the EA

4.4.2 Simulation of the boost converter

Figure 4.29 shows the simulation model of the boost converter circuit with open-loop control in Simulink environment. The circuit consists of a FC stack block, an inductor L and it's series resistance r_L, a MOSFET switch, a diode D_1, a capacitor C and it's series resistance r_C, a variable load resistor R, a PWM modulator block and a scope.

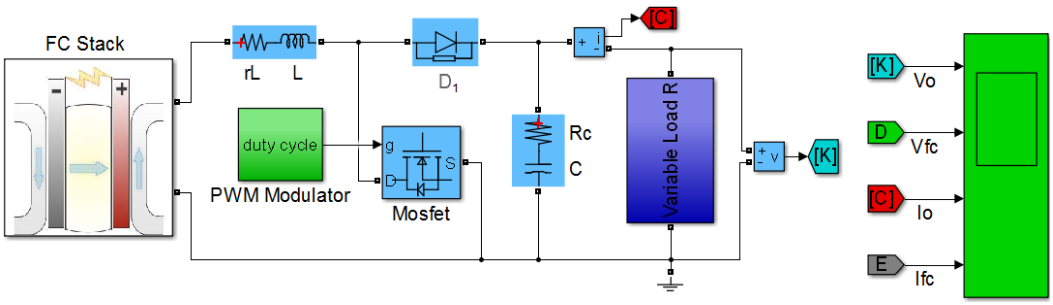


Figure 4.29: The simulation model of the boost converter with open-loop control.

Figure 4.30 shows the bode-plot of the magnitude and the phase of the control-to-output transfer function of the boost converter power stage with open-loop control. The plot indicates that the converter has a GM of 33.4 dB at a frequency of 327 Hz and a PM of $-54.4°$ at a cross over frequency of 7.5 kHz, with a total phase of $-234.4°$. Since the total phase of the control-to-output transfer function of the boost converter exceeds $-180°$ at f_c, the system is unstable. Therefore, compensation for the feedback loop is required in order to ensure stability.

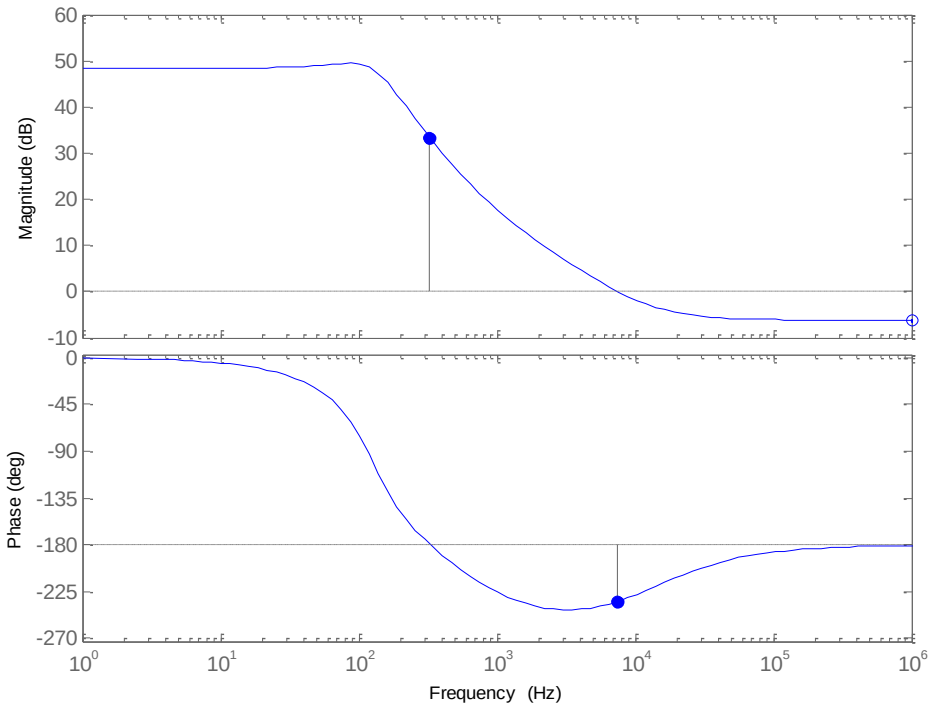


Figure 4.30: The bode-plot of the magnitude and the phase of the control-to-output transfer function of the boost converter power stage with open-loop control.

Figure 4.31 shows the waveforms of the output voltage and the output current of the boost converter and the FC stack at full-load with open-loop control. V_O and I_O steadily increase after start-up and reach their mean value of 95.6 V and 8.6 A in 16 ms. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 36.3 V in 11 ms. While I_{FC} overshoots at start-up, and then steadily decreases and reaches its mean value of 27.5 A at in ms.

Figure 4.32 shows the waveforms corresponding to the output voltage and the output current of the boost converter and the FC stack at minimum-load with open-loop control. V_O and I_O steadily increase after start-up, and reach their mean value of 93.59 V and 0.468 A in 72.5 ms and 65.5 ms respectively. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 58.52 V in 14 ms. While I_{FC} overshoots at start-up and then steadily decreases and reaches its mean value of 0.87 A in 9.5 ms.

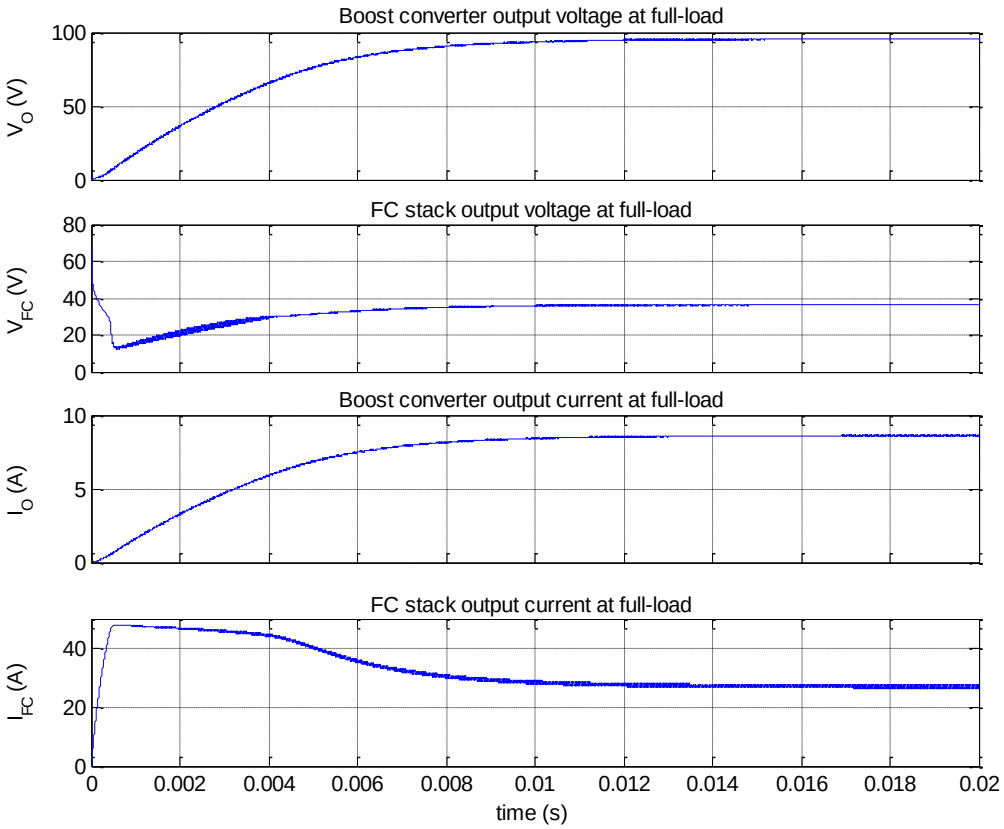


Figure 4.31: The waveforms of the output voltage and the output current of the boost converter and the FC stack at full-load with open-loop control.

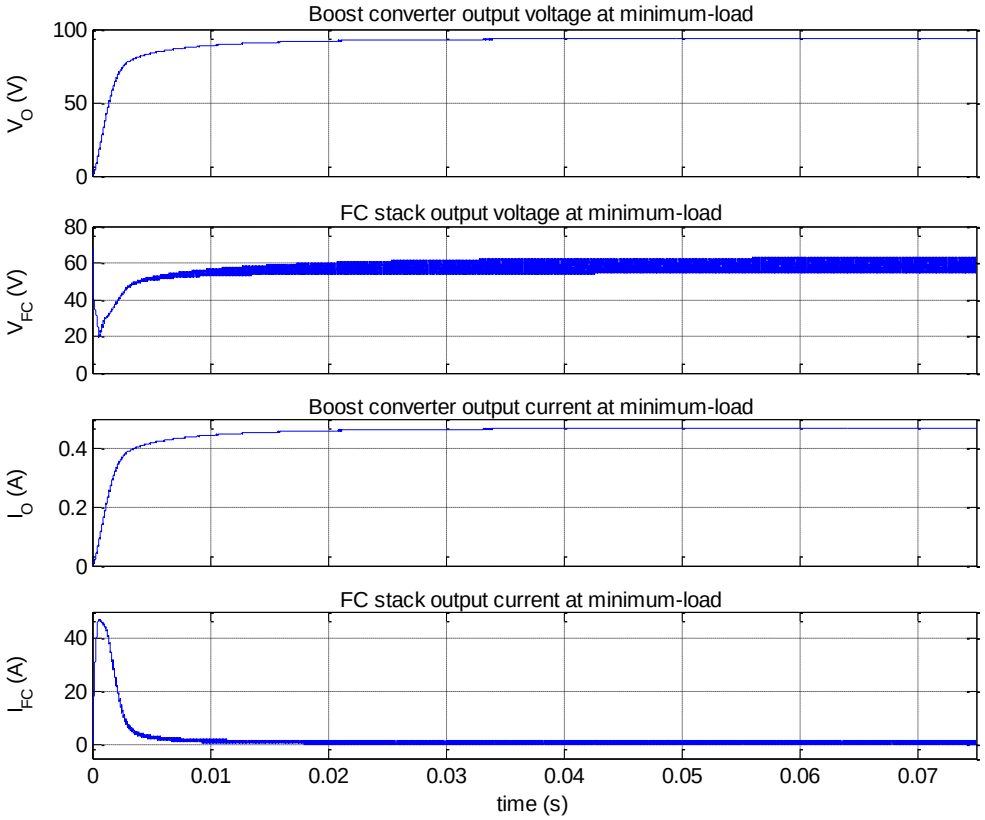


Figure 4.32: The waveforms of the output voltage and the output current of the boost converter and the FC stack at minimum-load with open-loop control.

Figure 4.33 shows the waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at full-load with open-loop control. The converter has a ΔV_O of 0.65 V and a ΔI_O of 55 mA, while the FC stack has a ΔV_{FC} of 0.5 V and a ΔI_{FC} of 1.12 A.

Figure 4.34 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the boost converter and the FC stack at minimum-load with open-loop control. The converter has a ΔV_O of 30 mV and a ΔI_O of 0.20 mA, while the FC stack has a ΔV_{FC} of 8.8 V and a ΔI_{FC} of 1.5 A.

A comparison of the results in Figure 4.33 and Figure 4.34 show that ΔV_O and ΔI_O are greater at full-load, while ΔV_{FC} and ΔI_{FC} are greater at minimum load

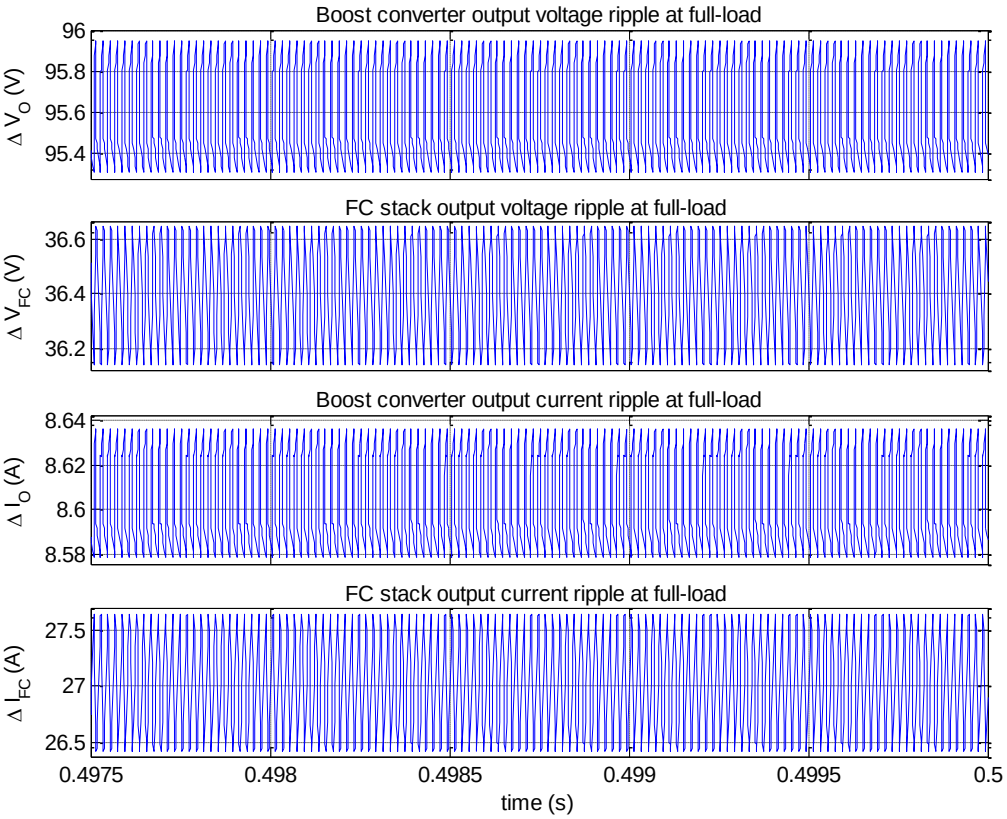


Figure 4.33: The waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at full-load.

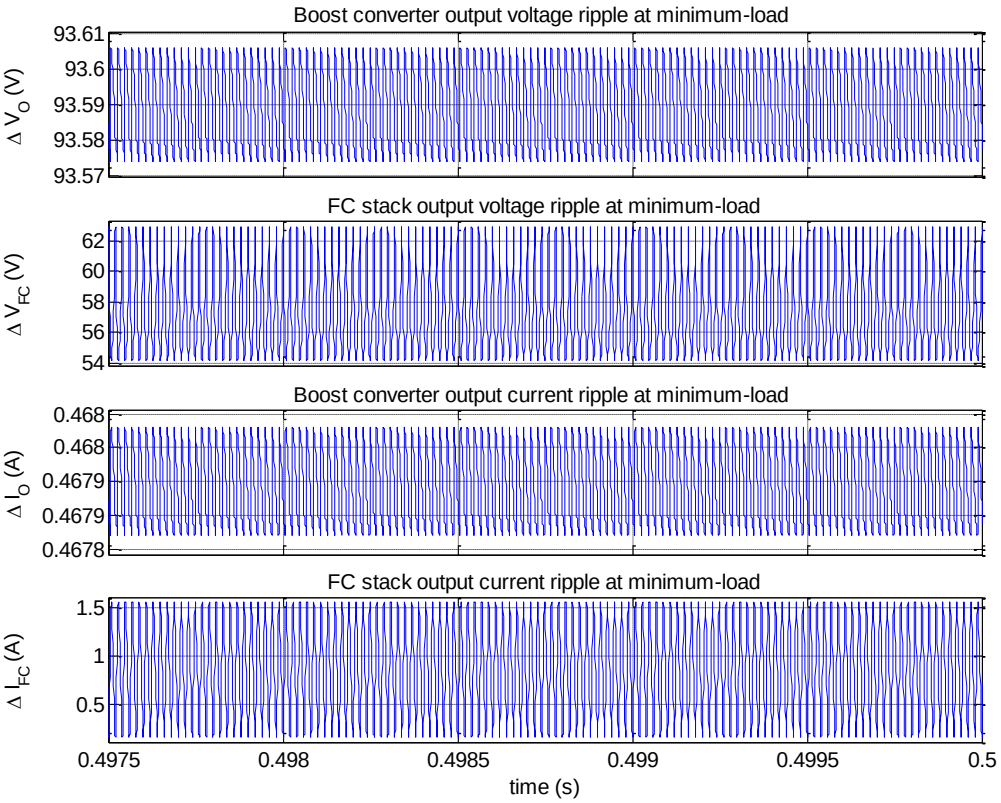


Figure 4.34: The waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at minimum-load.

Figure 4.35 shows the simulation model of the boost converter with VMFC in Simulink environment. The model consists of the power stage and the feedback loop.

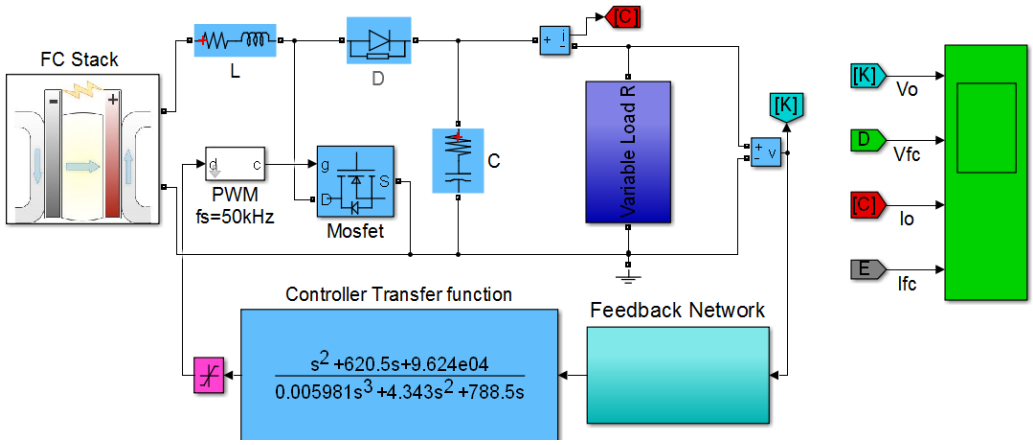


Figure 4.35: The simulation model of the boost converter with VMFC.

Figure 3.35 shows the bode-plot of the magnitude and the phase of the voltage transfer function of the designed and compensated type III EA for the boost converter controller with two zero-pole pairs. The controller has zero-pole pairs at 49.37 Hz and 57.78 Hz, and a cross over frequency at 20.2 Hz with a total PM of $-84°$.

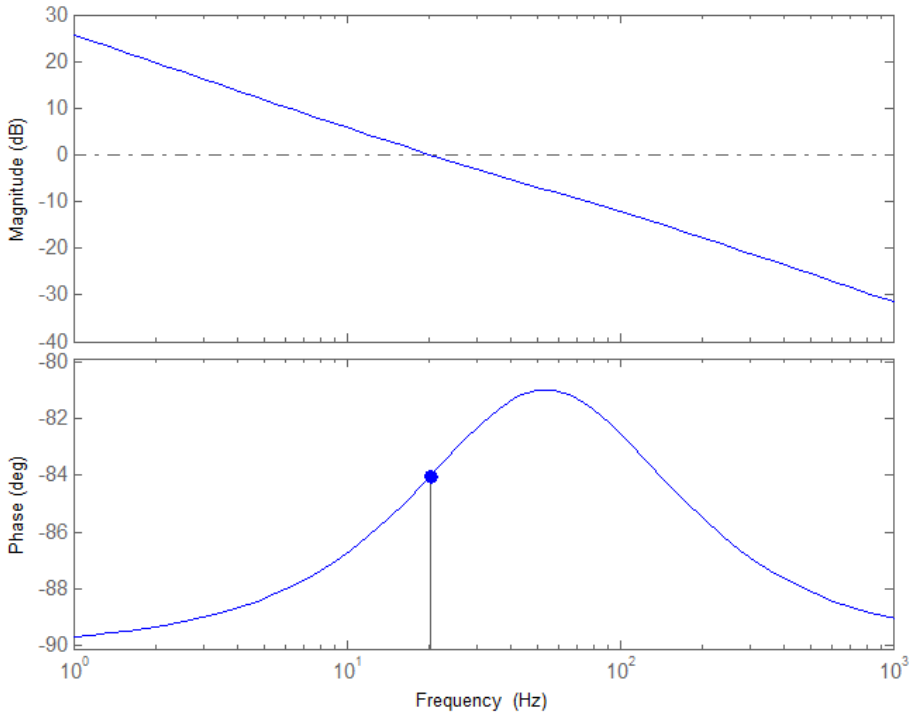


Figure 4.36: The bode-plot of the magnitude and the phase of the voltage transfer function for the designed and compensated type III EA boost converter controller with two zero-pole pairs.

Figure 4.37 shows the bode-plot of the magnitude and the phase of the loop gain for the boost converter. The system has a GM of – 5.27 dB at 122 Hz and a PM of 53.3° at a cross over frequency of 69.1 Hz.

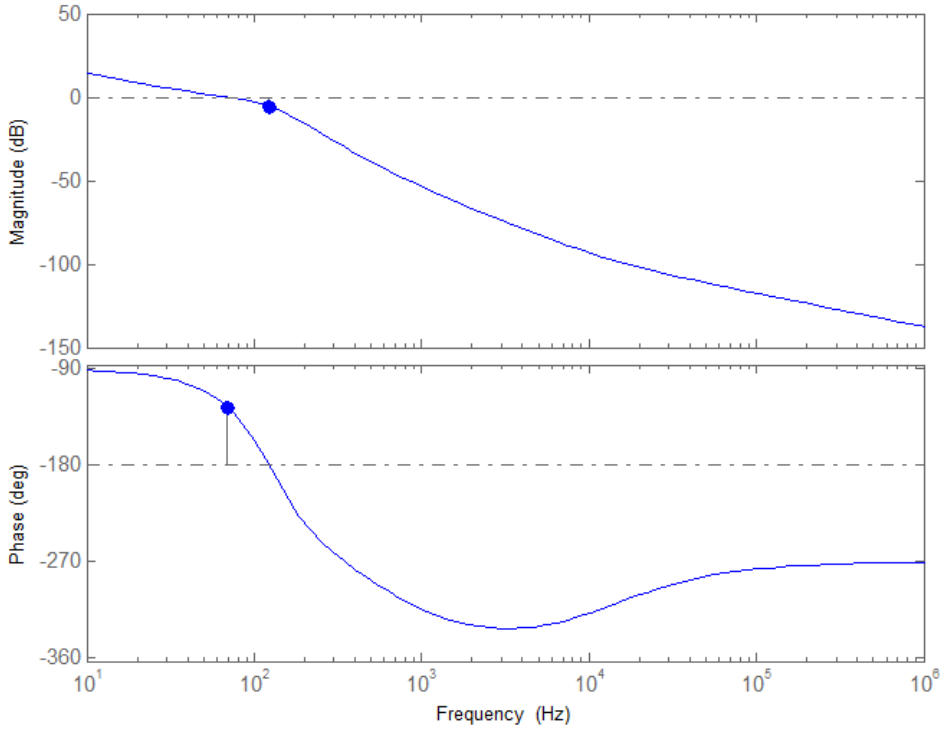


Figure 4.37: The bode-plot of the magnitude and the phase of the loop gain (T) for the boost converter.

Figure 4.38 shows the waveforms of the output voltage and the output current of the boost converter and the FC stack at full-load with VMFC. V_O and I_O steadily increase after start-up and reach their peak value of 81.4 V and 7.1 A in 25 ms, and dip between 2.5 ms and 4 ms, and then they steadily increase and reach their mean value of 100 V and 9 A in 42 ms. On the other hand, V_{FC} dips after start-up and then overshoots, and steadily decreases and reaches its mean value of 62.62 V in 41 ms. While I_{FC} overshoots at start-up and then dips and steadily increases to a peak of 13.2 A and slightly dips again, and then steadily increases again and reaches its mean value of 16.96 A in 41 ms.

Figure 4.39 shows the waveforms of the output voltage and the output current of the boost converter and the FC stack at minimum-load with VMFC. V_O and I_O steadily increase after start-up and reach their mean value of 100 V and 0.5 A in 23 ms and 19 ms. On the other hand, V_{FC} dips after start-up and then steadily increases and reaches its mean value of 65.5 V in 2 ms. While I_{FC} overshoots at start-up, then sharply decreases and becomes discontinuous, and then steadily increases to its mean value of 1 A.

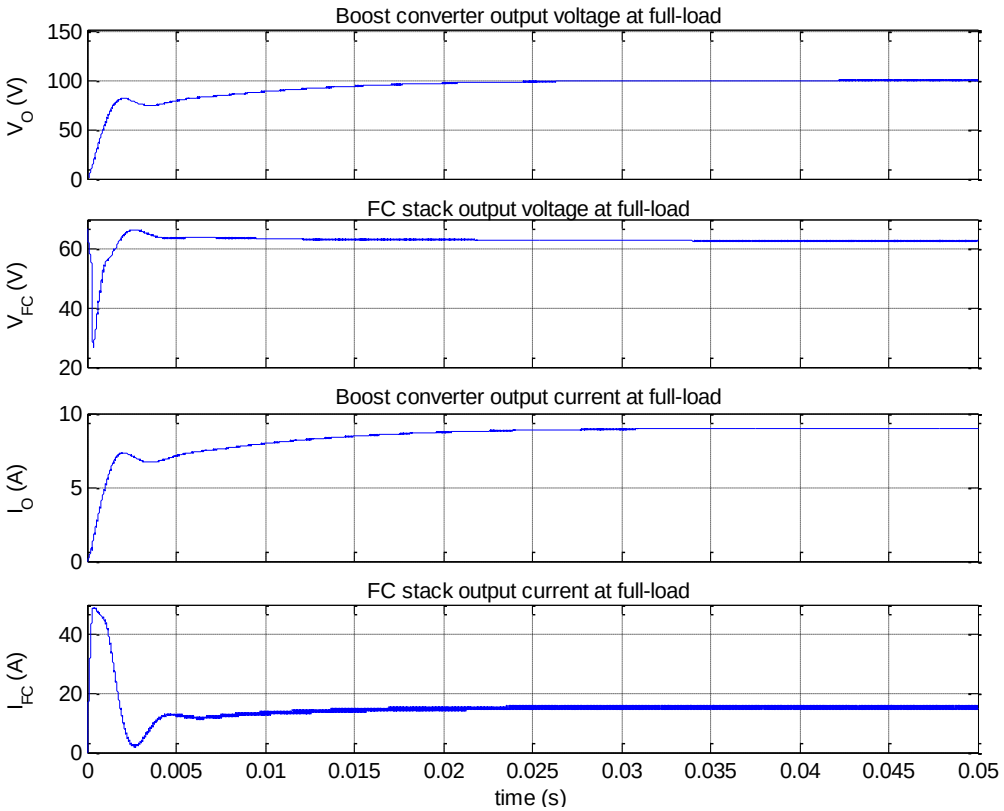


Figure 4.38: The waveforms of the output voltage and the output current of the boost converter and the FC stack at full-load with VMFC.

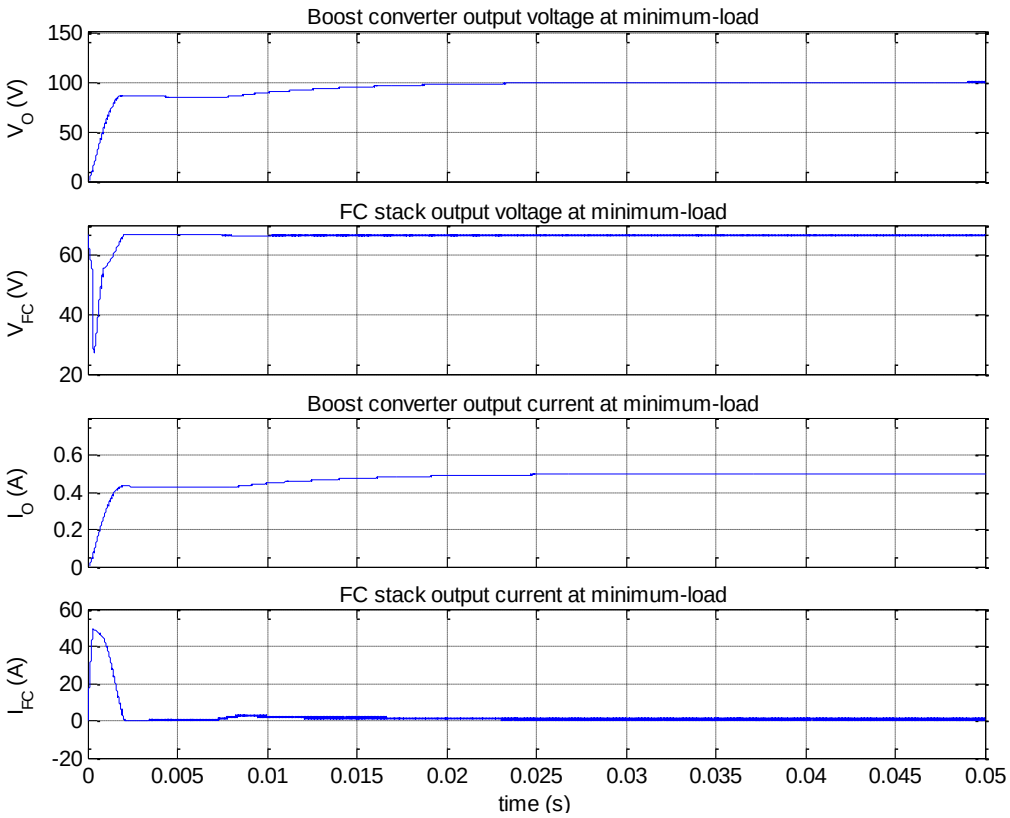


Figure 4.39: The waveforms of the output voltage and the output current of the boost converter and the FC stack at minimum-load with VMFC.

Figure 4.40 shows the waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at full-load with VMFC. The converter has a ΔV_O of 0.4 V and a ΔI_O of 33 mA, while the FC stack has a ΔV_{FC} of 0.38 V and a ΔI_{FC} of 1.49 A.

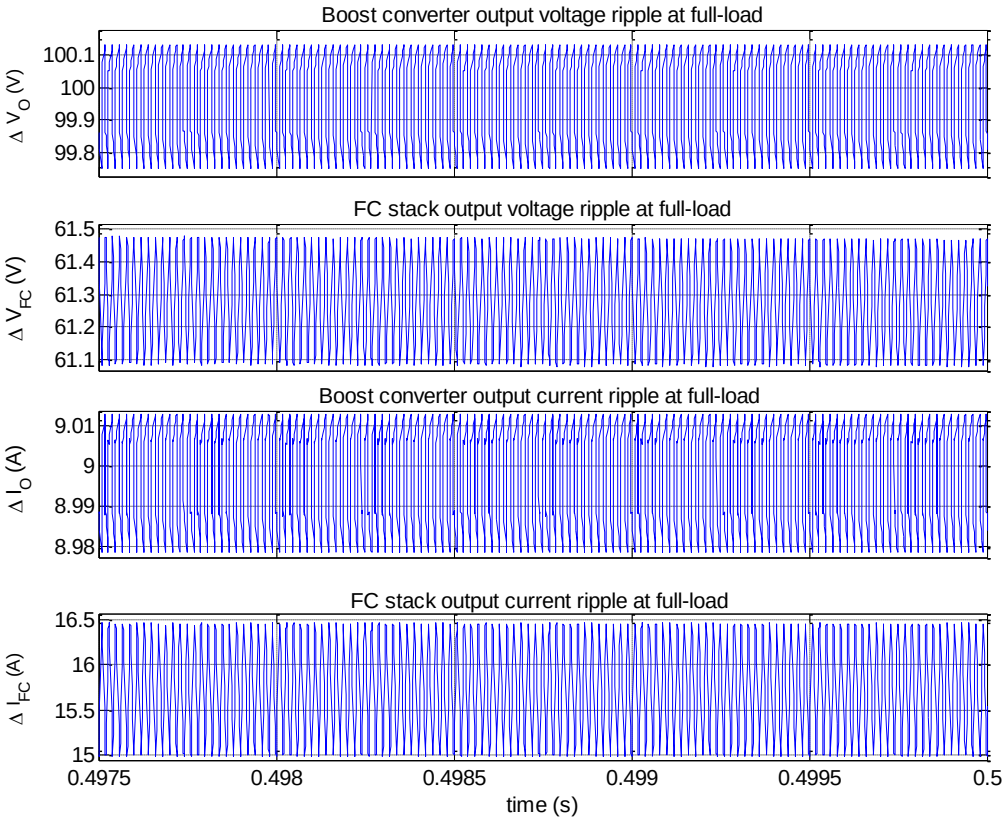


Figure 4.40: The waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at full-load with VMFC.

Figure 4.41 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the boost converter and the FC stack at minimum-load with VMFC. The converter has a ΔV_O of 30 mV and a ΔI_O of 60 mA, while the FC stack has a ΔV_{FC} of 0.35 V and a ΔI_{FC} of 1.3 A.

Figure 4.42 shows the waveforms of the output voltage and the output current of the boost converter and the FC stack in response to load transients. The output voltage and the output current of the converter and the FC stack stabilise shortly after start-up. Then at 0.25 s, a load transient is introduced, as a result: V_{FC} increases, I_{FC} decreases, V_O slightly overshoots and then stabilises again at 100 V and I_O decreases. Another load transient is introduced at 0.45 s, as a result: V_{FC} increases slightly, I_{FC} decreases again, V_O slightly overshoots and then stabilizes at 100 V again and I_O decreases again.

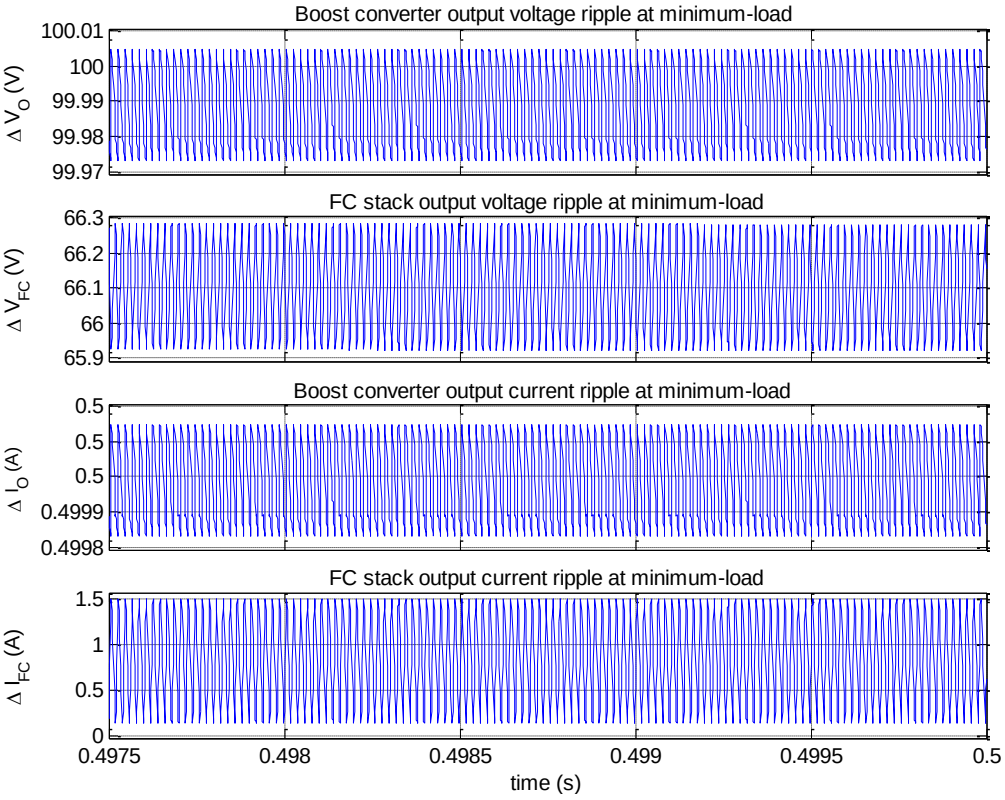


Figure 4.41: The waveforms of the output voltage ripple and the output current ripple of the boost converter and the FC stack at minimum-load with VMFC.

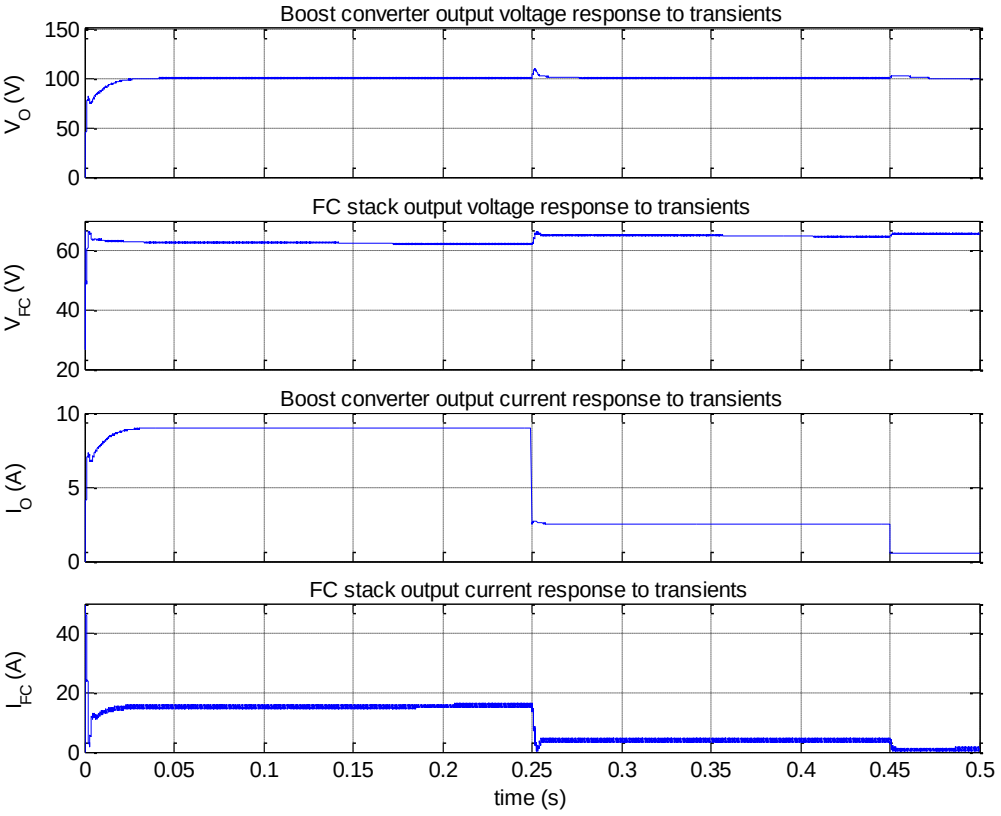


Figure 4.42: The waveforms of the output voltage and the output current of the boost converter and FC stack in response to load transients.

4.5 Control and Simulation of the Sepic Converter

4.5.1 Control of the Sepic Converter

Figure 4.43 shows the circuit of the sepic converter with open-loop control. The circuit consists of the power stage, the MOSFET gate driver and the pulse width modulator.

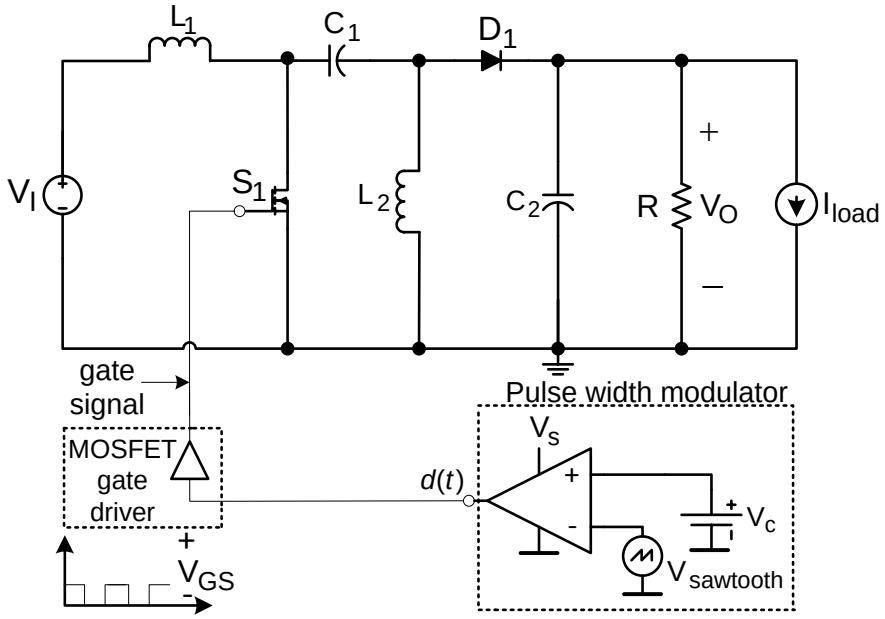


Figure 4.43: The circuit of the sepic converter with open-loop control.

Figure 4.44 shows the circuit of the sepic converter with PCMFC. The circuit consists of the power stage, the feedback network, the compensated EA and the pulse width modulator. The pulse width modulator constitutes an S-R latch, a clock, ramp voltage V_{ramp} and a comparator. In PCMFC, both the output voltage and the inductor peak current are sampled. The feedback network samples the output voltage while the sense resistor R_i samples the total inductors peak current. The compensated EA produces a compensated error voltage V_c and then feeds it to the modulator. At the modulator: V_{ramp} compensates for sub-harmonic oscillations prevalent in V_{sense}, the clock sets the latch to initiate the switching of the gate driver, the comparator compares V_c with V_{sense} and whenever V_{sense} is greater than V_c it resets the latch and ultimately the switch. Once V_{sense} is less than V_c, the clock sets the latch again and the process repeats indefinitely.

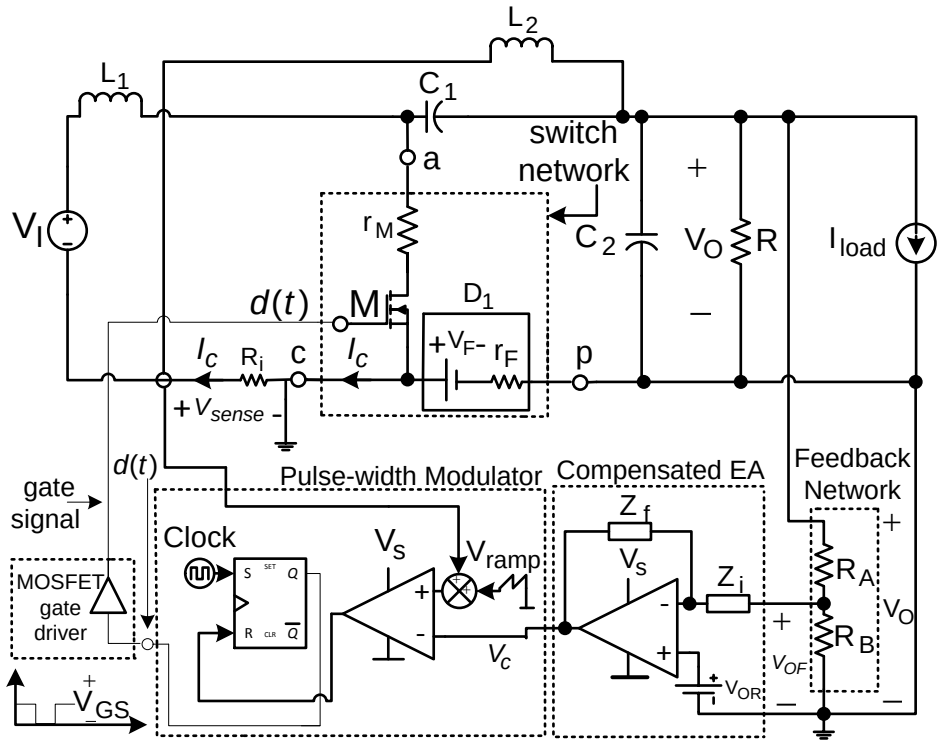


Figure 4.44: The circuit of the sepic converter with PCMFC.

Table 4.3 shows the parameter and component values for the feedback network, pulse-width modulator and compensated EA of the designed sepic converter controller. A MATLAB code was used to calculate the parameter and component values of the controller and to generate bode-plots of the transfer functions (See Appendix C3: Code for the design of the sepic converter controller). The compensated EA was used for the design of a type II voltage controller and an S-R latch and a comparator with a compensated V_{sense} was used for the design of the peak current controller.

Table 4.3: The parameter and component values for the feedback network, the pulse width modulator and the compensated EA of the designed sepic converter controller.

Parameter & component list for EA, Voltage FN and Pulse width Modulator		
Component /parameter	Value	comments
V_{tm}	2.5 V.	Sawtooth amplitude
V_{ref} & V_{sense}(max)	2.5 V.	Output voltage reference and sensed inductor-current voltage
R_i	0.0833 Ω	Current sense resistor
R_A, R_B, Rcomp, R_{fb1}	39kΩ, 1kΩ, 1kΩ, 39MΩ	Resistor values for the voltage FN and EA
C_{comp}, C_{hf}	61.21 nF, 11.78 nF	Capacitor values for the EA.

4.5.2 Simulation of the Sepic Converter Circuit Models

Figure 4.45 shows the simulation model of the sepic converter with open-loop control in Simulink environment. The model consists of a FC stack, an input inductor L_1 and its series resistance r_{L1}, a coupling capacitor C_1 and its series resistance r_{C1}, an output inductor L_2 and its series resistance r_{L2}, a PWM switch, an output capacitor C_2 and its series resistance r_{C2}, a variable load resistor R and a scope. The switching elements: the MOSFET and the diode are replaced with the PWM SWITCH model

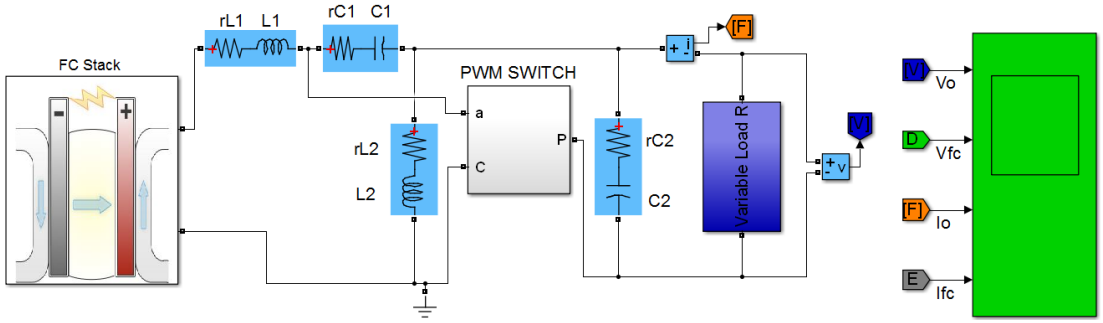


Figure 4.45: The simulation model of the sepic converter with open-loop control.

Figure 4.46 shows the bode-plot of the magnitude and the phase of the control-to-output transfer function of the sepic converter power stage with open-loop control. The plot indicates a DC gain of 55.6 dB, two resonant peaks at 81 Hz and 441 Hz and a large phase delay after the second resonant frequency with a total phase delay of $794°$. Controlling the converter beyond the second resonant frequency would be impossible, because of the large phase delay. The complex poles and the complex zeros of the transfer function cause the large phase delay. Large phase delay is an intrinsic characteristic of the control-to-output transfer function of the sepic converter topology, and this presents a huge challenge when considered from a control perspective, especially when using a voltage mode controller. When the phase delay is too large, a voltage mode controller is inadequate to perform the required output voltage regulation due to its limited phase boost function. In such cases, the alternative is to use a current mode controller, which consists of a voltage controller and a current controller.

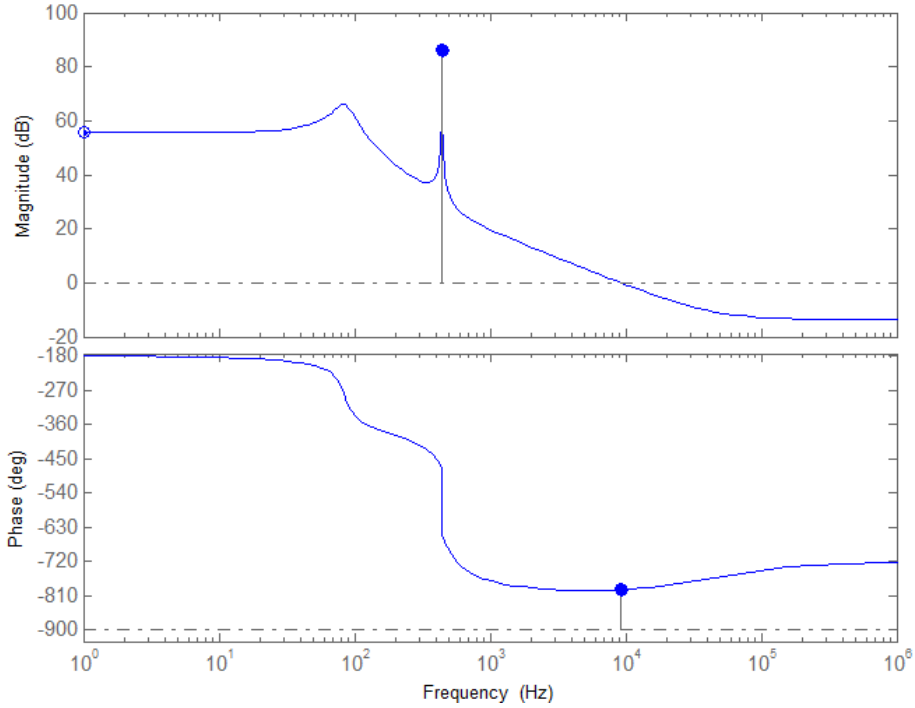


Figure 4.46: The bode-plot of the magnitude and the phase of the control-to-output transfer function of the sepic converter power stage with open-loop control.

Figure 4.47 shows the bode-plot of the magnitude and the phase of the control-to-output transfer function of the sepic converter power stage with peak current control. The plot exhibits low magnitude at low frequencies, high magnitude beyond the converter switching frequency and a smaller phase compared to that of the control-to-output transfer function with open-loop control.

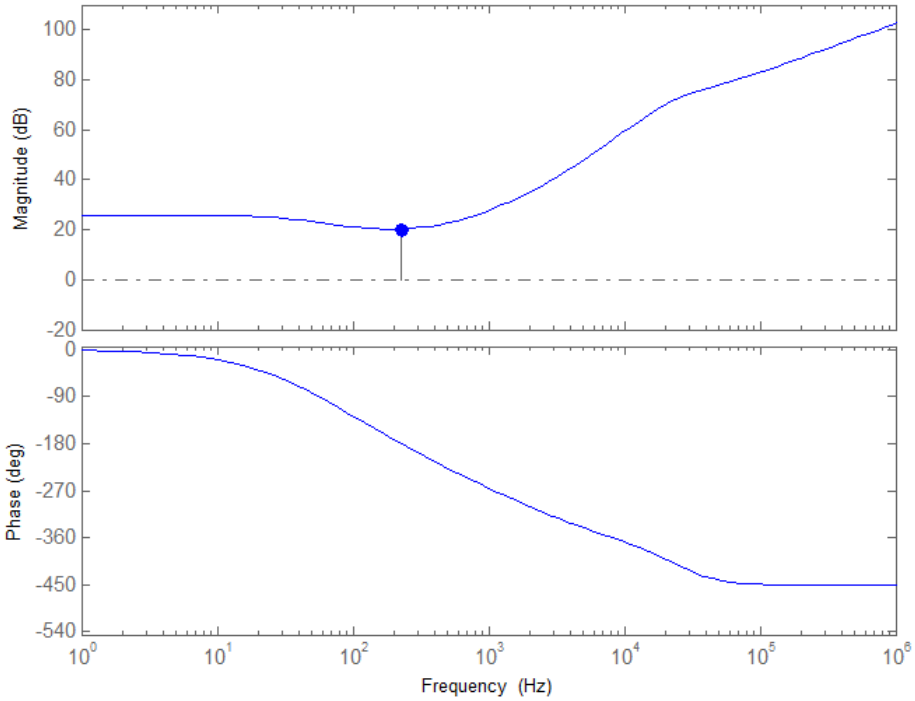


Figure 4.47: The bode-plot of the magnitude and the phase of the control-to-output transfer function of the sepic converter power stage with peak current control.

Figure 4.48 shows the waveforms of the output voltage and the output current of the sepic converter and the FC stack at full-load with open-loop control. V_O and I_O steadily increase after start-up and reach their mean value of 90.7 V and 8.17 A in 8 ms. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 37.1 V in 10 ms. While I_{FC} overshoots at start-up, and then steadily decreases with minor oscillations and reaches its mean value of 25.4 A in 15 ms.

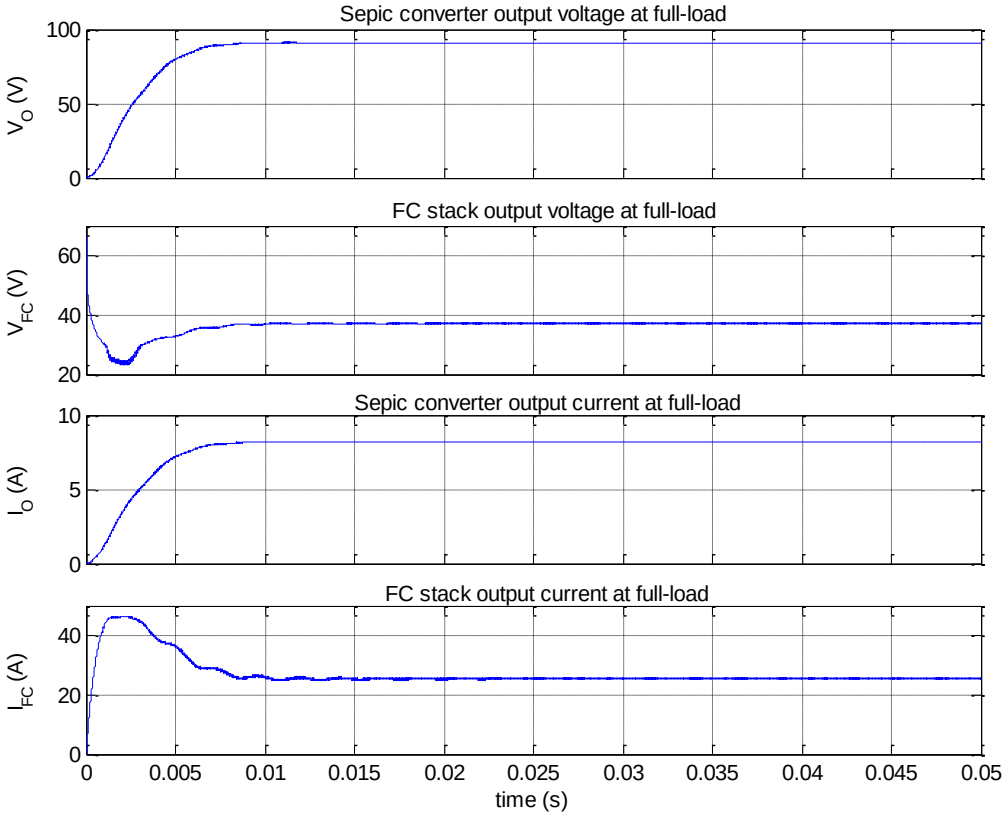
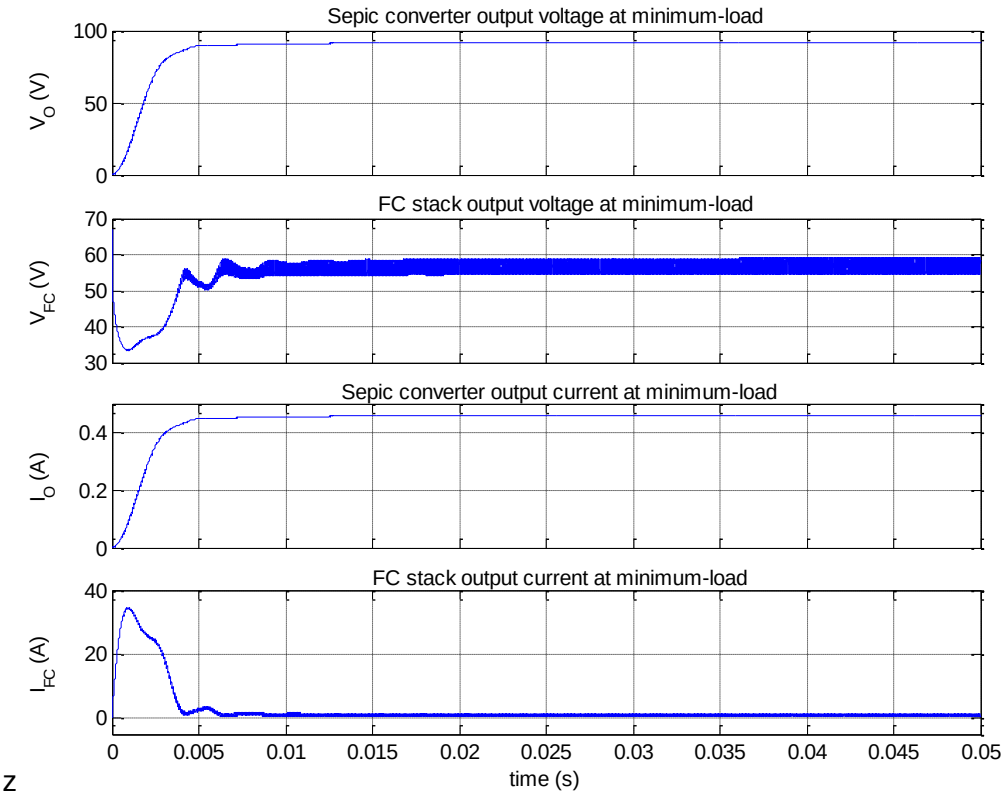


Figure 4.48: The waveforms of the output voltage and the output current of the sepic converter and the FC stack at full-load with open-loop control.

Figure 4.49 shows the waveforms corresponding to the output voltage and the output current of the sepic converter and the FC stack at minimum-load. V_O and I_O steadily increase after start-up and reach their mean value of 91.5 V and 0.46 A in 12.5 ms and 7 ms respectively. On the other hand, V_{FC} sharply drops after start-up, then steadily increases and oscillates between 4 ms and 8ms, and then reaches its mean value of 57 V in 10 ms. While I_{FC} overshoots at start-up, then sharply decreases and oscillates between 4 ms and 8 ms and then reaches its mean value of 1 A in 10 ms.



z

Figure 4.49: The waveforms of the output voltage and the output current of the FC stack and the sepic converter at minimum-load with open-loop control.

Figure 4.50 shows the waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack at full-load with open-loop control. The converter has a ΔV_O of 0.46 V and a ΔI_O of 40 mA, while the FC stack has a ΔV_{FC} of 0.3 V and a ΔI_{FC} of 0.7 A.

Figure 4.51 shows the waveforms corresponding to the output voltage and the output current of the sepic converter and the FC stack at minimum-load with open-loop control. The converter has a ΔV_O of 20 mV and a ΔI_O of 0.1 mA, while the FC stack has a ΔV_{FC} of 4.8 V and ΔI_{FC} of 0.7 A.

A comparison of the results in Figure 4.50 and Figure 4.51 indicates that ΔV_{FC} and ΔI_{FC} are greater at minimum-load, while ΔV_O and ΔI_O are greater at full-load.

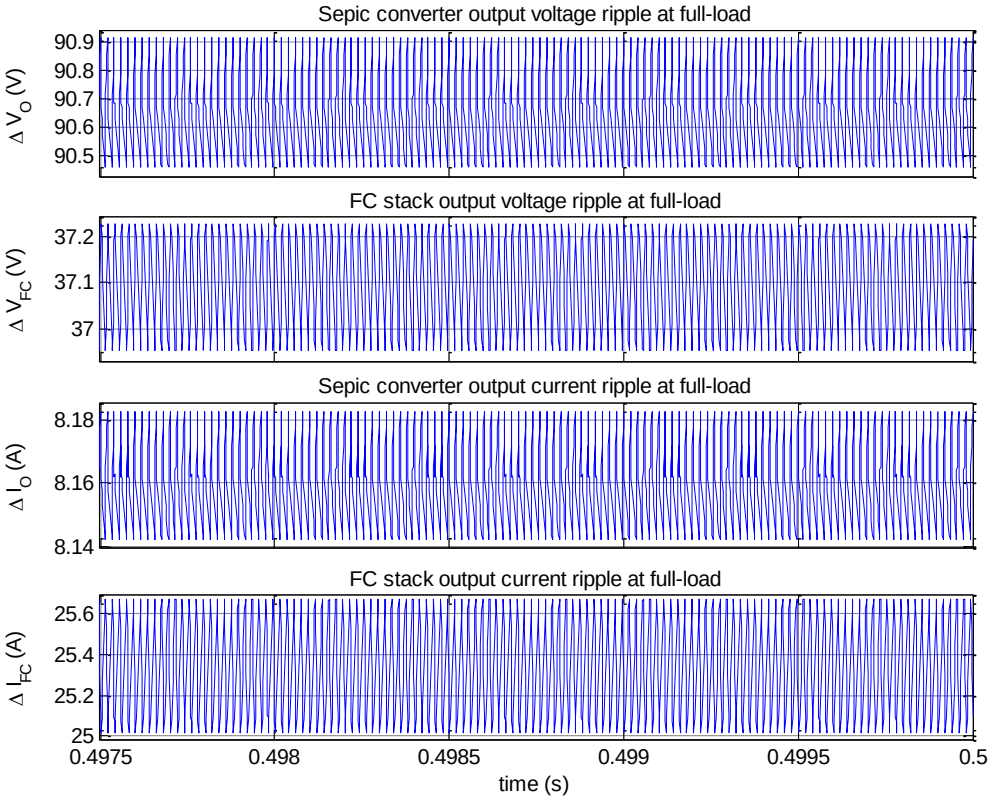


Figure 4.50: The waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack at full-load with open-loop control.

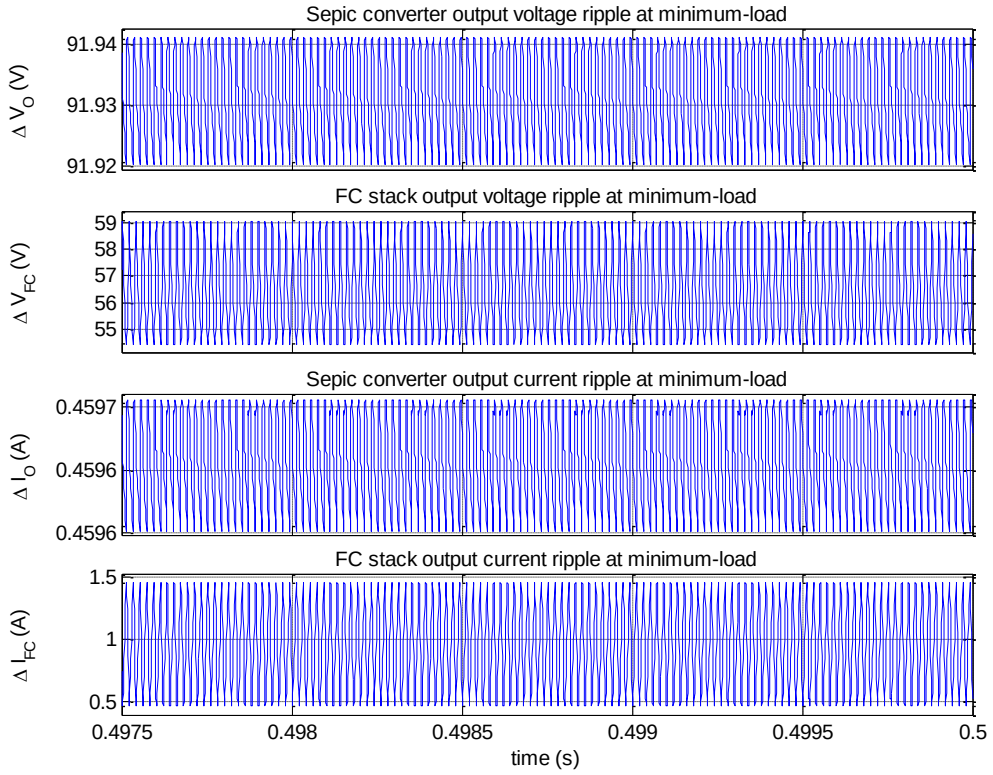


Figure 4.51: The waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack with open-loop control at minimum-load.

Figure 4.52 shows the simulation model of the sepic converter with PCMFC in Simulink environment. The model consists of the power stage, the voltage and current feedback loops.

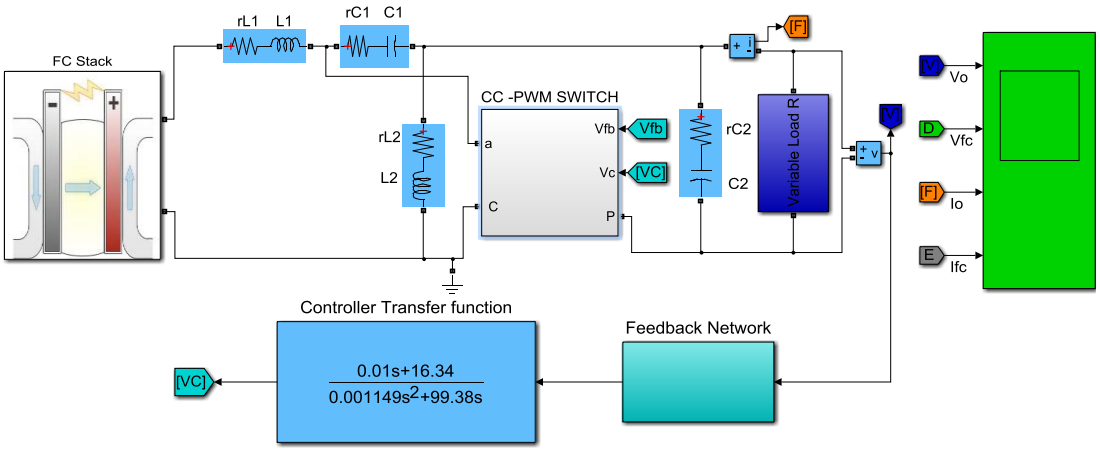


Figure 4.52: The simulation model of the sepic converter with PCMFC.

Figure 4.53 shows the bode-plot of the magnitude and the phase of the voltage transfer function of the designed and compensated type II EA for the sepic converter controller with a single zero-pole pair. The controller has a single zero-pole pair at 260 Hz and 13.77 kHz, a cross over frequency at 1.89 kHz and a total PM of $-15.7°$.

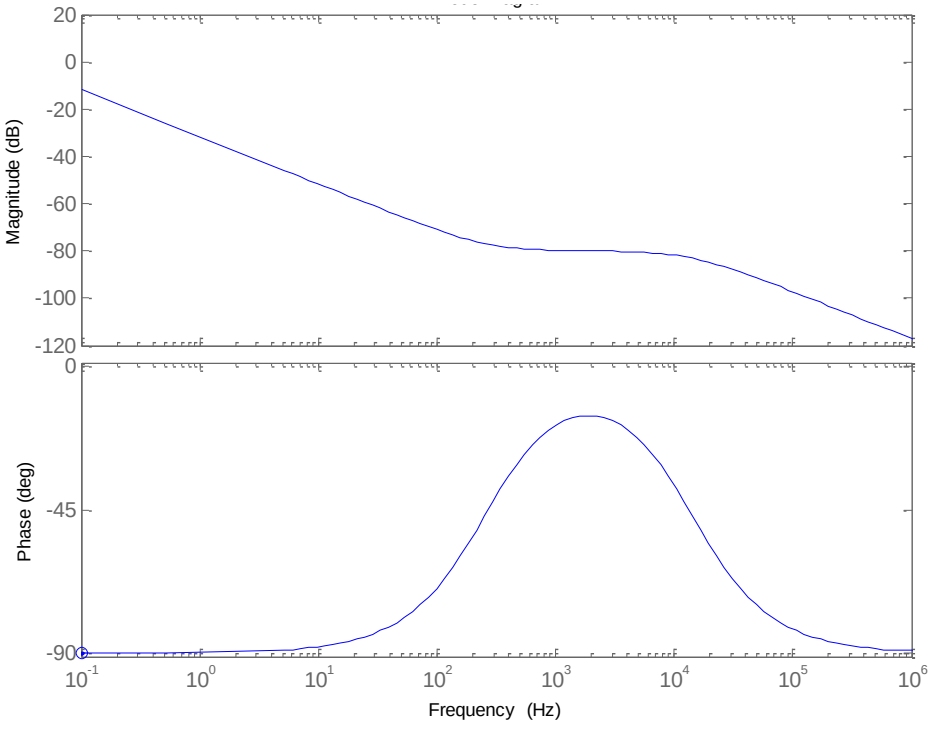


Figure 4.53: The bode-plot of the magnitude and the phase of the voltage transfer function for the designed and compensated type II EA for the sepic converter controller with a zero-pole pair.

Figure 4.54 shows the bode-plot of the magnitude and the phase of the loop gain (T) for the sepic converter. The system has a GM of – 46.2 dB at 70.8 Hz and a PM of $89.1°$ at 0.518 Hz.

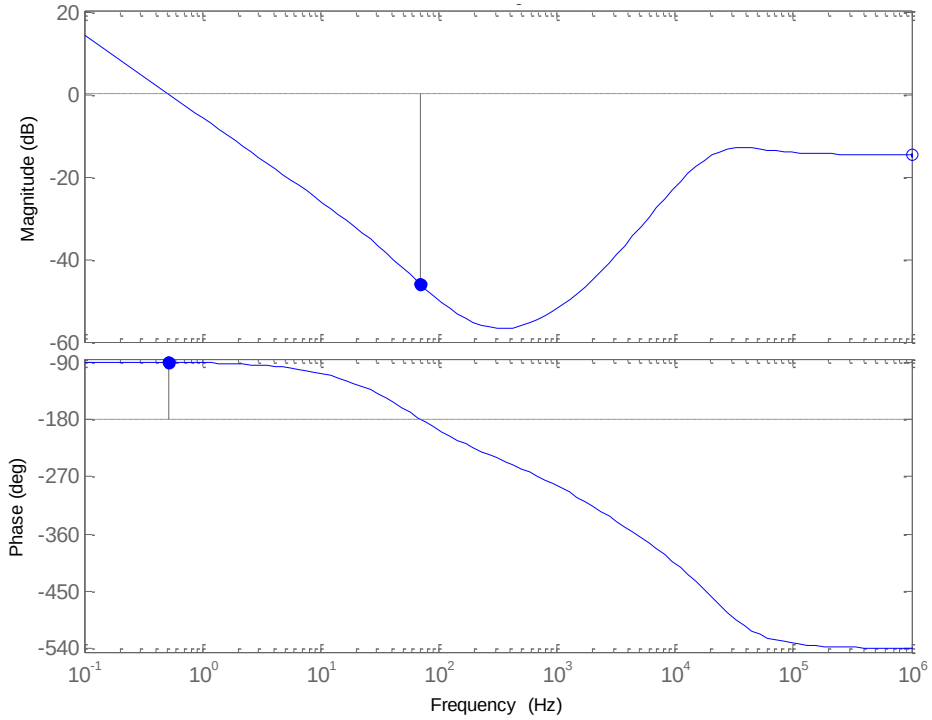


Figure 4.54: The bode plot of the magnitude and the phase for the loop gain (T) of the sepic converter.

Figure 4.55 shows the waveforms of the output voltage and the output current of the sepic converter and the FC stack at full-load with PCMFC. V_O and I_O sharply increase after start-up and then dip between 0.65 ms and 14 ms, and steadily increase again and reach their mean value of 100 V and 9 A in 750 ms. On the other hand, V_{FC} is stable after start-up, and then at 14 ms steadily decreases and reaches its mean value of 59 V in 960 ms. While I_{FC} sharply overshoots at start-up and becomes discontinuous between 0.11 ms and 2 ms, and then steadily increases and reaches its mean value of 18.5 A in 440 ms. The initial dip in V_O and I_O is due to the input inductor zero, which causes the output of the system to go in the oppose direction when a control command is initially issued.

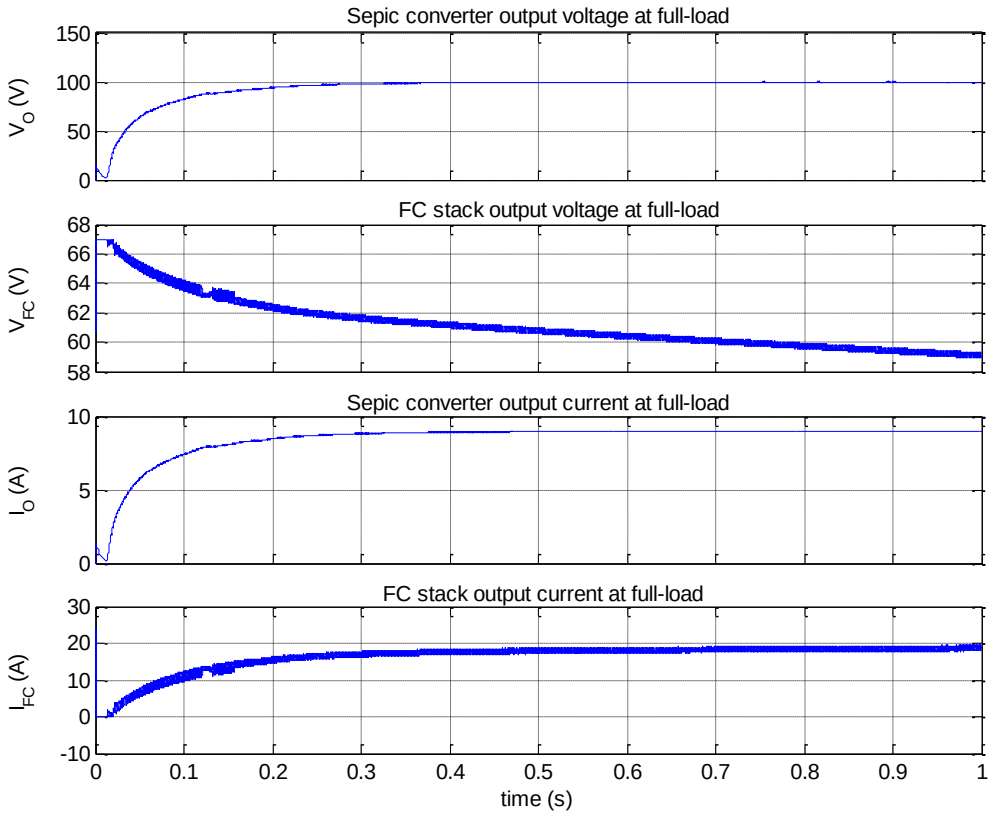


Figure 4.55: The waveforms of the output voltage and the output current of the FC stack and the sepic converter at full-load with PCMFC.

Figure 4.56 shows the waveforms corresponding to the output voltage and the output current of the sepic converter and the FC stack at minimum-load with PCMFC. V_O and I_O steadily increase after start-up and stabilise between 0.2 ms and 15 ms, and then steadily increase again and reach their mean value of 100 V and 0.5 A in 34.2 ms. On the other hand, V_{FC} dips after start-up and stabilises between 0.3 ms and 15 ms, and then oscillates between 20 ms and 34ms and reaches its mean value of 65.5 V in 34.2 ms. While I_{FC} overshoots at start-up, then sharply drops and becomes discontinuous between 0.3 ms and 15 ms, and then steadily increases with oscillations between 20 ms and 34 ms and reaches its mean value of 0.8 A in 34.2 ms.

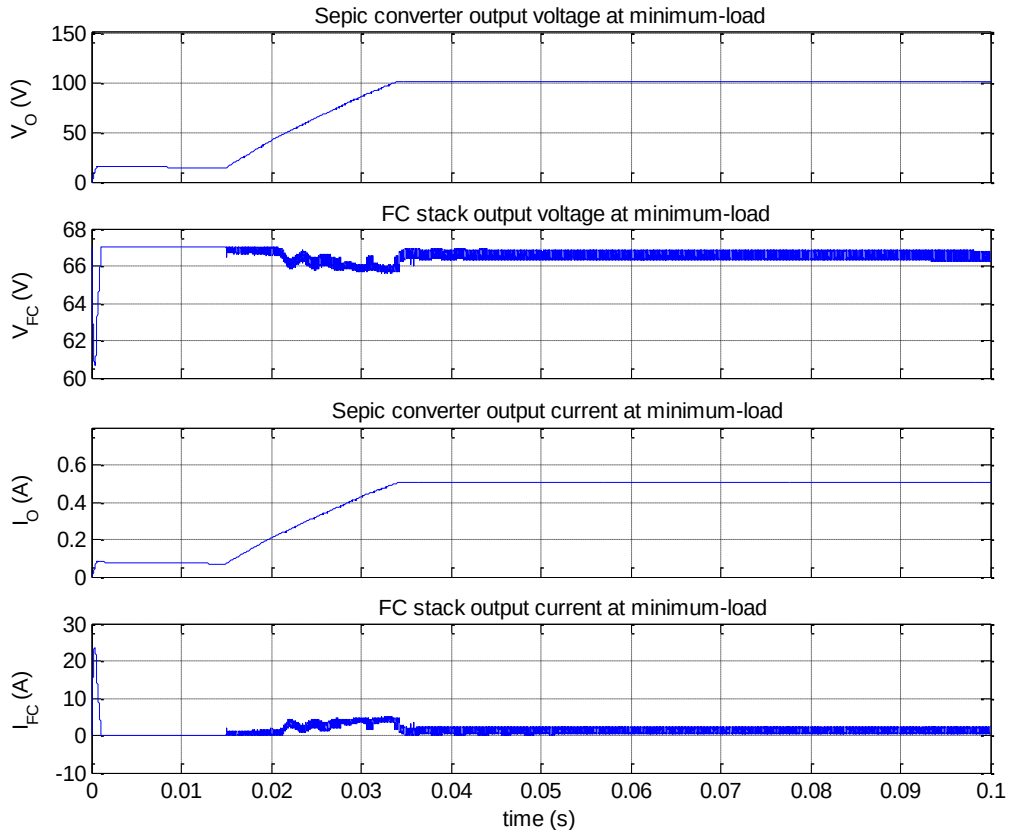


Figure 4.56: The waveforms of the output voltage and the output current of the sepic converter and the FC stack at minimum-load with PCMFC.

A comparison of the results in Figure 4.55 and Figure 4.56 indicate that V_O is stabilised at 100 V. The results also indicate that the system has high ripple content and poor response dynamics at minimum-load than at full-load.

Figure 4.57 shows the waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack at full-load with PCMFC. The converter has a ΔV_O of 1 V and a ΔI_O of 92 mA, while the FC stack has a ΔV_{FC} of 1.5 V and a ΔI_{FC} of 4.5 A.

Figure 4.58 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the sepic converter and the FC stack at minimum-load with PCMFC. The converter has a ΔV_O of 2 mV and a ΔI_O of 0.1 mA, while the FC stack has a ΔV_{FC} of 0.3 V and a ΔI_{FC} of 1 A.

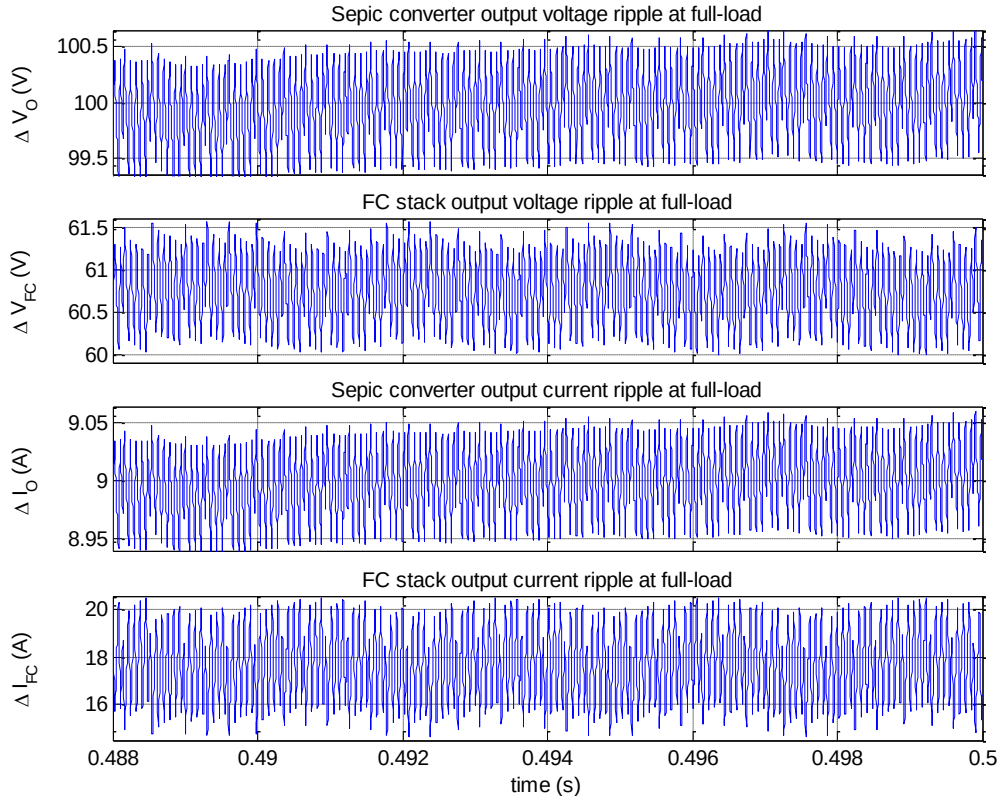


Figure 4.57: The waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack at full-load with PCMFC.

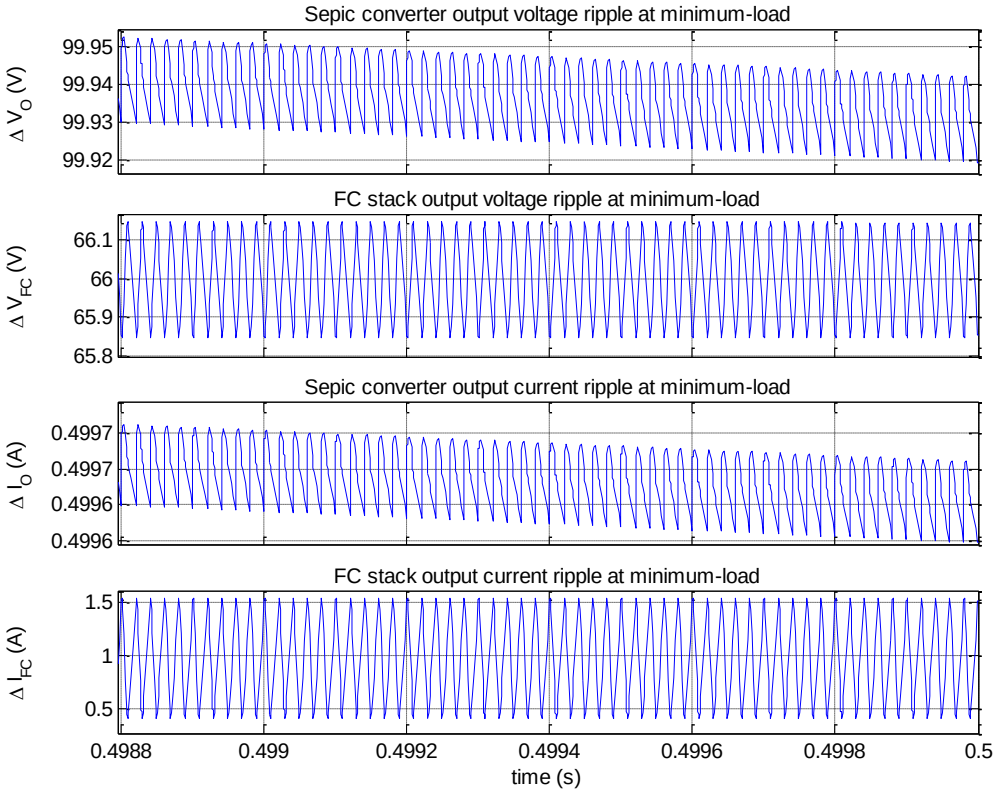


Figure 4.58: The waveforms of the output voltage ripple and the output current ripple of the sepic converter and the FC stack at minimum-load with PCMFC.

A comparison of the results in Figure 4.57 and Figure 4.58 indicate that ΔV_O and ΔI_O reduce with PCMFC. On the other hand, ΔI_{FC} and ΔV_{FC} increase at full-load while ΔV_{FC} decreases and ΔI_{FC} increases at minimum-load with PCMFC.

Figure 4.59 shows the waveforms of the output voltage and the output current of the sepic converter and the FC stack in response to load transients. V_O and I_O stabilise at 100 V and 9 A in 34 ms after start-up regardless of variations in V_{FC}. At 0.75 s, a load transient is introduced, as a result: V_O slightly overshoots and then stabilises at 100.1 V, I_O decreases and stabilises at 2.5 A, V_{FC} increases and develops high ripple content and I_{FC} decreases and develops high ripple content. At 0.9 s, another load transient is introduced, as a result: V_O slightly overshoots and stabilises at 100.1 V again, I_O decreases again and stabilises at 0.5 A, V_{FC} increases and retains high ripple content and I_{FC} decreases and retains high ripple content.

The results in Figure 4.59 indicate that V_O is stable regardless of load transients. This is proof that the modelling of the sepic converter is valid and that the designed PCMFC controller works.

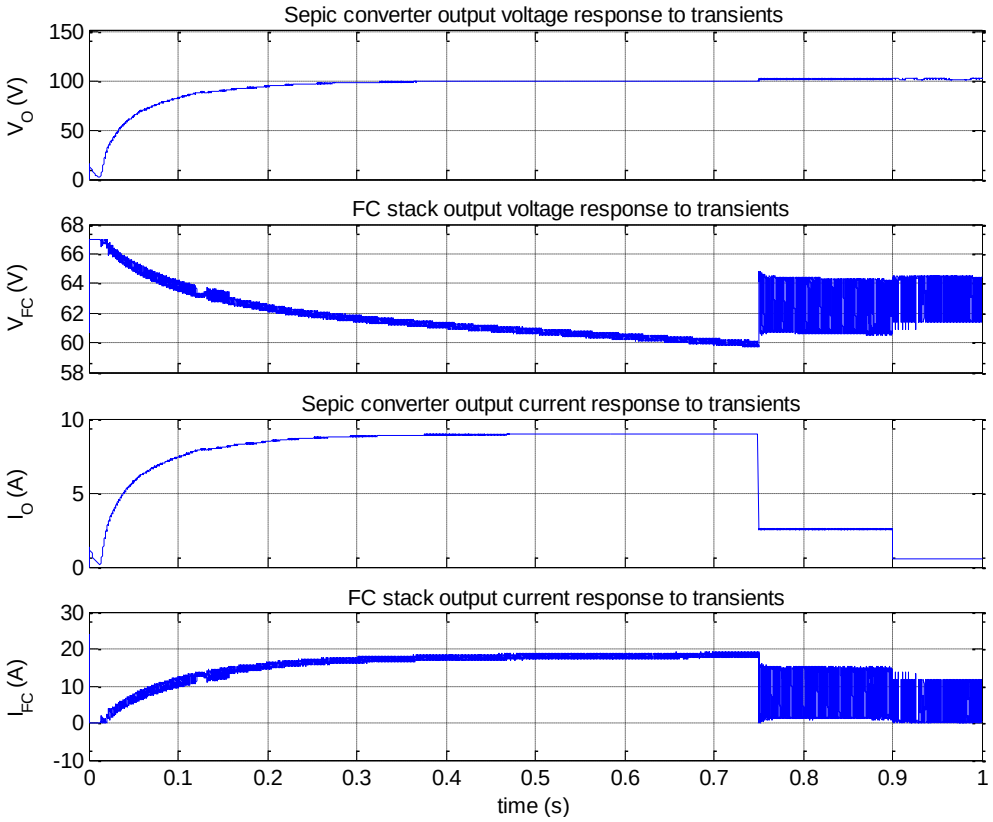


Figure 4.59: The waveforms of the output voltage and the output current of the sepic converter and the FC stack in response to load transients.

4.6 Control and Simulation of the IBVM Converter

4.6.1 Control of the IBVM Converter

Figure 4.60 shows the circuit of the IBVM converter with open-loop control. The circuit consists of two input inductors, two MOSFET switches, two MOSFET gate drivers, an energy transfer capacitor C_1 and two output capacitors C_2 and C_3, four diodes $D_1 - D_4$, a variable load resistor R, a load current I_{load} and a pulse-width modulator. The two input inductors are interleaved together in order to form two legs of boost converters.

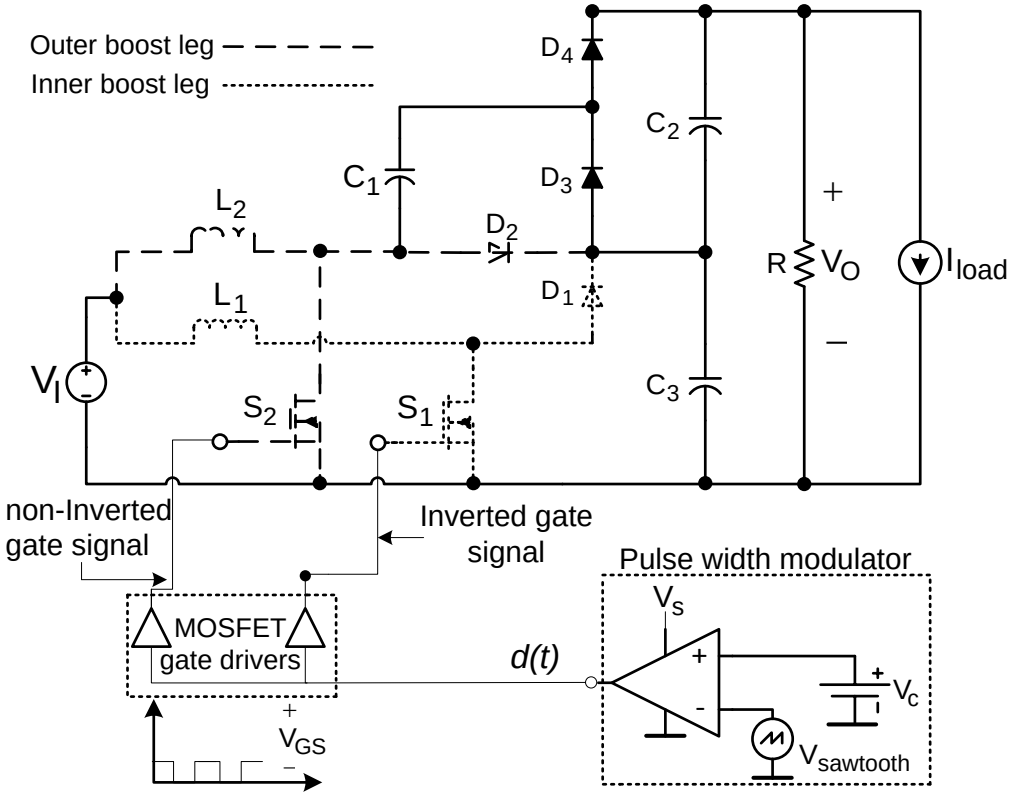


Figure 4.60: The circuit of the IBVM converter with open-loop control.

Figure 4.61 shows the circuit of the IBVM converter with PCMFC. The circuit consists of the power stage, the feedback network, the compensated EA and the pulse-width modulator. However, for the simulation and the experiment two compensated EAs are used for the design of two type III voltage controllers, one for each boost leg of the converter. The functional description of the feedback loop is similar to that given for the sepic converter. A MATLAB code was used to calculate the parameter and component values of the controllers and to generate bode-plots of the transfer functions (See Appendix C4: Code for the design of the IBVM converter controller).

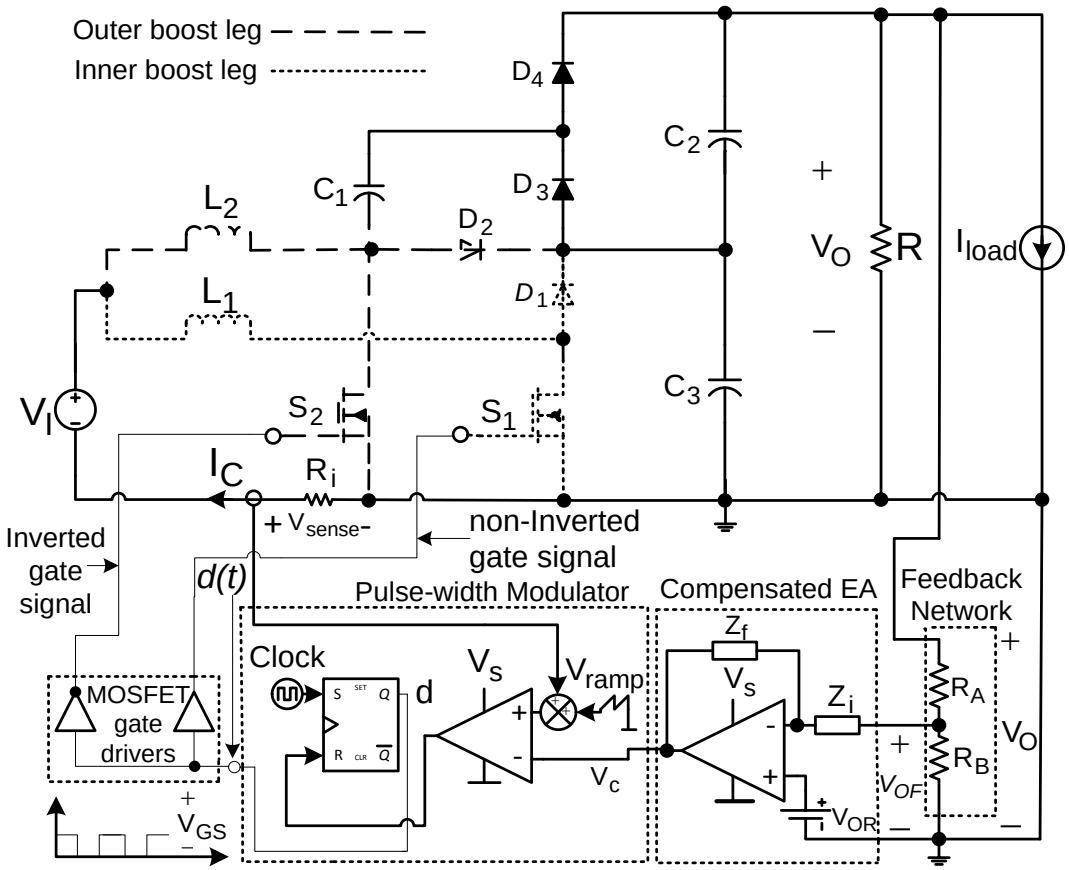


Figure 4.61: The circuit of the IBVM converter with PCMFC.

Table 4.4 shows the parameter and the component values for the feedback network, the pulse-width modulator and the compensated EAs of the designed IBVM converter controllers.

Table 4.4 The parameter and component values for the feedback network, the pulse-width modulator and the compensated EAs of the designed IBVM converter controller.

Parameter & component list for EA, Voltage FN and Pulse-width Modulator		
Component /parameter	Value	comments
V_{ref}, V_{tm} & V_{sense}(max)	2.5 V	Output voltage reference, sawtooth & sensed inductor-current voltage
R_i	0.169 Ω	Current sense resistor
R_A, R_B	79 kΩ, 1 kΩ	Resistor values for the FN
R_1, R_2, R_3, R_4, R_5	1.2 MΩ, 119.5 kΩ, 121.8 kΩ, 100.32 kΩ, 105 kΩ	Resistor values for the inner and outer boost leg EAs
C_1, C_2, C_3, C_4, C_5 & C_6	17.72 nF, 1.81 nF, 1.6 nF 1.99 nF, 22.51 nF, 1.73 nF	Capacitor values for the inner & outer boost leg EAs

4.6.2 Simulation of the IBVM converter circuit models

Figure 4.62 shows the simulation model of the IBVM converter with open-loop control in Simulink environment. The model consists of a FC stack, two input inductors L_1 and L_1 with their series resistances r_{L1} and r_{L2}, two Modulator & PWM Switch models, an energy transfer capacitor C_1 with its series resistance r_{C1}, two output capacitors C_2 and C_3 with their series resistances r_{C2} and r_{C3}, two diodes D_3 and D_4, a variable load resistance R and a scope.

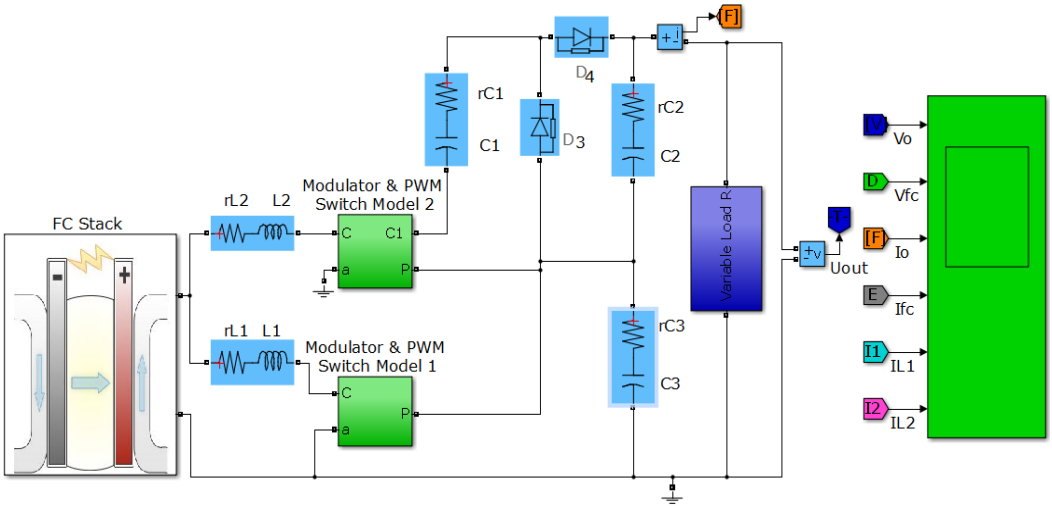


Figure 4.62: The simulation model of the IBVM converter with open-loop control.

Figure 4.63 shows the bode-plots of the magnitude and the phase of the control-to-output transfer functions for the IBVM converter power stage with open-loop control, derived with respect to the inner and outer boost legs of the converter. The plots indicate that the converter control-to-output transfer function derived with respect to the inner boost leg has a GM of 38.9 dB at a frequency of 453 Hz, and a PM of $-8.14°$ at a frequency of 82.6 kHz, with a total phase of $-188.14°$. While that derived with respect to the outer boost leg has a GM of 40.2 dB at a frequency of 426 Hz, and a PM of $-8.15°$ at a frequency of 82.6 kHz, with a total phase of $-188.15°$. Since the phase of the control-to-output transfer functions exceeds $-180°$ at the cross over frequency, the system is deemed unstable and it would still be unstable even with feedback control. Therefore, compensation for the feedback loop is required in order to ensure stability.

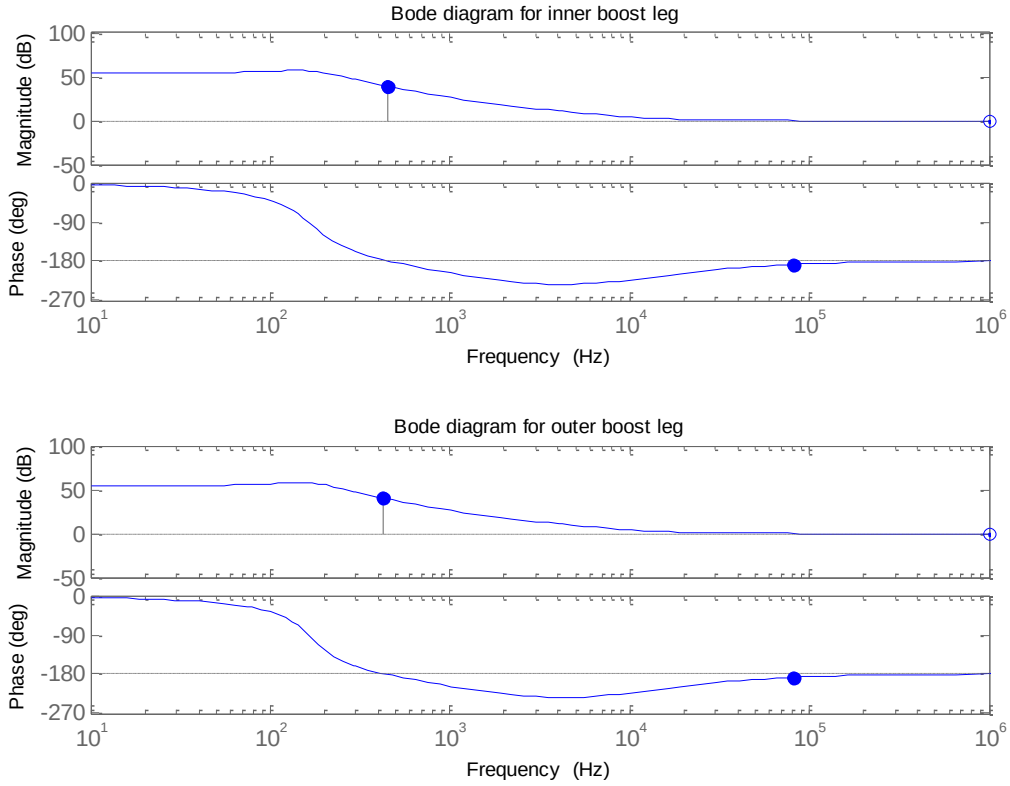


Figure 4.63: The bode-plots of the magnitude and the phase of the control-to-output transfer functions for the IBVM converter power stage with open-loop control, derived with respect to the inner and outer boost legs of the converter.

Figure 4.64 shows the waveforms of the output voltage and the output current of the IBVM converter and the FC stack at full-load with open-loop control. V_O and I_O steadily increase after start-up and reach their mean value of 197.8 V and 4.44 A in 40 ms. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 36 V in 40 ms. While I_{FC} overshoots at start-up and then steadily decreases and reaches its mean value of 28 A in 41 ms. I_{L1} and I_{L2} overshoot at start-up and then steadily decrease and reach their mean value of 14 A in 32 ms and 27 ms respectively.

Figure 4.65 shows the waveforms corresponding to the output voltage and the output current of the IBVM converter and the FC stack at minimum-load with open-loop control. V_O and I_O steadily increase after start-up and reach their mean value of 174 V and 0.435 A in 70 ms. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 53.5 V in 32 ms. While I_{FC} overshoots at start-up, and then steadily decreases and reaches its mean value of 1.75 A in 42.5 ms. I_{L1} and I_{L2} overshoot at start-up and then steadily decrease and reach their mean value of 0.875 A in 20.5 ms and 16.5 ms respectively.

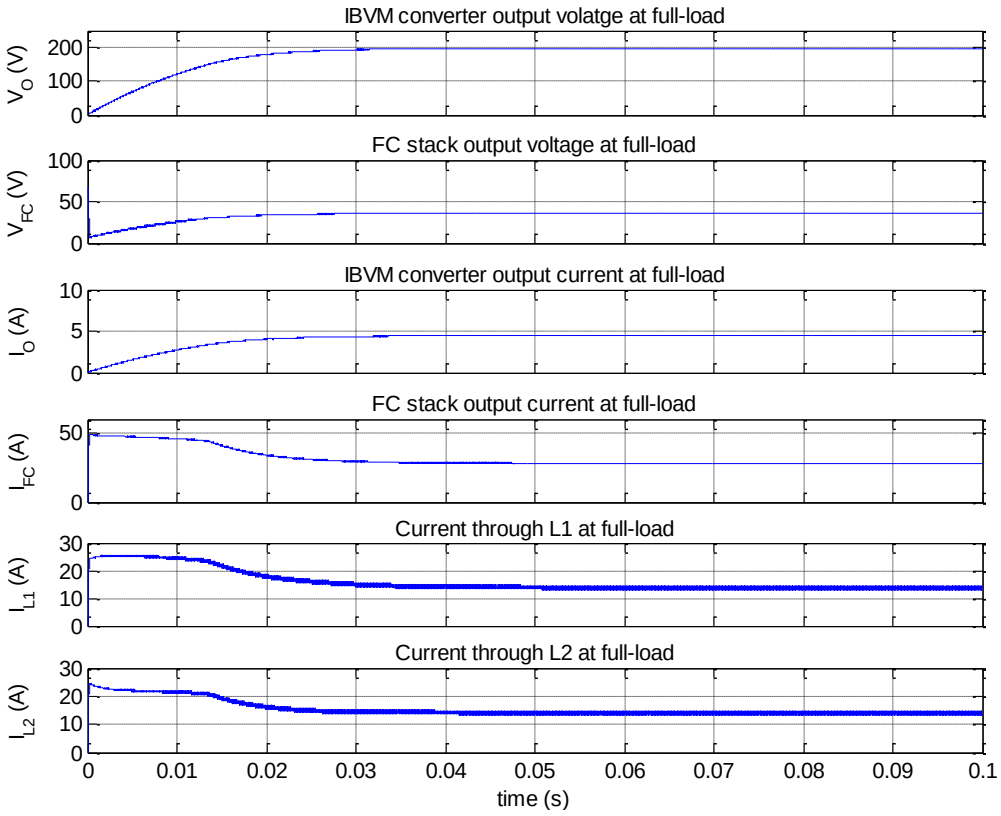


Figure 4.64: The waveforms of the output voltage and the output current of the IBVM converter and the FC stack at full-load with open-loop control.

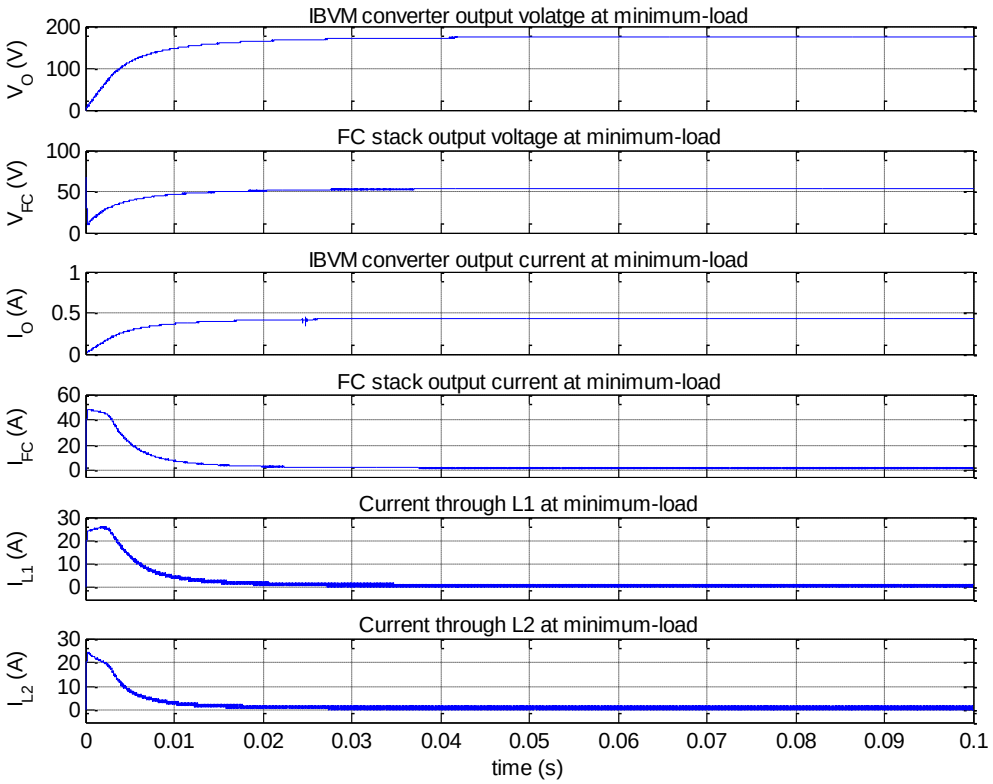


Figure 4.65: The waveforms of the output voltage and the output current of the IBVM converter and the FC stack at minimum-load with open-loop control.

Figure 4.66 shows the waveforms of the output voltage ripple and the output current ripple of the IBVM converter and the FC stack at full-load with open-loop control. The converter has a ΔV_O of 1 V and a ΔI_O of 18 mA, while the FC stack has ΔV_{FC} of 0.22 V and a ΔI_{FC} of 0.6 A. On the other hand the inductors have a ΔI_{L1} and ΔI_{L2} of 1.5 A.

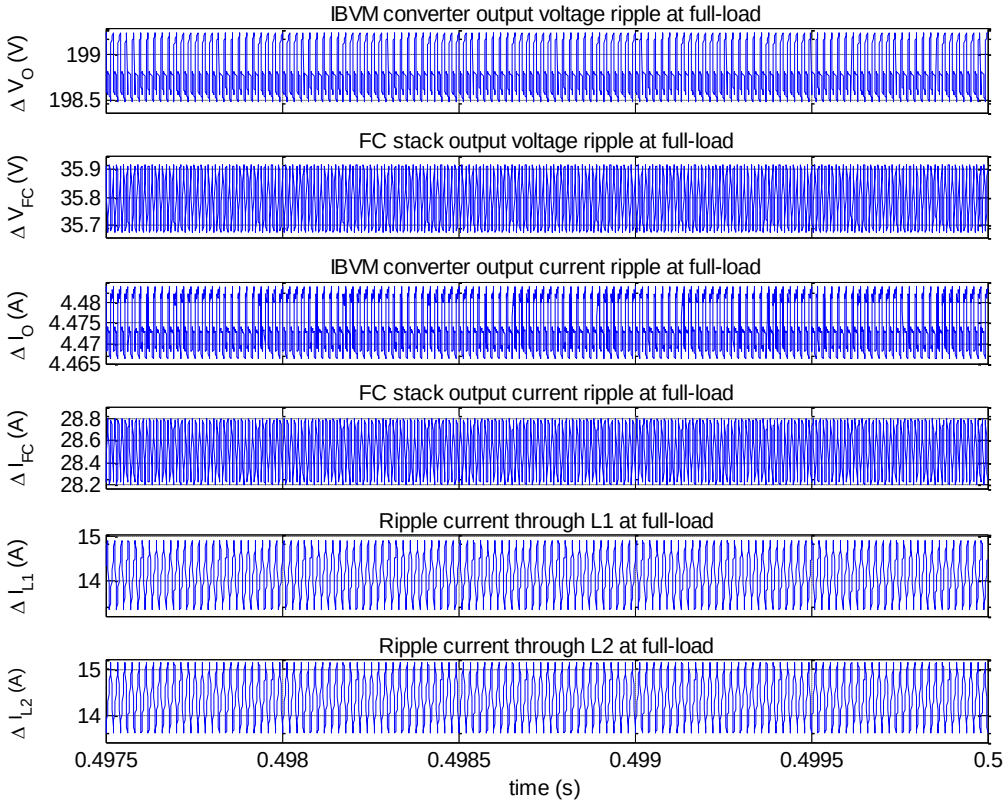


Figure 4.66: The waveforms of the output voltage ripple and the output current ripple of the IBVM converter and the FC stack at full-load with open-loop control.

Figure 4.67 shows the waveforms corresponding to the output voltage ripple and the output current ripple of the IBVM converter and the FC stack at minimum-load with open-loop control. The converter has a ΔV_O of 90 mV and a ΔI_O of 0.2 mA, while the FC stack has a ΔV_{FC} of 1 V and a ΔI_{FC} of 0.3 A. On the other hand, the inductors have a ΔI_{L1} and a ΔI_{L2} of 1.5 A.

A comparison of the results in Figure 4.66 and Figure 4.67 show that ΔI_{FC} is lower than ΔI_{L1} and ΔI_{L2} at both full-load and minimum-load. This validates the discussed inductor-interleaving feature of the IBVM converter, where the total current ripple (ΔI_{FC}) of the source is less than the sum of the inductors current ripple (ΔI_{L1} and ΔI_{L2}).

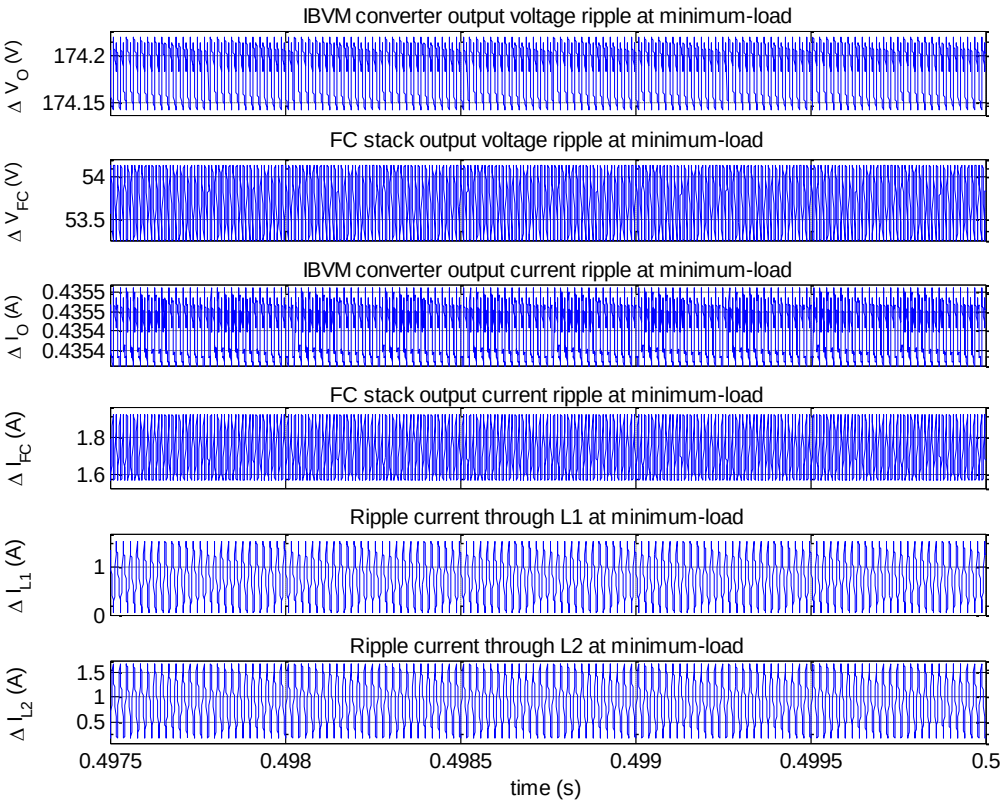


Figure 4.67: The waveforms of the output voltage ripple and the output current ripple of the IBVM converter and FC stack at minimum-load with open-loop control.

Figure 4.68 shows the simulation model of the IBVM converter with PCMFC in Simulink environment. The model consists of the power stage and the feedback loop.

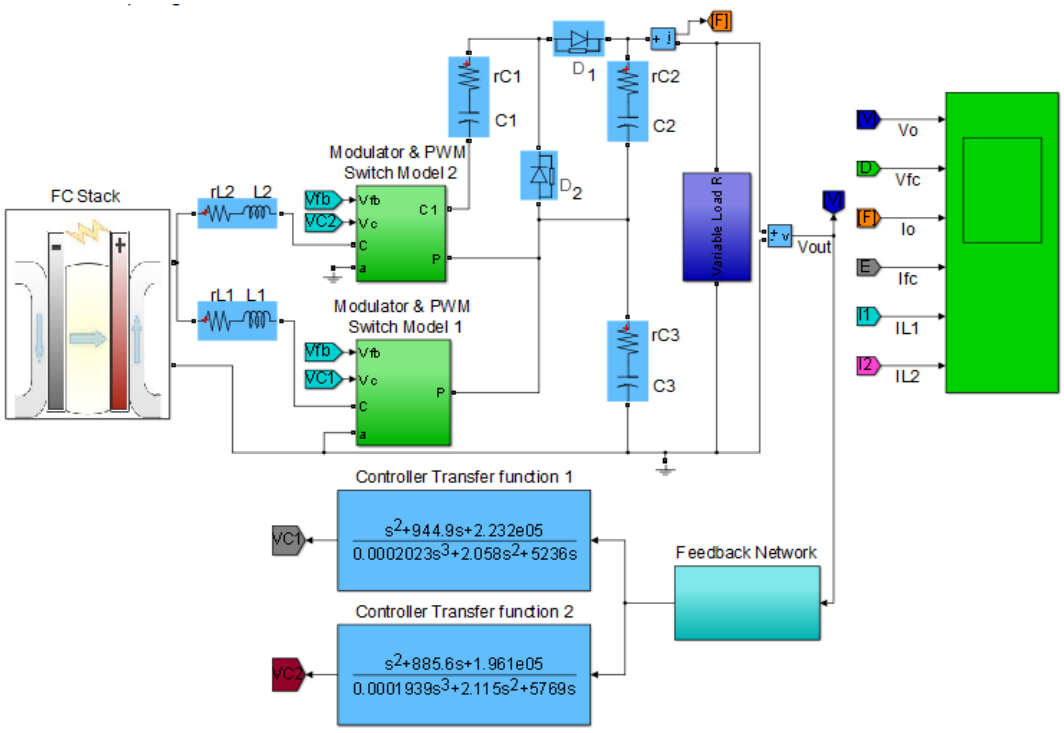


Figure 4.68: The simulation model of the IBVM converter with PCMFC.

Figure 4.69 shows the bode-plots of the magnitude and the phase of the voltage transfer functions of the designed and compensated type III EAs for the IBVM converter controllers with two zero-pole pairs, derived with respect to the inner and outer boost legs of the converter. The converter voltage transfer function derived with respect to the inner boost leg has zero-pole pairs at 75.19 Hz and 809.73 Hz, and a maximum phase boost of 112.2° at 246.75 Hz. While that derived with respect to the outer boost leg has zero-pole pairs at 70.47 Hz and 868.16 Hz, and a maximum phase boost of 116.42° at 24.35 Hz.

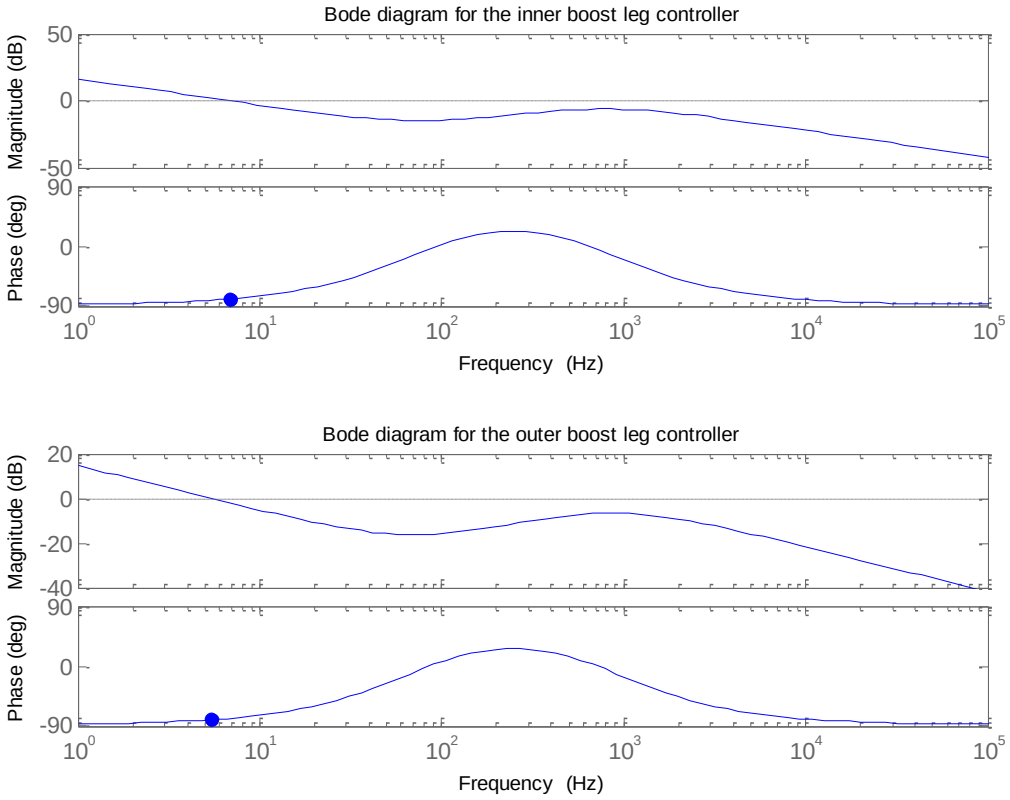


Figure 4.69: The bode-plots of the magnitude and the phase of the voltage transfer functions of the designed and compensated type III EAs for the IBVM converter controllers with zero-pole pairs, derived with respect to the inner and outer boost legs of the converter.

Figure 4.70 shows the bode-plots of the magnitude and the phase of the loop gains for the IBVM converter with PCMFC, derived with respect to the inner and outer boost legs of the converter. The converter loop gain derived with respect to the inner boost leg has a GM of -16 dB at 2.47 kHz, and a PM of 110° at a cross over frequency of 310 Hz. While that derived with respect to the outer boost leg has a GM of -16.4 dB at 2.61 kHz, and a PM of 118° at a cross over frequency of 229 Hz. Since the total phase of the converter loop gains is less than $-180°$ at the cross over frequency, the feedback system of the converter with the designed controllers is deemed stable.

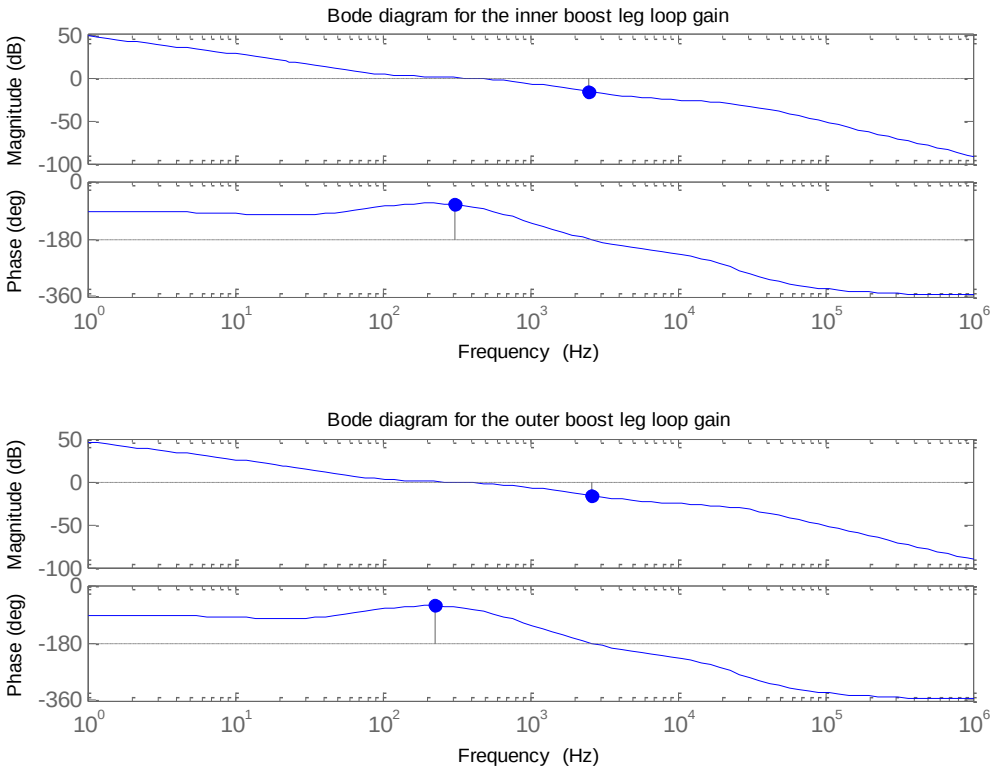


Figure 4.70: The bode-plots of the magnitude and the phase of the loop gain for the IBVM converter with PCMFC, derived with respect to the inner and outer boost legs of the converter.

Figure 4.71 shows the waveforms of the output voltage and the output current of the IBVM converter and the FC stack at full-load with PCMFC. V_O and I_O steadily increase after start-up and reach their mean value of 200 V and 4.5 A in 140 ms. On the other hand, V_{FC} sharply drops after start-up and then steadily increases and reaches its mean value of 62 V in 130 ms. While I_{FC} overshoots at start-up, and then steadily decreases and reaches its mean value of 16 A in 10 ms. I_{L1} and I_{L2} overshoot at start-up, and then steadily decrease and reach their mean value of 6 A and 10 A in 7 ms and 10 ms respectively.

Figure 4.72 shows the waveforms corresponding to the output voltage and the output current of the IBVM converter and the FC stack at minimum-load. V_O and I_O steadily increase after start-up and reach their mean value of 200 V and 0.5 A in 14.5 ms. On the other hand, V_{FC} sharply drops after start-up, and then steadily increases and reaches its mean value of 64 V in 15 ms. While I_{FC}, I_{L1} and I_{L2} overshoot at start-up and sharply drop and then steadily decrease and reach their mean value of 1.5 A, 0.5 A and 1 A in 15 ms, respectively.

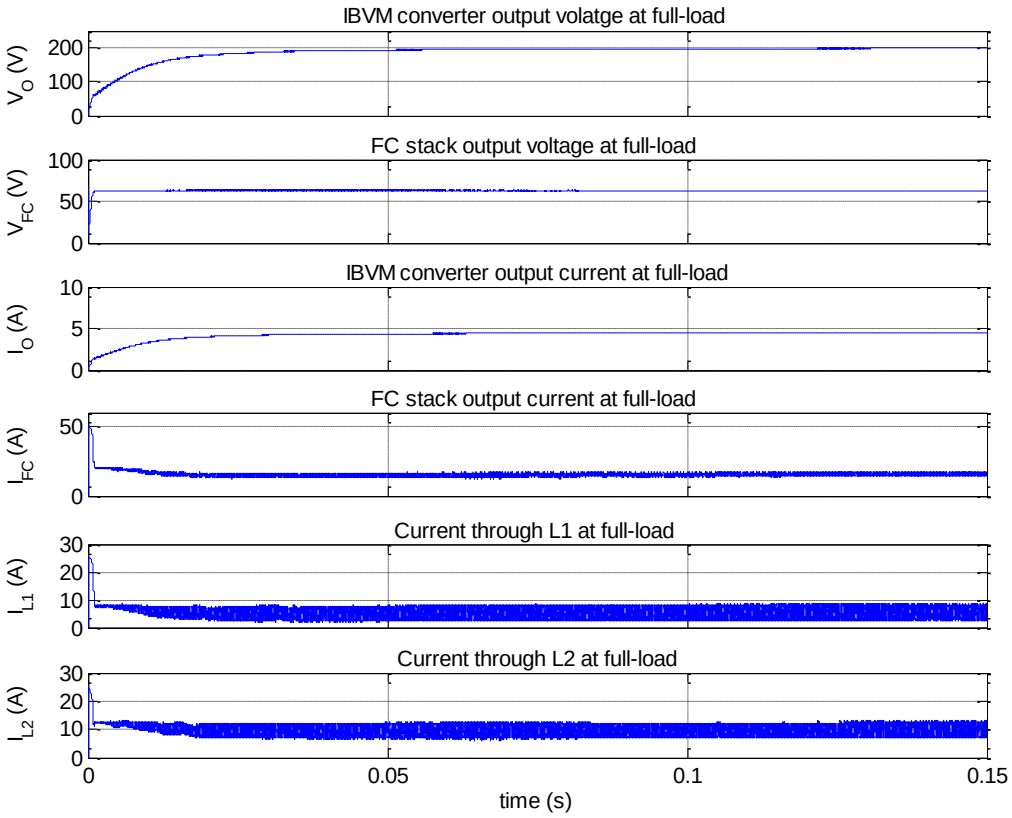


Figure 4.71: The waveforms of the output voltage and the output current of the IBVM converter and the FC stack at full-load with PCMFC.

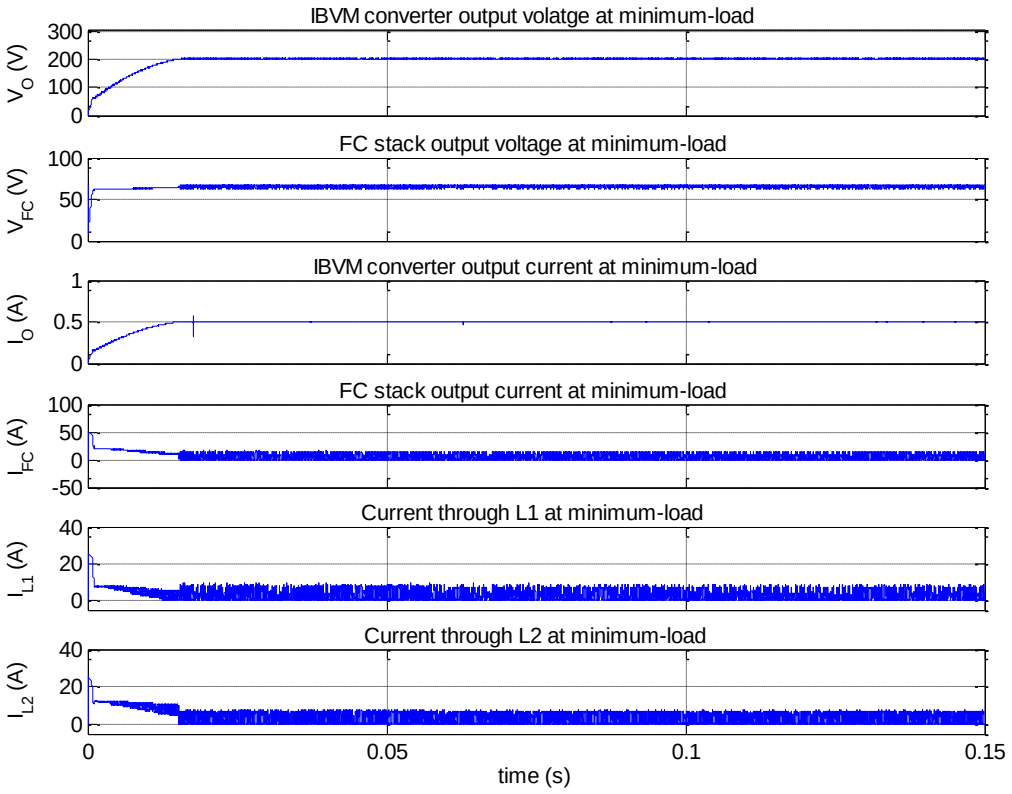


Figure 4.72: The waveforms of the output voltage and the output current of the IBVM converter and the FC stack at minimum-load with PCMFC.

Figure 4.73 shows the waveforms of the output voltage ripple and the output current ripple of the IBVM converter and the FC stack at full-load with PCMFC. The converter has a ΔV_O of 0.6 V and a ΔI_O of 20 mA, while the FC stack has a ΔV_{FC} of 0.53 V and a ΔI_{FC} of 3 A. On the other hand, the inductors have a ΔI_{L1} and ΔI_{L2} of 4.5 A.

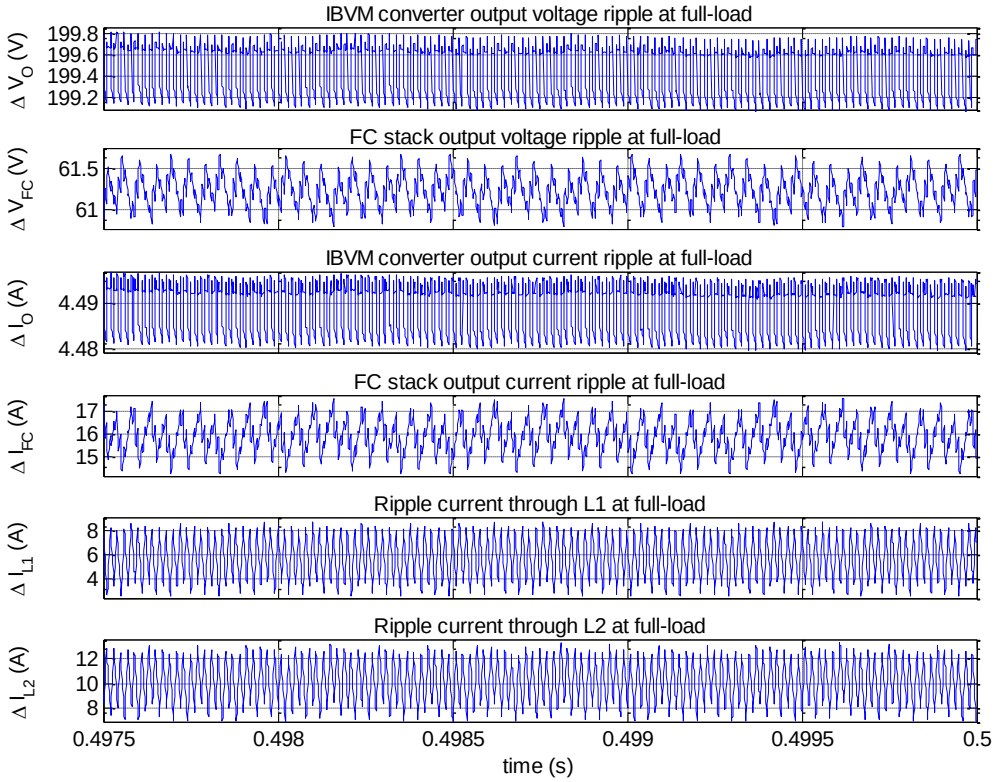


Figure 4.73: The waveforms of the output voltage ripple and the output current ripple of the IBVM converter and the FC stack at full-load with PCMFC.

Figure 4.74 shows the waveforms of the output voltage and the output current of the IBVM converter and the FC stack in response to load transients. The inductors current, the output voltage and the output current of the converter and the FC stack stabilizes at 75 ms after start-up. At 0.25 s, a load transient is introduced, as a result: V_{FC} slightly increases and develops moderate ripple content, I_{FC} decreases and develops high ripple content, V_O remains stable at 200 V, I_O decreases, I_{L1} and I_{L2} decrease and develop high ripple content. At 0.45 s, another load transient is introduced, as a result: V_{FC} slightly increases, I_{FC} slightly decreases and its ripple content slightly reduces, V_O remains stable at 200 V, I_O decreases again, I_{L1} and I_{L2} decrease again and their ripple content slightly reduce.

The results in Figure 4.74 indicates that V_O stabilizes at 200 V regardless of load transients. This is proof that the modelling of the IBVM converter is valid and that the designed controllers work.

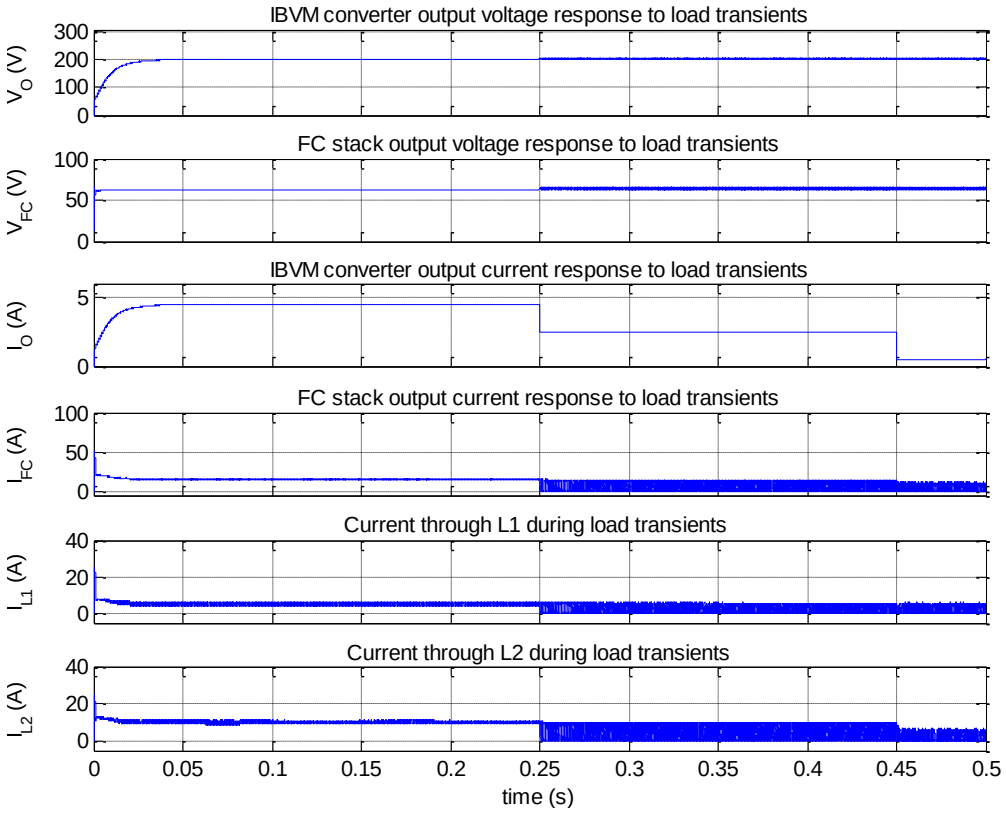


Figure 4.74: The waveforms of the output voltage and the output current of the IBVM converter and the FC stack in response to load transients.

4.7 Relative evaluation of the converters performance and the simulation results

4.7.1 Relative evaluation of the converters performance

Figure 4.75 shows the DC voltage transfer function as a function of the duty cycle at full-load for the designed and simulated converter models. The ICFFB converter, the boost converter and the sepic converter have a minimum and maximum DC voltage transfer function of 1.5 and 2.8. While the IBVM converter has a minimum and maximum DC voltage transfer function of 3 and 5.5. The range of the converters duty cycle corresponding to the given range of the converters DC voltage transfer function are 0.014 – 0.48 for the ICFFB converter, 0.397 – 0.676 for the boost and the IBVM converter and 0.62 – 0.755 for the sepic converter.

The results show that the ICFFB, the boost and the sepic converter have the lowest DC voltage transfer function while the IBVM converter has the highest. The results also show that the ICFFB converter has the lowest duty cycle, followed by the boost and the IBVM converter, while the sepic converter has the highest. Further, the results indicate that a converter with a higher DC voltage transfer function produces a higher output voltage than a converter with a lower DC voltage transfer function. Therefore, the IBVM

converter will produce a much higher output voltage than the other topologies. However, the literature reviewed reports that, a topology with a higher DC voltage transfer function will require system components that have higher voltage ratings and vice versa. While a topology with a higher duty cycle will have higher switching losses and vice versa.

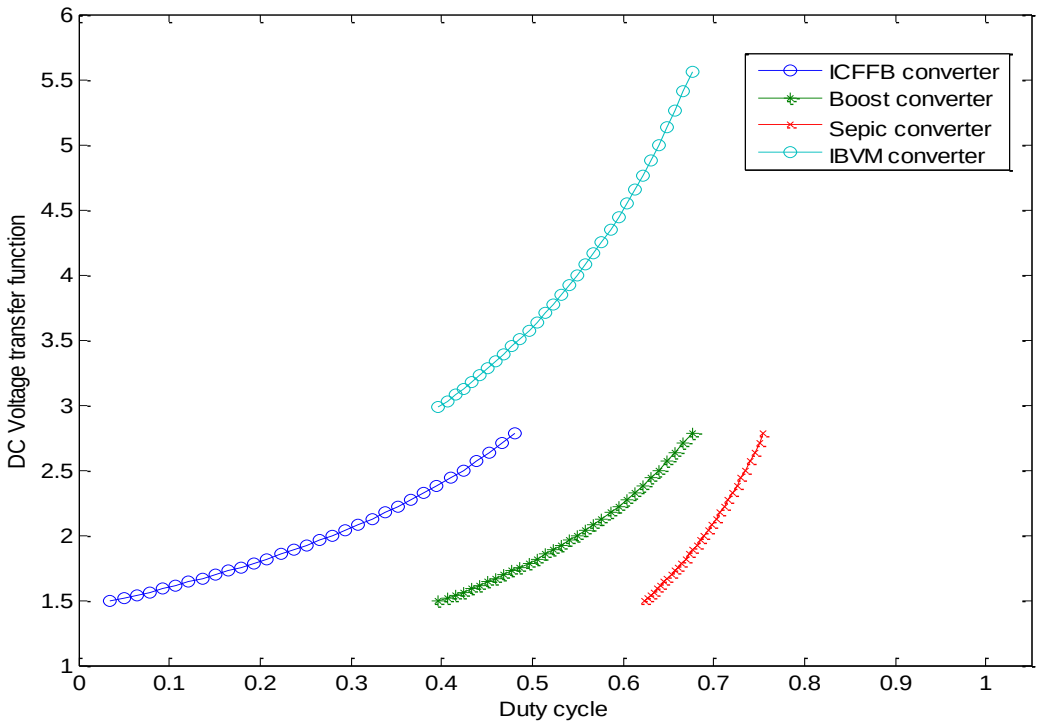


Figure 4.75: The DC voltage transfer function as a function of the duty cycle at full-load for the designed and simulated converter models.

Figure 4.76 (a) to (b) show the FC stack output current ripple (ΔI_{FC}) vs. the converters duty cycle at full-load. Figure 4.76 (a) shows ΔI_{FC} vs. the boost converter duty cycle: the stack output current ripple steadily increases for duty cycle values below 0.5 and reaches its maximum value at a duty cycle of 0.5, and then it steadily decreases for duty cycle values greater than 0.5. Figure 4.76 (b) shows ΔI_{FC} vs. the ICFFB converter duty cycle: the behaviour of the stack output current ripple is similar to that with the boost converter. Figure 4.76 (c) shows ΔI_{FC} vs. the sepic converter duty cycle: the stack output current ripple is inversely proportional to the converter duty cycle. Figure 4.76 (d) shows ΔI_{FC} vs. the IBVM converter duty cycle: the behaviour of the stack output current ripple is opposite of that with the boost converter.

The results indicate that ΔI_{FC} is lower when the FC stack is interfaced with the IBVM converter. Therefore, the IBVM converter is a better option for lower ΔI_{FC} requirements.

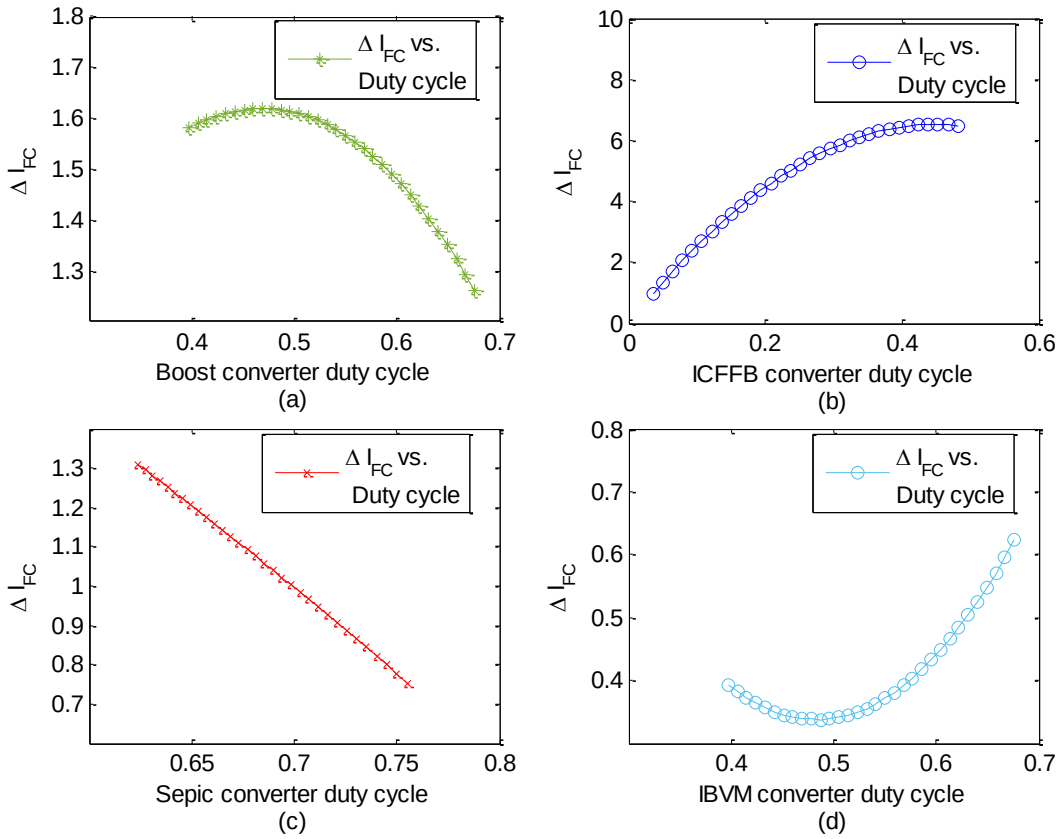


Figure 4.76: The FC stack output current ripple vs. the converters duty cycle at full-load.

(a) ΔI_{FC} vs. boost converter duty cycle. (b) ΔI_{FC} vs. sepic converter duty cycle. (c) ΔI_{FC} vs. ICFFB converter duty cycle. (d) ΔI_{FC} vs. IBVM converter duty cycle

Figure 4.77 (a) and (b) show the FC stack output current ripple pie charts for the simulated converter models with open-loop control. Figure 4.77 (a) shows that the FC stack has the highest ΔI_{FC} when interfaced with the ICFFB converter and vice versa when interfaced with the IBVM converter. While Figure 4.77 (b) shows that the FC stack has the highest ΔI_{FC} when interfaced with the boost converter and vice versa when interfaced with the ICFFB and IBVM converters.

The results indicate that ΔI_{FC} is lowest when the stack is interfaced with the IBVM converter at both full-load and minimum-load.

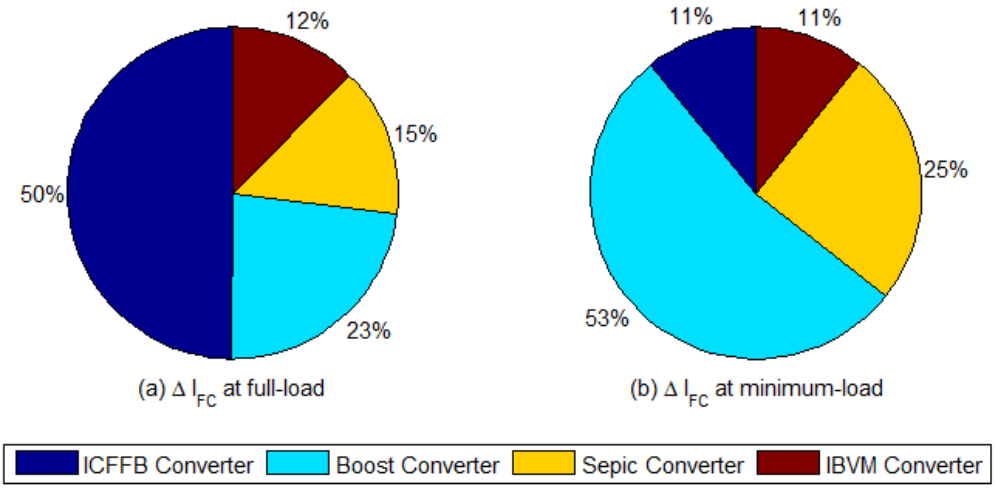


Figure 4.77: The FC stack output current ripple pie charts for the simulated converter models with open-loop control.

(a) ΔI_{FC} at full-load. (b) ΔI_{FC} at minimum-load.

Figure 4.78 (a) and (b) show the FC stack output voltage ripple for the simulated converter models with open-loop control. Figure 4.78 (a) shows that the FC stack has the highest ΔV_{FC} when interfaced with the ICFFB converter and vice versa when interfaced with the IBVM converter. While Figure 4.78 (b) shows that the FC stack has a highest ΔV_{FC} when interfaced with the boost converter and vice versa when interfaced with the IBVM converter.

The results indicate that ΔV_{FC} is lowest when the stack is interfaced with the IBVM converter at both full-load and minimum-load.

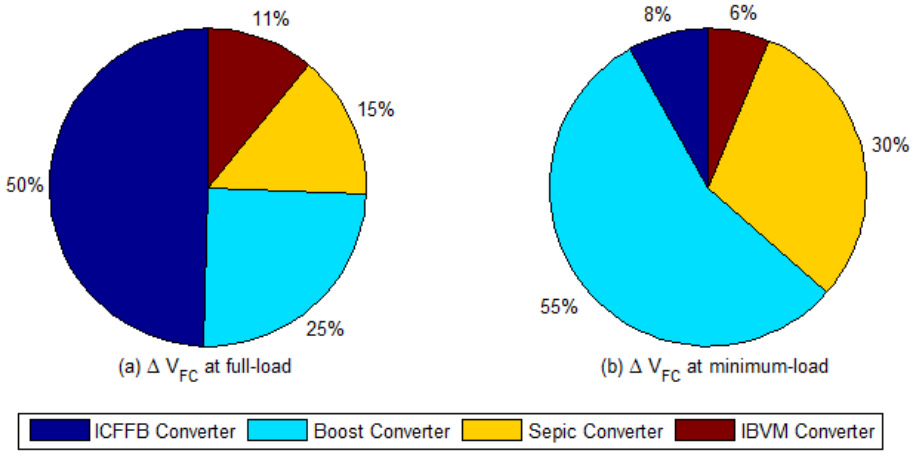


Figure 4.78: The FC stack output voltage ripple pie charts for the simulated converter models with open-loop control.

(a) ΔV_{FC} at full-load. (b) ΔV_{FC} at minimum-load.

Table 4.5 shows a summary of the FC stack and the converters simulation results with open-loop control. The results show that the converters output voltage are below the

specified design values. They also show that the stack has the lowest ΔI_{FC} and ΔV_{FC} when interfaced with the IBVM converter.

Table 4.5: A summary of the FC stack and the converters simulation results with open-loop control

Parameter	Converter Topology at full-load				Converter Topology at minimum-load				unit
	ICFFB	Boost	Sepic	IBVM	ICFFB	Boost	Sepic	IBVM	
V_O	89.8	95.6	90.7	197.8	89.9	93.59	91.5	174	V
V_{FC}	37.6	36.3	37.1	36	56	58.52	57	53.5	V
I_O	8.08	8.6	8.17	4.44	0.45	0.468	0.46	0.435	A
I_{FC}	26.4	27.5	25.4	28	1.03	0.87	1	1.75	A
ΔV_O	0.4	0.65	0.46	1	0.006	0.030	0.02	0.090	V
ΔV_{FC}	1	0.5	0.3	0.22	1.3	8.8	4.8	1	V
ΔI_O	0.3	0.055	0.04	0.018	0.0011	0.0007	0.0001	0.0002	A
ΔI_{FC}	2.4	1.12	0.7	0.6	0.31	1.5	0.7	0.3	A

Figure 4.79 (a) and (b) show the FC stack output current ripple and output voltage ripple for the simulated converter models at full-load with PCMFC. The results show that the stack has the lowest ΔI_{FC} and ΔV_{FC} when interfaced with the IBVM converter, and vice versa when interfaced with the ICFFB and sepic converter.

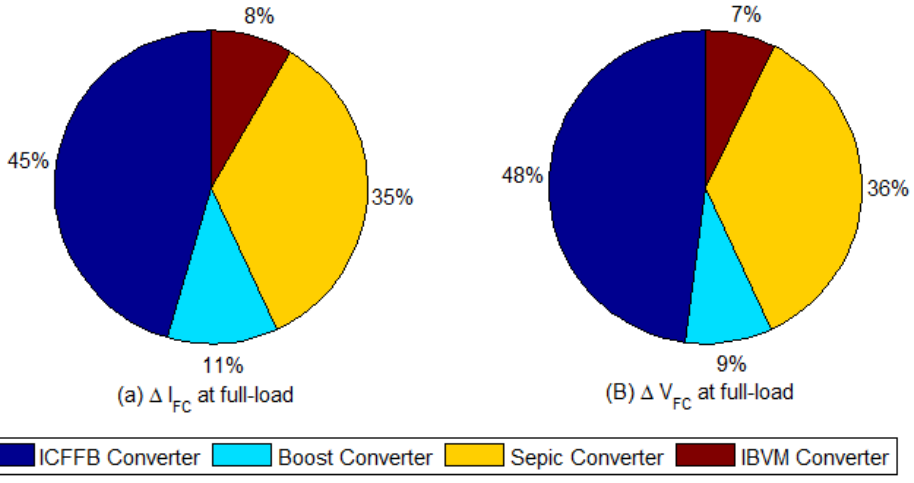


Figure 4.79: The FC stack output current ripple and voltage ripple for the simulated converter models at full-load with PCMFC.

(a) ΔI_{FC} at full-load. (b) ΔV_{FC} at full-load.

Table 4.6 shows a summary of the FC stack and the converters simulations results with PCMFC. The results show that the converters output voltages are equivalent to the specified design values. This is proof that the modelling of the converters carried out in chapter three is valid and that the designed converter controllers work.

Table 4.6: A summary of the FC stack and the converters simulation results with feedback control

Parameter	Converter Topology at full-load				Converter Topology at minimum-load				unit
	ICFFB	Boost	Sepic	IBVM	ICFFB	Boost	Sepic	*IBVM	
V_O	100	100	100	200	100	100	100	-	V
V_{FC}	62	62.62	59	62	66.7	65.5	53.5	-	V
I_O	9	9	9	4.495	0.5	0.5	0.435	-	A
I_{FC}	17	16.96	18.5	15.76	0.75	1	1.75	-	A
ΔV_O	0.4	0.4	1	0.6	0.002	0.030	0.090	-	V
ΔV_{FC}	2	0.38	1.5	0.3	0.5	0.35	1	-	V
ΔI_O	0.039	0.033	0.092	0.020	0.0001	0.060	0.0002	-	A
ΔI_{FC}	5.9	1.49	4.5	1.1	1.7	1.33	0.3	-	A

*The IBVM results at minimum-load are omitted because this work only considered IBVM circuit modelling at full-load.

4.7.2 Conclusion

The ICCFB, the boost, the sepic and the IBVM converter models were simulated at both full-load and minimum-load with both open-loop control and feedback control. The results obtained with open-loop control indicate that the converters output voltages do not match those given in the converters design specifications. This is so because a converter with open-loop control cannot track the output voltage to its output voltage reference. While the results obtained with feedback control indicate that the converters output voltages were stabilised and match those given in the converters design specifications. This verifies the ability of a converter with feedback control to track the output voltage to its output voltage reference. Further, the relative evaluation of the converters performance and the simulation results indicate that the IBVM converter is a better option for low FC stack output current and voltage ripple requirements. The IBVM converter also has an added advantage of providing high DC voltage transfer function without the use of a transformer. This reduces the cost of the system by eliminating the high cost incurred by using transformers and yet provides high DC voltage gains.

CHAPTER 5
EXPERIMENT OF THE IBVM CONVERTER PROTOTYPE CIRCUIT

5.1 Introduction

This chapter presents the prototype circuit and the experimental results of the IBVM converter. The experiment was carried out in order to validate the circuit modelling and the simulation results for the IBVM converter.

Table 5.1 shows the design specifications for the IBVM converter prototype circuit. The parameter and component values for the converter power stage were determined by using the parameter and component equations derived in chapter three. Table 5.2 shows the component and parameter values for the IBVM converter prototyped circuit.

Table 5.1: The design specifications for the IBVM converter prototype circuit.

parameter	Value	Comments
Output power P_O	0 – 900 W	Nominal P_O of 0 – 30 W
Input voltage V_I	36 – 67 VDC	Nominal V_I: 58 VDC
Output voltage V_O	200 VDC	Nominal output voltage
Efficiency target η	90 %	optimised at full-load
Input current ripple	$\leq$ 30 % of I_L	For load range of 0 – 100 %
Output voltage ripple Δv_O	< 1 % of V_O	
Switching frequency f_s	$\cong$ 50 kHz	

Table 5.2 The parameter and component values for the IBVM converter prototype circuit.

Component /parameter	Value	comments
V_{ref}, V_{tm}	2.5 V	V_O Reference, sawtooth voltage
$L_1, L_2, C_1 = C_2 = C_3$	224 µH, 263.5µH, 680 µF	Power-stage components
R_A, R_B	79 kΩ, 1kΩ	Feedback Resistors
R_1, R_2, R_3, R_4, R_5	1.2 MΩ, 119.5 kΩ, 121.8 kΩ, 100.32 kΩ, 105 kΩ	Resistor values for the Error Amplifiers (EAs)
C_1, C_2, C_3, C_4, C_5, C_6	17.72 nF, 1.81 nF, 1.6 nF 1.99 nF, 22.51 nF, 1.73 nF	Capacitor values for the EAs

Figure 5.1 shows the experimental setup for the experiment of the IBVM converter prototype circuit. The experimental setup consists of a digital multimeter, a 1 kW PEMFC stack, a variable electronic load, a 100 MHz LeCroy digital oscilloscope, a Laptop, a Hydrogen gas supply pipe, a dual variable DC power supply, a 1 kW PEMFC stack controller and the IBVM converter prototype circuit.

Pure Hydrogen gas is supplied to the PEMFC stack via the Hydrogen gas supply pipe. Then the PEMFC stack produces an output voltage that varies in the range of 36 V to 66 V relative to the power – load, by converting the Hydrogen gas into electricity and water. The stack controller monitors and ensures safe operation of the stack. The IBVM converter couples to the stack and converts the stack output voltage to a higher and stable converter output voltage of about 200 V. The variable electronic load connects to the output of the converter and presents a variable power – load. The dual variable DC power supply provides auxiliary power to the stack controller and the converter controller. The oscilloscope is used to measure and capture various experimental voltage waveforms, while the Laptop is used to store the captured waveforms.

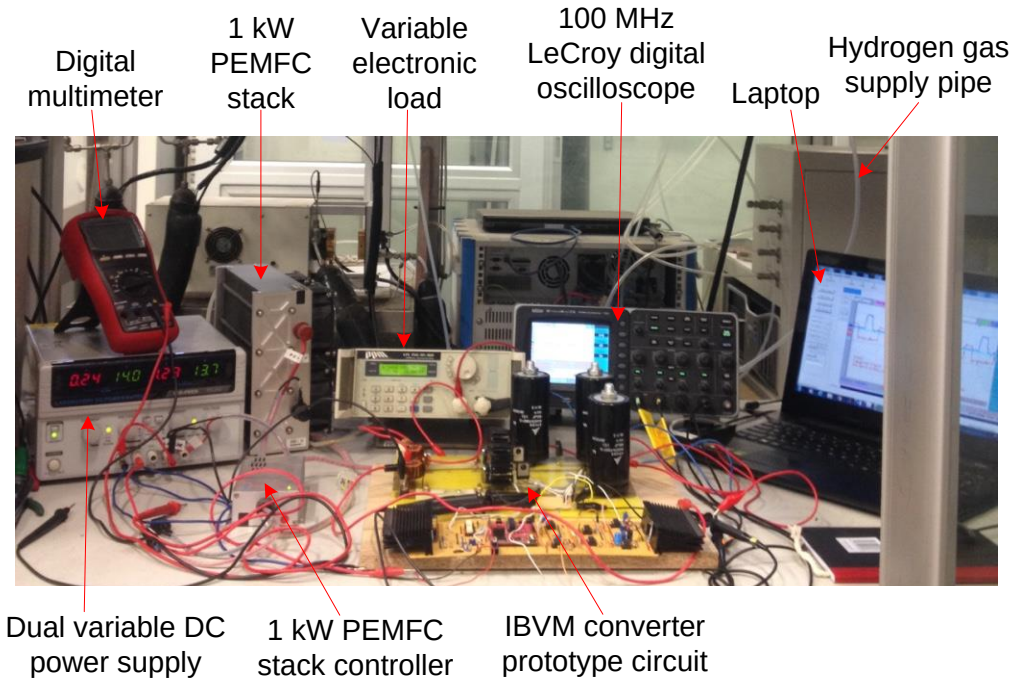


Figure 5.1: The experimental setup for the experiment of the IBVM converter prototype circuit.

5.2 The IBVM converter prototype circuit

Figure 5.2 shows the IBVM converter prototype circuit. The circuit consists of the input voltage terminals V_I+ and V_I-, two homemade toroid input inductors L_1 and L_2, an outer and inner boost leg shunt, two IRFP260N MOSFETs, two TLP251 gate drivers, four RURG5060 ultrafast diodes, a Texas instruments Launchpad with an

MSP430G2553 microcontroller unit (MCU), a differential amplifier (DA), two compensated error amplifiers (EAs), two summing amplifiers, a low pass filter, two LM7805 voltage regulators, two voltage regulator heat sinks and three PG – 6DI aluminium electrolytic capacitors: C_1, C_2 and C_3.

The PEMFC stack output voltage is fed to the converter via the input voltage terminals, and then the converter boosts this voltage to a higher converter output voltage (V_O) of about 200 V. A portion of V_O is fed back to the inverting input of the DA as converter output feedback voltage (V_{OF}) in order to produce an error voltage (V_e). V_e is fed to the compensated EAs and the low pass filter and then the summing amplifiers adds up their outputs to produce V_c. The MCU reads V_c from the summing amplifier outputs on its two analogue inputs and then generates two PWM signals that are phase shifted by $180°$ out of phase. Then the gate drivers amplify the PWM signals to a higher gate-to-source voltage that is compatible with the switching voltage of the MOSFETs.

The DA was realised by using the CA3130 operational amplifier (OP-Amp) configured as a differential amplifier (DA). The OP-Amp has two inputs, an inverting input and a non-inverting input. In order to configure the Op-Amp as a DA, an attenuated V_{OF} was fed to the inverting input and an output reference voltage (V_{OR}) equivalent to 2.5 V was fed to the non-inverting input. A resistive voltage divider feedback network was used to attenuate V_{OF}. Ideally, when V_{OF} is equal to V_{OR}, then V_e is zero. But when V_{OF} deviates from V_{OR}, V_e becomes non-zero and reaches a maximum at 2.5 V.

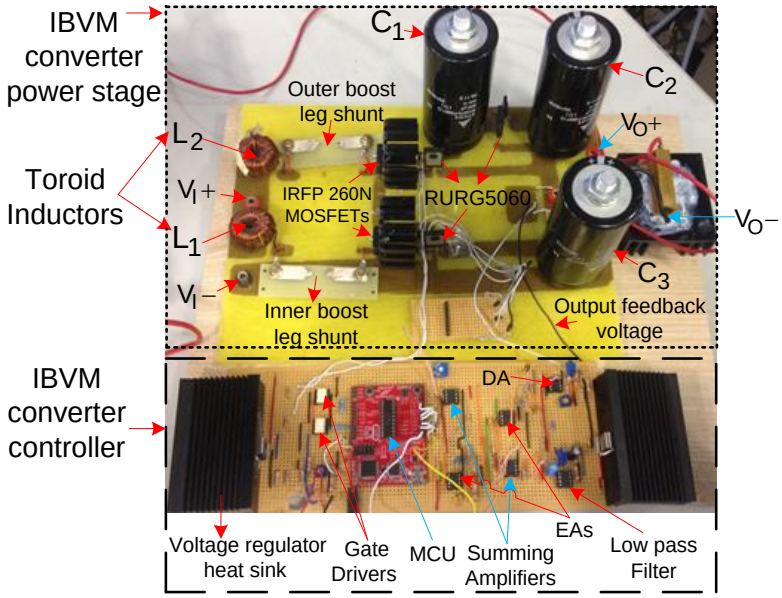


Figure 5.2: The IBVM converter prototype circuit.

5.2.1 MSP430G2553 MCU

The MSP430G2553 MCU is a low cost and low power mixed signal processor (Texas Instruments, 2013) with several programmable peripherals and pin-outs (See Appendix D1: MSP430G2553 Microcontroller device pin-out and Appendix D2: Device functional block diagram of the MSP430G2553 MCU). Some of the peripherals that are used for the converter controller application are the input/output (I/O) pins, the system clock, the timers, the ADC module and the CPU. The device data sheet gives more details about the MCU.

Figure 5.3 shows the key program algorithm steps followed in writing up the C code program required to generate two PWM gate signals. Code composer studio (CCS) IDE and its programmer tool were used to develop the C code (See Appendix D) and to program the MCU. The first step in the algorithm is to start the MCU; at this point, the device is powered up. The second step consists of the declaration of constants, functions and variables that are used in the program. The third step consists of the initialization of variables, I/O pins, ADC10 module and timers. The fourth step consists of the ADC10 module continuously sampling the summing amplifiers outputs via the analogue input pins and then converting the sampled analogue voltage values to a digital format.

Special functions registers are used in order to configure and initialize the I/O pins, the timers and the ADC10 module (See Appendix D3: MSP430G2553 C-code for IBVM Converter Control). Timer0_A3 and Timer1_A3 are configured to operate as up/down counters at a fixed switching frequency of 50 kHz, with the initial count of Timer1_A3 having a $180°$ phase delay from that of Timer0_A3 in order to warrant a $180°$ phase shift between the two generated PWM gate signals. The ADC10 module is configured to have a reference voltage of 2.5 V, to sample V_c on the two analogue input pins and to operate with the lowest clock source speed in order to ensure accuracy of the sampled voltage.

The ADC10 module has a 10-bit resolution which is equivalent to a decimal value of 0 to 1023. Therefore, the minimum analogue value it can sample is equal to decimal zero and the maximum analogue value it can sample is equal to decimal 1023. According to Texas Instruments (2013), the formula that describes the analogue-to-digital conversion of the ADC10 module is given as

$$N_{ADC} = 1023 \frac{V_c - V_R(-)}{V_R(+) - V_R(-)}. \quad (5.1)$$

Where N_{ADC} is the analogue-to-digital conversion of the ADC10 module, $V_R(-)$ is the negative reference voltage of the ADC10 module and $V_R(+)$ is positive reference voltage of the ADC10 module. The MCU data sheet gives eight options for reference voltage configurations. In this work, $V_R(+)$ corresponds to 2.5 V while $V_R(-)$ corresponds to 0 V.

The ADC10 module repeatedly samples and performs the analogue-to-digital voltage conversion of V_c. The results of the conversions are stored in the ADC10MEM register by default. An alternative is to copy and store them in global variables for easy manipulation of the data. In this work, the global variables ADCRead and ADCRead1 are used for storage. Then Timer0_A3 and Timer1_A3 use the values in the variables to adjust the duty cycle of the generated PWM signals. The duty cycle of the signals is proportional to the ratio of V_c to $V_R(+)$. Once the duty cycle of the signals are adjusted, the program loops back to step four and the MCU updates the global variables and then the process repeats.

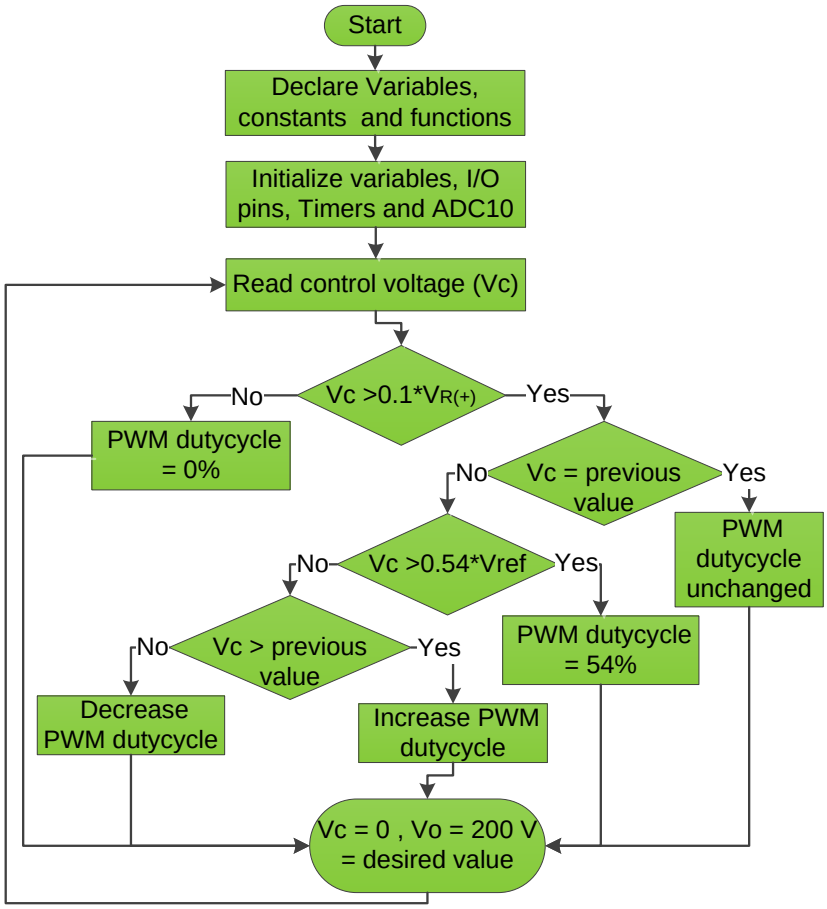


Figure 5.3: The key program algorithm steps followed in writing up the C code program required to generate two PWM signal using the MSP430G2553 MCU.

5.3 Experimental results

This section discusses the experimental results of the IBVM converter prototype circuit and the PEMFC stack. A four-channel LeCroy waveAce214 100 MHz Oscilloscope with a sampling rate of 1GS/s was used for voltage measurements.

The following experimental results were obtained; the gate-to-source voltage and the drain-to-source voltage of the MOSFETs, the inductors current ripple, the voltage across the lower output capacitor (C_3), the output voltages of the PEMFC stack and the IBVM converter prototype circuit.

A variable 350 W electronic load was used as the load for the IBVM converter prototype circuit. The load was varied in the range of 20 W to 30 W in increments of 10 W.

5.3.1 The gate-to-source voltage

Figure 5.4 shows the gate-to-source voltage waveforms of the MOSFETs at 20 W power – load. The waveform captured at CH1 corresponds to the voltage measured between the gate and source of the MOSFET on the inner boost leg. While the waveform captured at CH2 corresponds to the voltage measured between the gate and source of the MOSFET on the outer boost leg. The measurements of the waveform captured at CH1 are displayed in blue below the two waveforms, and the measurements of the waveform captured at CH2 are similar to those at CH1.

The results show that the gate-to-source voltage waveform captured at CH1 has a frequency of 49.99 kHz, an amplitude of 13.6 V, a duty cycle of 39 % and a period of 20 µS. Further, the results show that the phase difference between the voltage waveforms captured at CH1 and CH2 is 188.1°

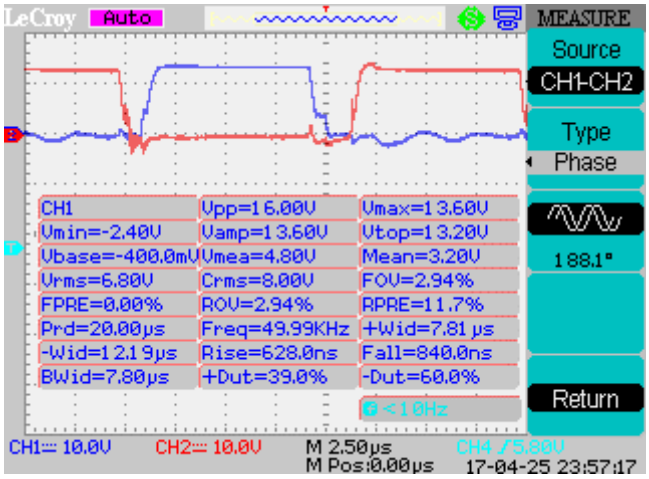
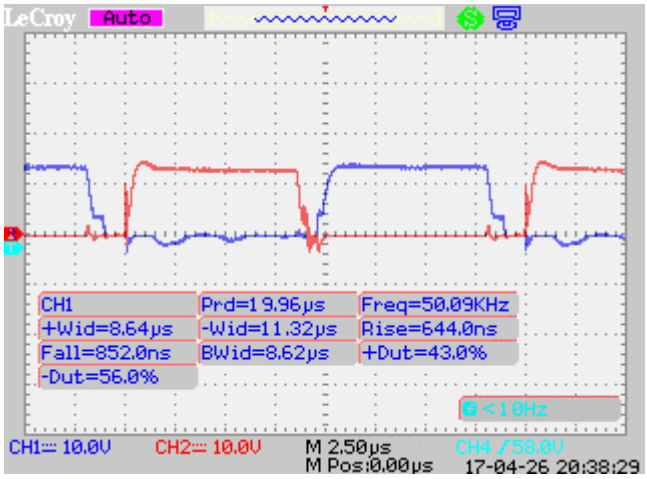


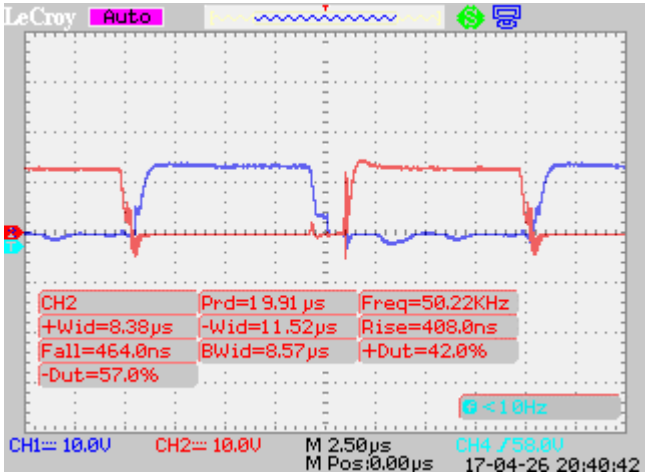
Figure 5.4: The gate-to-source voltage waveforms of the MOSFETs at 20 W power-load.

Figure 5.5 shows the frequency and the time measurements of the gate-to-source voltage waveforms of the MOSFETs at 30 W power – load. Figure 5.5 (a) shows the frequency and the time measurements of the gate-to-source voltage waveform captured at CH1. While Figure 5.5 (b) shows the frequency and the time measurements of the gate-to-source voltage waveform captured at CH2.

The results show that the gate-to-source voltage waveform captured at CH1 has a frequency of 50.09 kHz, a duty cycle of 43 % and a period of 19.96 µS , while that captured at CH2 has a frequency of 50.22 kHz, a duty cycle of 42 % and a period of 19.91 µS .



(a)



(b)

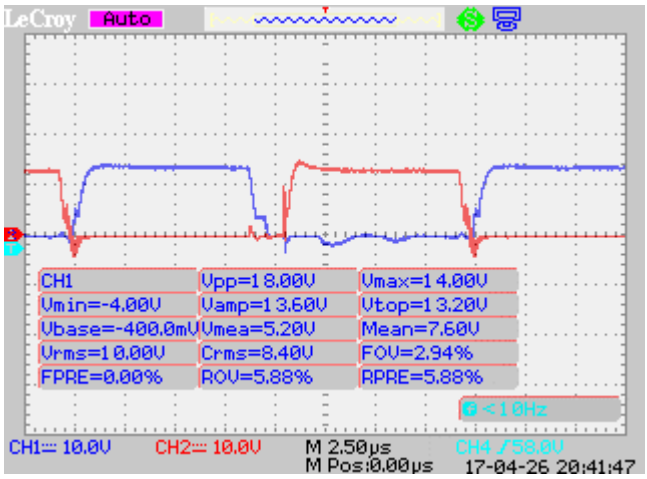
Figure 5.5: The frequency and the time measurements of the gate-to-source voltage waveforms of the MOSFETs at 30 W power-load.

(a) The frequency and the time measurements of the gate-to-source voltage waveform captured at CH1. (b) The frequency and the time measurements of the gate-to-source voltage waveform captured at CH2.

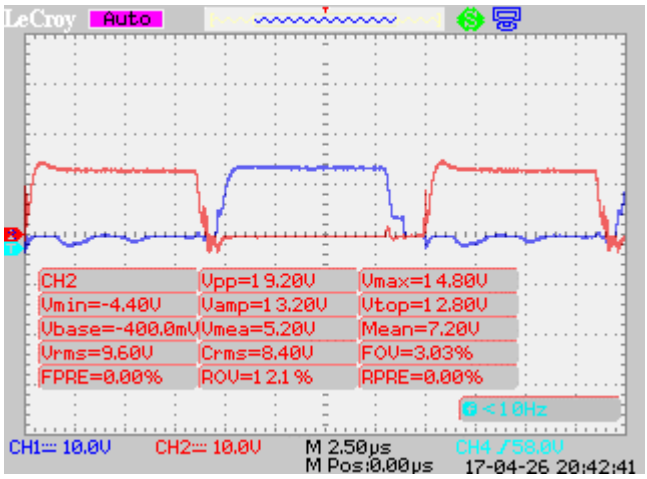
Figure 5.6 shows the voltage measurements of the gate-to-source voltage waveforms of the MOSFETs at 30 W power – load. Figure 5.6 (a) shows the voltage measurements

of the gate-to-source voltage waveform captured at CH1, while Figure 5.6 (b) shows the voltage measurements of the gate-to-source voltage waveform captured at CH2.

The results show that the gate-to-source voltage waveform captured at CH1 has a mean of 7.60 V, an amplitude of 13.6 V, a peak-to-peak of 18.V, a maximum of 14 V and an rms of 10 V. While the gate-to-source voltage waveform captured at CH2 has a mean of 7.20 V, an amplitude of 13.2 V, a peak-to-peak of 19.2.V, a maximum of 14.8 V and an rms of 9.6 V.



(a)



(b)

Figure 5.6: The voltage measurements of the gate-to-source voltage waveforms of the MOSFETs at 30 W power-load.

(a) The voltage measurements of the gate-to-source voltage waveform captured at CH1. (b)The voltage measurements of the gate-to-source voltage waveforms waveform captured at CH2.

Figure 5.7 shows the gate-to-source voltage waveforms of MOSFETs out of phase by 182.9° at 30 W power-load.

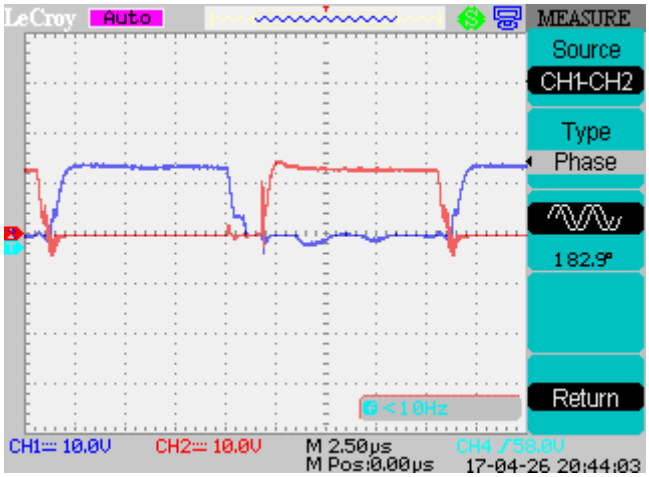


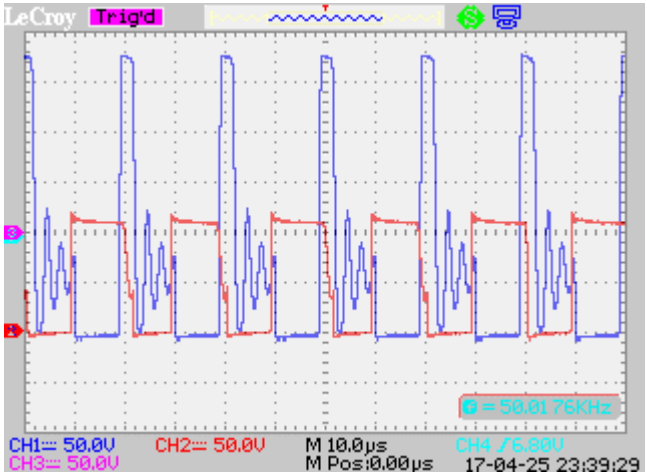
Figure 5.7: The gate-to-source voltage waveforms of the MOSFETs out of phase by 182.9° at 30 W power-load.

5.3.2 The drain-to-source voltage

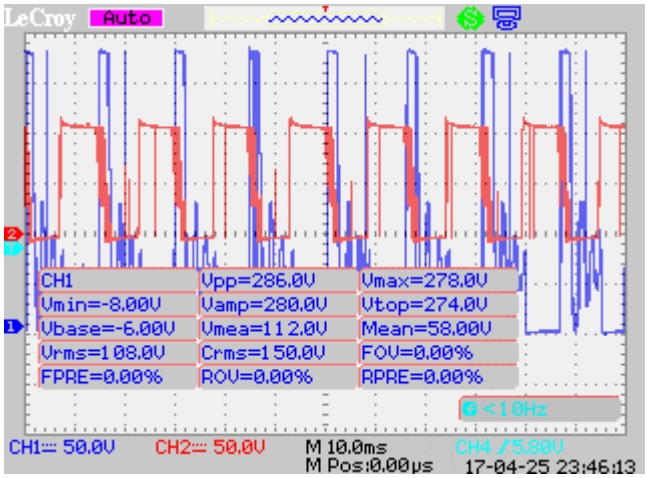
Figure 5.8 shows the drain-to-source voltage waveforms of the MOSFETs at 20 W power-load. Figure 5.8 (a) shows the drain-to-source voltage waveforms of the MOSFETs, Figure 5.8 (b) shows the drain-to-source voltage waveforms and the voltage measurements of the voltage waveform captured at CH1 and Figure 5.8 (c) shows the drain-to-source voltage waveforms and the voltage measurements of the voltage waveform captured at CH2. The waveform captured at CH1 corresponds to the voltage measured between the drain and source of the MOSFET on the inner boost leg. While the waveform captured at CH2 corresponds to the voltage measured between the drain and source of the MOSFET on the outer boost leg. The voltage measurements of the voltage waveform captured at CH1 are displayed in blue, while those of the voltage waveform captured at CH2 are displayed in red.

The results show that the drain-to-source voltage waveform captured at CH1 has a mean of 58 V, an amplitude of 280 V, a peak-to-peak of 286.V, a maximum of 278 V and an rms of 108 V. While that captured at CH2 has a mean of 56 V, an amplitude of 110 V, a peak-to-peak of 126 V, a maximum of 118 V and an rms of 76 V.

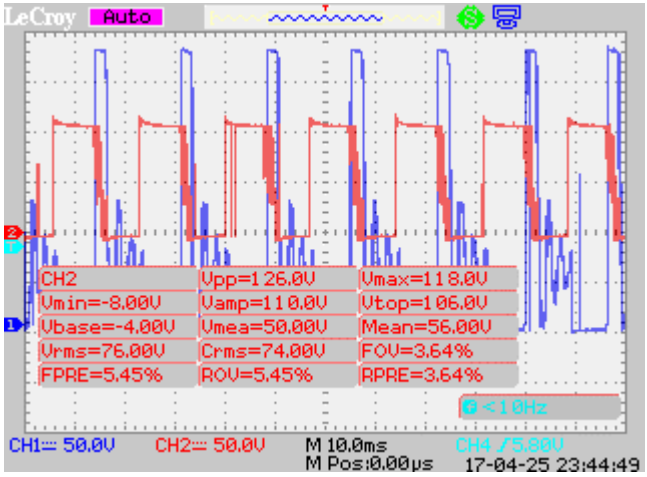
A comparison of the results indicates that the drain-to-source voltage of the waveform captured at CH1 is greater than that at CH2 and has voltage ringing before turn off, while that at CH2 has smooth turn on and turn off transitions. The disparity in the voltage waveforms is due to an imbalance in the voltage sharing between the boost legs of the IBVM converter. While the voltage ringing is attributed to the parasitic elements of the MOSFET and the high voltage that appears across its drain and source.



(a)



(b)



(c)

Figure 5.8: The drain-to-source voltage waveforms of the MOSFETs at 20 W power – load.

(a) The drain-to-source voltage waveforms. (b) The drain-to-source voltage waveforms and the voltage measurements of the voltage waveform captured at CH1. (c) The drain-to-source voltage waveforms and the voltage measurements of the voltage waveform captured at CH2.

Figure 5.9 shows the drain-to-source voltage waveforms of the MOSFETs at 30 W power – load. The waveform captured at CH1 has smooth turn on transitions and develops ringing before turn off, while that captured at CH2 has smooth turn on and turn off transitions

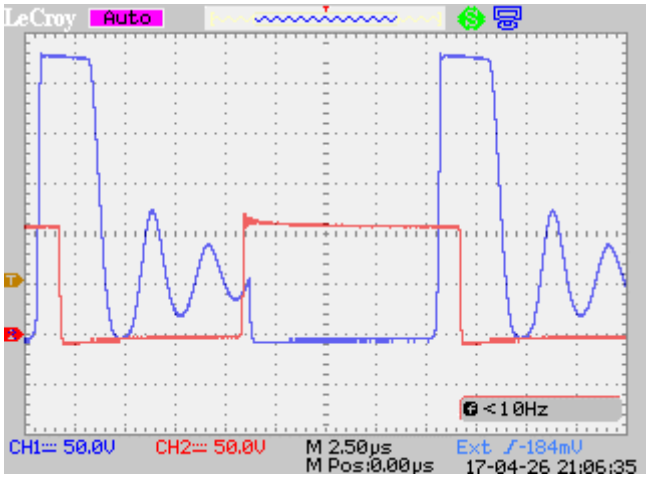
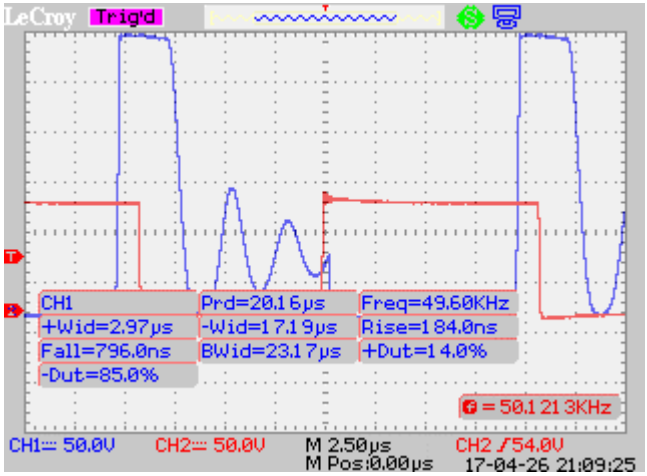


Figure 5.9: The drain-to-source voltage waveforms of the MOSFETs at 30 W power – load.

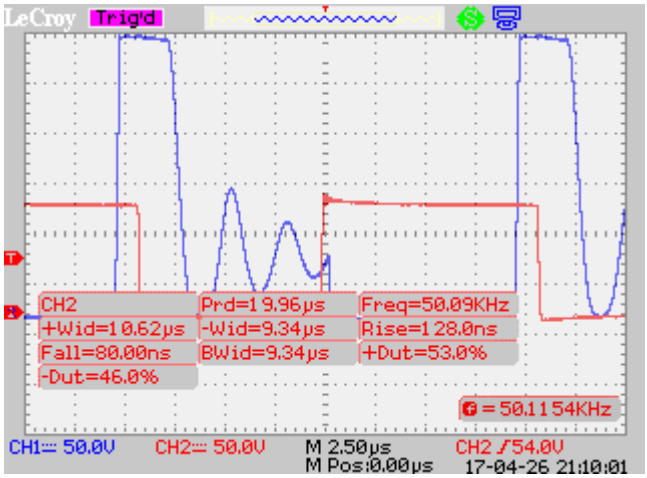
Figure 5.10 shows the frequency and the time measurements of the drain-to-source voltage waveforms of the MOSFETs at 30 W power- load. Figure 5.10 (a) shows the frequency and the time measurements of the drain-to-source voltage waveform captured at CH1 and Figure 5.10 (b) shows the frequency and the time measurements of the drain-to-source voltage waveform captured at CH2.

The results show that the drain-to-source voltage waveform captured at CH1 has a frequency of 49.60 kHz, a duty cycle of 14 % and a period of 20.16 µS . While that captured at CH2 has a frequency of 50.09 kHz, a duty cycle of 53 % and a period of 19.96 µS .

A comparison of the results shows that the on time duty cycle of the waveform captured at CH1 is less than that of the waveform at CH2. This is so because the voltage ringing in the drain-to-source voltage of the MOSFET on the inner boost leg reduces the on-time duty cycle of the drain-to-source voltage by inducing early turn off transitions.



(a)



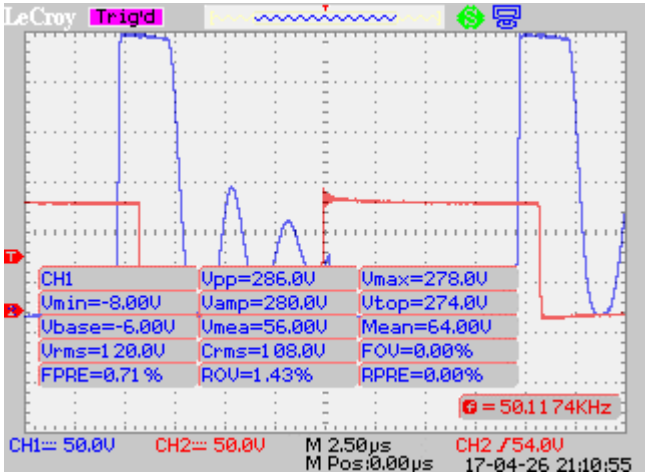
(b)

Figure 5.10: The frequency and the time measurements of the drain-to-source voltage waveforms of the MOSFETs at 30 W power – load.

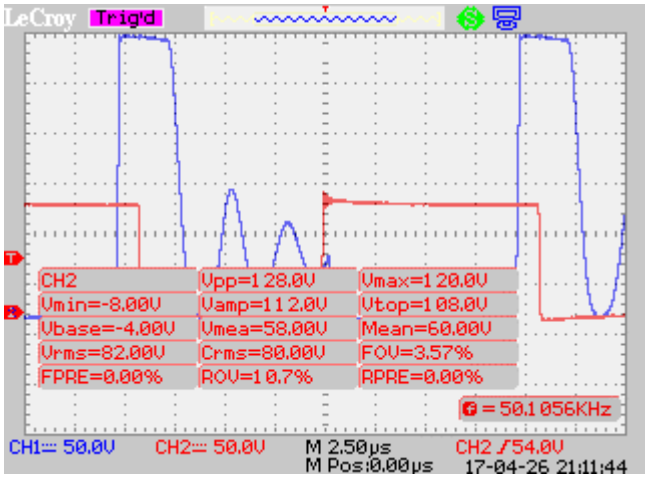
(a) The frequency and the time measurements of the drain-to-source voltage waveform captured at CH1. (b) The frequency and the time measurements of the drain-to-source voltage waveform captured at CH2.

Figure 5.11 shows the voltage measurements of the drain-to-source voltage waveforms of the MOSFETs at 30 W power – load. Figure 5.11 (a) shows the voltage measurements of the drain-to-source voltage waveform captured at CH1 and Figure 5.11 (b) shows the voltage measurements of the drain-to-source voltage waveform captured at CH2.

The results show that the drain-to-source voltage captured at CH1 has a mean of 64 V, an amplitude of 280 V, a peak-to-peak of 286 V, a maximum of 278 V and an rms of 120 V. While the drain-to-source voltage captured at CH2 has a mean of 60 V, an amplitude of 112 V, a peak-to-peak of 128 V, a maximum of 120 V and an rms of 82 V.



(a)



(b)

Figure 5.11: The voltage measurements of the drain-to-source voltage waveforms of the MOSFETs at 30 W power – load.

(a) The voltage measurements of the drain-to-source voltage waveform captured at CH1. (b) The voltage measurements of the drain-to-source voltage waveform captured at CH2.

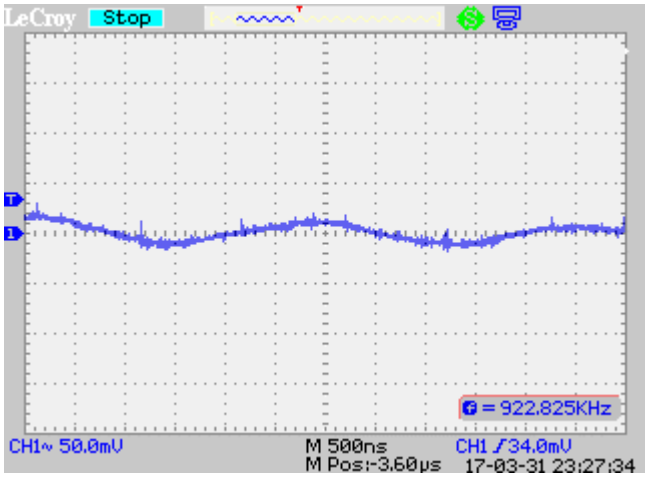
5.3.3 The inductors current ripple

Figure 5.12 shows the voltage waveforms corresponding to the inductors current ripple. Figure 5.12 (a) shows the voltage waveform corresponding to the inductor current ripple of L_1 and Figure 5.12 (b) shows the voltage waveform corresponding to the inductor current ripple of L_2. The voltage waveforms were captured across an LTSR 25-NP current sensor connected in series with the respective inductor. The LTSR 25-NP gives out an output voltage corresponding to the inductor current ripple. The average inductor current is by

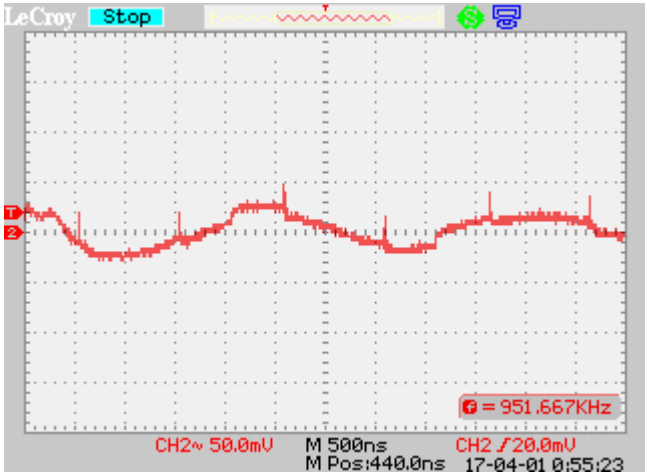
$$I_{average} = \frac{V_{sensor}}{V_R} \times I_{max}, \qquad (5.2)$$

where V_{sensor} is the sensor output voltage, V_R is the sensor reference voltage specified as 2.5 V and I_{max} is the maximum measureable current of the sensor specified as 25 A.

The results show that the voltage corresponding to the inductor current of L_1 given in Figure 5.12 (a) is equal to 68 mV, while that corresponding to the inductor current ripple of L_2 given in Figure 5.12 (b) is equal to 40 mV. The average inductor currents are determined by using Eq. (5.2) and they given as 0.68 A and 0.4 A. The results also show that the inductors current ripple are out of phase, as discussed is chapter 3 and 4, this is desirable for the reduction of the PEMFC stack output current ripple.



(a)



(b)

Figure 5.12: The voltage waveforms corresponding to the inductors current ripple. (a) The voltage waveform corresponding to the inductor current ripple of L_1. (b) The voltage waveform corresponding to the inductor current ripple of L_2.

5.3.4 The PEMFC stack output voltage, the voltage across C_3 and the output voltage of the IBVM converter prototype circuit

Figure 5.13 shows the voltage waveform and the voltage measurements of the PEMFC stack output voltage at no-load. The results show that at no-load, the stack has a mean of 64 V, an amplitude of 4 V, a peak-to-peak of 4 V, a maximum of 66 V and an rms of 64 V.

The results indicate that the maximum measured stack output voltage at no-load is 1 V less than the maximum stack output voltage specified in the user manual.

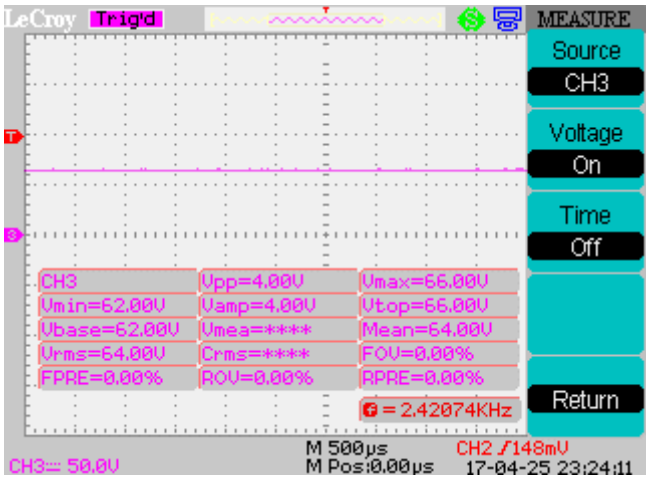
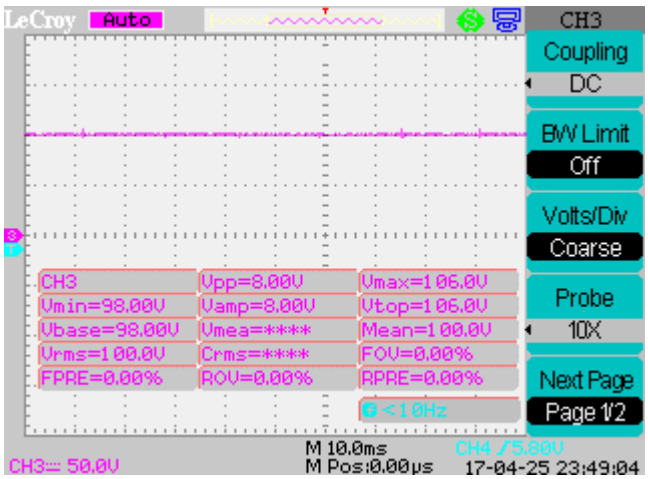


Figure 5.13: The voltage waveform and the voltage measurements of the PEMFC stack output voltage at no-load.

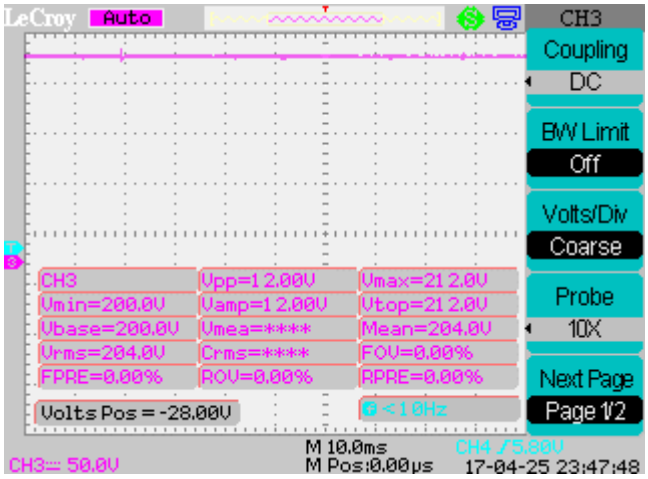
Figure 5.14 shows the voltage waveforms and the voltage measurements of the voltage across C_3 and the output voltage of the IBVM converter prototype circuit at 20 W power – load. Figure 5.14 (a) shows the voltage waveform and the voltage measurements of the voltage across C_3 and Figure 5.14 (b) shows the voltage waveform and the voltage measurements of the output voltage of the IBVM converter.

The results show that the voltage across C_3 has a peak-to-peak of 8 V, a mean of 100 V, an amplitude of 8 V, a maximum of 106 V and an rms of 100 V. While the IBVM converter output voltage has a peak-to-peak of 12 V, a mean of 204 V, an amplitude of 12 V and an rms of 204 V. The measured voltage across all capacitors was equal.

A comparison of the voltage across C_3 and the converter output voltage indicates that the converter output is approximately twice to that of C_3. This validates the analysis of the voltage-balancing feature of the IBVM converter carried out in chapter 3.



(a)



(b)

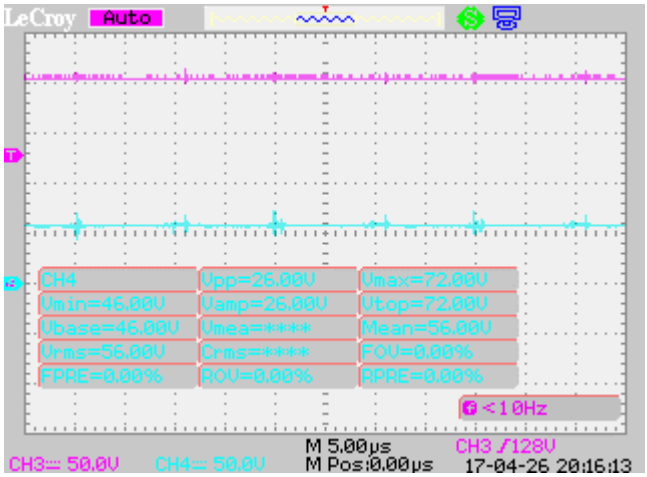
Figure 5.14: The voltage waveforms and the voltage measurements of the voltage across C_3 and the output voltage of the IBVM converter prototype circuit at 20 W power – load.

(a) The voltage waveform and the voltage measurements of the voltage across C_3. (b) The voltage waveform and the voltage measurements of the output voltage of the IBVM converter.

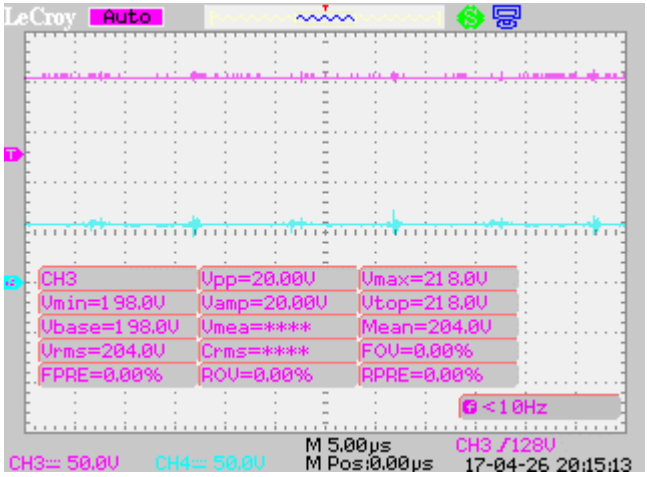
Figure 5.15 shows the voltage waveforms and the voltage measurements of the PEMFC stack output voltage and the output voltage of the IBVM converter prototype circuit at 30 W power – load. Figure 5.15 (a) shows the output voltage waveforms and the voltage measurements of the PEMFC stack output voltage captured at CH4 and Figure 5.15 (b) shows the output voltage waveforms and the voltage measurements of the output voltage of the IBVM converter prototype circuit captured at CH3. In the diagram, the pink waveform corresponds to the output voltage of the IBVM converter, while the aqua waveform corresponds to the PEMFC stack output voltage.

The results show that the PEMFC stack output voltage has a peak-to-peak of 26 V, a mean of 56 V, an amplitude of 26 V, a maximum of 76 V and an rms of 56 V. While the

output voltage of the IBVM converter has a peak-to-peak of 20 V, a mean of 204 V, an amplitude of 20 V and an rms of 204 V.



(a)



(b)

Figure 5.15: The voltage waveforms and the voltage measurements of the PEMFC stack output voltage and the output voltage of the IBVM converter prototype circuit at 30 W power – load.

(a) The voltage waveforms and the voltage measurements of the PEMFC stack output voltage captured at CH4. (b) The voltage waveforms and the voltage measurements of the output voltage of the IBVM converter prototype circuit captured at CH3.

5.4 Conclusion

Specific experimental measurements were carried out in order to evaluate the performance of the PEMFC stack and the IBVM converter prototype circuit, and to verify the simulation results of the converter. The results obtained show that the output voltage of the IBVM converter corresponds to that given in the converter design specifications and that it is stable over a range of power – load, regardless of variations in the PEMFC stack output voltage. This is proof that the modelling, the design and the simulation results of the converter are valid, and that the system works. The results

also show that there is a disparity between the drain-to-source voltages of the MOSFETs due to an imbalance in the voltage sharing between the inner boost leg and the outer boost leg of the converter. As a result, voltage ringing develops in the drain-to-source voltage of the MOSFET on the inner boost leg of the converter.

CHAPTER 6
CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

The main objective of the research given in chapter one was to stabilise the output voltage of a FC stack, and to design and develop a converter prototype circuit for a 1 kW PEMFC stack power supply unit. Specific design goals were outlined such as stable converter output voltage and low PEMFC stack output current ripple, and then particular aims were outlined and carried out in order to achieve the objective of the research. These included a literature review in chapter two of the past and present converter topologies that are used in FC power conditioning.

In chapter three, the large and small signal models, the dynamic and parameter equations, the DC transfer functions and the small signal transfer functions of the ICFFB, the boost, the sepic and the IBVM converter topologies were derived. The values of the parameters and components for the power stage of each topology were also calculated by using the derived component and parameter equations.

In chapter four the design of converter controllers, the simulation of the converter models and the relative evaluation of the converters performance and simulation results were covered. The simulation results obtained for a 1 kW PEMFC stack power supply unit indicate that the FC stack output voltage was stabilised and that the stack output current ripple and output voltage ripple were reduced. The results also indicate that the IBVM converter offers low FC stack output current ripple, low FC stack output voltage ripple and high DC voltage gain compared to the other topologies.

Furthermore, the experiment of the IBVM converter prototype circuit was covered in chapter five. Several experimental measurements were carried out in order to evaluate the performance of the 1 kW PEMFC stack and the IBVM converter prototype circuit, and to verify the simulation results. However, as a safety measure: the converter maximum load was set to 30 W, instead of 1 kW, due to limitations in the power handling capability of the PCB. Nevertheless, the simulation results shows 1 kW and 200 V as specified, while the experimental results shows 30 W and 200 V respectively. The experimental results show that: the stack output current ripple was reduced, the output voltage of the converter corresponds to that given in the converter design specifications and that it was stabilised at the desired output voltage level regardless of variations in the PEMFC stack output voltage. The results also show that there is a disparity between the drain-to-source voltages of the MOSFETs due to an imbalance in the voltage sharing between the inner and outer boost legs of the converter.

Lastly, a comparison of the simulation and the experimental results of the IBVM converter output voltage correlates. This confirms that the mathematical modelling and power stage design, the controller design and the simulations results of the system are valid. However, I reiterate that even though the experiment could only reach 30 W due to PCB limitations, the experiment is deemed to work as the simulation and therefore, the research objective to design and develop a converter prototype circuit for a 1 kW PEMFC stack power supply unit was achieved.

6.2 Recommendations

The future research needs to consider solutions that will eliminate or reduce the imbalance in the voltage sharing between the boost legs of the IBVM converter and the disparity between the drain-to-source voltages of the MOSFETs.

BIBLIOGRAPHY

Abdeen, M., 2008. Green energies and the environment. *Renewable and Sustainable Energy Reviews,* September, 12(7), pp. 1789-1821.

Abd, E. M., Ahmed, M. & Mahmoud, S., 2014. Effect of process parameters on the dynamic behavior of polymer electrolyte membrane fuel cells for electric vehicle applications. *Ain Shams Engineering Journal,* 5(1), pp. 75-84.

Andrea, C., 2011. *Stability of Peak-Current-Controlled fourth order Step Up / Down DC/DC converters,* Salerno: University of Salerno.

An-Yeol, J., Joung-Hu, P. & Hee-Jong, J., 2013. Analysis and design of phase-interleaving series-connected module-integrated converter for DC-link ripple reduction of multi-stage photovoltaic power systems. *Progress in Photovoltaics: Research and Applications,* 21(5), p. 1189–1203.

B.T.Lynch, 2008. *Under the hood of a DC/DC Boost converter,* Dallas,Texas: Texas Instruments.

Ben-Yaakov, S. & Adar, D., 1994. *Average models as tools for studying the dynamics of switch mode DC-DC converters.* Taipei, s.n.

Brooke, S., 2007. *Fuel cell.* [Online]
Available at: http://www.britannica.com/EBchecked/topic/221374/fuel-cell
[Accessed 25th February 2014].

Bryant, B. & Kazimierczuk, M., 2004. *Small-signal duty cycle to inductor current transfer function for boost PWM DC-DC converter in continuous conduction mode.* s.l., s.n.

Bryant, B. & Kazimierczuk, M., 2005. Open-Loop Power-Stage Transfer Functions Relevant to Current-Mode Control of Boost PWM Converter Operating in CCM. *IEEE Transactions on Circuits and Systems I: Regular Papers,* 52(10), pp. 2158 - 2164.

Bryant, B. & Kazimierczuk, M., 2007. Voltage-Loop Power-Stage Transfer Functions With MOSFET Delay for Boost PWM Converter Operating in CCM. *IEEE Transactions on Industrial Electronics ,* 54(1), pp. 347 - 353.

C.A.Ramos-Paja & E. Arango, R. G. A.-M. C. C., 2011. DC/DC pre-regulator for input current ripple reduction and efficiency improvement. *Electric Power Systems Research,* 81(11), p. 2048–2055.

Carbon Trust Advisory, 2013. *Rural Electrification in South Africa with Platinum-Based Fuel Cells using Methanol Fuel,* Johannesburg: Anglo American Platinum,Ballard Power Systems.

Changrong, L. & Jih-Sheng, L., 2007. Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load. *IEEE Transactions on Power Electronics,* 22(4), pp. 1429-1436.

Changrong, L. & Jih-Sheng, L., 2007. Low Frequency Current Ripple Reduction Technique With Active Control in a Fuel Cell Power System With Inverter Load. *IEEE Transactions on Power Electronics,* 22(4), pp. 1429 - 1436.

Cheng, K., Sutanto, D., Ho, Y. & Law, K., 2001. *Exploring the power conditioning system for fuel cell.* Vancouver, IEEE 32nd Annual Power Electronics Specialists Conference, pp. 2197-2202.

Chevron, 2013.Chevron. [Online]
Available at: http://www.chevron.com/globalissues/energysupplydemand/
[Accessed 20 Feb 2014].

Czarlcowslci, D. & Kazimierczuk, M. K., 1992. *SPICE COMPATIBLE AVERAGED MODELS OF PWM FULL-BRIDGE DC-DC CONVERTER.* San Diego, IEEE, pp. 488 - 493.

Dervisoglu, R., 2012. *Wikipedia.* [Online]
Available:http://en.wikipedia.org/wiki/File:Solid_oxide_fuel_cell_protonic.svg
[Accessed 21st February 2014].

Dixon, L. H. J., 1983. *Closing the feedback loop,* s.l.: s.n.

Dr.Ray, R., 2006. Analyzing the Sepic Converter. *Power Systems Design Europe*, 6 November, pp. 14 - 18.

Eliana, A., Javier, C. & Roberto, G., 2010. *Asymmetric interleaved DC-DC switching converters:Generation, Modelling and Control.* 1st ed. Saarbrucken: LAP Lambert Academic Publishing.

Farooque, M. & Maru, H., 2002. Fuel cells-the clean and efficient power generators. *proceedings of the IEEE,* 89(12), pp. 1819-1829.

Geethalakshmi, B. & Sreeram, P., 2014. *Modeling and analysis of an integrated PV array and SEPIC converter.* Kanyakumari, IEEE.

Gert, K. A., Christian, K., Sgren, B. & Frede, B., 2002. *A new green power inverter for fuel cells.* Aalborg East, IEEE, pp. 727-733.

Haiping, X., Xuhui, W. & Li, K., 2004. *Dual-phase DC-DC converter in fuel cell electric vehicle.* CELAYA, IEEE Proceedings from International Power Electronics Congress.

Hangseok, C., 2011. *Practical Feedback Loop Design Considerations for Switched Mode Power Supplies,* s.l.: Fairchild Semiconductor.

Horizon Fuel Cell Technologies, 2013. [Online]
http://media.wix.com/ugd/047f54_86b712599dda8542adcca251d9904ca4.pdf.
Available at: http://www.horizonfuelcell.com/
[Accessed 21 February 2014].

J. S. Anu, R., Kanagapriya, T. & Seyezhai, R., 2012. *Design and analysis of Interleaved Boost Converter for renewable energy source.* Kumaracoil, IEEE, pp. 447 - 451.

J.Larminie & A.Dicks, 2003. *Fuel Cell Systems Explained.* 2nd ed. Chichester: John Wiley & Sons Ltd.

James, E., Chris, N. & Paul, H., 2007. An emerging market in fuel cells? Residential combined heat and power in four countries. *Energy Policy,* 35(4), pp. 2173-2179.

Jin, W. et al., 2004. Low cost fuel cell converter system for residential power generation. *IEEE Transactions on Power Electronics,* 19(5), pp. 1315-1322.

Kazimierczuk, M. K., 2000. Transfer function for current modulator in PWM converters with current-mode control. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* 47(9), pp. 1407 - 1412.

Kazimierczuk, M. K., 2008. *Pulse-width Modulated DC-DC Power Converters.* Ohio: John Wiley and Sons.

Kirubakaran, A., Shailendra, J. & Nema, R., 2009. A review on fuel cell technologies and power electronic interface. *Renewable and Sustainable Energy Reviews,* 13(9), pp. 2431-2432.

Kittipeerachon, K. & Bunlaksananusorn, C., 2004. *FEEDBACK COMPENSATION DESIGN FOR SWITCHED MODE POWER SUPPLIES WITH A RIGHT-HALF-PLANE (RHP) ZERO.* s.l., s.n., pp. 236 - 241.

Kittipeerachon, K. & Bunlaksananusorn, C., 2004. *Practical compensation circuit design of switched mode power supplies.* Singapore, IEEE Conference on Power Electronics and Drive Systems.

Kong, X., T.Choi, L. & M.Khambadkone, A., 2004. *Analysis and control of isolated current-fed full bridge converter in fuel cell system.* Busan, IEEE, pp. 2825-2830.

Larmine, J. & Dicks, A., 2003. *Fuel cell systems explained.* 2nd ed. Chichester: Wiley.

Lepiller, C., 2010. *Fuel Cell Basics.* [Online]
Available at: http://www.pragma-industries.com/reports/fuel-cell-explained/#Applications
[Accessed Wednesday January 2014].

Maja, H., Leonardo, P. & Prasad, E., 2004. *Design of a wide input range DC-DC converter with a robust power control scheme suitable for fuel cell power conversion.* Texas, Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE, p. 374– 379.

Martin, R., Johannes, v. & Christo, P., 2008. *Full Bridge DC-DC Converter as Input Stage for a Fuel Cell based Inverter System.* Durban, SATNAC.

Matheepot, P., Wattana, K. & Phatiphat, T., 2013. *Study of Two-phase Interleaved Boost Converter using coupled inductors for Fuuel cell.* Krabi, IEEE, pp. 1 - 6.

Michael, W. E., Michael, R. & Douglas, J., 2001. Fuel Cell Systems: Efficient, Flexible Energy Conversion for the 21st Century. *Proceedings of the IEEE,* 89(12), pp. 1808-1816.

Middlebrook, R., 1989. Modeling current-programmed buck and boost regulators. *IEEE Trans. Power Electron.,* 4(1), p. 36–52.

Middlebrook, R. & Cuk, S., 1976. *A general unified approach to modeling switching converter power stages.* Cleveland, OH, s.n.

Middlebrook, R. D., 1987. Topics in multiple-loop regulators and currentmode currentmode. *IEEE Trans. Power Electron.,* 2(1), p. 109–124.

Miranda, U., Bellar, M., da Silva Neto, J. & Aredes, M., 2006. *Evaluation of Reduced Component Count Converters for Low Harmonic Distortion AC Drive Systems.* Montreal, IEEE, pp. 2504 - 2509.

Mushsin, T. & Zehra, U., 2009. Design of a PEM fuel cell system for residential application. *International Journal of Hydrogen Energy,* 34(12), pp. 5242-5248.

O.Alavi & S.Dolatabadi, 2015. Analysis and Simulation of Full-Bridge Boost Converter using Matlab. *BALKAN JOURNAL OF ELECTRICAL & COMPUTER ENGINEERING (bajece),* 3(2), pp. 64-69.

Omar, H., Joeri, V. & Philippe, L., 2012. Analysis, Modeling, and Implementation of a Multidevice Interleaved DC/DC Converter for Fuel Cell Hybrid Electric Vehicles. *IEEE Transactions on Power Electronics ,* 27(11), pp. 4445 - 4458.

Palma, L., 2012. *DC/DC converter topology selection for low frequency ripple reduction in PEM fuel cell applications.* Sorrento, IEEE.

Palma, L., 2013. *Current Source Converter Topology Selection for Low Frequency Ripple Current Reduction in PEM Fuel Cell Applications.* Vienna , Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE , pp. 1577 - 1582.

Ralph, E. & Robert, N., 2013. *World Energy Resources ,* London: World Energy Council.

Ridley, R., 1990. *A New Small-Signal Model for Current-Mode Control,* Blacksburg: Virginia Polytechnic Institute and State University.

Ridley, R., 1991. A New, Continuous-Time Model For Current-Mode Control. *IEEE TRANSACTIONS ON POWER ELECTRONICS,* 6(2), pp. 271-280.

Ridley, R., 1999. *An Accurate and Practical Small-Signal Model for Current-Mode Control,* Camarillo: Ridley Engineering , Inc..

Robert, W. E. & Dragan, M., 2001. *Fundamentals of Power Electronics.* 2nd ed. New York: KLUWER ACADEMIC PUBLISHERS.

Rosas-Caro, J. C. et al., 2011. A Family of DC-DC Multiplier Converters. *Engineering Letters,* 19(57), pp. 1-11.

Rosas-Caro, J. C. et al., 2011. *Hybrid Voltage-Multipliers Based Switching Power Converters.* Tlajomulco de Zúñiga, American Institute of Physics, pp. 29-43.

Rosas-Caro, J. C., Ramirez, J. M., Peng, F. Z. & Valderrabano, A., 2010. A DC–DC multilevel boost converter. *IET Power Electronics,* 3(1), pp. 129 - 137.

S.Kamtip & Bhumkittipich, K., 2011. *Design and Analysis of Interleaved Boost Converter For Renewable Energy Applications.* Chiang Rai, Energy Procedia.

Saijun, Z. & Xiaoyan, Y., 2012. *Design Considerations of the Interleaved Boost.* Scottsdale, IEEE ,34th InternationalTelecommunications Energy Conference (INTELEC), pp. 1- 6.

SAinfo reporter, 2012. *South Africa's energy supply.* [Online]
Available : www.southafrica.info/business/economy/infrastructure/energy.htm
[Accessed 21st February 2014].

Sammes, N. & Boersma, R., 1999. Small-scale fuel cells for residential applications. *Journal of Power Sources,* 1-2(86), pp. 98-110.

Shailendra, J., Jin, J., Xinhong, H. & Srdja, S., 2012. Modeling of Fuel-Cell-Based Power Supply System for Grid Interface. *IEEE Transactions on Industry Applications,* 48(4), pp. 1142 - 1153.

Shailendra, J., Jin, J., Xinhong, H. & Srdja, S., 2012. Modeling of Fuel-Cell-Based Power Supply System for Grid Interface. *IEEE Transactions on Industry Applications,* 48(4), p. 1142.

Smithsonian Institute, 2008. *Smithsonian National Museum of America.* [Online]
Available at: http://americanhistory.si.edu/fuelcells/basics.htm
[Accessed 21st February 2014].

Takuya, O., Atushi, A. & Takao, K., 2007. Potential Evaluation of Energy Supply System in Grid Power Systems ,Commercial, and Residential Sectors by Minimizing Energy Cost. *Electrical Engineering in Japan,* 160(2), pp. 9-18.

Tan, F. & Middlebrook, R., 1995. A unified model for current-programmed converters. *IEEE Transactions on Power Electronics,* 10(4), pp. 397 - 408.

Tanrioven, M. & Alam, M., 2006. Modeling,Control, and Power Quality Evaluation of a PEM Fuel Cell-Based Power Supply System for Residential Use. *IEEE Transactions on Industry Applications ,* 42(6), pp. 1582-1583.

Tanrioven, M. & Alam, M. S., 2006. Modeling, Control, and Power Quality Evaluation of a PEM Fuel Cell-Based Power Supply System for Residential Use. *IEEE Transactions on Industry Applications ,* 42(6), pp. 1582 - 1589.

Texas Instruments, 2013. *MIXED SIGNAL MICROCONTROLLER,* Dallas: Texas Instruments semiconductor products.

Thomas, A., Goran, A. & Lennart, S., 2001. Distributed generation:a defination. *Electric Power Systems Research,* 57(3), pp. 195-204.

Troy, A. et al., 2002. *Design considerations for 48V fuel cell to split single phase inverter system with ultracapacitor energy storage.* Cairns, Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual, pp. 2007-2012.

US Department of Energy, 2005. *Fuel cell handbook.* 6th ed. Morgantown ,WV: University press of the pacific.

Vatché, V., 2004. *Fast Analytical Techniques for Electrical and Electronic circuits.* 1st ed. Cambridge: Cambridge University Press.

Vatché, V., 2004. *Fast Analytical Techniques for Electrical and Electronic Circuits.* 1st ed. Cambridge: Cambridge University Press.

Vázquez, A., Aguilar, C., Canales, F. & Ponce, M., 2008. *Integrated power conditioner topology for fuel cell based power supply systems.* Rhodes, IEEE ,Power Electronics Specialists Conference, pp. 223-229.

Vázquez-Blanco, A., Aguilar-Castillo, C., Canales-Abarca, F. & Arau-Roffiel, J., 2009. *Two-stage and Integrated Fuel Cell Power Conditioner:performance Comparison.* Washingston, IEEE,Applied Power Electronics Conference and Exposition, pp. 453-455.

Virgilio, V. et al., 2013. Black-Box Behavioral Modeling and Identification of DC-DC converters with Input Current Control for Fuel Cell Power Conditioning. *IEEE Transactions on Industrial Electronics,* 61(4), p. 1891.

Vorpérian, V., 1990. Simplified analysis of PWM converters using model of PWM switch. Part I. *IEEE Transactions on Aerospace Electronics System,* 25(9), p. 490–496.

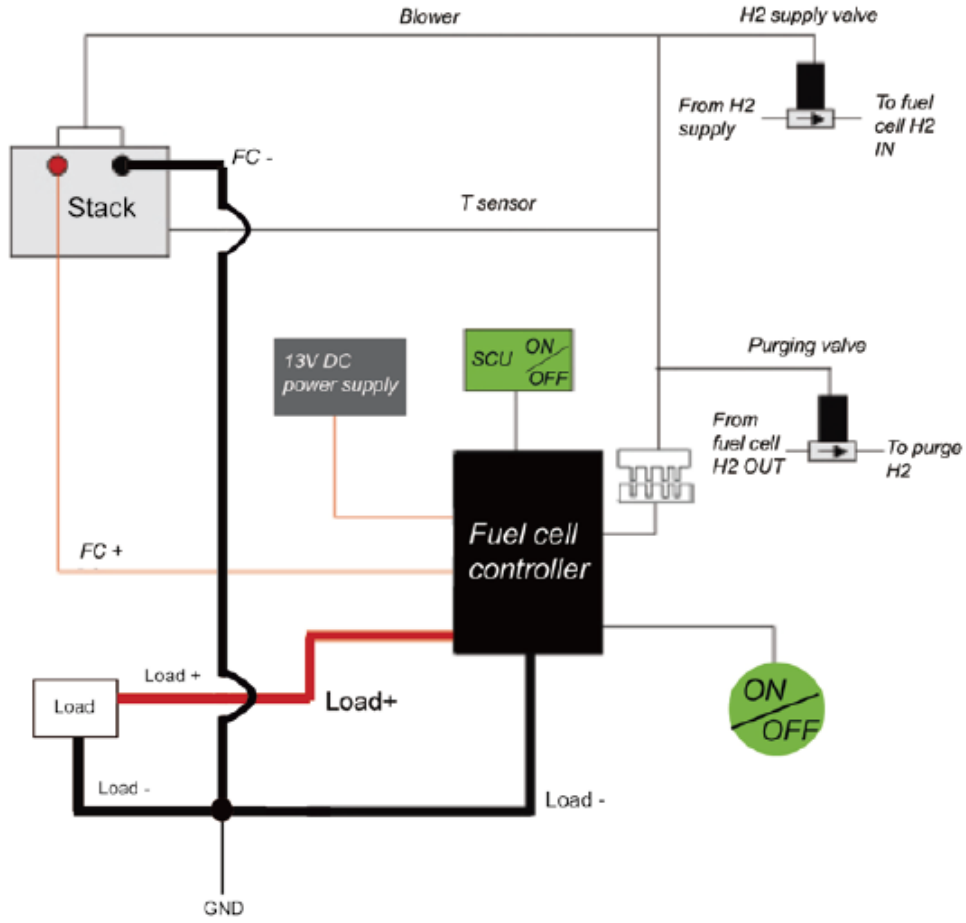
Wikipedia, 2014. *Wikipedia.* [Online]
Available at: http://en.wikipedia.org/wiki/Load_profile
[Accessed 16 March 2014].

Young-Sang, K. et al., 2012. *Design and efficiency analysis of stand-alone power conditioning system for fuel-cell.* Seoul, IEEE , Vehicle Power and Propulsion Conference (VPPC), pp. 1357 - 1361.

Yu, X., Starke, M., Tolbert, L. & Ozpineci, B., 2007. Fuel cell power conditioning for electric power applications: a summary. *IET Electrical Power Applications,* 1(5), pp. 643-656.

APPENDICES

Appendix A: H-1000 PEMFC stack system setup



SCU: Short Circuit Unit
GND: Grounding

Appendix B: H-1000 PEMFC stack technical specifications

Type of fuel cell	PEM
Number of cells	48
Rated Power	1000W
Performance	28.8V @ 35A
H2 Supply valve voltage	12V
Purging valve voltage	12V
Blower voltage	12V
Reactants	Hydrogen and Air
External temperature	5 to 30ºC
Max. stack temperature	65ºC
H2 Pressure	0.45-0.55bar
Hydrogen purity	≧99.995% dry H2
Humidification	self-humidified
Cooling	Air (integrated cooling fan)
Stack weight (with fan & casing)	4000 grams(±100grams)
Controller weight	400 grams(±30grams)
Dimension	23.3cm x 26.8cm x 12.3cm
Flow rate at max output*	13 L/min
Start up time	≦30S at ambient temperature
Efficiency of stack	40% @ 28.8V
Low voltage shut down	24V
Over current shut down	42A
Over temperature shut down	65℃
External power supply**	13V(±1V),8A

*The flow rate may change with the power output
**System electronics need external power supply
*** The Specification is subject to change without notice.

Appendix C: MATLAB M-FILE Codes

Appendix C1: Code for the design of the ICFFB converter controller

```
Clc %clear screen

VI = 36; % Input voltage
Vo = 100; %Output voltage
rC = 0.0177; % Series equivalent resistance of the output Capacitor
D = 0.679; % The maximum duty cycle full load
rL = 0.1; %The Inductor series equivalent resistance
R = 11.11; % The load resistor at full load
C = 250e-6; % Capacitance of the output capacitor
L = 57.67e-3; % inductance of the input inductor
rM =0.1; %MOSFET series resistance
rD = 0.1; %Diode forward resistance
Vf = 1; % Diode forward voltage drop
r = ((rM*D)+((1-D)*rD)+rL) % The total parasitic resistance
s = tf('s');
Vtm = 2.5; % Amplitude of modulator voltage
% damping ratio
```

```
Zeta = (C*((r*(R+rC))+(((1-D)^2)*(R*rC)))+L)/(2* sqrt(((L*C)*(R+rC))*((R*(1-D)^2)+r)))
Q = 1/(2*Zeta) % quality factor
fc = 200%((R*(1-D)^2)-r)/(2*pi*L)% 1e3 ;
wc = 2*pi*fc % Controller cross over frequency in rad/s
Zn = -(1/(C*rC)) % LHP zero in rads/s
wzn = -Zn % Frequency of LHP in rad/s
fzn = 1/(2*pi*C*rC) % frequency of the LHP zero
Zp =((R*(1-D)^2)-r)/L % RHP zeroin rad/s
wzp = Zp % Frequency of RHP in rad/s
fzp =((R*(1-D)^2)-r)/(2*pi*L) %frequency of the RHP
FO = (1/(2*pi))*sqrt(((R*(1-D)^2)+r)/(L*C*(R+rC))) %Corner frequency
wo = sqrt(((R*(1-D)^2)+r)/(L*C*(R+rC))) % corner frequency in rad/s
Tm = 1/Vtm % Transfer function of modulator
PM = 60; % Desired phase of Vo
Tpx = (-(Vo*rC)/((1-D)*(R+rC))) % Magnitude of output-to-control T.F
Den2 = (C*((r*(R+rC))+(((1-D)^2)*(R*rC)))+L)/((L*C)*(R+rC))
Den1 = (r+(((1-D)^2)*R))/((L*C)*(R+rC))
Num = (s+(1/(C*rC)))*(s-(1/L)*(R*(1-D)^2)-r)
Den = s^2+(s*Den2)+Den1
Tp = Tpx*(Num/Den) % Converter powerstage control-to-output T.F


% Define parameters for the design of the double lead controller
Vref = 2.5 % reference voltage of the error amplifier
Beta = Vref/Vo % transfer function of the feedback network
R1 = 1.2e6;
RB = 1e3;
RA = RB*((1/Beta)-1)
h11 = (RA*RB)/(RA+RB) %h-parameter feedback network gain

%Transfer functions of the controller
Tmp = Tm*Tp%vo(s)/vc(s).Transfer function (T.F) of modulator and ICFFB power stage
Tk = Tm*Tp*Beta ; % vf(s)/vc(s). Modulator,power-stage and feedback network T.F
QTk = -180 + (atand(fc/fzn))-(atand(fc/fzp))-(atand(((2*Zeta*fc)/fo)/(1-((fc/fo)^2))))%
Phase of Tp for (w/wo)>=1.

Qm = PM-QTk-90 % Required phase boost from the controller
K = tand((Qm/4)+ 45)^2;% Controller phase boost

% The frequencies of the poles and zeros of the controller
fzc = fc/(sqrt(K))
fpc = fc*(sqrt(K))

%T.F magnitude for the pulse-width modulator,power stage and feedback network
Tko = ((Beta*Vo)/(Vtm*(1-D)))*(((R*(1-D)^2)-r)/((R*(1-D)^2)+r))
Tkm=Tko*(((sqrt(1+(fc/fzn)^2))*(sqrt(1+(fc/fzp)^2)))/(sqrt((1-
(fc/fo)^2)^2+((2*Zeta*fc)/fo)^2)))
Tc = 1/Tkm

% Calculation of Controller resistors and capacitors
R3 = (R1*(R1-(h11*(K-1))))/((K-1)*(R1+h11))
C2 = Tkm/(wc*(R1+h11))
C1 = C2*(K-1)
R2 =(sqrt(K))/(wc*C1)
C3 = (R1+h11)/(wc*(sqrt(K))*((R1*R3)+(h11*(R1+R3))))

%Calculation converter impedances
```

```
Zf = (s + (1/(R2*C1)))/(s*C2*(s+((C1+C2)/(R2*C1*C2)))) %Feedback Impendance
Zi=(h11+((R1*R3)/(R1+R3)))*((s+((R1+h11)/(C3*(R3*(R1+h11)+(h11*R1)))))/(s+(1/(C
3*(R1+R3))))) %Input impedance

%The Loop Gain for converter
Tc = Zf/Zi %The voltage transfer function of controller. vc(s)/ve(s)= -vc(s)/vf(s)= -Av(s).
T = Tc*Tmp*Beta % vf(s)/ve(s).The loop gain of the converter

%The closed-loop control-to-output voltage transfer function
Tcl = (Tc*Tmp)/(1+(Beta*Tc*Tmp)) % vo(s)/vr(s),A(s)/1+Beta*A(s)
Tclo = 1/Beta % The control-to-output transfer function at f = 0

%The open-loop output-to-control voltage transfer function of ICFFB converter
bodeplot(Tp),
```

Appendix C2: Code for the design of the boost converter controller

```
Clc %clear screen
VI = 36; % Input voltage
Vo = 100;  %Converter output voltage
rC = 0.0178; %ESR of the output Capacitor
D = 0.676; % Converter Maximum duty cycle
Dmin = 0.4; %Converter minimum duty cycle
Dbar = (1-Dmin); %
rL = 0.1; % Inductor ESR
R = 11.11; %Load resistor at full load
C =680e-6; % Output capacitor
L =287.91e-6; % Inductor
rM =0.1; % MOSFET series resistor
rD = 0.1; % Diode forward resistor
Vf = 1; % Diode forward voltage drop
r = ((rM*D)+((1-D)*rD)+rL); % Total parasitic resistance
s = tf('s');
Vtm = 2.5; % Amplitude of modulator  voltage
% damping ratio
Zeta = (C*((r*(R+rC))+(((1-D)^2)*(R*rC)))+L)/(2* sqrt(((L*C)*(R+rC))*((R*(1-D)^2)+r)));
Q = 1/(2*Zeta); % quality factor
fc1 = ((R*(1-D)^2)-r)/(2*pi*L);% Frequency of RHP in Hz
fc =0.1*fc1; % Controller cross over frequency
wc = 2*pi*fc % Controller cross over frequency in rad/s
Zn = -(1/(C*rC)) % LHP zero
wzn = -Zn; % Frequency of LHP zero in rad/s
fzn = 1/(2*pi*C*rC); % frequency of the LHP zero in Hz
Zp =((R*(1-D)^2)-r)/L; % RHP zeroin rad/s
wzp = Zp;
fzp =((R*(1-D)^2)-r)/(2*pi*L); %frequency of the RHP in Hz
fo = (1/(2*pi))*sqrt(((R*(1-D)^2)+r)/(L*C*(R+rC))); %Corner frequency
wo = sqrt(((R*(1-D)^2)+r)/(L*C*(R+rC))); % corner frequency in rad/s
Tm = 1/Vtm; % T.F of modulator
PM = 65; % Desired phase of Vo
Tpx = (-(Vo*rC)/((1-D)*(R+rC))); % Magnitude of control-to-output T.F
Den2 = (C*((r*(R+rC))+(((1-D)^2)*(R*rC)))+L)/((L*C)*(R+rC));
Den1 = (r+(((1-D)^2)*R))/((L*C)*(R+rC));
Num = (s+(1/(C*rC)))*(s-(1/L)*(R*(1-D)^2)-r);
Den = s^2+(s*Den2)+Den1;
Tp = Tpx*(Num/Den); %Converter power stage Control-to-output T.F
```

```
% Define parameters for the design of the double lead controller
Vref = 2.5; % reference voltage of the error amplifier
Beta = Vref/Vo; % transfer function of the feedback network
R1 = 1.2e6;
RB = 1e3;%Lower resistor of feedback network
RA = RB*((1/Beta)-1); % Upper resistor of feedback network
h11 = (RA*RB)/(RA+RB); %h parameter of the feedback network gain

%Transfer functions of the controller
Tmp = Tm*Tp;%vo(s)/vc(s). T.F of the pulse width modulator and boost power stage
Tk = Tm*Tp*Beta; % vf(s)/vc(s). Modulator,power-stage and feedback network T.F
QTk = (atand(fc/fzn))-(atand(fc/fzp))-(atand(((2*Zeta*fc)/fo)/(1-((fc/fo)^2))))% Phase of
Tp for (w/wo)<=1.
Qm = PM-QTk-90; % Required phase boost from the controller
K = tand((Qm/4)+ 45)^2; % Controller phase boost

% Frequencies of the poles and zeros of the controller are
fzc = fc/(sqrt(K));
fpc = fc*(sqrt(K));

%Magnitude of the T.F of the pulse-width modulator,power stage and feedback
network
Tko = ((Beta*Vo)/(Vtm*(1-D)))*(((R*(1-D)^2)-r)/((R*(1-D)^2)+r));
Tkm=Tko*(((sqrt(1+(fc/fzn)^2))*(sqrt(1+(fc/fzp)^2)))/(sqrt((1-
(fc/fo)^2)^2+((2*Zeta*fc)/fo)^2)));
Tcfc = 1/Tkm;

% Calculation of Controller resistors and capacitors
R3 = (R1*(R1-(h11*(K-1))))/((K-1)*(R1+h11))
C2 = Tkm/(wc*(R1+h11))
C1 = C2*(K-1)
R2 =(sqrt(K))/(wc*C1)
C3 = (R1+h11)/(wc*(sqrt(K))*((R1*R3)+(h11*(R1+R3))))

%Calculation converter impedances
Zf = (s + (1/(R2*C1)))/(s*C2*(s+((C1+C2)/(R2*C1*C2)))); % Feedback Impendance
Zi=(h11+((R1*R3)/(R1+R3)))*((s+((R1+h11)/(C3*(R3*(R1+h11)+(h11*R1)))))/(s+(1/(C
3*(R1+R3))))); % Input Impendance

%The Loop Gain converter
Tc = Zf/Zi %Controller voltage controller T.F. vc(s)/ve(s)= -vc(s)/vf(s)= -Av(s).
T = Tc*Tmp*Beta % vf(s)/ve(s).The loop gain for the boost converter

%The closed-loop control-to-output voltage transfer function
Tcl = (Tc*Tmp)/(1+(Beta*Tc*Tmp)); % vo(s)/vr(s),A(s)/1+Beta*A(s)
Tclo = 1/Beta; % The control-to-output transfer function at f = 0

%The open-loop control-to-output voltage transfer function
bodeplot(Tp)
```

Appendix C3: Code for the design of the sepic converter controller

```
Clc % Clear screen
s=tf('s');
Vin = 36; % Input voltage
Vo = 100; % Converter output voltage
```

```
Ic = 30 % Total current through the common port of the CC-PWM Switch
Vref = 2.5; %Controller Reference voltage
Vsen = 2.5; % Maxium amplitude of the voltage sensed acrossed the shunt resistor
C1 = 135.914e-6; %Capacitance of the energy transfer Capacitor
C2 = 543.65e-6; % Capacitance of the output capacitor
rC1 = 9.01e-3; %ESR of the energy transfer capacitor
rC2 = 6.81e-3; %ESR of the output capacitor
D =Vo/((0.90*Vin)+Vo); % Converter maximum on time duty cycle
Dbar = (1-D); % Converter minimum off time duty cycle
fs = 50e3; % Converter switching frequency
L1 = 610e-6; %Input inductor
L2 =L1;%Output inductor
R = 11.11; %Load resistor at maximum load
G = 1/R; % Conductance of load resistor
L=(L1*L2)/(L1+L2) % The total inductance of the converter
Ts = 1/fs; % Period of the Converter switching
Qp = 2/pi; % Quality factor
Zeta = 1/(Qp*2); % Damping factor of the converter
Ri = Vsen / Ic; % Value of the shunt resistor
Ko = (1/Ri); % Conductance of the shunt resistor
Vap = Vin + Vo; %Voltage across the active & passive ports of the CC-PWM-Switch
Vac = Vin; % Voltage across the active and common port of the CC-PWM Switch
Vcp = Vo; % Voltage across the common & passive port of the CC-PWM  Switch
Sn =(( Vin*Ri)/L); % Slew rate of the inductor current during on time
Sf = (Vo*Ri)/L; % Slew rate of the inductor current during off time
Se = (Sn*(1+((Qp*pi)/2)))/(Qp*pi*Dbar);%Slope of the external Ramp
Vslope = (Vo*Ri*Ts)/L;
wn = pi/Ts;
He = (1 + (s/(Qp*wn))+(s^2/wn^2)); % Open loop Sampling gain
go = (Ts/L)*(((1-D)*(Se/Sn))+(1/2)-D);
gf = (D*go)-((D*Dbar*Ts)/(2*L));
Ia = Ic*D;
gi =  -(Ia/Vap);
gr =( Ic/Vap);
Gt = (gi+gr+G+(Dbar*(go-gf)));
Ac = (Ko*Dbar)/Gt;
wzn = 1/(rC2*C2); % Real LHPZ
ws = 2*pi*fs; % switching frequency in rad/s
Cs = 4/(L*ws^2) %models subharmonic oscillations of current loop
wp = Gt/(C2+Cs);%deminatant pole of the power stage

%Converter transfer fuctions using the full model equations
a1 = (L1*(D/Dbar)^2 + L2)*(1/R);
a2 = L1*(C1 + ((D/Dbar)^2)*C2 ) + L2*(C1 + C2);
a3 = (L1*L2*C1)/(R*Dbar^2);
a4 = (L1*L2*C1*C2)/(Dbar^2);

Num1 =-(1+s*rC2*C2);
Num2=(1-(s*(L1*(D/Dbar)^2)*(1/R))+(s^2*C1*(L1+L2))-(s^3*(((L1*L2*C1)/R)*
(D/Dbar)^2)));
Ds =  1 + a1*s + a2*s^2 + a3*s^3 + a4*s^4;
Kd = Vin/Dbar^2;

Tp = ( Kd*((Num1*Num2)/Ds)); % Converter power stage control-to-output T.F
bodeplot(Tp);
```

```
wz =(Dbar^2*R)/(L1*D^2);%Real RHPZ
wzn = 1/(rC2*C2); % Real LHPZ
wzc = sqrt(D/(L2*C1));
wzc2 = -sqrt((Dbar^2*R)/(L1*L2*C1*D))
%Quality factor
Qzc = (Dbar^2*R*L1*D^2)/(wzc*((L1^2*D^4)-(Dbar^4*R^2*C1*(L1+L2))));

%Control to output voltage transfer function.
Voc=Ac*(((1+(s/wzn))*(1-(s/2.6e3))*(1-(s/(0.2057*2.98e3))+(s^2/(2.98e3)^2)))/
((1+(s/wp))*(1+(s/(Qp*wn))+(s^2/wn^2))));

% Calculation of Controller resistors and capacitors
Fzea = (1/10)*2.6e3;
Fhf =  27.011e3*0.5;
Rcomp = 1000;
Rfb1 = 39e6;
Gea = Rcomp/RB; % Controller gain
Ccomp = 1/(Fzea*2*pi*Rcomp);
Chf = 1/(2*pi*Rcomp*Fhf);

%Transfer functions of the controller
Tcomp=Gea*((s+(1/(Rcomp*Ccomp)))/(Chf*h11*s*(s+((Ccomp+Chf)/(Chf*Ccomp*Rc
omp)))))
%The Loop Gain for the sepic converter
T = Tcomp*Voc;
```

Appendix C4: Code for the design of the IBVM converter controllers

```
clc % Clear screen
s=tf('s');
Vin = 36; % Converter Input voltage
Vo = 200; %Converter output voltage
Vsen = 2.5; % Maximum amplitude of the voltage sensed acrossed the shunt resistor
C= 680e-6;%Capacitance of C1,C2 and C3.
Ceq =((Ceq*Ceq)/(Ceq+Ceq)); %Equivalent capacitance at the output node
rC = 2*17.8e-3;%ESR of the Capacitors at the output node
rL = 0.1; % Inductor ESR
rM =0.1; % Series resistor of MOSFET switch
rD = 0.1; % Diode forward resistance
Dmin =1- ((0.9*Vin*2)/Vo);% Converter duty cycle
r = ((rM*Dmin)+((1-Dmin)*rD)+rL); % Total parasitic resistance of the inner boost leg
r2 = (rL+(Dmin*rM)); % Total parasitic resistance of the outer boost leg
L =288e-6;%Inductance for inductor on the inner boost leg
L2 =287.31e-6; % Inductance for inductor on the outer boost leg
R = 44.44; % Load resistor at full load
G = 1/R; % Conductance of load resistor
Qn = 2/pi; % Quality factor of the open-loop sampling gain
fs = 50e3;% Converter Switching Frequency
Ts = 1/fs; % Converter switching period
Is1 = 14.79; % Maximum Current through the inner boost leg
Is2 = 14.79; % Maximum Current through the outer boost leg
Ic = Is2; % Current through the common port of the

%parameters for the small signal switch
Rsen1 = Vsen / Is1; %shunt resistor for inner boost leg current sensing
Rsen2 = Vsen / Is2; %shunt resistor for outer boost leg current sensing
```

```
Ko = (1/Ri);
Dbar = (1-Dmin)
M =1/Dbar;
Vap = Vo/2;
Vcp = (Vo/2)-Vin;
Ia = Ic*Dmin
gi =  -(Ia/Vap)
gr =( Ic/Vap)
Sn =((((Vap*(1-Dmin)*Ri))/L)); %On time slew rate of inner boost leg inductor current
Sn1 =((((Vap*(1-Dmin)*Ri))/L2)) %On time slew rate of outer boost leg inductor current
Sf =( (Vcp*Ri)/L); %Off time slew rate of inductors current
Se = ((1 + ((Qn*pi)/2))*Sn)/(Qn*Dmin*pi); %Slope of inner boost leg external ramp
Se1 = ((1 + ((Qn*pi)/2))*Sn1)/(Qn*Dmin*pi);%Slope of  outer boost leg external ramp
Vslope = ((Vo-Vin)*Rsen1*Ts)/L;
Vslope1 = ((Vo-Vin)*Rsen1*Ts)/L2;
go = (Ts/L)*(((1-Dmin)*(Se/Sn))+(1/2)-Dmin);
go1 = (Ts/L2)*(((1-Dmin)*(Se1/Sn1))+(1/2)-Dmin);
gf = (Dmin*go)-((Dmin*Dbar*Ts)/(2*L))
gf1 = (Dmin*go1)-((Dmin*Dbar*Ts)/(2*L2))

Tpx = (-(2*Vo*rC)/((Dbar*(R+(2*rC)))))%Magnitude of Converter control-to-output T.F

Den2 = ((C*((r*(R+(2*rC)))+(((Dbar)^2)*(R*rC))))+(2*L))/((L*C)*(R+(2*rC)));
Den3=(C*((r2*(R+(2*rC)))+(((Dbar*rC)*((Dbar*R)+(2*rM))))))+(2*L2))/((L2*C)*(R+(2*r
C)));
Den1 = ((2*r)+(((Dbar)^2)*R))/((L*C)*(R+(2*rC)));
Den4 = ((2*r2)+(((Dbar)^2)*R)+(2*Dbar*rM))/((L2*C)*(R+(2*rC)));%outer loop for L2
Num = (s+(1/(C*rC)))*(s-((1/L)*(((R*(Dbar)^2)/2)-r)));
Num1 = (s+(1/(C*rC)))*(s-((1/L2)*(((R*(Dbar)^2)/2)-r))); %outer loop for L2
Den = s^2+(s*Den2)+Den1;
Den5 = s^2+(s*Den3)+Den4;%outer loop for L2
Tp = Tpx*(Num/Den); % Converter control-to-output T.F with respect to Inner boost leg
Tp1 = Tpx*(Num1/Den5); % Converter control-to-output T.F with respect to outer boost
leg
Gt = (gi+gr+G+(Dbar*(go-gf)))
Gt1 = (gi+gr+G+(Dbar*(go1-gf1)))
Ac =(R/Ri)/((2*M)+(((R*Ts)/(L*M^2))*((Se/Sn)+(1/2))));
Ac1 =(R/Ri)/((2*M)+(((R*Ts)/(L2*M^2))*((Se1/Sn1)+(1/2))));
wzn = 1/(2*rC*C); % LHPZ
wzp = (1/(L/((R*Dbar^2)-r))); % RHPZ
wzn1 = 1/(2*rC*C); %Frequency of LHPZ in rad/s
wzp1 = (1/(L2/((R*Dbar^2)-r))); %Frequency of RHPZ in rad/s
ws = 2*pi*fs; % Converter switching frequency in rad/s
wn = ws/2;
Cs = 4/(L*ws^2)
Cs1 = 4/(L2*ws^2)
wp = ((2*L*M^3)+(R*Ts*((Se/Sn)+(1/2))))/((C+Cs)*M^3*R*L)
wp1 = ((2*L2*M^3)+(R*Ts*((Se1/Sn1)+(1/2))))/((C+Cs1)*M^3*R*L2)

% damping ratio of the Converter control-to-output T.F with respect to inner boost leg
Zeta=(C*((r*(R+(2*rC)))+(((1-Dmin)^2)*(R*rC)))+(2*L))/(2*sqrt(((L*C)*(R+(2*rC)))* ((R*
(1-Dmin)^2)+(2*r))))
Q = 1/(2*Zeta); % quality factor of Converter vo/d T.F with respect to inner boost leg
% damping ratio of the Converter control-to-output T.F with respect to inner boost leg
Zeta1=((C*((r2*(R+(2*rC)))+(((Dbar*rC)*((Dbar*R)+(2*rM))))))+(2*L2))/(2*sqrt((L2*C)*(
R+(2*rC))* ((2*r2)+(((Dbar)^2)*R)+(2*Dbar*rM))));
Q1 = 1/(2*Zeta1);% quality factor of Converter vo/d T.F with respect to outer boost leg
```

```
% Corner frequency of converter inner boost leg control-to-output T.F in hertz
fo = (1/(2*pi))*sqrt(((R*(1-Dmin)^2)+(2*r))/(L*C*(R+(2*rC))))
% Corner frequency of converter outer boost leg control-to-output T.F in hertz
fo1 = (1/(2*pi))*sqrt(((2*r2)+(((Dbar)^2)*R)+(2*Dbar*rM))/(L2*C*(R+(2*rC))));
% Corner frequency of converter inner boost leg control-to-output T.F in rad/s
wo = sqrt(((R*(1-Dmin)^2)+(2*r))/(L*C*(R+(2*rC))));
% Corner frequency of converter outer boost leg control-to-output T.F in rad/s
wo1 =sqrt(((2*r2)+(((Dbar)^2)*R)+(2*Dbar*rM))/(L2*C*(R+(2*rC))));
%Control-to-output T.F for the current loop with respect to the inner boost leg
Voc = Ac *(((1+(s/wzn))*(1-(s/wzp)))/((1+(s/wp))*(1+(s/(Qn*wn))+(s^2/wn^2))));
%Control-to-output T.F for the current loop with respect to the outer boost leg
Voc1 = Ac1 *(((1+(s/wzn1))*(1-(s/wzp1)))/((1+(s/wp1))*(1+(s/(Qn*wn))+(s^2/wn^2))));

%Define parameters for the design of the double lead controller
fzn = wzn/(2*pi);
fzp = wzp/(2*pi);
fzn1 = wzn1/(2*pi);
fzp1 = wzp1/(2*pi);
fwp = wp/(2*pi);
fwp1 = wp1/(2*pi);

fc = 0.1*fzp; % cross over frequency for inner boost leg controller
fc1 = 0.1*fzp1; % cross over frequency for outer boost leg controller
Vtm = 2.5; % Amplitude of Voltage
Tm = 1/Vtm % T.F of Modulator
PM =65; % Desired phase of Vo
wc = 2*pi*fc % Cross over frequency of inner boost leg controller in rad/s
wc1 = 2*pi*fc1 Cross over frequency of outer boost leg controller in rad/s

Vref = 2.5 ;% reference voltage of the error amplifier
Beta = Vref/Vo ;% transfer function of the feedback network
R1 = 1.2e6;
RB = 1e3;% Lower resistor of the voltage feedback network
RA = RB*((1/Beta)-1) % Upper resistor of the voltage feedback network
h11 = (RA*RB)/(RA+RB) %h parameter of voltage feedback network gain

%Transfer functions of the inner and outer boost leg controllers
Tmp = Tm*Tp;%vo(s)/vc(s)
Tmp1 = Tm*Tp1; %vo(s)/vc1(s).
Tk = Tm*Tp*Beta; % vf(s)/vc(s)
Tk1 = Tm*Tp1*Beta; % vf(s)/vc1(s)
%Phase of Vo for (wc/wo)>1..
QTk = -180 + (atand(fc/fzn))-(atand(fc/fzp))-(atand(((2*Zeta*fc)/fo)/(1-((fc/fo)^2))));
%Phase of Vo for (wc1/wo1)>1..
QTk1=-180+(atand(fc1/fzn1))-(atand(fc1/fzp1))-(atand(((2*Zeta1*fc1)/fo1)/(1-((fc1/
fo1)^2))));
Qm = PM-QTk-90 % Required phase boost from inner boost leg controller
Qm1 = PM-QTk1-90% Required phase boost from outer boost leg controller
K = tand((Qm/4)+ 45)^2 %phase boost of inner boost leg controller
K1 = tand((Qm1/4)+ 45)^2%phase boost of inner boost leg controller

% Frequencies of the poles and zeros of the controller
fzc = fc/(sqrt(K))
fzc1 = fc1/(sqrt(K1))
fpc = fc*(sqrt(K))
fpc1 = fc1*(sqrt(K1))
```

```
%Magnitude of Modulator,power stage and feedback network T.Fs
Tko = ((Beta*Vo*2)/(Vtm*(1-Dmin)))*(((R*(1-Dmin)^2)-(2*r))/((R*(1-Dmin)^2)+(2*r)));
Tko1=((Beta*Vo*2)/(Vtm*(1-Dmin)))*(((R*(1-Dmin)^2)-(2*r2))/((R*(1-Dmin)^2)
+(2*r2)));
Tkm=Tko*(((sqrt(1+(fc/fzn)^2))*(sqrt(1+(fc/fzp)^2)))/(sqrt((1-(fc/fo)^2)^2+((2*Zeta*fc)
/fo)^2)));
Tkm1=Tko1*(((sqrt(1+(fc1/fzn1)^2))*(sqrt(1+(fc1/fzp1)^2)))/(sqrt((1-(fc1/fo1)^2)^2+
((2*Zeta1*fc1)/fo1)^2)));
Tcfc = 1/Tkm;
Tcfc1 = 1/Tkm1;

% Calculation of Type 3 Controller resistors and capacitors
R3 = (R1*(R1-(h11*(K-1))))/((K-1)*(R1+h11));
R4 = (R1*(R1-(h11*(K1-1))))/((K1-1)*(R1+h11));
C2 = Tkm/(wc*(R1+h11));
C4 = Tkm1/(wc1*(R1+h11));
C1 = C2*(K-1);
C5 = C4*(K1-1);
R2 =(sqrt(K))/(wc*C1);
R5 =(sqrt(K1))/(wc1*C5);
C3 = (R1+h11)/(wc*(sqrt(K))*((R1*R3)+(h11*(R1+R3))));
C6 = (R1+h11)/(wc1*(sqrt(K1))*((R1*R4)+(h11*(R1+R4))));
%Calculation converter impedances
Zf = (s + (1/(R2*C1)))/(s*C2*(s+((C1+C2)/(R2*C1*C2))));
Zf1 = (s + (1/(R5*C5)))/(s*C4*(s+((C5+C4)/(R5*C5*C4))));
Zi=(h11+((R1*R3)/(R1+R3)))*((s+((R1+h11)/(C3*(R3*(R1+h11)+(h11*R1)))))/(s+(1/(C
3*(R1+R3)))));
Zi1=(h11+((R1*R4)/(R1+R4)))*((s+((R1+h11)/(C6*(R4*(R1+h11)+(h11*R1)))))/(s+(1/(
C6*(R1+R4)))));

%The controllers transfer functions
Tc = Zf/Zi ;% Inner boost leg controller transfer function
Tc1 = Zf1/Zi1; %Outer boost leg controller transfer function

%The Loop Gains of converter
T = Tc*Tmp*Beta; % Converter loop gain with respect to the inner boost leg
T1 = Tc1*Tmp1*Beta; % Converter loop gain with respect to the outer boost leg
```

Appendix D: MSP430G2553 Microcontroller unit

Appendix D1: MSP430G2553 Microcontroller device pin-out

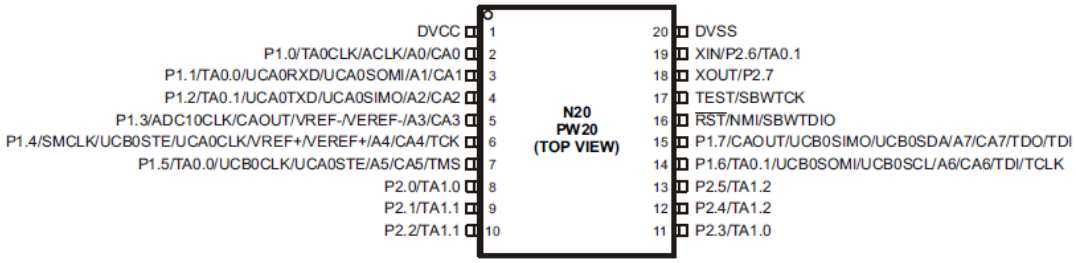


Figure D.1: The MSP430G2553 Microcontroller device pin-out

(Adapted from Texas Instruments, 2013).

Appendix D2: Device functional block diagram of the MSP430G2553 MCU

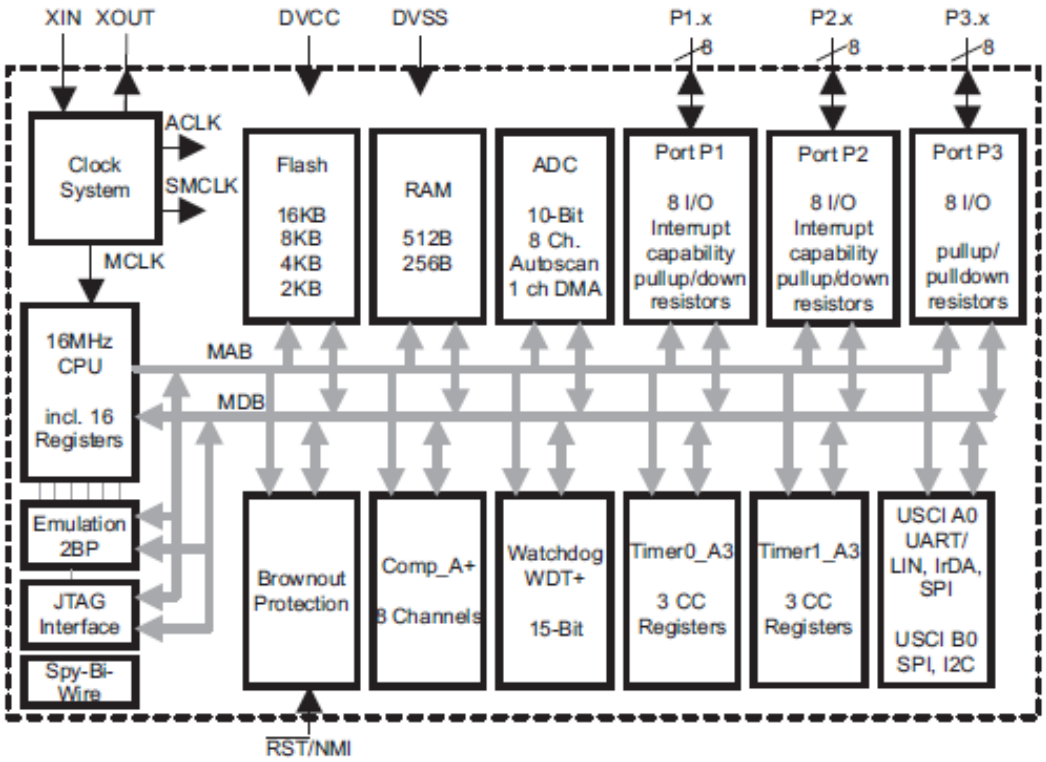


Figure D.2: The device functional block diagram of the MSP430G2553 MCU. (Adapted from Texas Instruments, 2013).

Appendix D3: MSP430G2553 C-code for IBVM Converter Control

```
/*
 * MSP430G2553 IBV Converter Controller Code
 * Makani Mwinga
 * October 2015
 *
 * PWM code using both TimerA_0 and TimerA_1
 */
#include "msp430.h"

/* Declare Functions */
void ADCSetup(void);
//void Soft_startUP(void);

#define PWM_increment (1024/100)

/* Declare global variables*/
unsigned int ADCDATA [2]= {0};
unsigned int ADCRead = 0;
unsigned int ADCRead1 = 0;

/* The main function of the program */
void main(void) {
unsigned int PWM_duty1;
unsigned int PWM_duty2;

/*** Stop Watchdog timer ***/
```

```
WDTCTL = WDTPW + WDTHOLD;

/*
 * Set Clock to operate at approximately 5MHz speed equivalent
 * to a clock period of 200 ns
 */
 BCSCTL1 = RSEL3 + RSEL2 + RSEL1 + RSEL0 + XT2OFF + XTS ;//+ XT2OFF;
 DCOCTL =  DCO2 + DCO1 + DCO0;

 /* Initialize ADC10 Setup Function*/
        ADCSetup();

          /*** GPIO Set-Up ***/
P1DIR = 0x00;
P2DIR = 0x00;
P1DIR |= BIT2;                                  // P1.2 set as output
P1SEL |= BIT2;                                  // P1.2 selected Timer0_A Out1
P2DIR |= BIT1;                                  // P2.1 set as output
P2SEL |= BIT1;                                  // P2.1 selected Timer1_A Out1

/*** Timer0_A Set-Up ***/
TA0CCTL0 |= CCIE;               //Interrupt enabled
TA0CCR0 = 97;                                   // PWM Period
TA0CCTL1 |= OUTMOD_2;               // TA0CCR1 output mode = set/reset
TA0CTL |= TASSEL_2 + MC_3 + ID_1;  // SMCLK, Up Mode (Counts to TA0CCR0)

/*** Timer1_A Set-Up ***/
TA1CCR0 = 97;                                   // PWM Period
TA1CCTL1 |= OUTMOD_2;                       // TA1CCR1 output mode = reset/set

_BIS_SR(GIE);                   // Enable global interrupt


while(1){

          if(ADCRead > 300){
            ADCRead = 300;
            Soft_startfLAG = 1;
           }
          if(ADCRead1 > 400){
            ADCRead1 = 400;
           }

           PWM_duty1 = (ADCRead/PWM_increment);
           PWM_duty2 = (ADCRead1/PWM_increment);

           if(ADCRead > 30){
              if(PWM_duty1 < 29){
              PWM_duty1 +=1 ;
              TA0CCR1 = PWM_duty1;
            }
          }
           if(ADCRead1 > 30){
              if(PWM_duty2 < 29){
              PWM_duty2 +=1 ;
              TA1CCR1 = PWM_duty2;
           }
```

```
        }
            if(ADCRead =< 20){
                if(PWM_duty1 >= 39){
                  PWM_duty1 -=1;
                }
            }
            if(ADCRead1 =< 20){
                if(PWM_duty2 >= 39){
                    PWM_duty2 -=1;
                }
            }

 }
}
          //ADC10 Setup
void ADCSetup(void){
  P1DIR |= 0x03;
  ADC10CTL0 = ADC10ON + MSC + ADC10SHT_2 + SREF_1 + REFON + REF2_5V
+ ADC10IE + ADC10IFG ;
  ADC10CTL1 = INCH_1 + ADC10DIV_0 + CONSEQ_3;
  ADC10DTC1 = 2;                    //Number of conversations.
  ADC10AE0 |= 0x03; // Enable A0 ,P1.0
  ADC10SA = (short)&ADCDATA[0];       // ADC10 data transfer starting address.
  _delay_cycles(30);// Delay and wait for ADC10 Voltage reference to settle down.
  ADC10CTL0 |= ENC + ADC10SC; // Enable Sampling and start conversion.
}


          //ADC10 interrupt Service Routine
#pragma vector = ADC10_VECTOR
__interrupt void ADC10_ISR (void){
   ADCRead1 = ADCDATA[1];
   ADCRead = ADCDATA[0];
   ADC10CTL0 &= ~ADC10IFG;  // clear interrupt flag
   ADC10SA = (short)&ADCDATA[0]; // ADC10 data transfer starting address.

 }

#pragma vector=TIMER0_A0_VECTOR
__interrupt void Timer_A (void) {
TA1CTL |= TASSEL_2 + MC_3 + ID_1;       // SMCLK, Up Mode (Counts to
TA1CCR0)
TA0CCTL0 &= ~CCIE;
}
```