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A Modified Modulation Scheme for Three-Level Diode-Clamped Matrix Converter under Unbalanced Input Conditions

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***Abstract*—The three-level diode-clamped matrix converter topology has outstanding performance under ideal operating conditions. However, input disturbance can influence the waveforms at the output side of the converter due to the direct coupling between the input and output. This paper proposes a modified modulation scheme for three-level diode-clamped matrix converter during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input. With this modulation technique, sinusoidal and balanced output voltages are guaranteed and the input current harmonics are minimized. Experimental results are presented to demonstrate the feasibility and effectiveness of the proposed modulation scheme.**

Keywords—Different transformer turns ratios of the isolation transformer, three-level diode-clamped matrix converter, unbalanced input voltages, modified modulation scheme

1. Introduction

Multilevel power converters [1, 2] have a number of advantages including lower output voltage distortion and semiconductor device voltage stress. These features make them very suitable for high-power, high-voltage applications, such as large variable-speed motor drives, high-voltage direct-current transmission, railway traction and manufacturing [3-7]. Matrix converters (MCs) also have advantages such as four-quadrant operation, sinusoidal input and output currents and no large energy storage elements. By combining the advantages of multilevel converters and MCs, the multilevel MCs [8-20] are receiving a lot of attention.

Lots of multilevel MC topologies have been studied, consisting of multi-modular MCs [8-12], diode-clamped MCs [13-17], and capacitor-clamped (flying capacitor) MCs [18-20]. The three-level diode-clamped matrix converter (TLDCMC) [16, 17] inherits the features of the conventional multilevel inverter and the indirect matrix converter (IMC). The phase opposite disposition (POD) modulation method and phase disposition (PD) modulation method can both be applied to the TLDCMC under the assuming ideal input voltages [16, 17]. However, in practice, the input voltages are likely to be unbalanced. Due to the lack of dc-link energy storage, the input disturbance will be transferred directly to the load, thereby influence the quality of the output waveform. Meanwhile, the input current will also become distorted.

Several strategies have been proposed to suppress the problems associated with unbalanced input voltages for low voltage MCs. The feed-forward compensation strategy was proposed in [21]. The fluctuation of virtual dc-link voltage is compensated by modifying the modulation index of inverter stage. As a result, balanced sinusoidal output currents are obtained, but the input current distortion is not considered. Casadei et al. [22] divide the unbalanced input voltage into positive and negative sequence components and modify the input power factor angle. Experimental results were presented in [23] with nearly sinusoidal input and output currents under unbalanced input voltage. Lei et al. [24] simplify the implementation of the method in [22], and use a notch filter to obtain the expected input power factor angle. Yan et al. [25] propose two improved double line voltage synthesis strategies for MC to eliminate the input current harmonic under unbalanced condition. Li et al. [26] propose three modulation strategies to eliminate the weak input current of MC based on a mathematic construction. Rojas et al. [27] also proposed three control schemes based on the predictive control algorithms to compensate for the input voltage unbalance producing good quality input and output current waveforms. Lei et al. [28] utilize a feedback control strategy to modify input reference current. Resonant controllers are used to regulate input current and instantaneous active power, so as to directly eliminate the input current harmonics and meanwhile ensure the load absorbing constant active power under unbalanced input voltage.

For high voltage applications, the large power exaggerates the negative effects introduced by unbalanced input voltages. In three-phase systems, the harmonics will degrade the power quality and also cause disturbance to other consumers and communication equipment [29]. Obviously, the option adding large extra active power filter is often uneconomical. Satisfying load command by adopting a modified modulation scheme is a good way to eliminate the harmonics at the output of the converter. Similar to the indirect MC, this paper proposes a modified modulation scheme for the TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input. The modified modulation scheme can achieve good performance in both the input currents and output voltages.

This paper contributes significant details, a full analysis and experimental results to the basic principles of this modulation method [30].

This paper is organized as follows: the converter topology is introduced in Section 2. Then, Section 3 presents the modified modulation scheme for TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input. Finally, the effectiveness of the modified modulation scheme is verified by experimental results in Section 4.

2. Topology of TLDCMC

The topology of TLDCMC is shown in Fig. 1, which consists of a second-order inductive-capacitor high frequency input filter, a three-phase three-winding isolation transformer, a cascaded-rectifier and a three-level diode-clamped inverter.

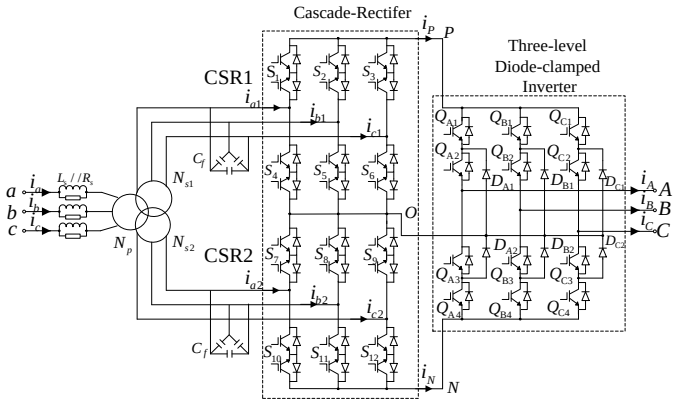


Fig. 1. Topology of TLDCMC.

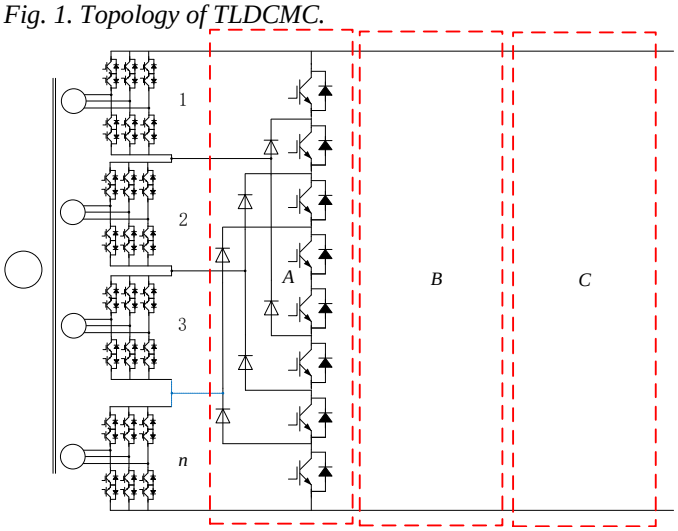


Fig. 2 Topology of the general multilevel diode-clamped matrix converter

The cascade rectifier consists of two bidirectional, three-phase current source rectifiers (CSRs) modules connected in series. These two CSR modules are composed of six bidirectional switch units (S_1-S_6 and S_7-S_{12}). Each bidirectional switch is realized by two insulated-gate bipolar transistors (IGBTs) with anti-parallel diode pairs connected to a common emitter configuration. The rectifier stage provides three output terminals, *P*, *O* and *N*. The inverter stage is a three-level diode-clamped voltage source inverter, the value of dc-link voltage is time-varying.

This topology has following advantages:

- This topology can be extended to a general multilevel diode-clamped MC easily as shown in Fig. 2. If (*n*-1) bidirectional CSR modules are cascaded to construct a cascaded-rectifier that can provide *n* output terminals, the cascaded-rectifier would be connected to an *n*-level diode clamped inverter.
- Similar to the IMC, the rectifier stage and the inverter stage can be controlled independently. A similar modulation scheme can be used for TLDCMC.
- The TLDCMC can overcome the voltage rating limits of the power semiconductors for high-voltage applications and avoid the voltage balance issue associated with conventional multi-level topologies. The corresponding derivation is shown in Section 3.2.

3. Modified modulation scheme under unbalanced input conditions

Modulation schemes for the TLDCMC operating under balanced input voltage conditions have been studied in [16] and [17]. In practice, the unbalanced input voltage is a potential problem. In this part, the modified modulation scheme for TLDCMC during operation with unbalanced input voltages and same transformer turns ratios is presented, firstly. The main idea of the modified modulation scheme is as follow: a modified modulation matrix for rectifier stage is given to maintain the constant average dc-link voltage, and the balanced output voltage is obtained by the normal POD method. The TLDCMC can avoid voltage balance issue associated with conventional multi-level topologies. By modifying the modulation signals in the inverter stage, the modified modulation scheme is extended to fit the TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input.

3.1. Unbalanced input voltages condition under same transformer turns ratios

Assume the primary-to-secondary turns ratios of the isolation transformer are same, the modified modulation method is presented. In addition, the sinusoidal input current is derived and maximum output voltage is analyzed.

3.1.1 Modified modulation matrix for rectifier stage

For the convenience, the variables in the three-phase system are represented by space vector as

$$\vec{x} = \frac{2}{3}\left(x_a + x_b e^{j2\pi/3} + x_c e^{j4\pi/3}\right) \tag{1}$$

For the space vector $\vec{x}$ and $\vec{y}$, if the space vector $\vec{x}$ satisfy $x_a + x_b + x_c = 0$, the following formulation can be established

$$\frac{3}{2}\vec{x}\cdot\vec{y} = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}^T \begin{bmatrix} y_a \\ y_b \\ y_c \end{bmatrix} \tag{2}$$

Considering the unbalanced grid, the input voltage vector can be represented as

$$\dot{V}_{in} = V_p e^{j(\omega_i t+\theta_p)} + V_n e^{j(-\omega_i t+\theta_n)} \tag{3}$$

where V_p and V_n are the amplitudes of positive and negative sequence input phase voltage vectors, respectively. θ_p and θ_n are the initial angle of positive and negative sequence input phase voltage vectors, respectively. ω_i is the angular frequency of the input phase voltage.

The balanced output voltage vector and output current vector are assumed to be:

$$\begin{cases} \dot{V}_{out} = V_{om} e^{j(\omega_o t+\theta_o)} \\ \dot{i}_{out} = I_{om} e^{j(\omega_o t+\theta_o-\psi_o)} \end{cases} \tag{4}$$

where ψ_o is the angle that the load current lags the output voltage. V_{om} and I_{om} are the amplitudes of output voltage and output current vectors. θ_o is the initial angle of output phase voltage vectors. ω_o is the angular frequency of the output phase voltage.

Then the output power can be calculated as

$$P_o = \frac{3}{2}\dot{V}_{out} \cdot \dot{i}_{out} \tag{5}$$

In addition, the input power can be expressed by

$$P_{in} = \frac{3}{2}\dot{V}_{in} \cdot \dot{i}_{in} \tag{6}$$

According to active power balance

$$P_o = P_{in} \tag{7}$$

The rectifier modulation matrix is defined as $\overrightarrow{M_{REC}}$ for current source rectifier. Assume the $\overrightarrow{M_{REC}}$ as

$$\dot{M}_{REC} = M_p e^{j(\omega_i t+\theta_p-\psi_p)} + M_n e^{j(-\omega_i t+\theta_n-\psi_n)} \tag{8}$$

where ψ_p and ψ_n are the power factor angle of positive and negative sequence input voltage vectors, respectively. M_p and M_n are the modulation factors of positive and negative sequence input voltage vectors, respectively.

The average dc-link voltage V_{dc} of the cascaded-rectifier can be given by

$$V_{dc} = 2V_{po} = 2V_{on} = \frac{3N_s}{N_p}\dot{V}_{in} \cdot \dot{M}_{REC} \tag{9}$$

where V_{po} and V_{on} are the average dc-link voltage of rectifier1 and rectifier2, respectively. N_p/N_s is the primary-to-secondary turns ratios of the isolation transformer. And it meets $\frac{N_p}{N_{s1}} = \frac{N_p}{N_{s2}} = \frac{N_p}{N_s}$.

Combining (3), (8) and (9), the average dc-link voltage of cascaded-rectifier can be expressed as

$$\begin{aligned} V_{dc} = \frac{3N_s}{N_p}\{ & V_p M_p \cos\psi_p + V_n M_n \cos\psi_n + \\ & V_p M_n \cos(2\omega_i t + \theta_p - \theta_n + \psi_n) + \\ & V_n M_p \cos(-2\omega_i t + \theta_n - \theta_p + \psi_p)\} \end{aligned} \tag{10}$$

As shown in (10), the value of average dc-link voltage consists of a dc term and a second order harmonic. Since the second order term brings low order harmonics to both sides of the converter, the modulation matrix has to be carefully selected for purposes of elimination. The following equations can be obtained

$$\begin{cases} M_p V_n = M_n V_p \\ \psi_p = \pi - \psi_n = \varphi_i \end{cases} \tag{11}$$

where φ_i is the power factor angle of the unbalanced input voltage.

Then, the modified modulation matrix can be described by

$$\dot{M}_{REC} = M_p\left(e^{j(\omega_i t+\theta_p-\varphi_i)} - \frac{V_n}{V_p}e^{j(-\omega_i t+\theta_n+\varphi_i)}\right) \tag{12}$$

To make full use of the input voltage and meet $|\overrightarrow{M_{REC}}| < 1$, the modified modulation matrix is chosen as follow

$$\dot{M}_{REC} = \frac{V_p e^{j(\omega_i t+\theta_p-\varphi_i)} - V_n e^{j(-\omega_i t+\theta_n+\varphi_i)}}{V_p + V_n} \tag{13}$$

Then the average dc-link voltage can be calculated as

$$V_{dc} = 2V_{po} = 2V_{on} = \frac{3N_s}{N_p}(V_p - V_n)\cos\varphi_i \tag{14}$$

The modified rectifier modulation matrix can also be used in all *n*-1 CSR modules of general multilevel diode-clamped MC. As a result, it will yield *n* levels for the dc-link voltage.

3.1.2 Modulation for inverter stage

When the number of inverter levels increases, it is more difficult to realize the modulation of the inverter stage using the space vector pulse width modulation (SVPWM). Thus, the carrier modulation scheme is considered for inverter stage due to the simple implement scheme. For simplicity, the POD method is adopted in this paper, but the technique can be applied to other modulation methods.

Assume that the desired output phase voltages are

$$\begin{cases} u_A = \sqrt{2}U_{oRMS}\cos(\varphi_A) \\ u_B = \sqrt{2}U_{oRMS}\cos(\varphi_B) \\ u_C = \sqrt{2}U_{oRMS}\cos(\varphi_C) \end{cases} \tag{15}$$

where U_{oRMS} is the root mean square (RMS) of the output phase voltage respectively. φ_A, φ_B and φ_C denote the phase angle of output voltages, respectively.

To maximize the utilization of dc-link voltage, the zero-sequence u_{NO} is considered, the modulation signals u_{io} are as follow

$$u_{io} = u_i + u_{NO}, \quad i \in \{A, B, C\} \tag{16}$$

where the zero-sequence u_{NO} is chosen by

$$u_{NO} = -\frac{\min(u_A, u_B, u_C) + \max(u_A, u_B, u_C)}{2} \tag{17}$$

Normalizing the u_{io}, the modulation signals are obtained as

$$\bar{u}_{io} = 2\frac{u_{io}}{V_{dc}} \tag{18}$$

The modulation signals can be normalized as

$$d_{ip}=\begin{cases}\dfrac{u_{io}}{V_{po}}, & when\ \ u_{io}\ge 0\\ 0, & when\ \ u_{io}\le 0\end{cases}\qquad i\in\{A,B,C\} \tag{19}$$

$$d_{in}=\begin{cases}0, & when\ \ u_{io}\ge 0\\ \dfrac{-u_{io}}{V_{on}}, & when\ \ u_{io}\le 0\end{cases}\qquad i\in\{A,B,C\} \tag{20}$$

where d_{ip} denotes the duty cycle of the switching state P (Q_{i1} and Q_{i2} are *ON*, while Q_{i3} and Q_{i4} are *OFF*.); d_{in} denotes the duty cycle of the switching state N (Q_{i1} and Q_{i2} are *OFF*, while Q_{i3} and Q_{i4} are *ON*.).

Assume that the input line-to-line voltage of rectifier stage is u_{ab} and u_{ac} during the modulation period T_s. The duty ratio of the active vector u_{ab} is d_α. The POD method for the inverter stage can be implemented as shown in Fig. 3.

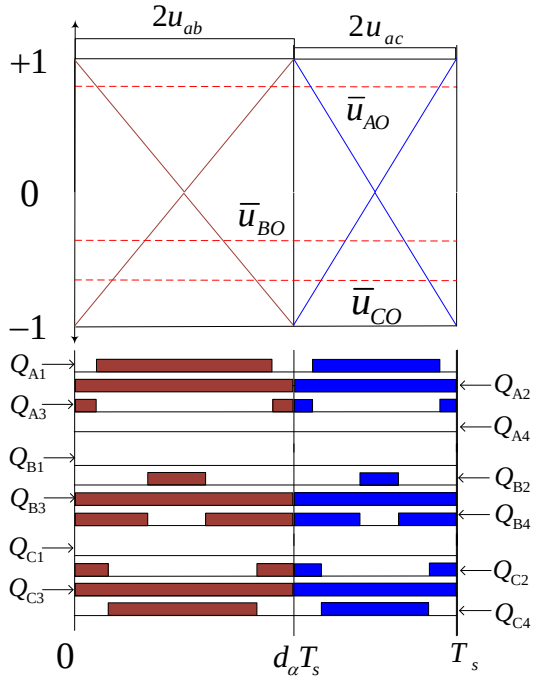


Fig. 3. POD method for inverter stage.

By adjusting the rectifier modulation matrix, the method can suppress the effect introduced by unbalanced inputs, which is a simple and easy way to implement. Since the limitation of inverter modulation index, the maximum amplitude of output phase voltage is

$$\left(U_{om}\right)_{\max}=\frac{\sqrt{3}N_s}{N_p}\left(V_p-V_n\right)\cos\varphi_i \tag{21}$$

If the input voltage is seriously unbalanced, the maximum amplitude of output voltage will decrease. If the amplitudes of positive and negative sequence input phase voltage vectors are equal, the maximum amplitude of output voltage will be zero and the desired output voltage can't be synthesized.

For the *n*-level inverter, the multicarrier-based method with *n*-1 carriers should be applied.

3.1.3 Input current derivations

As for the unbalanced input voltage, the input currents can be derived as

$$\vec{i}_i=\frac{N_s}{N_p}\vec{M}_{REC}\left(i_P-i_N\right) \tag{22}$$

where $\vec{i}_i$ is the space vectors of source current i_i.

The average dc-link current in a switching period can be expressed as follow

$$\begin{cases}i_P=d_{Ap}i_A+d_{Bp}i_B+d_{Cp}i_C\\ i_N=d_{An}i_A+d_{Bn}i_B+d_{Cn}i_C\\ i_O=-\left(i_P+i_N\right)=0\end{cases} \tag{23}$$

The neutral point current i_O equals zero when the dc-link voltage is balanced. Then, after some manipulations with (14), (19), (20), and (23), the following equation can be obtained

$$i_P-i_N=\frac{2P_oN_p}{3N_s(V_p-V_n)\cos\varphi_i} \tag{24}$$

where $P_o=u_Ai_A+u_Bi_B+u_Ci_C$ represents the output active power.

Combining (13), (22) and (24), the input current space vector can be derived as

$$\vec{i}_i=\frac{2P_o\left(V_pe^{j(\omega_it+\theta_p-\varphi_i)}-V_ne^{j(-\omega_it+\theta_n+\varphi_i)}\right)}{3\cos\left(\varphi_i\right)\left(V_p^2-V_n^2\right)} \tag{25}$$

If P_o is constant, the input current i_i is sinusoidal and unbalanced with the proposed modulation scheme under unbalanced input voltages according to (25).

3.2 Unbalanced input voltages condition under different transformer turns ratios

The TLDCMC does not require balance of the dc-link voltage. In fact, there is no constraint for same transformer turns ratios of the isolation transformer. The modified modulation scheme for same transformer turns ratios in Section 3.1 is extended in this part. By modifying the modulation signals of the inverter stage, the modified modulation scheme is extended to fit the TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input. The desired output voltage and input current are obtained.

3.2.1 Output voltage derivations

Considering the same modulation matrix as (13) at rectifier stage and different transformer turns ratios for an isolation transformer at the input ($\frac{N_p}{N_{s1}}\neq\frac{N_p}{N_{s2}}$), the average dc-link voltage of the two rectifiers can be calculated as

$$\begin{cases}V_{po}=\frac{3N_{s1}}{2N_p}\left(V_p-V_n\right)\cos\varphi_i\\ V_{on}=\frac{3N_{s2}}{2N_p}\left(V_p-V_n\right)\cos\varphi_i\end{cases} \tag{26}$$

The average dc-link voltages of the two rectifiers are unequal. In order to get the balanced output voltage, the load side switching function is adjusted to compensate dc-link voltage.

To maximize the utilization of dc-link voltage, the modulation signals are given by

$$u_{io} = u_i + u_{NO1} + u_{NO2}, \quad i \in \{A, B, C\} \tag{27}$$

where u_{io} are the modulation signals and u_{NO1}, u_{NO2} are the zero-sequence signals, respectively. And the zero-sequence signals are selected as follow

$$\begin{cases} u_{NO1} = \dfrac{V_{po} - V_{on}}{2} \\ u_{NO2} = -\dfrac{\min(u_A, u_B, u_C) + \max(u_A, u_B, u_C)}{2} \end{cases} \tag{28}$$

The modulation signals can be normalized as (19) and (20). Then, the balanced output voltage can be obtained. By adding additional zero sequence components u_{NO1} to the inverter modulation signals, the method can suppress the effect introduced by different transformer turns ratios of the isolation transformer and obtain the desired output voltage as the equal situation.

From (26) and (28), when the transformer turns ratios are same, the zero-sequence signal u_{NO1} equals zero and the modulation signals become exactly same as (16).

Due to the limitation of inverter modulation index, the maximum amplitude of output phase voltage is

$$(U_{om})_{\max} = \frac{\sqrt{3}(N_{s1}+N_{s2})}{2N_p}(V_p - V_n)\cos\varphi_i \tag{29}$$

when the transformer turns ratios are equal, (29) becomes (21).

3.2.2 Input current derivations

As for the different transformer turns ratios, the average dc-link current in a switching period can be expressed as follow

$$\begin{cases} i_P = d_{Ap} i_A + d_{Bp} i_B + d_{Cp} i_C \\ i_N = d_{An} i_A + d_{Bn} i_B + d_{Cn} i_C \\ i_O = -\left(\left(\dfrac{u_{AO}}{V_{po}} - \dfrac{u_{AO}}{V_{on}}\right) i_A + \left(\dfrac{u_{BO}}{V_{po}} - \dfrac{u_{BO}}{V_{on}}\right) i_B \right. \\ \qquad \left. + \left(\dfrac{u_{CO}}{V_{po}} - \dfrac{u_{CO}}{V_{on}}\right) i_C \right) \end{cases} \tag{30}$$

The neutral point current i_O is not zero when the dc-link voltage V_{po} is not equal to V_{on}. Then, after some manipulations with (15), (19), (20), (26), (27), (28) and (30), the following equation could be obtained

$$\frac{N_{s1}}{N_p} i_P - \frac{N_{s2}}{N_p} i_N = \frac{2P_o}{3(V_p - V_n)\cos\varphi_i} \tag{31}$$

where $P_o = u_A i_A + u_B i_B + u_C i_C$ represents the output active power.

The input current space vector $\vec{i_i}$ could be expressed as follows

$$\vec{i_i} = \vec{M}_{REC}\left(\frac{N_{s1}}{N_p} i_P - \frac{N_{s2}}{N_p} i_N\right) \tag{32}$$

After some manipulations with (13), (31) and (32), the input current can be written as

$$\vec{i_i} = \frac{2P_o\left(V_p e^{j(\omega_i t + \theta_p - \varphi_i)} - V_n e^{j(-\omega_i t + \theta_n + \varphi_i)}\right)}{3\cos(\varphi_i)\left(V_p^2 - V_n^2\right)} \tag{33}$$

Compared (33) with (25), the input current is same and not affected by the different transformer turns ratios.

Through the analysis of this section, the TLDCMC can work under the situation that V_{po} is not equal to V_{on}. The desired output voltage and input current can also be obtained. The modified modulation scheme is fit for TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input.

4. Experimental results

To verify the modified modulation scheme, a low-voltage experimental prototype is implemented as shown in Fig. 4. The related component parameters are listed in Table.1. The cascaded-rectifier uses the SVPWM method and the POD method is employed in the three level diode clamped inverter. In addition, with an appropriate switching sequence, the zero current commutation is implemented. In the cascaded-rectifier, the IGBT module FF300R12KT3_E is used for the four quadrant power switches. The IGBT module F3300R12ME4_B23 and F3300R12ME4_B23 are connected in series as the one phase leg of the three level diode clamped inverter. The voltage stresses of the switches are related to the input line-to-line peak voltage of secondary transformer. The input voltage and the output current can be measured through the sensor circuits. A floating-point digital signal processor (DSP, TMS320F28335) and a field programmable gate array (FPGA, EP2C8J144C8N) are equipped with the controller board. The desired duty ratios of the switches are calculated in DSP and transmitted to FPGA. Then, the desired switching sequences and commutation process are implemented in FPGA.

The following three conditions are experimentally tested to verify the modified modulation scheme. The *Condition I* is experimentally tested to verify that the TLDCMC can avoid the voltage balance issue associated with conventional multi-level topologies. In practical application, to maintain the same voltage stress for the semiconductor device at inverter stage, the transformer turns ratios of the isolation transformer are usually same. Thus, the *Condition II* and *Condition III* with same transformer turns ratios are considered.

Condition I: The converter is fed by balanced input voltage 220V/50Hz (RMS). The transformer used for experiments has a fixed primary to secondary ratio of 380:200 and 380:100 respectively.

Condition II: The converter is fed by balanced input voltage 115V/50Hz (RMS). The phase shifts among three input phase voltages are 120 degrees. The transformer used for experiments has a fixed primary to secondary ratio of 380:200.

Condition III: The a-phase and b-phase input voltages are 115V/50Hz (RMS), while c-phase input voltage is 81V/50Hz (RMS). The phase shifts among three input phase voltages are

120 degrees. The transformer used for experiments has a fixed primary to secondary ratio of 380:200.

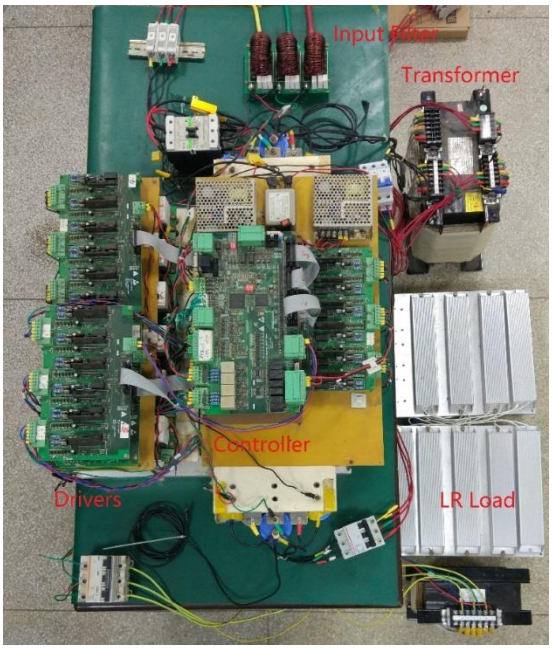


Fig. 4. The experimental prototype of TLDCMC.

Table 1. Component parameters of experimental prototype

Parameters	Value
Switching frequency (f_s)	5kHz
Input filter inductor (L_s)	0.6mH
Input filter capacitor (C_{f1}, C_{f2})	22uF
Damping resistor (R_s)	9Ω
Load resistor (R)	13.33Ω
Load inductor (L_o)	6mH
Current sensor	LT308-S7

Fig. 5 shows the experimental waveforms under *Condition I*, when the amplitude and frequency of desired output phase voltage are set to 140V/30Hz. As seen, the nearly sinusoidal input currents are achieved when the isolation transformer has different transformer turns ratios. As for the conventional three-level diode clamped inverter, the voltages of the two dc-link capacitors should be controlled to achieve equal voltage. However, the TLDCMC can avoid the voltage balance issue. As seen in Fig. 4 (a), the dc-link voltages of two rectifiers are different because of the different transformer turns ratios of the isolation transformer. However, the balanced output currents are obtained as seen in Fig. 4 (c). The output line-to-line voltage is characterized by five levels.

Fig. 6-7 shows the experimental waveforms under *Condition II*, when the amplitude and frequency of desired output phase voltage are set to 80V/30Hz and 80V/60Hz, respectively. As seen, the balanced input currents and output currents are achieved when the input voltages are balanced. The input and output currents are nearly sinusoidal. The distortion of input currents is mainly caused by the dead-time, device voltage drop, distorted no-load current in the transformer, and so on. The related total harmonic distortion (THD) values of input and output currents are listed in Table 2.

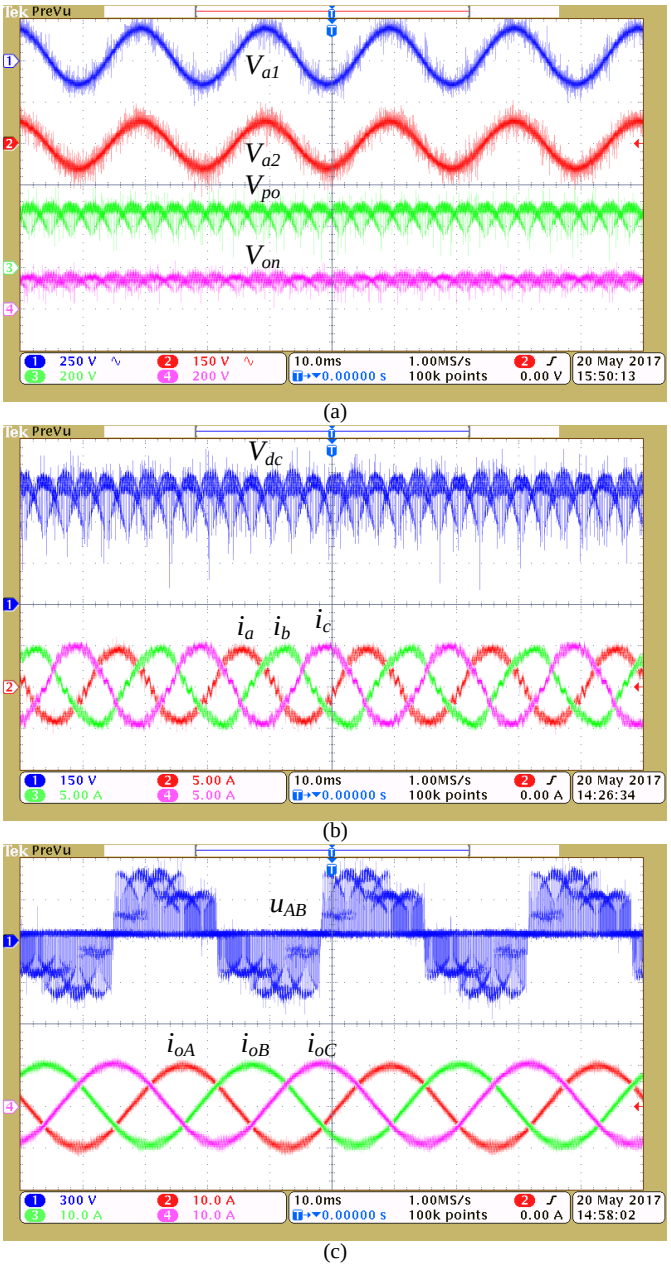
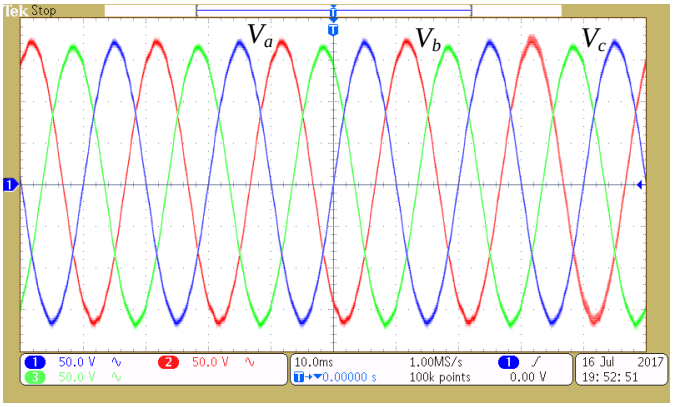
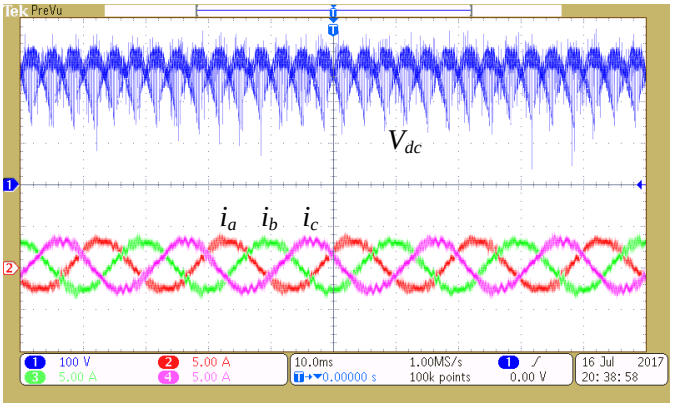


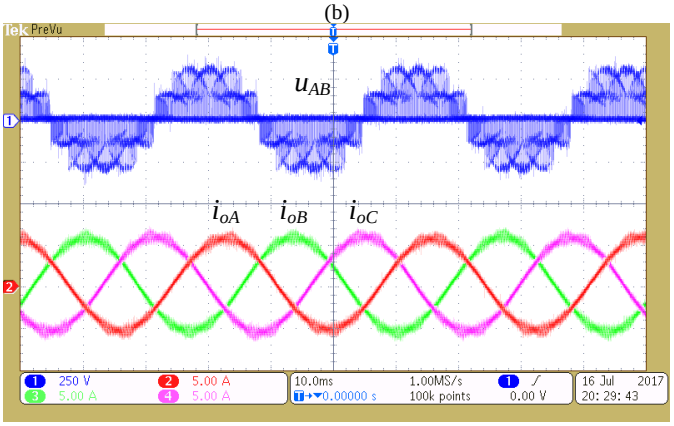
Fig. 5. The experimental waveforms with a reference output phase voltage of 140V/30Hz under Condition I.
(a) Ch1: the a1-phase input voltage of the secondary transformer winding1 V_{a1}, Ch2: the a2-phase input voltage of the secondary transformer winding2 V_{a2}, Ch3: the average dc-link voltage of rectifier1 V_{po} Ch4: the average dc-link voltage of rectifier2 V_{on}
(b) Ch1: the dc-link voltage V_{dc}, Ch2: the a-phase input current, Ch3: the b-phase input current, Ch4: the c-phase input current.
(c) Ch1: the output line-to-line voltage U_{AB}, Ch2: the A-phase output current, Ch3: the B-phase output current, Ch4: the C-phase output current.



(a)

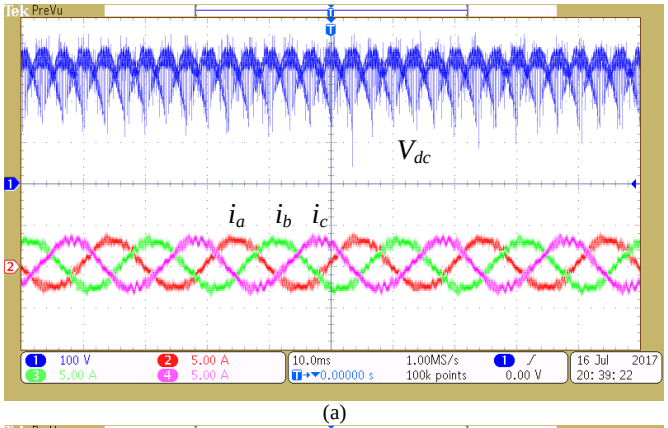


(b)

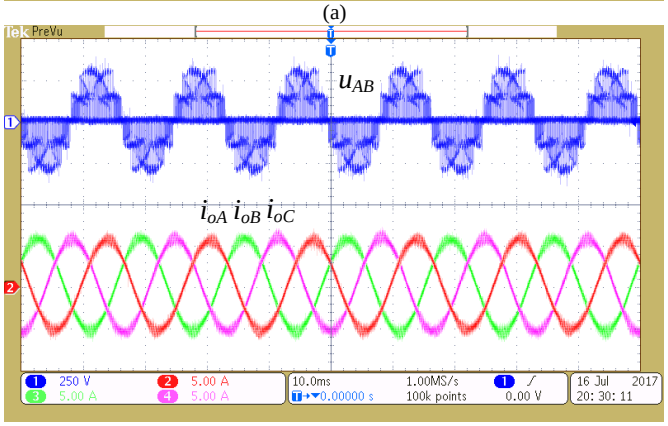


(c)

Fig. 6. The experimental waveforms with a reference output phase voltage of 80V/30Hz under Condition II.
(a) Ch1: the input phase voltage V_a, Ch2: the input phase voltage V_b, Ch3: the input phase voltage V_c.
(b) Ch1: the dc-link voltage V_{dc}, Ch2: the a-phase input current, Ch3: the b-phase input current, Ch4: the c-phase input current.
(c) Ch1: the output line-to-line voltage U_{AB}, Ch2: the A-phase output current, Ch3: the B-phase output current, Ch4: the C-phase output current.



(a)



(b)

Fig. 7. The experimental waveforms with a reference output phase voltage of 80V/60Hz under Condition II.
(a) Ch1: the dc-link voltage V_{dc}, Ch2: the a-phase input current, Ch3: the b-phase input current, Ch4: the c-phase input current.
(b) Ch1: the output line-to-line voltage U_{AB}, Ch2: the A-phase output current, Ch3: the B-phase output current, Ch4: the C-phase output current.

Fig. 8-9 shows the experimental waveforms under *Condition III*, when the amplitude and frequency of desired output phase voltage are set to 80V/30Hz and 80V/60Hz, respectively. As seen, the nearly sinusoidal input currents and output currents are achieved when the input voltages are unbalanced. The related THD values of input and output currents are listed in Table 2. Comparing the output current waveforms under *Condition II* and *Condition III*, there are no obvious difference between them. The modified modulation scheme is verified by the experimental results.

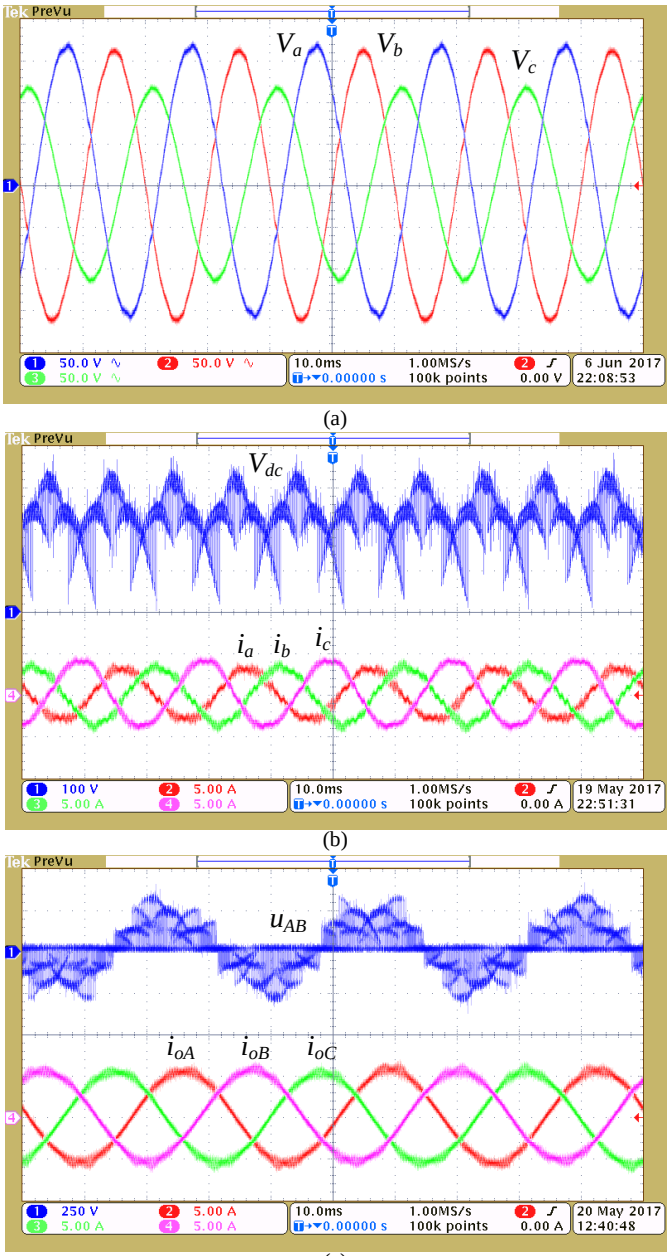


Fig. 8. The experimental waveforms with a reference output phase voltage of 80V/30Hz under condition III.
(a) Ch1: the input phase voltage V_a, Ch2: the input phase voltage V_b, Ch3: the input phase voltage V_c.
(b) Ch1: the dc-link voltage V_{dc}, Ch2: the a-phase input current, Ch3: the b-phase input current, Ch4: the c-phase input current.
(c) Ch1: the output line-to-line voltage U_{AB}, Ch2: the A-phase output current, Ch3: the B-phase output current, Ch4: the C-phase output current.

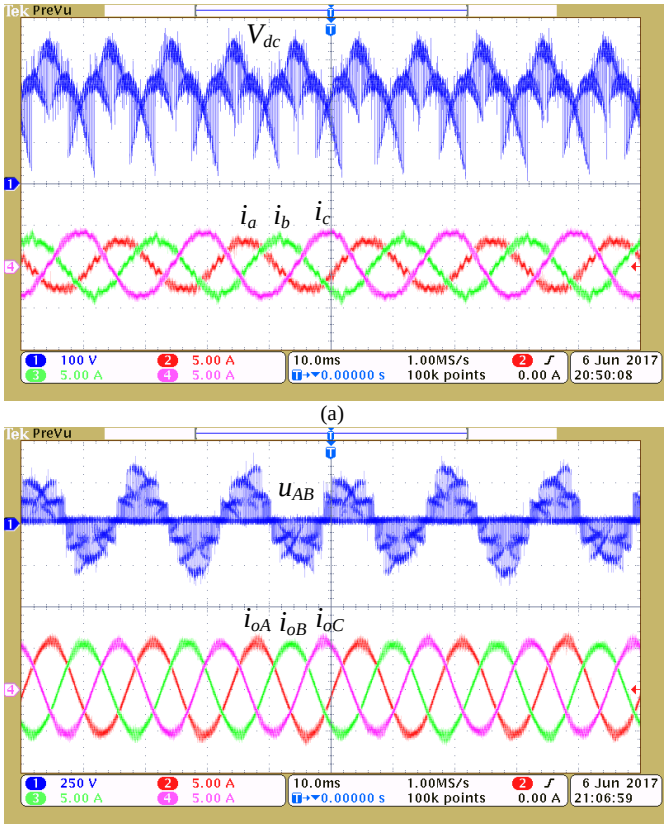


Fig. 9. The experimental waveforms with a reference output phase voltage of 80V/60Hz under Condition III.
(a) Ch1: the dc-link voltage V_{dc}, Ch2: the a-phase input current, Ch3: the b-phase input current, Ch4: the c-phase input current.
(b) Ch1: the output line-to-line voltage U_{AB}, Ch2: the A-phase output current, Ch3: the B-phase output current, Ch4: the C-phase output current.

Table 2. THD values of the input and output currents under *Condition II* and *III*

Condition (%)	i_a	i_b	i_c	i_A	i_B	i_C
II-80V/30Hz	12.32	12.25	12.37	4.49	4.52	4.54
II-80V/60Hz	12.12	12.58	13.50	2.90	3.05	2.94
III-80V/30Hz	13.00	11.92	8.87	4.87	4.93	4.80
III-80V/60Hz	13.03	11.50	8.65	3.82	3.80	3.73

5. Conclusion

This paper has presented the implementation of a modified modulation scheme for the TLDCMC during operation with unbalanced input voltages and when different transformer turns ratios are used for an isolation transformer at the input. The good performance of input and output currents is obtained. The modified modulation scheme is also applicable to the generalized multilevel diode-clamped matrix converter under unbalanced input voltage. The experimental results validate the correctness and feasibility of the proposed modulation method and the feature that the TLDCMC can avoid the voltage balance issue associated with multi-level topologies.

Moreover, the modified modulation scheme can be also used under ideal operating conditions.

6. References

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