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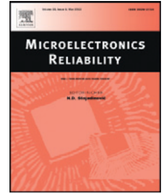

Impact of the gate driver voltage on temperature sensitive electrical parameters for condition monitoring of SiC power MOSFETs

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ABSTRACT

Condition monitoring using temperature sensitive electrical parameters (TSEPs) is widely recognized as an enabler for health management of power modules. The on-state resistance/forward voltage of MOSFETs, IGBTs and diodes has already been identified as TSEPs by several researchers. However, for SiC MOSFETs, the temperature sensitivity of on-state voltage/resistance varies depending on the device and is generally not as high as in silicon devices. Recently the turn-on current switching rate has been identified as a TSEP in SiC MOSFETs, but its temperature sensitivity was shown to be significantly affected by the gate resistance. Hence, an important consideration regarding the use of TSEPs for health monitoring is how the gate driver can be used for improving the temperature sensitivity of determined electrical parameters and implementing more effective condition monitoring strategies. This paper characterizes the impact of the gate driver voltage on the temperature sensitivity of the on-state resistance and current switching rate of SiC power MOSFETs. It is shown that the temperature sensitivity of the switching rate in SiC MOSFETs increases if the devices are driven at lower gate voltages. It is also shown, that depending on the SiC MOSFET technology, reducing the gate drive voltage can increase the temperature sensitivity of the on-state resistance. Hence, using an intelligent gate driver with the capability of customizing occasional switching pulses for junction temperature sensing using TSEPs, it would be possible to implement condition monitoring more effectively for SiC power devices.

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1. Introduction

The degradation of solder joints and wirebonds in traditional packaging systems usually results in an increase in the thermal resistance and hence, a higher junction temperature [1]. The use of temperature sensitive electrical parameters (TSEPs) for identifying the junction temperature of power semiconductors is one of the main techniques used for the implementation of condition monitoring strategies [2], which can be used for assessing ageing damage, improving the lifetime of the module and defining operational constraints. The use of TSEPs for condition monitoring has made the electrothermal characterization of power devices and modules essential for effective implementation.

Silicon carbide power devices have demonstrated a superior energy conversion efficiency due to the lower switching losses and on-state voltages. The wide bandgap of SiC (~3.3 eV) although beneficial for high temperature applications, nevertheless, makes condition monitoring using TSEPs more challenging since the electrical parameters are less temperature sensitive.

The turn-on current switching rate dI_{DS}/dt has previously been shown to increase with temperature and has thus been identified as a potential TSEP [3]. Due to the impact of parasitic inductance under high dI/dt conditions, the temperature sensitivity was shown to improve when the SiC MOSFET was driven at slower switching speeds. However, since the advantages of SiC are best exploited when driven at high switching speeds, the ability to sense the junction temperature using the switching rate, without increasing the switching losses is a critical challenge. Advanced intelligent gate drivers [4] would be a fundamental tool for implementing these techniques, where an advanced gate driver capable of momentarily implementing customized switching pulses as part of a condition monitoring strategy, would be a significant advantage. In this sense, a diagnostic pulse can be designed to maximize the temperature sensitivity of the current switching rate and/or on-state resistance of the device during the parameter evaluation and perform multiple measurements to minimize ambient noise.

This paper evaluates how the gate driver voltage (V_{GG}) of SiC MOSFETs can be used to maximize the temperature sensitivity of the on-state resistance $R_{DS\text{-}ON}$ and the switching rate of the drain current dI_{DS}/dt for more effective junction temperature sensing. The information generated here can be used for the development of condition monitoring strategies in SiC devices/modules in the future.

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2. Impact of gate driver voltage on temperature sensitivity of the on-state resistance

2.1. MOSFET on-state resistance analysis

The on-state resistance of a MOSFET device ($R_{DS\text{-}ON}$) is the resistance between the drain and the source of a MOSFET during conduction. This resistance is comprised mainly by 3 different components given by Eq. (1), as the current path within the MOSFET is formed by different layers [5].

$$R_{DS-ON} \sim R_{CH} + R_{JFET} + R_{DRIFT} \tag{1}$$

R_{CH} is the channel resistance which is inversely proportional to the carrier density within the channel as well as carrier mobility. Since the carrier density in the channel has a positive temperature coefficient due to the reduction of the threshold voltage with temperature and the effective mobility has a negative temperature coefficient, the temperature dependency of the channel resistance depends on the gate-source voltage V_{GS}. When V_{GS} is close to the threshold voltage (V_{TH}), then R_{CH} has a negative temperature coefficient, however, as V_{GS} increases and the channel becomes fully formed with carriers, the negative temperature coefficient of the effective mobility dominates hence, the temperature coefficient of R_{CH} becomes positive. The other two main resistive components, namely the JFET region resistance R_{JFET} (which is minimized for trench MOSFETs) and the drift region resistance R_{DRIFT}, have positive temperature coefficients. The gate voltage V_{GS} applied to turn-on the device affects the value of the resistance. This is a well-known fact and is one of the reasons why SiC MOSFETs require a high gate voltage in order to properly invert the channel and obtain a low on-state resistance compared with silicon MOSFETs [6,7], as well as avoiding a negative temperature coefficient, which can cause thermal runaway in case of paralleled devices.

In addition to the intrinsic device resistance modelled by Eq. (1), there are parasitic resistances which add to the total resistance of the packaged MOSFET chip. These include the wirebond resistances, metallization, solder, mounting substrate, etc., which will add to the total resistive path within the packaging, as shown in Fig. 1. It is important to mention that a recent packaging trend consists in the addition of a kelvin connection so as to minimize the impact of the stray inductances on the switching performances. The use of this additional terminal for evaluating bond-wire degradation and chip degradation has been demonstrated in [8] by characterizing the on-state voltage.

2.2. SiC MOSFET on-state resistance characterization

Fig. 2 shows the measured on-state resistance for a 1200 V/24 A SiC MOSFET with datasheet CMF10120D from Cree/Wolfspeed, at different V_{GS} voltages, ranging from 10.5 V to 20 V and temperatures of 22 °C and 125 °C.

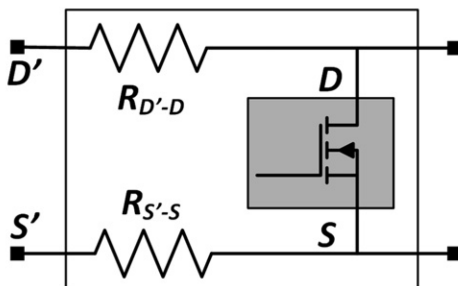

Fig. 1. Impact of stray resistances on the measured on-state resistance of a packaged MOSFET and kelvin connection.

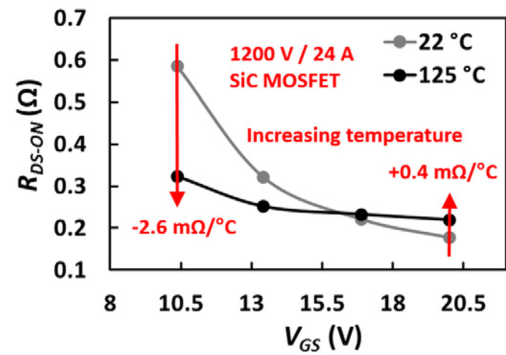

Fig. 2. Measured $R_{DS\text{-}ON}$ of a 1200 V/24 A SiC MOSFET as a function of V_{GS} for 22 °C and 125 °C.

The on-state resistance was measured at low currents by injecting a sensing current of 50 mA and measuring the on-state voltage with a digital multimeter Hameg HMC8012 while applying different gate voltages. The measurements were made using a basic test setup and the measured values agree with datasheets and literature. In Fig. 2, it can be seen that the temperature coefficient of $R_{DS\text{-}ON}$ is negative at low V_{GS} and becomes positive as V_{GS} increases. This characteristic is peculiar to high voltage SiC MOSFETs because the channel resistance is a considerable fraction of the total resistance unlike silicon MOSFETs where the total resistance is dominated by the voltage blocking drift region. This is because the resistance of the drift region in SiC is smaller since significantly thinner layers are required for blocking high voltages as a result of the higher critical electric field in SiC. The on-state resistance of a 1200 V/20 A Si MOSFET from IXYS, with datasheet number IXFX20N120P as a function of the gate voltage is shown in Fig. 3, for temperatures of 22 °C and 125 °C. It can be clearly observed how, for the voltage range selected, there is no impact of the gate voltage on the on-state resistance. However, the temperature sensitivity is considerably higher with +6.4 mΩ/°C. In the case of the SiC MOSFET, the temperature sensitivities for a gate voltage of 20 V and 10.5 V are +0.4 mΩ/°C and −2.6 mΩ/°C respectively.

Recently, after the emergence of SiC Trench MOSFET devices, it seems to be the technology adopted by different manufacturers. Trench MOSFETs have a lower input capacitance and a lower on-state resistance for the same device area compared with a planar MOSFET. This reduction of the on-state resistance appears as a result of the reduced channel resistance together with the elimination of the JFET region of the MOSFET [5,9], as can be seen from Eq. (1).

The on-state resistance of a 650 V/39 A trench SiC MOSFET from Rohm, with datasheet reference SCT3060AL is shown in Fig. 4, where the on-state resistance as a function of temperature has been characterized for gate voltages of 20 V and 10.5 V. The temperature sensitivities are +0.14 mΩ/°C and −1.0 mΩ/°C respectively.

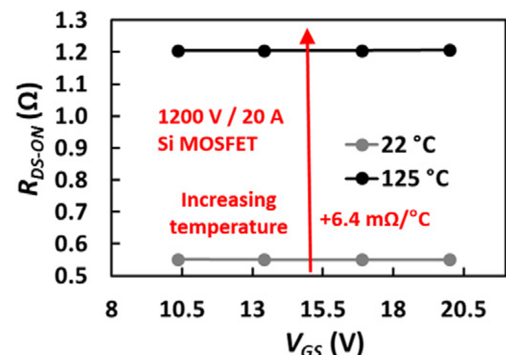

Fig. 3. Measured $R_{DS\text{-}ON}$ of a 1200 V/20 A Si MOSFET as a function of V_{GS} for 22 °C and 125 °C.

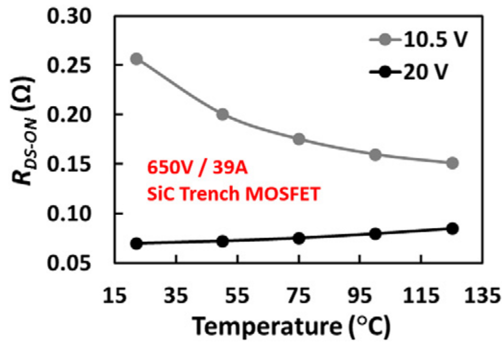

Fig. 4. Measured R_{DS-ON} of a 650 V/39 A SiC Trench MOSFET as a function of temperature, for different V_{GS} voltages.

2.3. Discussion on condition monitoring and additional considerations

An important remark about the on-state resistance is that it is defined by the thickness of the different layers of the MOSFET (voltage rating) and the chip area (current rating). The effectiveness of this particular TSEP should be studied for each MOSFET, especially given the different generations available on the market [7]. This also includes the study of the variability of the on-state resistance for devices of the same technology but different process batches. However, calibration and normalization techniques can help with this issue.

In the case of power modules with multiple chips in parallel, the negative temperature coefficient of the on-state resistance when the devices are driven at low V_{GS} values can lead to thermal runaway. The higher temperature sensitivity of the on-state resistance at low V_{GS} voltages could be exploited using an intelligent gate driver capable of applying customized occasional switching pulses for junction temperature estimation. The on-state voltage could be characterized at low V_{GS} for a determined sensing cycle, resulting in a higher on-state voltage thereby making the characterization/measurement easier. Once the sensing cycle is complete, the output voltage of the gate driver can then be adjusted to the normal V_{GS} value, hence limiting the risk of thermal runway in case of parallel chips. In addition to the increased temperature sensitivity, the on-state resistance contribution of the MOSFET chip would be higher, compared with the parasitic resistances of the packaging. Again, this aids junction temperature sensing.

Methods already used for condition monitoring [8] would benefit from the magnification of the monitored parameter since increasing the nominal on-state resistance will increase the on-state voltage measured. In [10], a gate driver which can modify the output voltage and the output resistance was presented for achieving active thermal control, and in [11] the gate resistance was modified for identifying the junction temperature using the turn-off delay time as TSEP for SiC MOSFETs, thereby suggesting that the technology for implementing these techniques is already available.

Another TSEP with its temperature sensitivity affected by both the gate resistance and gate driver voltage V_{GG} is the current switching rate. This TSEP will benefit for the aforementioned intelligent gate drivers and measurement techniques, hence the next section evaluates the impact of the gate driver on the temperature sensitivity of the current switching rate

3. Impact of the gate driver voltage on the temperature sensitivity of the switching rate

3.1. SiC MOSFET switching rate analysis

Previous research [3] shows that the switching rate of the drain current during turn-on (dI_{DS}/dt) could be an effective TSEP for SiC MOSFETs and that its temperature sensitivity is improved when the magnitude of the switching rate is reduced.

The temperature sensitivity of the turn-on transient is determined by the negative temperature coefficient of the threshold voltage (V_{TH}). For both Si and SiC MOSFETs, the impact of the negative temperature coefficient of the threshold voltage is manifested in the forward time shift of the current transient defined by Eq. (2). The value t_{TH} defines the point in time when the gate voltage V_{GS} reaches the threshold voltage. R_G is the total gate resistance, C_{ISS} the input capacitance and V_{GG} the output voltage of the gate driver, including the internal drop in the gate driver IC.

$$t_{TH} = R_G C_{ISS} \ln\left(\frac{V_{GG}}{V_{GG} - V_{TH}}\right) \tag{2}$$

Switching the devices at lower switching rates (with higher R_G) minimizes the hindering effect of the parasitic inductances on the temperature sensitivity of the turn-on transient, as was explained in [3]. Neglecting parasitic inductance, the switching rate of the drain current of a MOSFET in saturation is given by Eq. (3), and its temperature dependency modelled by Eq. (4).

$$\frac{dI_{DS}}{dt} = \beta(V_{GS}(t) - V_{TH})\frac{dV_{GS}}{dt} \tag{3}$$

where $\beta = \frac{W\mu C_{OX}}{L}$

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{dV_{GS}}{dt}\left(\frac{d\beta}{dT}(V_{GS}(t) - V_{TH}) - \beta\frac{dV_{TH}}{dT}\right) \tag{4}$$

Eq. (4) can be rewritten as Eq. (6), using the expression of the transconductance of a MOSFET in saturation given by Eq. (5).

$$g_{mS} = \beta(V_{GS}(t) - V_{TH}) \tag{5}$$

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{dV_{GS}}{dt}\frac{dg_{mS}}{dT} \tag{6}$$

where

$$\frac{dg_{mS}}{dT} = \frac{d\beta}{dT}(V_{GS}(t) - V_{TH}) - \beta\frac{dV_{TH}}{dT} \tag{7}$$

From Eqs. (3) and (5), it can be seen that the technology dependent parameters that determine the switching rate and transconductance are the threshold voltage and the gain factor (β) which depends on die size and carrier mobility. β reduces with temperature because the effective mobility reduces with temperature. The temperature coefficient of β and the threshold voltage oppose each other and the Zero-Temperature-Coefficient (ZTC) point is where the effects are counterbalanced and the transconductance is temperature invariant. In the case of Si MOSFETs, the negative temperature coefficient (TC) of the V_{TH} is dominated by the reduced β at higher temperatures, hence, the transconductance has an overall negative TC. The result of this is that the switching rate in Si MOSFETs either has a negative TC or is temperature invariant. However, in the case of the SiC MOSFET, the saturation transconductance has a positive TC because the negative TC of V_{TH} dominates the negative TC of β [3]. Hence, SiC MOSFETs have the unique property of switching-on faster at higher temperatures.

3.2. SiC MOSFET switching rate characterization

The turn-on transient was studied using a double pulse test setup. The DC link voltage V_{DC} used was 600 V, an inductor L of 2 mH and the freewheeling diode was a 1200 V/16A SiC Schottky diode with datasheet reference C4D10120A from Cree/Wolfspeed. Using small DC heaters attached to the devices, the operating temperature of the device

can be defined. The values were adjusted from ambient to 150 °C. By allowing sufficient time to reach a steady state, it can be assumed that the junction temperature is equal to the case temperature.

The current turn-on transients were measured using a current probe Tektronix TCP312 and a Tektronix probe amplifier model TCPA300. The current rating of the probe is 30 A DC, with a rise time of 3.5 ns and a bandwidth of 100 MHz. The waveforms were captured using a Lecroy Wavesurfer 104MXs-B (bandwidth of 1 GHz and a rise time of 300 ps).

In [3] it was shown that the temperature sensitivity is higher for higher rated current devices, with higher input capacitances. Hence a 1200 V/42A SiC MOSFET from Cree/Wolfspeed with datasheet reference CMF20120D has been selected for the evaluating the impact of the gate driver output voltage (V_{GG}) on the temperature sensitivity of the switching rate.

The turn-on transient of the drain current at different temperatures for $V_{GG} = 20$ V and an external gate resistance $R_G^{EXT} = 47\ \Omega$ is shown in Fig. 5. 20 V is the maximum gate voltage recommended for minimal conduction losses. The duration of the pulse which determines the load current is 50 μs, hence the self-heating impact can be considered negligible.

In Fig. 5 the aforementioned increase of the switching rate and shift in time of the turn-on transient with temperature are clearly identified. A higher temperature sensitivity during the initial stages of the turn-on transient, when the value of V_{GS} is low, is also observed. Investigations of the impact of the gate driver voltage on the temperature sensitivity of dI_{DS}/dt have been performed by varying the gate driver V_{GG} voltages from 10.5 V to 20 V and the gate resistances from 47 Ω to 220 Ω. The gate resistances used are 47 to 220 Ω since the reduced switching rates minimize the impact of the stray inductances on the temperature sensitivity of the switching rate, as was evaluated in [3]. The turn-on transients for a gate resistance of 47 Ω and a gate driver voltage $V_{GG} = 13.5$ V at different temperatures are presented in Fig. 6.

Analyzing Eq. (7), the temperature dependency of the transconductance is determined by the temperature dependency of the threshold voltage and the gain factor. For low gate driver voltages, close to the threshold, the contribution of the gain factor (negative) is smaller and the impact of the temperature coefficient of the threshold voltage is more dominant.

Using the measured transients, the switching rate has been calculated as the average slope for the set of measurements performed. Fig. 7 presents the switching rate as a function of the temperature for different gate resistances while and Fig. 8 presents the switching rate as a function of the temperature for different gate driver voltages.

From Fig. 7, it is clearly observed that for a fixed gate driver voltage V_{GG}, when the MOSFET is slowed down by means of increasing the gate resistance, the rate of change of dI_{DS}/dt with temperature decreases. Considering a temperature range from 50 °C to 150 °C with a gate voltage of 20 V and $R_G^{EXT} = 47\ \Omega$, the temperature coefficient of dI_{DS}/dt is

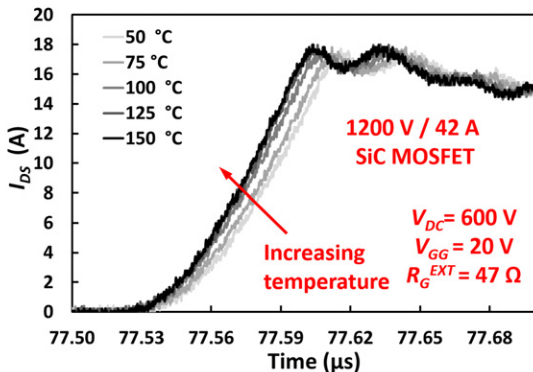

Fig. 5. I_{DS} during turn-on of a 1200 V/42 A SiC MOSFET at different temperatures. $V_{GG} = 20$ V and $R_G = 47\ \Omega$.

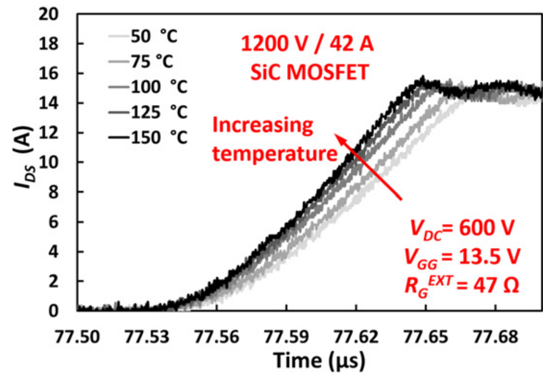

Fig. 6. I_{DS} during turn-on of a 1200 V/42 A SiC MOSFET at different temperatures. $V_{GG} = 13.5$ V and $R_G^{EXT} = 47\ \Omega$.

0.24 A/μs °C whereas for $R_G^{EXT} = 100\ \Omega$ and 220 Ω, the temperature coefficient of dI_{DS}/dt reduces to 0.17 and 0.10 A/μs °C respectively.

However, evaluating Fig. 8, if the switching rate is reduced by means of reducing the gate driver voltage the temperature coefficient of dI_{DS}/dt is approximately constant. For an $R_G^{EXT} = 47\ \Omega$, the measured temperature coefficients of dI_{DS}/dt are 0.24, 0.22, 0.22 and 0.20 A/μs °C for gate voltages values of 20, 17, 13.5 and 10.5 V respectively.

An important distinction must be made between the temperature coefficient of the absolute switching rate and that of the relative switching rate, normalized to a reference value. Table 1 shows the measured temperature coefficient of dI_{DS}/dt at $V_{GG} = 20$ V, 13.5 V and 10.5 V with $R_G^{EXT} = 220\ \Omega$ and 47 Ω. It can be seen from Table 1 that increasing R_G^{EXT} from 47 Ω to 220 Ω reduces the temperature coefficient of the absolute switching rate (in A/μs °C). However, in terms of the percentage

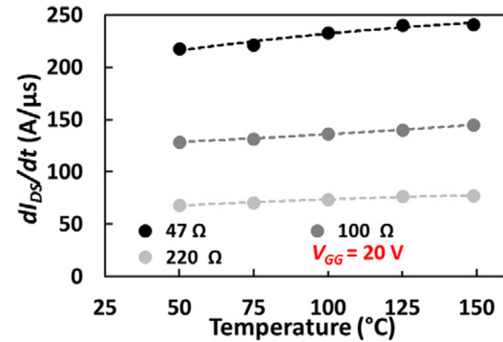

Fig. 7. dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET as a function of temperature for different gate resistances and $V_{GG} = 20$.

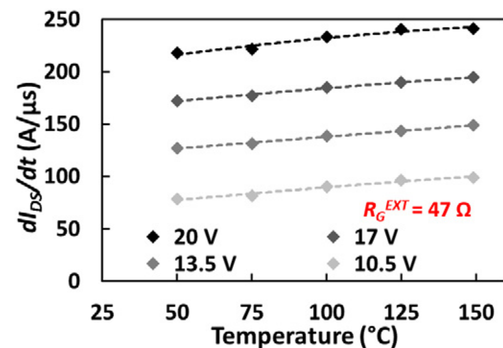

Fig. 8. dI_{DS}/dt during turn-on of a 1200 V/42 A SiC MOSFET as a function of temperature for different gate driver voltages and $R_G^{EXT} = 47\ \Omega$.

Table 1
Impact of gate driver on the temperature coefficient of the switching rate dI_{DS}/dt and the normalized increase.

	Temperature coefficient (A/μs °C)	Normalized increase (%)
$V_{GG} = 10.5$ V/$R_G^{EXT} = 47$ Ω	0.20	25.8
$V_{GG} = 10.5$ V/$R_G^{EXT} = 220$ Ω	0.07	32.3
$V_{GG} = 13.5$ V/$R_G^{EXT} = 47$ Ω	0.22	17.1
$V_{GG} = 13.5$ V/$R_G^{EXT} = 220$ Ω	0.08	22.0
$V_{GG} = 20$ V/$R_G^{EXT} = 47$ Ω	0.24	10.9
$V_{GG} = 20$ V/$R_G^{EXT} = 220$ Ω	0.10	13.9

increase, using the switching rate measured at 50 °C as reference, a larger R_G^{EXT} makes the impact of temperature on the switching rate more apparent. For example using a gate resistance R_G^{EXT} of 220 Ω, at $V_{GG} = 20$ V the switching rate increases by 13.9% over the temperature range of 50 °C to 150 °C, however at $V_{GG} = 10.5$ V, the percentage increase of the switching rate rises to 32.3%. Although the percentage increase of the switching rate with temperature is higher for low V_{GG}-High R_G^{EXT} combination, the lower temperature sensitivity of the switching rate will make the measurement more difficult (from the instrumentation perspective).

The normalized values of dI_{DS}/dt for gate driver voltages of 10.5 V and 20 V are presented in Fig. 9, for external gate resistances of 47 Ω and 220 Ω. It is clearly observed how reducing the gate driver voltage has a higher impact on the normalized (relative) switching rate increase with temperature than increasing the gate resistance.

3.3. Impact on condition monitoring and additional considerations

As was already mentioned in Section 2.3, there are already intelligent gate drivers with the ability to change the output resistance and/or the gate driver output voltage [10,11]. Together with gate drivers with di/dt control proposed for IGBTs [12], this suggests that it is possible to alter the gate drive resistance for occasional diagnostic pulses needed for on-line condition monitoring. Hence, the switching performance of the device is not sacrificed since the device is only slowed down during occasional diagnostic pulses. The TSEP could be characterized at low V_{GS} for a determined sensing cycle, resulting in a magnified temperature sensitivity of the monitored parameter for its characterization/measurement. The output of the gate driver will be adjusted to a low R_G^{EXT} and high V_{GG} during normal operation, minimizing the switching and conduction losses, when the sensing procedure finishes.

The switching rate is determined by the transconductance of the MOSFET and the threshold voltage. These two parameters are determined by the gate oxide, which has been a source of reliability problems for SiC MOSFETs. Hence, additional investigations are required into the impact of decreased oxide integrity on the accuracy of the TSEPs. Also, the impact of having multiple chips in parallel (for increasing the current capability) on the accuracy of the TSEP under non-uniform degradation conditions requires further studies.

4. Conclusion

The temperature sensitivity of the on-state resistance and switching rate of SiC MOSFETs can be improved by means of manipulating the gate driver voltage and output resistance as the results presented in this paper show.

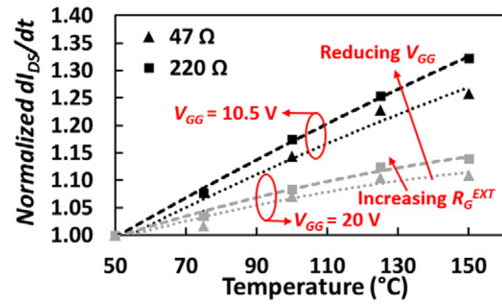

Fig. 9. Normalized dI_{DS}/dt as a function of temperature, for gate driver voltages of 10.5 and 20 V. $R_G^{EXT} = 47$ Ω and 220 Ω.

The higher temperature sensitivity of the on-state resistance and the current switching rate at low V_{GS} voltages could be exploited using an intelligent gate driver [4,10] capable of applying customized occasional switching pulses for junction temperature estimation, as it has been already proposed [11]. The temperature sensitivity for multiple chip modules together with the stability of the proposed TSEPs during the ageing of the power module should be the next research steps.

Acknowledgements

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