COMMISSION OF THE EUROPEAN COMMUNITIES

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COMMUNITY ACTIONS IN THE FIELD OF MICROELECTRONIC TECHNOLOGY

COUNCIL REGULATION (EEC) NO. 3744/81

FOURTH REPORT BY THE COMMISSION TO THE COUNCIL
AND THE EUROPEAN PARLIAMENT

EXPLANATORY MEMORANDUM

On 7 December 1981 the Council adopted Regulation No. 3744/81 concerning Community projects in the field of microelectronic technology.

Article 9 of this Regulation stipulates that each year the Commission shall forward to the European Parliament and to the Council a report on the development of the activities in the Community falling within the scope of the Regulation.

This document, which is the subject of a written procedure, is the fourth annual report on such activities.

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INTRODUCTION

On 7 December 1981, the Council adopted Regulation N° 3744/81[1] on Community actions in the field of microelectronics technology.

The actions were to address two domains of microelectronics : the "CAD for VLSI" (Computer Aided Design for Very Large Scale Integrated Circuits) and the "Equipment for Manufacturing and Testing VLSI".

Article 9 of the Regulation stipulates that the Commission shall each year forward to the Council and the European Parliament a report on the development of the activities in the Community falling within the scope of this Regulation. Although the validity of the Regulation has expired (31.12.1985) most of the projects launched have not been completed yet. The Commission, therefore, will continue submitting the yearly reports until all projects are completed. Before submission of the yearly report, its draft is presented to and discussed with the Consultative Committee which has been set up in order to advise the Commission on the implementation of the programme.

The first activity report on microelectronics (covering the period from the beginning of the programme until 15 July 1983) was submitted to the Council in October 1983 (COM (83) 564 final). The report covered the actions for the introduction of the Regulation, the various phases in the first call for proposals and its results, the reasons which led to the Commission amending the list of projects benefiting from Community support under Regulation N° 3744/81 and publishing a second call for proposals, and the work carried out to coordinate national activities and the dissemination of the results. It also covered the links between the Regulation and the ESPRIT research and development programme.

The second activity report (covering the period from 16 July 1983 until 30 June 1984) was submitted to the Council in October 1984 (COM (84) 567 final) and included the second call for proposals and its results, the progress of the projects launched through the first call for proposals, the work carried out to coordinate national activities and the dissemination of the results.

The third activity report (covering the period from 1 July 1984 until 30 June 1985) was submitted to the Council in December 1985 (COM(85) 776 final) and it included an account of the progress of the projects and of the other activities under the programme.

The present (fourth) report covers the period from 1 July 1985 until 30 June 1986 and it is organized in four sections and two annexes.

In section I is presented a summary appraisal of the programme to date. Section II gives a current status summary report for each of the 15 projects that were launched as a result of the two calls for proposals.

In sections III and IV is reported work on the two additional actions of Regulation 3744/81, i.e. on the coordination of national activities and on the dissemination of the results of the supported projects respectively.

Annex 1 is giving some details on the main activity (CAVE workshops) for the dissemination of the results of projects in the domain of CAD for VLSI.
Annex 2 presents a sample of exhibits related to the exploitation of results obtained from completed (or close to completion) projects. These exhibits have been produced by the concerned organizations during the course of their work.

I. SUMMARY APPRAISAL OF THE PROGRAMME TO DATE

The programme has been in operation approximately four and a half years. Seven of the projects were launched in early 1983 and 8 were launched in early 1984.

For most of the projects that are either completed or close to completion, it can be said that their achievements appear to be up to the initial expectations or more. However, an assessment of the overall programme has not been done yet.
The Commission has discussed and agreed with the Consultative Committee that an overall assessment of the programme should be made. It is expected that the Commission will invite one personality from industry or academia or research to head the task of the assessment. As it will be seen below, completion of the projects has started and the view is that the proper timing for launching the assessment would be within the last quarter of 1986.

It may be appropriate here, without attempting an out of scope analysis, to summarize the position of the Community in the two domains addressed by the programme (i.e. equipment and CAD for VLSI). It is believed that the position of the Community has not changed (or if it has this is very little) from the one reported last year.
The Community is still lagging considerably behind U.S. and Japan and it is still dependent on imports for most of the state of the art equipments that are used for the production and testing of VLSI circuits.
It is noted that from the discussions held with industry, research and academia (i.e. panels and workshops) for drafting the ESPRIT II workplan, it is becoming evident that more coordinated efforts at Community level are needed for developing advanced equipment. It is hoped that ESPRIT II will address sufficiently this area.
In CAD the situation is more encouraging because the Community appears not to be falling behind. In this case it can be noticed that the various coordinated actions on CAD (e.g. Regulation 3744/81, ESPRIT and national programmes) and industry's positive response to these actions are producing sizeable results.

The weakness of the Community reported last year (that seems to aggravate the situation in these technological domains) i.e. the scarcity of qualified, highly specialised personnel, still exists. However, initiatives like the ERASMUS[2], COMETT[3] and NEPTUNE[4] programmes indicate that there is a growing awareness of the need for coordinated actions at Community level.

The current situation within the framework of the programme can be summarized as follows:

In the equipment domain:

Of the 7 equipment projects launched, one (MR-12-ELT) is essentially completed, one (MR-05-SIE) is phased out and five are in progress. It is expected that the completion of these projects will contribute to the ability of the respective Community manufacturers to introduce equipment of increased competitivity in the world market. Already now the bi-directional transfer of know-how between manufacturers and users (partners) in the projects will considerably upgrade the Community technological level in this domain. Some of the equipment and know-how developed are being or will be used in ESPRIT projects that were launched in 1984 and 1985 or will be launched this year.
For some of the equipment developed under the programme there are early indications that their acceptance by the Community and the world market will be very wide. Such examples are: the "Low Pressure CVD" equipment (project MR-11-ASM), the "E-Beam Testing" equipment (project MR-15-CAM) and the "Plasma Etching" equipment (project MR-12-ELT).
Details are given in the individual project reports in Section II of this report.

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2 ERASMUS COM(85)756

3 COMETT COM(85)431

4 New European Programme for Technology Utilization in Education

In the CAD for VLSI domain :

Of the 8 CAD projects launched, two are completed and final reports were submitted, four are completed and the final reports are due now, and two are in progress. Most of the Community organisations that have any kind of interest in this technical domain are involved in these projects.
Results of these projects (either final or intermediate) are already used by the organisations involved in the VLSI circuits design and testing phases. Such examples can be taken from the largest project supported under the programme (project MR-04-CVT) or from much smaller projects such as the MR-03-KUL.

The overall programme :

Subject to confirmation by a formal assessment of the overall programme, the Commission, based on the individual project reports, is currently of the view that the programme will prove to be a successful one.

Considering the nature of the programme (i.e. advanced R and D in a highly competitive field where large investments are necessary and previous developments are becoming rapidly obsolete) some of the projects may not produce the intended results. However, even for these projects, side-effects such as the development or acquisition of know-how, the upgrading of the Community technological base and the (indirect) impact on the training or re-training of highly qualified personnel, will be substantial.

It is worth noting that the contribution of the programme in establishing the concept of Community-wide cooperation in this type and level of area of technology is considered to be remarkable. In this respect the Microelectronics Regulation 3744/81 programme is considered as one of the most important factors that paved the way to a widely acceptable and successful ESPRIT.

II. CURRENT STATUS OF THE SUPPORTED PROJECTS

The status of the 15 projects listed below is examined in the following pages of Section II.

PROJECT MR-01-IMG

Prime Contractor	: IMAG/MICADO
Participants	: TMC Ltd, SGS-ATES, RTC, PHILIPS SA PARIS, PHILIPS TELECOMMUNICATIE INDUSTRIE HILVERSUM
Title	: CERES (cascade environment for the realisation of electronic systems)
Total Community support	: 4 172 000 ECU
Duration	: 33 months
Started	: February 1983
Completion	: November 1985

AIMS AND CONTENT

To develop an integrated CAD system of VLSI circuits, supporting all the design stages from the initial specifications of the circuits to the production of the layout, test and documentation.

Main parts of this system :

- mixed mode simulation with a unique description language covering all the modelling levels (systems, behavioral, register transfer, logical gates, switch and electrical levels)
- fault modelling and fault simulation at different levels
- test data generation for PLAs
- logic compiler and silicon compiler
- general command and control language with integration of all the parts of the system
- graphical editor for circuit description (at all modelling levels)
- floor planner and leaf block design
- electrical modelling.

The main challenge of this programme is to integrate everything around a unique internal data structure.

EXPECTED DELIVERABLES

A set of reports structured in several volumes covering the following:

1) the functional architecture of the overall system together with a short description of the individual tools and pointers to the volumes containing more detailed information.

2) A set of research reports including motivations, overview of the state of the art, result of research and suggested avenues of attack and/or prototype specification where applicable.

3) Draft use documentation with examples on the developed languages and tools.

4) Evaluation reports on aspects of the system.

PROGRESS TO DATE

The project was completed on 31.10.85 and a final meeting was held on 12.11.85 at which some preliminary results were demonstrated.

A final report has not yet been delivered to the CEC and consequently no final assessment of the project has yet been made.

The indications are, however, that this has been a pioneering project to produce a VLSI design system which has partially achieved its rather ambitious goals and has produced several interesting spin-off results.

EXPLOITATION/DISSEMINATION

Continuation of aspects of the project within the industrial partners and the possible setting up of a company, by the Prime Contractor, to market the results of the project.

Participation to the CAVE workshops and publication of papers.

PROJECT MR-02-RAL

Prime Contractor	: RUTHERFORD APPLETON LABORATORY
Participants	: G.E.C. HIRST RESEARCH CENTRE, UNIVERSITY COLLEGE OF SWANSEA, N.V. PHILIPS EINDHOVEN, TRINITY COLLEGE OF DUBLIN
Title	: Three dimensional semiconductor device simulation including transient and thermal behaviour
Total Community support	: 1 774 000 ECU
Duration	: 36 months
Started	: April 1983
Completion	: April 1986

AIMS AND CONTENT

The aim is to develop robust and efficient algorithms to simulate either static or transient behaviour of semiconductor (silicon) devices. The behaviour of the device is modelled by solving Poisson's equation, the electron and hole current continuity equations and the heat flow equation by numerical techniques. The model includes expressions for relevant physical phenomena, e.g. band gap narrowing, field dependent mobilities, recombination mechanisms. The equation are to be solved in up to three spatial dimensions.

As well as studying the formulation and discretisation of these equations effort is directed towards improvements in non-linear equations solving, linear equation solving for sparse systems of equations and adaptive meshing techniques.

EXPECTED DELIVERABLES

The end deliverables proposed for the project were recommended sets of algorithms for the simulation of semiconductor devices. These algorithms will be tested by more than one partner on a range of typical semiconductor problems (benchmarks). The algorithms will be described using a pseudo-code language in sufficient detail for easy implementation by other users. The communication of algorithms at this level avoids problems of machine dependence of the deliverables and difficulties in modifying existing software to take advantage of ideas generated in the project.

PROGRESS TO DATE

The project was completed on 18.4.86.

The final interim report has not yet been delivered to the CEC and, of course, neither has the final consolidated report for the project.

The main project deliverables were modified after negotiation to produce robust 2D algorithms capable of extension to the 3D case and a code incorporating them capable of a better than state-of-the-art performance. A new ESPRIT project which starts with the 2D algorithms and aims to develop the 3D algorithms and a code incorporating them started immediately following the end of this project.

It has been decided to formally review the new project in early November 1986 and at the same time review the deliverables from the previous project since the two are intimately linked together. To this end, the final report from the preceding project will be delivered to the CEC in early September but will not be formally accepted until after this review.

EXPLOITATION/DISSEMINATION

Incorporation of the results of the 2D algorithms (extendable to 3D) in a code which would have an, at least, better than state-of-the-art performance. Continuation of the work to build a true 3D simulator in an ESPRIT project.

The 2D algorithms will be available to European industry and a code, incorporating them, produced by the end of the current project.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

A proposal for the extension of the project was submitted and approved for support under the ESPRIT second call (proposal No. 962).
Complementary work by the UK partners is under way in the ALVEY (UK) programme.

PROJECT MR-03-KUL

Prime Contractor	: ESAT LABORATORY, KATHOLIEKE UNIVERSITEIT LEUVEN
Participants	: LABORATOIRE D'AUTOMATIQUE DE MONTPELLIER (UNIVERSITE DU LANGUEDOC), N.V. PHILIPS EINDHOVEN, SIEMENS AG, SILVAR LISCO, BELL TELEPHONE
Title	: Mixed-mode behavioural verification system for MOS VLSI design
Total Community support	: 567 000 ECU
Duration	: 36 months
Started	: January 1983
Completion	: December 1985

AIMS AND CONTENT

The objective of this project is the development of a prototype system for the verification of behavioural correctness and testability of MOS VLSI design.

Both the top-down Boolean design phase as well as the bottom-up electrical and timing verification phase are envisaged.

DELIVERABLES

New to this system is that an expert system (DIALOG) is used to reduce the enormous amount of simulation time traditionally used in design by zooming in into potential critical trouble spots in the design (guided simulation) based on good design knowledge.

Therefore the expert system guides two Mixed-Mode simulators. One for top-down Boolean design covering RTL, functional, gate, switch level including assignable delay modelling (LOGMOS). Also a powerful fault-simulator with accurate fault models (FLOGMOS) has been developed.

The other simulators are a new electrical/switch level simulator (SWITCH) that includes device impedance and charge sharing and a segmented waveform analysis simulator (SWAN) which is 20 to 50 times faster than SPICE, but has the same accuracy.

In order to communicate with this system the user has a procedural structural description language (HILARICS), a symbolic, connectivity based graphics editor that makes the compaction too (CAMELEON), a procedural PLA, ROM generator (PLASCO).
The deliverables thus are in the form of the set of programmes CAMELEON, PLASCO, HILARICS, DIALOG, LOGMOS, FLOSMOS, SWITCH, SWAN.

RESULTS

All six reports have been received, the last covering the period till December 85. The project is now completed.

The contractors have not had any significant delays, but a small delay was reported on the data-base work because of under-estimation of the effort required. Corrective action have been taken.

First phase test versions of all programmes have been built and have been tested by the industrial partners. DIALOG, LOGMOS, SWITCH and PLASCO have been successfully used for debugging, simulation and designing of VLSI chips. DIALOG experiments show the feasibility of an expert system for guided simulation while SWITCH shows performance improvements of 20 to 50 times with respect to SPICE. The underlying principles of SWAN have been tested successfully and detailed transistor models have been entered in it. A first version of HILARICS has been interfaced to CAMELEON and new DIALOG whereby the knowledge base is built up using a PASCAL-PROLOG like language.

To date the tools developed are integrated into the CATHEDRAL I Silicon compiler, together with other tools developed in ESPRIT projects 97 and 1058. A new LISP environment LEXTOC for design style description has been implemented. Use of this language allows a remarkable circuit debugging speed of 20000 transistor/hr on a VAX 11/780. The design management system is embedded in CATHEDRAL I. The only fundamental differences in the outcome of the project are the extension of the packages currently in the system and the addition of a data-base prototype to the system.

EXPLOITATION/DISSEMINATION

In addition to the in-house use by the industrial partners commercial exploitation of the system (or parts of it) will be undertaken by the participating in the project software house (Silvar-Lisco) (e.g. PLASCO, SWITCH).

Dissemination is guaranteed through the CAVE workshops, publication of technical papers and the participation of two Universities. At the end of the project a two days open workshop was organized in Leuven on 27-28 January 1986, in which a lot of industrial people from all over Europe participated.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

The work done in this project interrelates well with other work done in ESPRIT 97 and 1058.

PROJECT MR-04-CVT

Prime Contractors	: CNET, CSELT, FI/DBP
Partners	: CII-HB, CIT-ALCATEL, CENG-LETI, IMAG, INRIA, THOMSON EFCIS, SGS-ATES, ITALTEL, OLIVETTI, AEG-TELEFUNKEN, STANDARD ELECTRIC LORENZ, THE UNIVERSITIES OF BOLOGNA, GENOVA, MILANO AND TORINO, THE UNIVERSITIES OF AACHEN, BREMEN, DARMSTADT, DORTMUND, KAISERSLAUTERN AND KARLSRUHE, GMD, FRAUNHOFER GESELLSCHAFT
Title	: CVT (CAD for VLSI for TELECOMMUNICATIONS)
Total Community Support	: 12 000 000 ECU
Duration	: 3 years and 4 months
Started	: February 1983
Completion	: May 1986

AIMS AND CONTENT

The overall objective of the CVT project is to implement an integrated CAD system to be used by system designers, with particular reference to the requirements of the telecommunication field.

From the user point of view, the main features required in the system are:
- to be simple, that is easily accessed by system designer
- to be fast and sure, providing system designers with a way to go from high level descriptions to silicon implementations either automatically (when possible) or with the help of an intelligent assistant suggesting solutions, providing tools and verifying and comparing results.

The system proposed has a modular structure for the following reasons :
- it has to take advantage of the existing tools;
- it has to be flexible, to cope with the foreseen evolution during the time of design methodologies, application tools and supporting hardware;
- it has to be multi-user, leaving to each designer (or Company) the opportunity to assemble the system in the way which best suits his (or its) needs and constraints.

Summarizing, the CVT project is aiming at the following main objectives:

- to define and implement the kernel of the integrated CAD system that is the design data base system and the user interface;
- to originate a complete set of tools for description, analysis and synthesis, to aid the designer during the architectural design phase, going from the initial specifications to floor plans (this is a key item towards the VLSI devices design, establishing a link between the two previously separated worlds of system designers and circuit designers);

- to define a set of coherent criteria for designing complex fault-tolerant, possibly self-repairing architectures, easy to test with the aid of functional test generators;

- to develop symbolic layout tools, which are the VLSI way to layout (as a matter of fact, from one side they provide the circuit designer with an intermediate, easy to use description of the masks, and from the other side they make easier the task of developing tools for automatic placement and routing);

- to provide device models helping both, the technologists to produce the device structures which best suits the TLC application needs, and the circuit designers to obtain effective simulators for circuits manufactured using advanced VLSI technologies;

- to start the work on knowledge based system, which if successful and when successfully integrated with the previously defined system, will give rise to a second generation of integrated CAD systems.

DELIVERABLES

The kernel of an integrated CAD system (user interface and data base management system) plus a set of advanced CAD tools mainly in the areas of design at system level, testing, symbolic layout and device modelling.

RESULTS

The project was formally completed end of May 1986. The final report is currently compiled for submission around July/August 86.

During the course of the project the following events are also noted:

a. University of Pisa withdrew from the project (did not sign the contract). Their task was taken over by CSELT.

b. A new major task (task 5) was inserted for the integration of the system and shared between CSELT, CNET and FI/DBP and

c. the work programme for one of the subtasks was transferred from Univ. of Dortmund to Fraunhofer Inst. (it was requested by both parties) as of 1st August 1984.

The project has progressed well with only about 4 months delays in very few of the 36 subtasks and in the system integration task.

One of the subtasks has encountered serious problems (i.e. difficulties in implementing a specific theoretical approach) and it was decided to discontinue the work.

In a second subtask the contractors had requested to reduce the workprogramme because it was found that the theoretical and technical difficulties require extensive resources not foreseen when starting the project.

Neither of the above two subtasks is critical for the project. The contractors have assembled and successfully demonstrated the kernel of an integrated system. They have also tested in real applications (e.g. a 20000 transistors I.C.) many of the software tools.
In exhibit 2 Annex 2 to this report it is given a full list of the software tools developed under the project and a basic description of the CVT system.

EXPLOITATION/DISSEMINATION

In addition to the in-house use by the industrial partners the system (or part of it i.e. the tools) will be available through the participating research institutes (prime contractors) for use by other Community organisations.

The prime contractors have declared that the object code of the developed software tools will become available to Community organizations, free of charge (only at gathering cost) and with the only condition that they communicate to the CVT contractors any suggestions for improvements that they may have.

Dissemination was ensured through the CVT open workshops, the CAVE workshops, publication of papers and the participation of the University partners.

The first CVT open workshop took place in Torino (April 1984), the second in Darmstadt (April 1985) and the third in Grenoble (April 1986) where the kernel of the integrated system was demonstrated to invited representatives from industry, research and academia.
In addition to the in-house (for industrial and research) exploitation of the results, the prime contractors are currently negotiating with software houses that will undertake the commercialization of the system or its parts.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

ESPRIT projects 271 (ADVICE) and 802 (CVS) are very strongly related to CVT. Software tools, kernel system and the data base developed in CVT will be used by these ESPRIT projects.

PROJECT MR-05-SIE

Manufacturer	: SIEMENS A.G.
Users	: EFCIS SA, GRUNDIG AG, ITALTEL SpA
Title	: VLSI TESTER 764/780
Total Community support	: 6 712 000 ECU
Expected duration	: 36 months
Started	: January 1983

AIMS AND CONTENT

The aim of this project is the development of VLSI Testers SITEST 764 and SITEST 780. It is planned to develop other VLSI Testers based on a similar technology in order to be able to offer to the customers a whole family of VLSI Testers.
The two VLSI Testers SITEST 764 and 780 differ quite considerably in their performance. The essential features of VLSI Testers are the bit repetition rate with the related system accuracy and the maximum number of Pins per testhead. The corresponding figures are 12 MHz and 64 Pins for the SITEST 764 and 50 MHz and 256 Pins for the SITEST 780.

EXPECTED DELIVERABLES

The users will receive prototype equipment of VLSI Tester 764 in mid 1984 and prototype equipment of VLSI 780 in mid 1985. The users' experience, obtained through the use of the equipment for testing advanced VLSI circuits, will be documented (reports). It is expected that after completion of the project the testers will be fully commercialized.

PROGRESS TO DATE

Six progress reports have been submitted covering the period until end of November 1985. The hardware and software development and testing of the SITEST 764 is completed and the Hw/Sw integration (that had encountered some technical problems) was completed in November 1985. Four hardware prototypes are operational (one installed at Grundig and one at Italtel). This represents approx. 18 months delay in the original schedule of the SITEST 764.

Due to the technical difficulties encountered and the considerable increase in cost to develop both the SITEST 764 and SITEST 780, Siemens has announced their intention to "relax" some of the target specifications of the SITEST 780 and instead to produce an intermediate tester the SITEST 770 with target delivery automn 1988. The additional costs would be covered entirely by Siemens resources.

In view of the above the Commission held (1.2.85) a major project review in order to identify the associated problems (technical or other).

The results of the review can be summarized as follows:
the reasons for the delay can be broadly justified, the inherent difficulties of developing an advanced tester (the SITEST 780) are admittedly great but the timing and the new target specifications for the SITEST 770 (although well above the target specifications given in the Technical Annex of the Regulation 3744/81) are not the optimum compared to the current trends in the world market.

Considering all the factors and specifically the aims of the Council Regulation 3744/81, the efforts of Siemens to develop these testers that fit within their major programme of CAD/CAT integration and the reservations expressed by two of the partners (EFCIS and ITALTEL) in respect to the delays and the modifications of the technical targets, the Commission has requested all the partners to the project to review their position and workprogrammes.

Following a carefull review of the situation, the project participants and the Commission have agreed that the project be phased-out by the end of June 1986. This will allow a good coverage of the workprogrammes of the manufacturer and the users for the SITEST 764. Work however for either the SITEST 770 or SITEST 780 will not be continued within the project.
The final report is expected to be submitted by the end of August 1986.

PROJECT MR-06-STL

Prime Contractor	: STANDARD TELECOM LABS
Participants	: STANDARD ELECTRIC LORENZ, BRITISH TELECOM, G.E.C. TELECOM, LABORATOIRE CENTRAL DE TELECOMMUNICATIONS DE VELIZY
Title	: VLSI verification and compilation
Total Community support	: 677 000 ECU
Duration	: 40 months
Started	: January 1983
Completion	: June 1986

AIMS AND CONTENT

a) To reduce the time taken to produce correct and compact custom VLSI;

b) to formalise a conceptual framework in which designers can manage to think about the behaviour of VLSI systems;

c) to provide computer aids which will help designers to progress from the behaviours conceived for VLSI systems to circuits implementing those behaviours;

d) to establish the role of verification in VLSI design.

The intention is to apply techniques of programming and advances in the theory of computing to chip hardware design. The designer will specify the behaviour of the chip as a programme in a 'behaviour language', simulate the behaviour to show that it conforms to what is expected of it, and transform the behaviour into a layout which correctly implements it. The layout will be formed from cells some of which may have been constructed by the designer in a 'layout language'.

EXPECTED DELIVERABLES

a) Specifications of languages, calculi and user interfaces to computer aids;

b) reports by the user firms on the trials of the computer aids;

c) published technical papers;

d) programmes and related documents on which to base a programme product.

Once initial versions of the languages, the calculus and the computer aids have been devised, their soundness and practical utility will be examined by trying them out on real VLSI systems and verification strategies. The reports on the trials by the users will be relied on in the production of revised versions of the languages, the calculus and the computer aids.

PROGRESS TO DATE

The project had been extended and it was completed end of June 1986.

The major activity during this period was the preparation for the 2nd user trial. The LTS Tutorial and the Designers guide have been extensively revised and extended. The entire programme suite including the latest corrections and additions was released to the users prior to the two day user workshop. The workshop itself was a success with the users making extensive live use of the programmes. As most of the participants in this trial are engineers new to the system, the workshop was an introduction to the complete system not merely the layout aids which are the main feature of this trial.

Following the trial, work has concentrated on the generating the second set of floor-planning manipulations. As a number of comments have been made on the efficiency of these prototype tools considerable effort has been expended on analysing where they are least efficient and improving the efficiency where possible. Work has continued on the definition of LTS 1.5, mainly trying to clarify the consequences of various options. We have implemented an incremental type checker in the language analysis phase which will improve the perceived performance of the manipulator.

The final interim report (1.1.86-30.6.86) and the final consolidated report are to be delivered within the next few months after which an assessment of the achievements of this project can be made.

EXPLOITATION/DISSEMINATION

In house use by the prime contractor and on an agreed basis by the other partners. Contractually it is foreseen (as in all the other projects) that if the contractors do not exploit the results within one year from completion the results should be made available with commercial terms to other Community organizations.

Dissemination through the CAVE workshops. A series of lectures (for the Universities of Aston and Dublin) is based on work done under this project.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

The UK partners are carrying out complementary to this project work under the ALVEY (UK) programme.

It is noted also that British Telecom has allowed the "Astra" system, parts of which were developed under the project MR-09-DFT, to be used by this project for the initial user trials.

PROJECT MR-07-CRK

Prime Contractor	: UNIVERSITY COLLEGE OF CORK
Participants	: MICROELECTRONICS LABORATORY OF QUEENS UNIVERSITY OF BELFAST, ANALOG DEVICES, GEC
Title	: Two and three dimensional numerical modelling of MOS devices
Total Community support	: 366 000 ECU
Expected duration	: 36 months
Started	: February 1984
Expected completion	: February 1987

AIMS AND CONTENT

The project entails the development and application of a suite of computer programmes for numerical analysis of 2D and 3D MOS devices.

A hierarchical range of programmes will be developed, namely:

a) quasi-analytical models (micro-computer)
b) 2D static and transient, finite element and finite difference models (super mini-computer)
c) 3D static, finite element and finite difference models (super mini-computer)

The aims of the project are:

a) to develop finite element and finite difference computer programmes for the simulation of 2D and 3D MOS devices
b) to develop computer graphics packages compatible with and complementary to (a)
c) to develop simplified quasi-analytical computer programmes for use on micro-computers
d) to apply the above programmes to a wide range of MOS devices.

EXPECTED DELIVERABLES

The deliverables shall consist of a series of reports giving :

a) details of the software developed
b) the associated algorithms and numerical techniques
c) details of application to MOS devices of the suite of programmes.

PROGRESS TO DATE

Four interim reports have been received, and report No. 5 covering the period 1.11.85-30.4.86 is now due.

The project up to the last date reported was just over half completed and all tasks were on schedule. A number of deliverables have been received with the last report but not yet evaluated.

These are all in the form of technical reports and user manuals for some of the software package under development.

A review of this project will be held later this year to ascertain progress towards the technical goals and assess the deliverables received to date.

EXPLOITATION/DISSEMINATION

The computer programmes could be made available, on a commercial basis, to other European organizations as well as being used and further developed within the project partners organizations.

PROJET MR -08-PHL

Manufacturer	: N.V. PHILIPS GLOEILAMPENFABRIEKEN, Eindhoven
Users	: UNIVERSITE DE DELFT, BELL TELEPHONE, SIEMENS AG, FRAUNHOFER INSTITUT BERLIN
Title of project	: "High resolution Electron Beam Lithography"
Total Community support	: 2 224 000 ECUS
Starting date	: November 1983
Duration	: 3 years
Expected completion	: November 1986

AIMS AND CONTENT

The project is a joint effort of the five partners to further the development of high resolution lithography and its applications. The introduction of high-resolution E-beam lithography equipment will be accelerated, providing a tool for development and production of advanced IC's. Two main application fields will be explored i.e. direct write on wafers with submicron structured patterns and X-ray mask preparation.
The end result will be an improved product offering advanced lithographic equipment from European source. Technology for production of advanced IC's will be made available to European industry and to European maskmaking centre for X-ray masks.

EXPECTED DELIVERABLES

The manufacturer will deliver to the users a number of enhancements for the Electron Beam Pattern Generator (EBPG). Siemens/Fraunhofer will be using the equipment as a tool for the generation of X-ray masks. Bell/Delft will be using it for direct writing on wafers.
Both applications are expected to give results not only for improving the equipment but also for improving the respective parts of the process for manufacturing advanced VLSI circuits.

PROGRESS TO DATE

Five reports have been submitted covering until May 1986. The equipment manufacturer (Philips) has completed all of their tasks and all the equipment enhancements have been installed at the users' premises.

Work by the manufacturer is continued now as necessary for improving the prototype subassemblies when this is found advisable through the cooperation/feedback with the users.

The Siemens/Fraunhofer work programme: preliminary tests on the equipment are completed and the work is progressing on the investigation and optimization of X-ray mask writing process (mask technology and resist development process for sub-micron structures). The Bell/Delft work programme: it is well under way with a delay of about 4 to 6 months (due to late shipment of their equipment enhancements). Preliminary tests on the equipment are completed and work continues on resist and sub-micron patterns, marker detectors for direct writing on wafer and upgrading certain parameters of the equipment, as well as relevant experiments on the process at Bell Telephone. Overall the project seems to advance in a satisfactory way without any major (technical or other) problems.

Currently the possibility to extend in time the work on direct writing is considered. This will enable the partners to enhance some of their preliminary findings in this very important application of the equipment.

EXPLOITATION/DISSEMINATION

Commercial exploitation of the enhanced equipment will be undertaken by the manufacturer PHILIPS.

Dissemination as foreseen in the "General Measures" (page 44 of this report).

PROJECT MR-09-DFT

Principal contracting party	: UNIVERSITY OF DELFT
Associates	: I.C.S. Rotterdam, T.H. Eindhoven, T.H. TWENTE Enschede, BRITISH TELECOM RESEARCH LAB., P.C.S. Munich, I.C.N. Enschede
Title of project	: "The cooperative development of a hierarchical VLSI design system"
Total Community support	: 2 260 000 ECU
Starting date	: December 1983
Duration	: 2 years
Completion	: January 1986

AIMS AND CONTENT

The aim is the design, development and prototype production of a complete, consistent and integrated system for the CAD of VLSI. The system is to be implemented on intelligent design stations running a standardized portable operating system under which will be implemented a hierarchical multilevel file system plus management software to provide controlled access to stored relevant design and test data.

A complete set of efficient application programmes will be produced to work with the data and to support a range of design methods for VLSI. The system will be designed with the needs of independent designers in mind and will provide interfaces to fabrication facilities in silicon foundries.
Provision for the communication of individual workstations will be made via local or wide area networks to form a distributed design system which can include larger computational units.

DELIVERABLES

A prototype ICD system was demonstrated at the end of the project. Full documentation was available.
Software modules of parts of the system have been produced throughout the project lifetime. A 900 pages thick book "The Integrated Circuit Design Book" has been written and is published by Delft University Press. It details all the work that is being done.

RESULTS

All four reports have been received, the last one covering the period till December 1985. The project has now ended.

In general it may be stated that all partners have achieved their goals. All major components of the system are present and have been demonstrated.

In addition to the piecewise linear simulator, the project added to the system a switch level simulator and a timing simulator. Also an interactive and incremental design-rule checker was added. These items were not specified in the original Technical Annex. The project was able to produce more than originally promised. One partner, ICN, got bankrupt in October 1985. This did not cause any serious problem as all rights and obligations were immediately taken over by ICS.

EXPLOITATION/DISSEMINATION

In addition to the in-house use the system is commercialized by the ICD Co. (NL).

Dissemination is guaranteed through the CAVE workshops and the University partners. A two days open workshop was organized in Delft at the end of January 1986, in which participated many industrial people from all over Europe.

A public announcement of the project results was made in the Custom Electronics and Design Techniques Show (London, 5-7 November 1985). A publicity folder was printed, and ICD is Beta-test siting the system now. A lot of interest is noticed and sales are expected in Q4 of 86.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

The work is extended under ESPRIT (Project No. 991).
The UK partner is carrying out complementary work under the ALVEY (UK) programme and the Dutch partners under the NELSIS (Netherlands) programme.

Parts of the "Astra" system (British Telecom) have been developed under this project. The "Astra" system will be used in MR-06-STL.

PROJECT MR-10-MOV

Manufacturer	:	M.O.VALVE Company Ltd, London
Users	:	UNIVERSITY COLLEGE OF CORK, MOSTEK IRELAND Ltd CII-HONEYWELL BULL
Title of project	:	"Development and evaluation of manufacturing equipment for the production of low cost, high reliability packages suitable for hermetic protection of integrated circuits of high pin count"
Total Community support	:	942 000 ECU
Starting date	:	January 1984
Duration	:	3 years
Expected completion	:	January 1987

AIMS AND CONTENT

a) Define the requirements of the equipment by establishing package specifications as required by the micro-electronic industry with particular emphasis to the one required by each partner.

b) Develop the equipment for the manufacture of the packages of the chosen design.

c) Commission manufacturing equipment and demonstrate large scale production.

EXPECTED DELIVERABLES

1) a. Initial samples) To the users for assessment of the
   b. Final samples) equipment under development

2) Interim and Final reports. The final report will contain equipment description and specification.

PROGRESS TO DATE

Package specification and acceptance procedure, manufacturing method and specifications of equipment for package manufacturing have been defined during the first six months period.

The second period has concentrated on defining the method of fabrication. A review meeting took place on 19th March 1985 in London with positive results. The second interim report covering the period 1.7.84 to 31.6.85 has been accepted.

During the third and fourth period, constructions of sample packages was achieved. Prototypes will be delivered to the partners for assessment in August 1986.

General Comments

The cooperation between the partners and the management of the project are effective.

The choice of equipment appears good, there were some delays in the delivery of some equipments but now all outstanding equipment items are installed and operational.

The problem of the procurement of suitable type of material for package manufacturing has been adequately solved for the project itself but there still remains some concern about second source availability.

Mostek Ireland has ceased operations in October 1985.

Bull S.A. immediately offered to replace Mostek for the assessment of the high lead count package made for the project.
Decision was however delayed and the possibility to replace Mostek by another industrial partner was investigated.
Due to the short time that has been left for the project to run, new partner was not possible to be found.

Under these the Bull offer is now considered as the only workable solution. Detailed workprogramme and time schedule covering the work previously devoted to Mostek are under preparation.

Conclusion

Facilities installed and equipment received and commissioned appear to be satisfactory and should be effective. Further evidence of success it is hoped to be provided following evaluation of package samples by the users.

(3)

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the results of the project. A patent has been applied for.

Dissemination as per "General Measures" described in page 44.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

- The MO-Valve Company together with Thomson have submitted the ESPRIT (2nd call) proposal N° 830 "Packages for High Speed Digital GaAs Integrated Circuits". The proposal has been approved for support.

- CII-Honeywell Bull together with British Telecom, GEC, Marconi Research Centre, have submitted the ESPRIT (2nd call) Proposal N° 958 "High Performance VLSI Packaging for Complex Electronic Systems". The proposal has been approved for support.

- MO-Valve together with other British organizations are involved in the Alvey project "High Performance Packaging Interconnect".

PROJECT MR-11-ASM

Manufacturer	: ASM EUROPE BV, Bilthoven, Netherlands
Users	: MATRA-HARRIS SEMICONDUCTORS, INSA Lyon, PLESSEY RESEARCH CASWELL LTD
Title of project	: "Development of a refractory metal deposition process and related equipment"
Total Community support	: 1 169 000 ECU
Starting Date	: December 1983
Duration	: 42 months
Expected completion	: June 1987

AIMS AND CONTENT

The main aim of this project is the development of advanced equipment for chemical vapour deposition process (CVD) of refractory metals. Initially efforts will be concentrated on tungsten deposition and at a later stage other refractory metals will be investigated. Phase I of the project will cover straight-forward tungsten CVD and Plasma enhanced CVD in order to prove the feasibility and to gain experience at the users premises with all influencing parameters. Phase II will cover CVD process with improved features as deposition, automatic wafer handling, high throughput etc.

EXPECTED DELIVERABLES

Initially two equipment prototypes (Mark I) for low pressure CVD will be delivered to INSA and Plessey and one for plasma enhanced CVD to INSA. After the evaluation of the Mark I two advanced prototypes (Mark II) will be delivered to Matra-Harris and Plessey for further evaluation and optimization.

PROGRESS TO DATE

Four interim reports have been submitted covering the period until the end of 1985 and a fifth is due in July 1986.

Two equipment prototypes (Mark I for low pressure CVD) have been delivered to the users (Plessey and INSA).

The plasma enhanced version of MKI was delivered to Plessey in November 1985 and it is currently under testing.

The partners have agreed, for technical reasons, to prolong by approx. 6 months the period of experimenting with the Mark I and thereafter, based on their results, to commence the development of the updated version of the equipment (Mark II).

Matra-Harris in cooperation with Plessey have started their workprogrammes on selective deposition of tungsten on silicon substrates and due to the importance given to their workprogrammes their efforts are intensified.
Due to some infrastructural problems and redirection of their research efforts work at INSA has been discontinued. INSA is currently considering withdrawal from the project and the other partners may have to undertake the completion of INSA's workprogramme.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the equipment under development.

Dissemination as per general measures described in page 44.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

Results from this project are expected to be utilized in the ESPRIT project No. 554. Some complementary work is also carried out in ESPRIT project 1125.

The UK partner is carrying out complementary work under the ALVEY (UK) programme.
Philips (Netherlands) has indicated an interest for the project and the partners have agreed in a scheme for cooperation. Philips however will not receive any Community support for their contribution in the project.

PROJECT MR-12-ELT

Manufacturer	: ELECTROTECH RESEARCH LTD, Bristol, United Kingdom
Users	: SIEMENS AG, THOMSON/EUROTECHNIQUE
Title of project	: "MINSTREL, the development of a production orientated plasma/reactive ion etching system for all major processes"
Total Community support	: 1 140 000 ECU
Starting date	: November 1983
Duration	: 32 months
Expected completion	: June 1986

AIMS AND CONTENT

The aim of the project is to strengthen Europe as a leading equipment manufacturer for current and future VLSI devices. It is intended to meet the requirements of the worldwide semiconductor manufacturers through the remainder of this decade and into the 1990's. The final system will set new standards of performance and it is hoped that at the time of its introduction it will be significantly more advanced than any competitive system.
Emphasis will be given to such process requirements as throughput, selectivity, uniformity, inhibition of particulates whilst fully automated cassette-to-cassette, minimum floor space in critical clean room areas and ease of service access will be essential features, it is intended that the basic design will allow for varying etching modes to be conducted with minimal adjustment, it will have the ability to process all materials both in current use and planned future technologies, and will utilize new concepts in controlled environment for lowering particulate contamination.

EXPECTED DELIVERABLES

The manufacturer will deliver to the users initially a single chamber equipment prototype and later on a four chamber prototype.
Both users will test and improve the equipment carrying out their own R&D project. The end goal is the application of the equipment (system) for the preparation of 1 um line resolution for very high scale MOS circuits in an industrial environment.

RESULTS

The project is essentially completed.
The equipment manufacturer has finished the work foreseen in the workprogramme.
The users workprogrammes are expected to be completed end of June 1986.
The final report will be submitted in early September 86.

The two single-chamber prototypes had been delivered to Siemens and Thomson/Eurotechnique (April and July 1984 respectively) and the advanced four-chamber prototypes in April and November 1985.

In Siemens the prototypes were used mainly in the development of aluminium etching processes and in Eurotechnique mainly for polysilicon etching.

The project is considered to be a very successful one with nearly all the initial technical objectives achieved.

EXPLOITATION/DISSEMINATION

The manufacturer has already proceded in the commercialization of the equipment and the interest indicated by the industry is very keen.

Exhibit No. 5 of Annex 2 to this report gives some basic information on the equipment.

Dissemination as per general measures described in page 44.

PROJECT MR-13-BUL

Principal contracting party	: CII-HONEYWELL BULL, Paris
Associates	: G.E.C. London, PLESSEY RESEARCH CASWELL Ltd, UNIVERSITY OF DUISBURG, UNIVERSITY OF AACHEN, AUTOMATION AND MICROELECTRONICS LABORATORY OF MONTPELLIER (LAMM)
Title of project	: "A CAD system for VLSI testing"
Total Community support	: 2 279 000 ECU
Starting date	: February 1984
Duration	: 3 years
Expected completion	: February 1987

AIMS AND CONTENT

Upgrade present test methods and CAD tools to cope with the needs of VLSI of late 80's.

Two main phases:

A) Analysis and specification :

Starting from the failure modes analysis of the most commonly used IC technologies and functional blocks

- define a method based on a combined implementation of built-in devices and comprehensive test generation algorithms
- Specify the CAD software to be developed and the associated data processing framework (including special purpose hardware if necessary).

B) Development and Integration :

- develop the CAD software modules and integrate them in a flexible integrated system, with easy to use interfaces.
- Implement examples of specific hardware to demonstrate feasibility and performances.

EXPECTED DELIVERABLES

- Reports on VLSI test methodology and design rules for testability
- Demonstration by examples of the capabilities of the CAD software system developed.
- Specifications of special purpose hardware (if any).
- Proposal of standards (if any).

PROGRESS TO DATE

Five interim reports have been received, the last covering the period 1.10.85-30.4.86. A total of some 38 deliverables in the form of technical reports and specifications for software tools have been received to date and in period 6 a number of these tools will be developed. Work is ongoing on all the project main work-packages although staffing problems have necessitated a reorganization of one of the tasks so that one participant has taken over the work of another. The contractual arrangements for this are currently being carried out.

The work to date is largely on schedule and an important integration phase is now being entered.

There will be a poster session and a demonstration from the CATE team at ESPRIT Technical Week 86.

EXPLOITATION/DISSEMINATION

The results of this project will be fully exploited by the participants within their own organizations as well as contributing to a parallel ESPRIT project. Other spin-offs from the project, especially those developed by the Universities, are capable of further, possibly, commercial exploitation within Europe.

PROJECT MR-14-EKC

Manufacturer	:	ELEKTRONIK CENTRALEN, Hoersholm, Denmark
Users	:	BRITISH TELECOM, SGS-ATES, MATRA S.A.
Title of project	:	"Static and dynamic burn-in systems"
Total Community support	:	1 841 000 ECU
Starting date	:	December 1983
Duration	:	3 years
Expected completion	:	March 1987

AIMS AND CONTENT

To develop and manufacture a general purpose dynamic burn-in/test system for complex integrated circuits.
A first prototype will be developed and manufactured to agreed specifications and delivered to the users. This will then be upgraded with the help of the feedback from the users to form the basis of a commercially realisable product.

EXPECTED DELIVERABLES

Design and manufacturing of 3 complete equipment prototypes will be delivered to the users. Reports on system performance will be produced by the users and a final version of the equipment will be provided allowing final trials and reports by the end of the project.

PROGRESS TO DATE

Four reports have been received covering until the end of 1985 and a fifth is due in July 1986.

During this period development work has been carried out on all hardware sub-assemblies and software modules of the system with close cooperation between manufacturer and users.

There is a considerable delay of about one year due to the fact that a key component (gate-array) had to be re-designed. However, the first prototype is now ready to be installed at the premises of British Telecom in August 1986.
Two more prototypes will be installed in Sept. and Oct. 1986 at the other two users.
Due to the above mentioned delay the contractors have requested to extend the duration of the project until the end of 1987, in order to allow the users to complete their workprogrammes that had been agreed initially.

EXPLOITATION/DISSEMINATION

Elektronik Centralen has sublicensed the commercial exploitation of the system to SCANTEST SYSTEMS A/S (Danish company, subsidiary of A/S ELBAU). SCANTEST is putting the final commercial details of the systems and has already started marketing activities. Details are given in Annex 2 of this report.

Dissemination as per general measures described in page 44.

PROJECT MR-15-CAM

Manufacturer	: CAMBRIDGE INSTRUMENTS LTD, Cambridge
Users	: SGS-ATES, CSELT Turin, Standard Elektrik Lorenz AG, SIEMENS AG
Title of project	: "Electron beam testing equipment for VLSI"
Total Community support	: 966 000 ECU
Starting date	: December 1983
Duration	: 2.5 years
Expected completion	: December 1986

AIMS AND CONTENT

The development and manufacture of an electron beam testing system for the testing and evaluation of advanced VLSI. The system to be based on the voltage contrast development work carried out at Siemens and the scanning electron microscope (SEM) systems developed by Cambridge Instruments. The equipment will be commercially realized by Cambridge Instruments. The development and manufacturing work will be carried out in 3 overlapping phases: Phase I - Development of basic equipment and extension of techniques; Phase II - Enhancements and transfer to the new instrumentation; Phase III - Upgrading of instrumentation to provide an automated system utilising the results of the earlier phases. Users will participate between Phases I, II and III.

EXPECTED DELIVERABLES

The manufacturer will deliver to the users a first equipment prototype (EB1). The equipment will be tried and tested by the users and the manufacturer based on the outcome of the trials will deliver an upgraded version (EB2). Reports on the system performance will be produced by the users.

PROGRESS TO DATE

The project has sustained a number of difficulties (including some modifications in the technical requirements of the users) that resulted in a delay of approx. 9 months.

The first EB1 unit was delivered to Siemens in Nov.1984 and the studies on the dynamic voltage measurements have started.
The second unit was delivered to CSELT/SGS in June 1985 and the third was delivered to SEL in September 1985.

The installations and trials at the users sites have progressed. Actual applications (e.g. with fast ECL memories) have indicated that the equipment is performing well. Many further improvements have been brought to upgrade the equipment and (from the users point) only a few minor improvements may be necessary. The project (including work at the users' sites) is expected to be completed beginning of 1987.

EXPLOITATION/DISSEMINATION

The manufacturer intends to commercialize the equipment under development.

Dissemination as per general measures described in page 44.

LIAISON WITH OTHER PROGRAMMES/PROJECTS

SGS-ATES and CSELT are participating in ESPRIT project No. 271 where the equipment developed under this project will be enhanced for automatic validation of ICs.

III. COORDINATION OF NATIONAL AND COMMUNITY ACTIVITIES

1. National Activities

Articles 1 to 3 of Regulation No. 3744/81 make provision for the setting up of an information and consultation "system" between the Member States and the Commission. The system covers all information of a scientific, economic and financial nature concerning any activities under the authority of the Member States in progress on the date the Regulation enters into force or contemplated after that date.

Because of shortage of staff when the programme was launched, the Commission felt it preferable to give priority to the direct support operations covered by the Regulation.

The Commission submitted (June 14th, 1984) for discussion in the Consultative Committee a proposal for a systematic approach for cross-exchange of information and concertation of activities.

Discussions (in subsequent meetings) on this subject concluded that although the Regulation had envisaged the setting up of a formal mechanism for information exchange between Member States and the Commission, there had been difficulties in reaching agreement on the form it would take. In any case much of the relevant information was being obtained informally. It was therefore agreed that, since there were now other Community programmes such as ESPRIT under way covering a broader area of technology, the procedure would be tackled within the framework of these programmes.

Within ESPRIT this activity will be continued for a much longer period than within the Regulation 3744/81 the validity of which expired at the end of 1985.

2. Community Activities

The work carried out on microelectronics within the framework of the ESPRIT[5] programme represents both a continuation and an expansion of the activities undertaken pursuant to Regulation No. 3744/81 and constitutes an indispensable complement to the development of advanced microelectronics within the Community.

Some of the ESPRIT projects either are drawing on information from or are follow-ups of projects launched under the Regulation No. 3744/81. This applies not only to CAD projects but also to equipment projects and to the (equipment) users research programmes. Some examples are: on CAD the ESPRIT project 802 that it is building on the results of project MR-04-CVT and on equipment the ESPRIT project 271 that is expanding work undertaken by the "equipment users" of project MR-15-CAM. Further details were given in the individual project reports.

The Commission is following closely these cases in order to facilitate the flow of information between the different programmes and projects.

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5 Ref. O.J. L67 of 9.03.1984, p. 54
O.J. L81 of 24.03.1984

IV. DISSEMINATION OF THE RESULTS

In each of the individual project reports reference is made to the various forms of utilisation and dissemination of the results.

The common elements (policy) to the dissemination that were followed troughout this programme can be summarized as follows :

1. Specific measures

The dissemination of the results for the CAD projects which are granted support under the Council Regulation 3744/81 is insured within the framework of the CAVE (CAD for VLSI in Europe) workshops.
The attached annex 1 gives an overall view of the work which has been done during the 7 workshops that have been organized until now.

For the dissemination of the results of the CVT project (the largest CAD project supported through Regulation 3744/81) three workshops were organized in Torino (12 and 13 May 1984) in Darmstadt (17, 18 and 19 April 1985) and in Grenoble (22 and 23 April 1986) where attendees from all the Community countries were invited.

The nature of the equipment projects involving higher users-suppliers relationship is somehow different and, specific measures for the dissemination of the results have not been adopted on top of those envisaged through the general measures described below.

2.General measures

It has been provided in all contracts that, upon completion of the projects, the contractors will produce a separate (from the final) report suitable for publication. The Commission is considering the possibility to collate and make available to the Community these reports. Publication of papers in recognized technical journals and delivery of lectures (specifically in projects where there is university participation) are additional means envisaged for the dissemination of the results.

The contractors are obliged within one year from completion of the projects to exploit commercially the results either themselves or to make them available to third parties in the Community.

ANNEX 1

REPORT ON THE CAVE WORKSHOPS

(Computer Aided design for Very large scale integration in Europe)

Background

The special aim of the CAVE workshops, which are held twice yearly, is to be used as one of the vehicles for disseminating the results of CAD for VLSI projects supported under the Council Regulation 3744/81. Also, the workshops are used to foster personal relationships at a technical level in order to smooth the path of future collaboration in the Community in R and D in CAD for VLSI. This is rather different from many technical workshops. In order to be successful the CAVE workshops must atract a kernel of attendees who will attend regularly so that personal relationships can be built up. There is also a smaller percentage of different attendees at each workshop to ensure fresh input of ideas. Most of the CAD for VLSI topics are covered at each workshop. The location of the workshops is rotated amongst the Member States. A technical committee comprised of representatives from all Member States is assisting the Commission in the organisation of the workshops.

Statistical information on the participants of the workshops is given in the attached Table 1.

First Workshop

This was organised in l'Aquila, Italy, on 24-26 May 1983 and it covered 5 CAD topics:

- simulation and modelling
- CAD systems
- testing
- layout and
- design methodologies.

Second Workshop

This was organised in Villard-de-Lans, France, on 12-14 December 1983, and it covered 4 CAD topics:
- VLSI design workstations
- WLSI testing
- compact MOS modelling and
- autolayout

For the first time a panel session on "collaboration in CAD R&D" was also held.

Third Workshop

This was organised in Rungsted, Denmark, on 14-16 May 1984 and it covered 4 CAD topics:
- specification languages
- expert systems for VLSI CAD
- multi-level simulation and
- silicon compilation

Two panel sessions on "Portability and compatibility of CAD tools" and on "EEC funded projects in CAD" were also held.

Fourth Workshop

This was organised in Het Meerdal, The Netherlands, on 11-13 December 1984 and it covered 4 CAD topics:
- tools for testability
- Interfacing process, device and circuit simulation
- Design Management and Databases
- Floor-planning

One panel session on "Education and Training in CAD for VLSI".

Fifth Workshop

This was organised in Erperheide, Belgium, on 21-23 May 1985 and it covered 4 CAD topics:

- Parameterized and soft cells
- Use of artificial intelligence languages in CAD
- High-level design and synthesis
- self-test strategies

One panel session on "Silicon Brokerage Interfaces" was also held.

Sixth Workshop

This was organised in Chester, UK, from 9 to 11 December 1985 and it had 4 half-day sessions on the following topics :

- Mixed Mode Simulation
- Automatic Place and Route
- Distributed CAD
- Automatic Test Pattern Generation.

There were also two panel sessions on the following topics :

- National Programmes in CAD for VLSI
- Special-Purpose CAD Hardware.

Seventh Workshop

This was organised in Patras, Greece, from 21 to 23 May 1986 and it had 4 half-day sessions on the following topics :

- Trends in CAD for VLSI
- Process Optimisation
- Benchmarking CAD Tools
- Use of Expert Systems in CAD for VLSI.

There was also a panel session on "User's Experience of Semi-Custom CAD Systems".

Comments

- In each workshop about 60% of the presentations are on work carried-out within projects funded through the Council Regulation 3744/81.

- The workshops have proved to be very successful until now. Many requests for participation are received. In May 1986 at Patras Spanish and Portuguese experts attended for the first time. The nominal size of the workshop (excluding local attendees) has been increased from 50 to 57 in recognition of the addition of two new member states.

- In the light of the above it is the Commission's intention to ensure the continuation of the workshops till after completion of all the CAD projects funded through the Council Regulation 3744/81.

TABLE 1

CAVE WORKSHOPS/PARTICIPANTS

Countries	1st Workshop May 1983		2nd Workshop Dec.1983		3rd Workshop May 1984		4th Workshop Dec.1984		5th Workshop May 1985	
	University	Industry + Research	University	Industry + Research	University	Industry + Research	University	Industry + Research	University	Industry + Research
Belgium	1	4	3	2	2	5	1	6	4	7
Denmark	1	1	-	2	-	2	1	1	1	1
France	2	5	3	15	2	5	2	5	6	2
Germany	5	4	5	3	5	4	5	3	6	2
Greece	2	-	2	-	2	-	2	-	1	-
Ireland	2	-	4	-	4	-	4	-	3	-
Italy	3	6	3	4	2	4	1	5	3	5
Luxembourg	-	-	-	-	-	-	-	-	-	-
Netherlands	1	3	2	4	4	3	6	5	2	1
United Kingdom	2	6	1	5	2	9	2	9	-	8
TOTAL	19	29	23	35	23	32	24	34	26	26

TABLE 1A

CAVE WORKSHOPS/PARTICIPANTS

	6th Workshop Dec. 85		7th Workshop May 86	
Countries	University	Industry + Research	University	Industry + Research
Belgium	0	3	0	4
Denmark	1	2	1	1
France	3	7	2	7
Germany	3	5	2	6
Greece	2	0	7	0
Ireland	3	0	4	0
Italy	1	7	2	7
Luxembourg	0	0	0	0
Netherlands	1	2	3	4
Portugal	0	0	1	0
Spain	0	0	1	0
United Kingdom	3	17	2	6
TOTAL	17	43	25	35

ANNEX 2

EXPLOITATION OF THE RESULTS OF PROJECTS SUPPORTED UNDER THE MICROELECTRONICS COUNCIL REGULATION (EEC) N° 3744/81

The Community through this programme does not support the commercialization phase of the results achieved in the projects. However, the project participants, in addition to their obligations for dissemination, have undertaken (in their contracts with the Commission) to exploit the results. If, within one year from completion of the project, steps towards exploitation are not taken, the contractors are obliged to make available (on normal commercial terms) the results of the project to other Community organizations who would like to exploit these results.
The exhibits included in this annex are a collection of material (in summary form) made available to the Commission by the project participants in order to verify their activities towards exploitation of the results.

LIST OF EXHIBITS

	Project Reference
Exhibit 1	MR-03-KUL
2	MR-04-CVT
3	MR-05-SIE
4	MR-09-DFT
5	MR-12-ELT
6	MR-14-EKC