

Article

An All-Electric-Aircraft Tailored SiC-Based Power Factor Correction Converter with Adaptive DC-Link Regulator

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Abstract: In recent years the aerospace industry has made a growing effort to develop a quieter and more environmentally friendly aircraft. In particular, several research activities have been focused on innovative solutions aimed at the design/optimization of an on-board electric system fully compatible with this new approach. A first important step in the evolution towards an All Electric Aircraft (AEA) is the replacement of the hydraulic actuators with fully electric ones. The transition process is not easy to carry out, since weight, size and reliability represent highly critical issues for aircraft applications. In this context, the significant improvements in semiconductor technologies can be exploited as a critical means to overcome the constraints mentioned. Indeed, this work proposes a Silicon Carbide (SiC) based Power Factor Correction (PFC) converter, whose design and control have been tailored in order to properly supply a wide range of on-board Electro-Mechanical Actuators (EMA). In particular, while the adopted circuit topology allows for power factor correction and bi-directional power flow, the SiC technology, thanks to the higher efficiency with respect to other semiconductor-based technologies, leads to a significant reduction in the overall system weight/volume. Furthermore, to meet the strict requirements in terms of dynamic and steady state performance imposed by the application, a novel adaptive regulator is conceived. A reduced-scale laboratory prototype of the SiC-based converter (3 kVA) is realized in order to verify the effectiveness of the proposed design and control approach.

Keywords: power factor correction (PFC); SiC (Silicon Carbide); aircraft applications; adaptive regulator; deadbeat control

1. Introduction

Nowadays, a relevant aviation trend is the *All Electric Aircraft* (AEA) concept; an aircraft with a centralized electric power system able to supply all aircraft loads and services. The main role of the electric power system is to convert the mechanical power of the shaft engine into electric one, which can then be employed, by means of on-board distribution and conversion systems, to satisfy various kinds of energy requests: heat/cold generation, mechanical actuation, lighting systems, and so on.

Aviation business has grown considerably in the last years, thus leading to a corresponding growth of the aircraft industry, which can assume a fundamental position in the near future thanks to constantly increasing air transportation demand. At the same time, a progressive electric hybridization of aircrafts has been observed. This evolution is driven by the inner properties of the electric energy, which is regarded as a privileged energetic vector [1–5], able to reduce global weight, operation/maintenance costs and environment polling, thanks to the associated high power density together with zero CO₂

emissions. As a consequence, advanced electric architectures are being developed with the aim of optimizing the on-board generation, distribution and storage systems with particular regard to performance, reliability and fault tolerance requirements. Indeed, a progressive electrification has interested most of the automotive sectors in the last years, pushing, above all, the development of high power/energy density storage solutions [6]. Nevertheless, a full AEA implementation would require, in most cases, performance levels of the electric storage systems which are not yet available. For this reason, at this stage, the primary objective is to eliminate both hydraulic and pneumatic systems with their associated equipment, thus improving the aircraft performance, especially with reference to medium-range routes [1]. In particular, this approach allows:

- reduction of fuel consumption by 8 to 10%
- reduction of takeoff weight by 6 to 7%
- reduction of direct maintenance costs by 4 to 6%
- reduction of maintenance time by 4 to 5%
- reduction of life cycle cost by 4 to 5%

For example, the implementation of some AEA elements on A-380, Boeing-787, and so on, has improved operational and economic performance of these aircraft, leading to a fuel consumption reduction in the 17 to 20% range.

Given the reliability, power density and fault-tolerance requirements, a specific development of the key components of the on board electric power system on which an AEA would be based has to be carried out in order to satisfy the constraints imposed. Indeed, this work is focused on a critical component of the power distribution system; the AC/DC converter connected to the main three-phase grid, operating at 200 V/400 Hz (which are electric parameters typical of the aircraft applications). This converter serves a double purpose:

- to feed the primary DC voltage for subsequent DC/DC conversion;
- to feed directly the actuation systems operating at high voltage.

The AC/DC conversion is usually carried out by using a two stage AC/DC and DC/DC converter usually implemented by a cascaded connection of a three-phase diode rectifier and chopper converter. Alternatively, it is possible to employ a single stage AC/DC converter called a Power Factor Correction (PFC) converter. This architecture can be obtained by different circuit topologies and by using silicon (Si) or silicon-carbide (SiC) based components. One stage AC/DC conversion can be achieved by using different topologies [7]:

- Third harmonic current injection rectifier
- Delta switch rectifier
- Vienna rectifier
- Swiss rectifier
- Six switches Current Source Rectifier (CSR)
- Six Switches Voltage Source Rectifier (VSR)

Each topology has its own advantages/disadvantages with respect to number of components, efficiency, control complexity, modularity, power quality indexes. In particular, for aircraft application, where the fault tolerance and efficiency attributes are the most critical ones, the more appropriate topology appears to be the Voltage Source Rectifier (VSR) [8,9]. Indeed, the VSR architecture allows the control of the input AC currents with minimum circuit complexity; moreover, its basic configuration can be easily re-arranged in interleaved structures, thus ensuring higher fault-tolerance capabilities.

This paper proposes a PFC SiC-based VSR converter in its standard configuration. The SiC solution guarantees [10,11]:

- **high efficiency operation:** the SiC components exhibit substantial efficiency improvement over the conventional Si based ones;

- **Electro-Magnetic Interference (EMI) input filter size reduction:** the SiC adoption allows to operate at very high switching frequency thus simplifying the design of the input passive filter;
- **weight and size reduction:** SiC devices ability to operate at higher temperature allows to minimize the cooling system size with a subsequent significant bulk reduction.

The SiC hardware solution has been paired with a proper software control solution in order to satisfy the strict performance requirements of the application considered. In particular, a novel DC-Link adaptive regulator has been conceived with the aim to improve both transient and steady state operations. The first part of this work deals with the mathematical model and the control algorithm of the PFC converter. A sizing procedure is then presented for the design/realization of a scaled prototype (3 kVA). Finally, both simulations and experimental tests are shown. The obtained results validate the effectiveness of the proposed PFC solution.

2. Mathematical Model

The proposed topology of Power Factor Correction converter is shown in Figure 1.

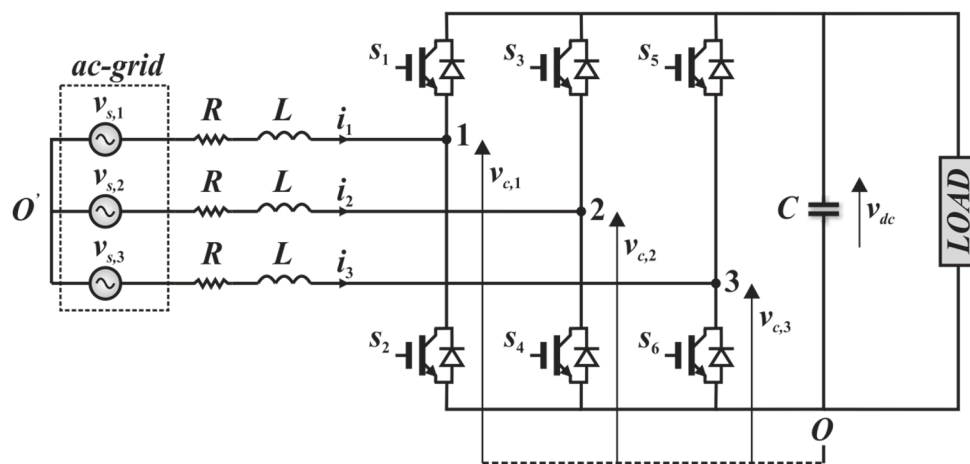


Figure 1. Proposed Power Factor Correction (PFC) converter.

This architecture falls in the VSR converter category. For each leg it employs two SiC devices, pulsed in complementary logic. The neatness of this configuration leads to a concise mathematical model:

$$\mathbf{v}_s = R \mathbf{i}_s + L \frac{d \mathbf{i}_s}{dt} + \mathbf{v}_c \tag{1}$$

with $\mathbf{v}_s, \mathbf{i}_s, \mathbf{v}_c$ the space vectors of the phase grid voltages, of the line currents, of the converter voltages. \mathbf{v}_s can be expressed as:

$$\mathbf{v}_s = \mathbf{v}_{s,p}^1 + \tilde{\mathbf{v}}_s = \mathbf{V}_{s,p}^1 e^{j\omega t} + \tilde{\mathbf{v}}_s \tag{2}$$

where $\mathbf{v}_{s,p}^1 = \mathbf{V}_{s,p}^1 e^{j\omega t}$ is the space vector of the fundamental positive sequence, while $\tilde{\mathbf{v}}_s$ is the space vector of the residual harmonic sequences. Equation (1) can be conveniently referred to a rotating frame synchronous with $\mathbf{v}_{s,p}^1$:

$$\begin{cases} V_{s,p}^1 + \tilde{v}_{sd} = R i_{sd} + L \frac{di_{sd}}{dt} - \omega L i_{sq} + v_{cd} \\ \tilde{v}_{sq} = R i_{sq} + L \frac{di_{sq}}{dt} + \omega L i_{sd} + v_{cq} \end{cases} \tag{3}$$

It should be noted that, by the choice of the reference frame, if the currents components i_{sd}, i_{sq} are constant, then the line currents are sinusoidal and symmetrical, thus absorbing average power only from the phase voltages fundamental positive sequence. The converter voltages v_{cd}, v_{cq} , which are the control variables in Equation (3), will be computed by the proposed control strategy.

3. Control Strategy

The control strategy has the aim to keep constant the DC-Link voltage v_{dc} , while absorbing from the grid a set of sinusoidal and symmetrical currents with unitary power factor. The overall control diagram is depicted in Figure 2. The input variables (left side of Figure 2) are the phase to phase voltages, the line currents and DC-Link voltage; the output variable (right side of Figure 2) is the reference space vector converter voltage, which is in turn the input of a space vector modulator block. The proposed algorithm is based on cascaded control: the outer loop regulates v_{dc} , while the inner loop regulates the AC currents.

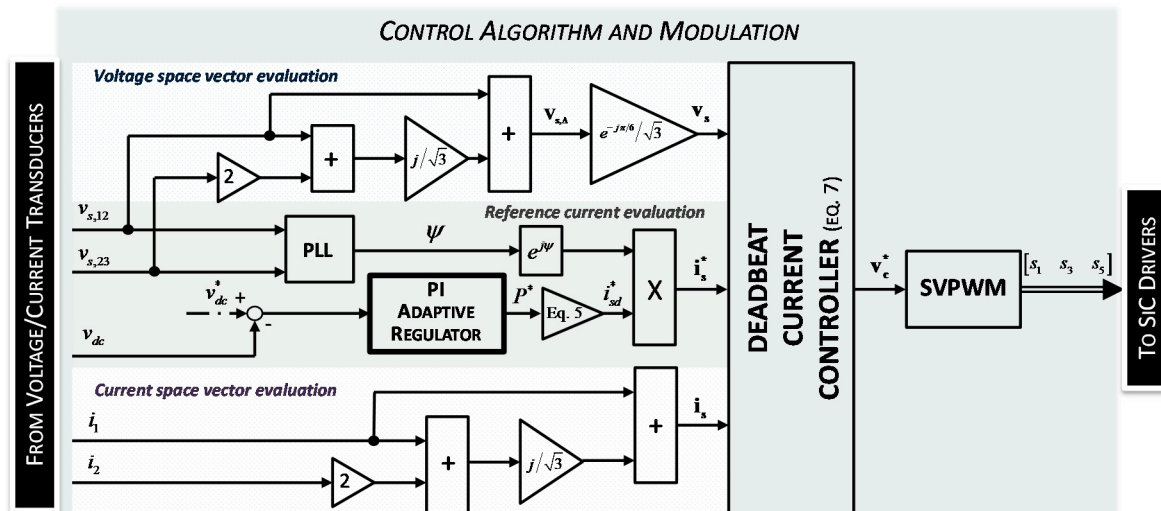


Figure 2. Control diagram.

The outer loop is built around a special proportional-integral (PI) adaptive regulator (check Section 3.1), whose output is the reference grid power P^* , which in turn gives the reference d axis current i_{sd}^* . Indeed, the DC-Link voltage can be controlled by means of the active power absorbed by the grid:

$$P = \frac{3}{2} V_{s,p}^1 i_{sd} \tag{4}$$

Equation (4) can be exploited to compute the reference current i_{sd}^* able to control the DC-Link voltage:

$$i_{sd}^* = \frac{2}{3} \frac{P^*}{V_{s,p}^1} \tag{5}$$

The reference current i_{sq}^* is instead set to zero with the aim to minimizing the line currents RMS value by achieving a unitary power factor. Since the currents tracking is performed in the fixed frame, the references i_{sd}^* , i_{sq}^* are then reported by the transformation:

$$\mathbf{i}_s^* = \left(i_{sd}^* + j i_{sq}^* \right) e^{j\psi} = i_{sd}^* e^{j\psi} \tag{6}$$

with \mathbf{i}_s^* the reference of the line currents space vector in the fixed frame and ψ the instantaneous phase angle of $\mathbf{v}_{s,p}^1$. The phase angle ψ is provided by a dq Phase Locked Loop (PLL) [12] which operates on the phase to phase grid voltages.

The reference \mathbf{i}_s^* drives the control inner loop, which is built around a minimum delay deadbeat controller [13], which imposes the tracking of the AC reference space vector current \mathbf{i}_s^* with a delay equal to two sampling intervals:

$$\mathbf{v}_c^*(t_k) = \frac{L}{T_s}(\mathbf{i}_s(t_k) - \mathbf{i}_s^*(t_k)) + \frac{\mathbf{v}_s(t_{k-1}) + 2\mathbf{v}_s(t_k) + \mathbf{v}_s(t_{k+1})}{2} - \mathbf{v}_c^*(t_{k-1}) \quad (7)$$

with L the boost inductance, T_s the sampling time interval and t_k the generic sampling time instant.

3.1. The Adaptive PI Regulator

The inner control loop should be able to guarantee reasonable overshoot/undershoot values of v_{dc} in transient condition, while being at the same time highly insensitive to DC-Link voltage ripples linked to load and/or electric grid intrinsic irregularities, such as dissymmetry in the source voltages or low frequencies components in the load power. These requirements are fully met by the proposed novel adaptive PI regulator.

The DC-Link power equation can be written as:

$$\frac{1}{2}C \frac{d}{dt} v_{dc}^2 = \frac{3}{2} \text{Re}\{\mathbf{v}_s \hat{\mathbf{i}}_s\} - \frac{3}{4}L \frac{d}{dt} i_s^2 - p_L \quad (8)$$

where p_L is the instantaneous power absorbed by the load. The sizing procedure of the proposed PI regulator can be easily conceived once the Equation (8) is properly simplified. In particular, by neglecting the boost inductors instantaneous power, typically a very small ratio of the rated power, and furtherly by considering that the grid power is dependent almost only on the interaction between \mathbf{i}_s and $V_{s,p}$, Equation (8) becomes:

$$\frac{1}{2}C \frac{d}{dt} v_{dc}^2 = P - p_L \quad (9)$$

Finally, by imposing $v_{dc} = v_{dc}^* + \Delta v_{dc}$, it can be easily verified that the Equation (9) can be linearized under the hypothesis $\Delta v_{dc} \ll v_{dc}^*$:

$$\frac{d}{dt} \Delta v_{dc} = \frac{P - p_L}{C v_{dc}^*} \quad (10)$$

This equation can be employed in order to size the PI regulator with respect to two different requirements: fast dynamic performance in transient conditions and strong disturbances rejection in steady state conditions. In particular, a satisfying system response, with respect to overshoot and settlement time dynamic properties, can be obtained by imposing that the real and imaginary components of the poles associated to the second order closed loop system are equal. It can be verified that the following relation applies:

$$k_i = \frac{1}{2} \left(\frac{k_p}{C v_{dc}^*} \right)^2 \quad (11)$$

with k_p , k_i the proportional, integral components of the PI regulator. Therefore, since k_i is linked to k_p as per Equation (11), the adaptive law is formulated once a criterion to adapt k_p is chosen. The proposed novel PI regulator employs two different values for k_p : the transient value k_p^{high} and the steady state value k_p^{low} . k_p^{high} , k_p^{low} are sized by using the following conditions:

$$k_p^{high} = \frac{r_p^{high} P_R}{\varepsilon_v^{high} v_{dc}^*}, \quad k_p^{low} = \frac{r_p^{low} P_R}{\varepsilon_v^{low} v_{dc}^*} \quad (12)$$

Equation (12) ensures that the PI regulator proportional component output is $r_p P_R$ (i.e., a ratio r_p of the rated power P_R) when the input error is $\varepsilon_v v_{dc}^*$ (i.e., a ratio ε_v of the reference DC-Link

voltage v_{dc}^*). The proposed values for r_p and ε_v , relative to transient and steady state conditions, are shown in Table 1.

Table 1. Values of r_p and ε_v for transient and steady state conditions.

Transient Condition		Steady State Condition	
$r_p^{high} = 1.00$	k_p^{high}, k_i^{high} $\varepsilon_v^{high} = 0.050$	$r_p^{low} = 0.05$	k_p^{low}, k_i^{low} $\varepsilon_v^{low} = 0.025$

The chosen values of $r_p^{low}, \varepsilon_v^{low}$ guarantees that the PI regulator, driven by the *steady state components* k_p^{low}, k_i^{low} , is able to keep the instantaneous voltage error Δv_{dc} under ε_v^{low} in correspondence of slow perturbations, while being highly insensitive to grid/load disturbances. On the other hand, the chosen values of the transient components $r_p^{high}, \varepsilon_v^{high}$ confer a fast dynamic performance to the PI regulator, which, driven by the components k_p^{high}, k_i^{high} , is able to keep the error Δv_{dc} around ε_v^{high} in presence of strong perturbations. The effective PI regulator components are set by means of the following procedure:

1. when Δv_{dc} is greater than ε_v^{low} the PI regulator components are set to the transient components;
2. when Δv_{dc} is kept under ε_v^{low} for an assigned time interval T_a , hence defined the PI regulator adaptive time, the following adaptive law is used:

$$\begin{cases} k_p(t) = k_p^{high} - \frac{k_p^{high} - k_p^{low}}{T_a} \int dt \\ k_i(t) = \frac{1}{2} \left(\frac{k_p(t)}{C v_{dc}^*} \right)^2 \end{cases} \quad (13)$$

i.e., $k_p(t), k_i(t)$ varies linearly, quadratically between the correspondent boundaries. In order to ensure a soft transition and to avoid stability issues, it is just enough to ensure that T_a is much greater than the settlement time granted to the closed loop system by the PI regulator driven with the transient components.

The proposed adaptive PI regulator has been tested numerically by performing a simulation in *Matlab/Simulink*TM environment with reference to a system characterized by $P_R = 3 \text{ kW}$, $C = 75 \mu\text{F}$ and $v_{dc}^* = 360 \text{ V}$ (check next section); the PI regulator adaptive time T_a has been set to 0.5 s, i.e., around 25 times the system settlement time.

Starting from a steady state condition with no load, at 0.5 s a rated load step variation occurs. The load condition is characterized by an assigned disturbance, equivalent to a 10% dissymmetry in the grid voltages. The relative effect is characterized with a harmonic injection at 800 Hz (i.e., two times the grid frequency of the considered electric system, check Section 4) in the load power. Figure 3 shows the behavior of the reference active power ratio P^*/P_R , of the relative voltage error $\varepsilon_v = \Delta v_{dc}/v_{dc}^*$ and of the proportional component $k_p(t)$. It can be noted that, in correspondence of the load perturbation at 0.5 s, the PI components are set almost instantaneously to the transient values; indeed the maximum undershoot is kept around 6%; however in the subsequent steady state operation, the reference active power oscillates considerably ($\pm 15\%$), due to the relatively high bandwidth of the PI regulator in this condition. This undesirable oscillation is practically zeroed by the proposed adaptive action which starts at 1 s and terminates at 1.5 s: indeed the reference active power is practically constant in the remaining time interval.

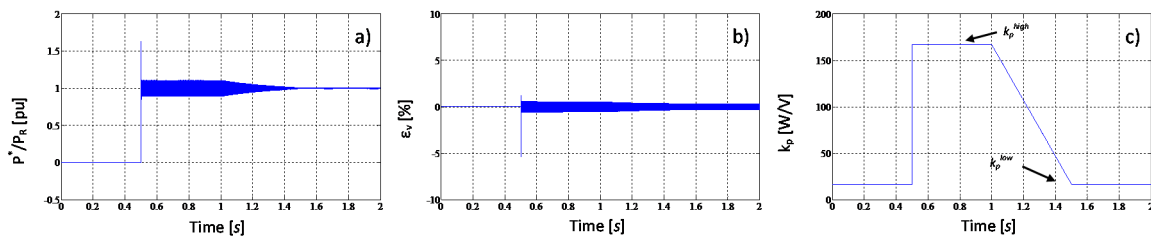


Figure 3. behavior of the reference power ratio (a), the relative voltage error (b) and the proportional component (c).

It can be concluded that the proposed adaptive PI regulator shows optimal performance both in steady state and transient condition with no need of a compensation action based on the DC load current measurement [14].

4. LC Filter Sizing Procedure

The proposed sizing procedure refers to a 3 kW PFC converter connected to a 200 V/400 Hz three-phase electric system with a rated DC-Link voltage of 360 V.

First, the optimal values of the boost inductance L and of the DC-Link capacitance C have to be determined. While L should be chosen in order to minimize the line currents Total Harmonic Distortion (THD), the capacitance C value should guarantee proper dynamic performance of the converter with respect to the DC-Link voltage undershoots/overshoots in transient conditions. A simple expression of the THD can be obtained if the converter output voltages are considered sinusoidal waveforms with superimposed rectangular alternative waveforms with amplitude $v_{dc}/6$ and frequency $1/T_s$. Under this hypothesis, it can be shown that the following relation is found:

$$\text{THD} = \left(\frac{1}{24\sqrt{3}} \frac{V_{dc,R} T_s}{L} \right) / I_{s,R} \quad (14)$$

with $V_{dc,R}$ the rated DC-Link voltage and $I_{s,R}$ the line currents rated value. The sizing of the DC-Link capacitor is carried with reference to a load step variation in which the power transferred to the load instantaneously changes from $-P_R$ to P_R , with P_R the PFC rated power. In this condition, the converter is able to drive the grid currents with a maximum power derivative $s_{P,max}$ given by

$$s_{P,max} = V_{s,R}^2 \left(\sqrt{\left(\frac{k_B}{L} \right)^2 - 2 \left(\frac{\omega_R I_{s,R}}{V_{s,R}} \right)^2} - \frac{1}{L} \right) \quad (15)$$

where $V_{s,R}$ is the grid rated voltage, k_B the converter boost factor and ω_R the rated angular frequency. Therefore, the DC-Link equation can be written as:

$$\frac{1}{2} C \frac{d}{dt} v_{dc}^2 = -P_R + s_{P,max} t \quad (16)$$

From (10) the v_{dc} time behavior is easily obtained:

$$v_{dc}(t) = \sqrt{V_{dc,R}^2 + \frac{1}{C} (s_{P,max} t^2 - 2P_R t)} \quad (17)$$

The minimum value of $v_{dc}(t)$, which quantifies the DC-Link undershoot with respect to the considered worst case condition, is reached at the undershoot time $t_{us} = P_R/s_{P,max}$ and is given by:

$$V_{dc,us} = \sqrt{V_{dc,R}^2 - \frac{P_R^2}{C s_{P,max}}} \quad (18)$$

By considering the undershoot much smaller than $V_{dc,R}$, the capacitance value C that complies with the desired relative DC-Link undershoot voltage $v_{dc,us}$ can be synthetically expressed as:

$$C \cong \left(\frac{P_R}{V_{dc,R}} \right)^2 \frac{1}{2s_{P,max}v_{dc,us}} \quad (19)$$

Since $s_{P,max}$ depends on the boost inductance L as per Equation (15), and L depends on the desired THD as per Equation (14), the functions $C = C(\text{THD})$ and $L = L(\text{THD})$ can be obtained. In particular, Figure 4 shows the C/L values that satisfy an imposed $v_{dc,us}$ set to 5% for different values of the desired THD in the range [1%, 5%].

As it can be noted from Figure 4a, the capacitance value rapidly decreases up to a THD value of about 2%. This consideration leads the optimal choice of the target THD, which has been set to 2.5%. The corresponding filter values are $C = 75 \mu\text{F}$ and $L = 2 \text{ mH}$, respectively.

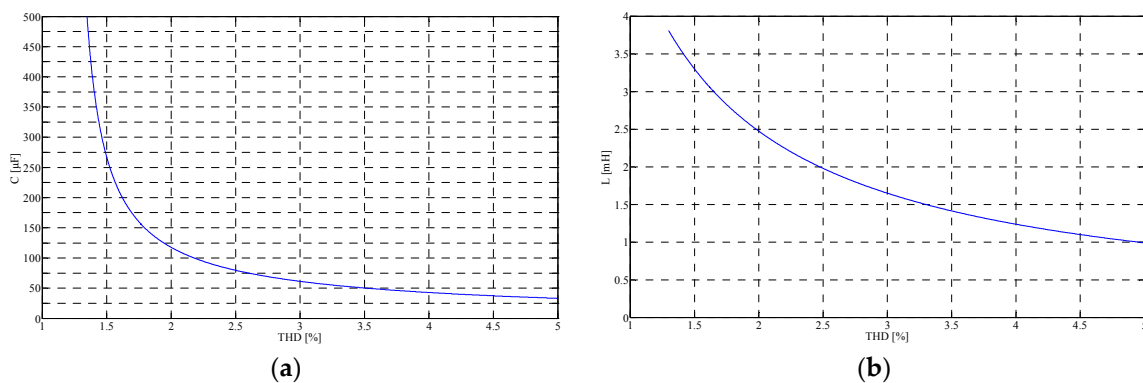


Figure 4. DC-Link capacitance C behavior (a) and boost inductance L behavior (b) versus the line currents Total Harmonic Distortion (THD) expressed in percent [%].

5. SiC Technology

The intrinsic characteristics of the SiC power devices can be exploited in order to significantly reduce the total weight/volume of the aircraft on board electric power system, thus satisfying critical issues that are typical of the aircraft applications. The SiC Wider Band Gap energy with respect to Si devices allows the SiC semiconductor to operate at higher junction temperature and to sustain a higher breakdown electric field. Therefore, at equal breakdown voltage, SiC devices are characterized by a thinner drift region and higher doping levels, consequently presenting a reduced specific conductive resistance and a lesser sensitivity to the operating temperature with regards to Si devices. The resulting reduced conduction losses, together with the possibility of operating at higher switching frequency, allows to improve the overall system efficiency. Since the power dissipation directly relates to the heat generation, the SiC performance allows to minimize the size of the power devices cooling system. Table 2 compares the main characteristics of the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) SiC based module CCS020M12CM2 by Cree with that of the IGBT Si based module FS25R12W1T4 by Infineon. From the reported data, the overall power dissipations (i.e., switching and conduction losses) of the considered modules at the aforementioned operating conditions are respectively 42 W and 138 W per component. By considering a maximum operating ambient temperature $T_a = 25 \text{ }^\circ\text{C}$ and by taking into account that the junction-case temperature

differences in the rated conditions are respectively 29.4 °C and 96.6 °C, the required minimum thermal resistances for the heatsinks are respectively 0.76 °C/W and 0.07 °C/W. This very high ratio ($\cong 10$) between the target heatsink thermal resistances leads to a substantial decrease of the size/weight of the cooling system ($>1/10$). The SiC choice appears therefore the optimal solution in the context of the aircraft applications.

Table 2. Main parameters of the simulated system.

Quantity	Cree CCS020M12CM2	Infineon FS25R12W1T4
Overall Switching Energy (mJ)	0.48	5.1
On-Resistance (m Ω)	80	90
Rated Current at $T_c = 100$ °C (A)	20	25
Rated Voltage (kV)	1.2	1.2
Junction-Case Thermal Resistance (°C/W)	0.75	0.7

6. Numerical Results

A preliminary numerical analysis has been conducted in order to validate both the control strategy and the sizing procedure. Several simulations have been performed in the *Matlab/Simulink*TM environment. In particular, the control algorithm has been developed directly in C-language code and implemented in the software by the integrated S-Function resources. This approach allowed the direct transfer of the control code on the Digital Signal Processor (DSP) hardware target device used during the experiments. The system's main parameters, together with the control quantities, are reported in Table 3.

Table 3. Main parameters of the simulated system.

Quantity	Symbol	Value
Grid rated voltage	$V_{s,R}$	200 V
Grid rated frequency	f_R	400 Hz
PFC rated power	P_R	3 kW
DC-Link rated voltage	$V_{dc,R}$	360 V
PFC rated current	$I_{s,R}$	9 A
DC-Link capacitance	C	75 μ F
Boost inductance	L	2 mH
Sampling time interval	T_s	50 μ s
Switching frequency	f_s	20 kHz

The whole simulation is performed over a time interval of 2 s. In order to evaluate the system performance under a worst-case scenario, unsymmetrical grid voltages have been considered by injecting a fundamental negative sequence with an amplitude set to 10% the rated one. In the first step, with no load, as soon as the PLL synchronizes, the DC-Link voltage is boosted to its rated value (360 V). At around 0.35 s a load step variation from zero to 3 kW occurs. Finally, at around 1 s, the load changes from 3 kW to zero. The boost action and the load perturbations are clearly highlighted by the grid power P behavior depicted in Figure 5a. From Figure 5b, it can be deduced that the voltage overshoot is lower than 50 V while the relative undershoot is contained under 10% ($\cong 40$ V). The unsymmetrical voltages cause a ripple at $2f_R$, which affects both P and v_{dc} . In any case, this disturbance is handled with good dynamic performance by the proposed adaptive DC-Link PI regulator. Indeed, the adaptation of the PI constants leads to a substantial decrease of the considered ripples, as can be noted at around 0.6 s, when the regulator adaptive action has been concluded.

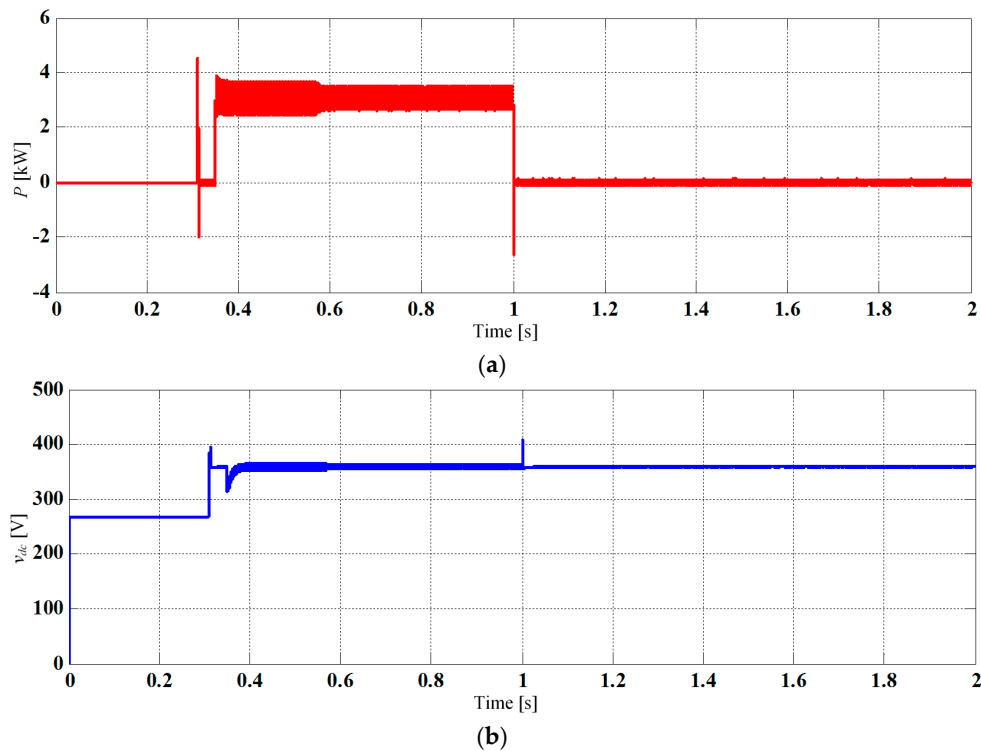


Figure 5. Behaviors of the absorbed power P (a) and of the DC-Link voltage v_{dc} (b) in the whole simulation interval.

The effectiveness of the DC-Link controller is confirmed in Figure 6, where the behavior of the grid voltages and of the line currents are detailed with reference to a steady state condition at the rated load. Indeed, even under a strong unsymmetrical supply, the line currents are practically sinusoidal and symmetrical, that is, the DC-Link voltage ripple generated by the grid voltages negative sequence is almost totally filtered out by the PI adaptive controller. The analysis carried out confirms that the proposed control is characterized by good dynamic performance at transient conditions and excellent disturbance rejection at steady state operations. Moreover, the THD evaluated is 2.25%, a value very close to the one imposed analytically (2.5%). Both the THD value obtained and the DC-Link voltage undershoot/overshoot therefore highlight the quality of the proposed sizing procedure.

Finally, Figure 7 shows the time behavior of dissipated power P_j (Figure 7a) and maximum junction temperature T_j (Figure 7b) related to the SiC modules. These results have been obtained by implementing a dynamic thermal mode of the electronic devices based on the components datasheet. It should be noted that the expected efficiency of the converter, in rated condition, is around 97.5%.

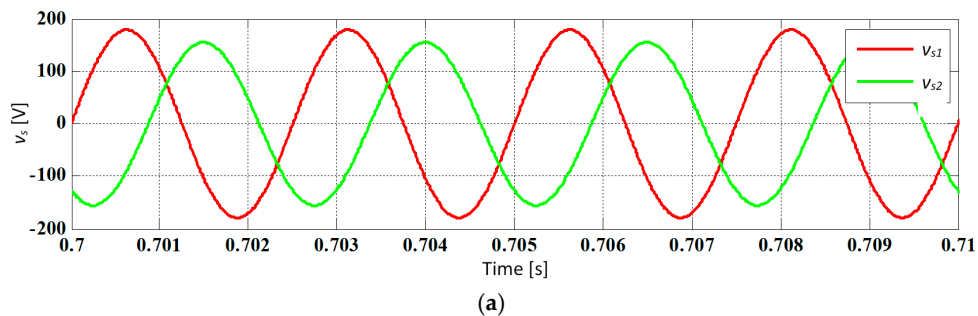


Figure 6. Cont.

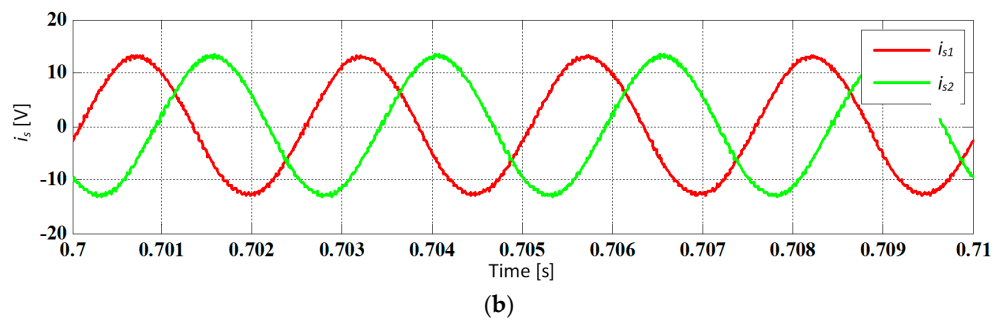


Figure 6. Grid voltages (a) and line currents (b) behaviors in steady state condition at the rated power.

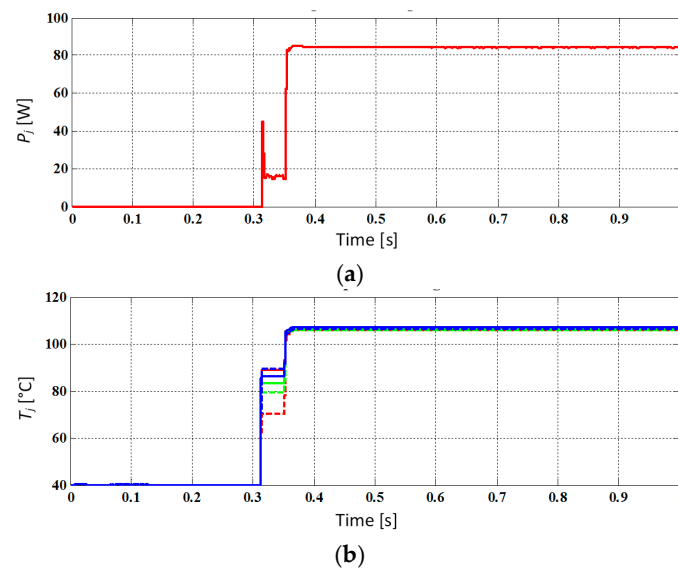


Figure 7. SiC dissipated power P_j (a) and relative junction temperature T_j (b) behaviors.

7. Experimental Results

The core of the technological innovation of the proposed conversion system is represented by the replacement of conventional Si based devices with SiC technology. In particular, the prototype has been built around the CCS020M12CM2 1.2 kV/20 A modules by CREE [15], driven by a CREE gate driver [16]. The control algorithm has been implemented on the Digital Signal Processor (DSP) Texas SM320F28335-EP [17]. All the components have been mounted on a custom PCB together with required voltages/currents transducers. Figure 8 shows the realized prototype.

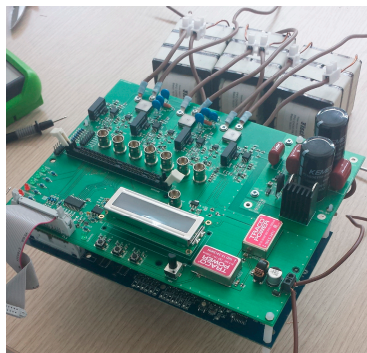


Figure 8. PFC prototype and boost inductors.

To prove the feasibility of the proposed control strategy, four different tests have been conducted:

- Test (a) Boost operation (Figure 9a);
- Test (b) 0 → 1.5 kW load step variation (Figure 9b);
- Test (c) 1.5 kW → 3 kW load step variation (Figure 9c);
- Test (d) 3 kW → 0 load step variation (Figure 9d).

In particular, it can be noted that the undershoots (that occur at around 0.2 s in Figure 9b,c) and the overshoot (that occurs at around 0.2 s in Figure 9d) of the DC-Link voltage are kept under 15%, thus confirming the results of the numerical analysis. The action of the adaptive PI controller also leads to similar results, with the DC-Link voltage ripple decreasing as the adaptive action is executed. Finally, Figure 10 shows the behavior of one line current in steady state condition with $P = 1.5$ kW (Figure 10a) and $P = 3$ kW (Figure 10b). The THD factors computed are 5% and 3% respectively, while the overall efficiency is 96.8% and 97.5% respectively. It can be pointed out that the numerical and experimental data are practically coincident with respect to the 3 kW load condition.

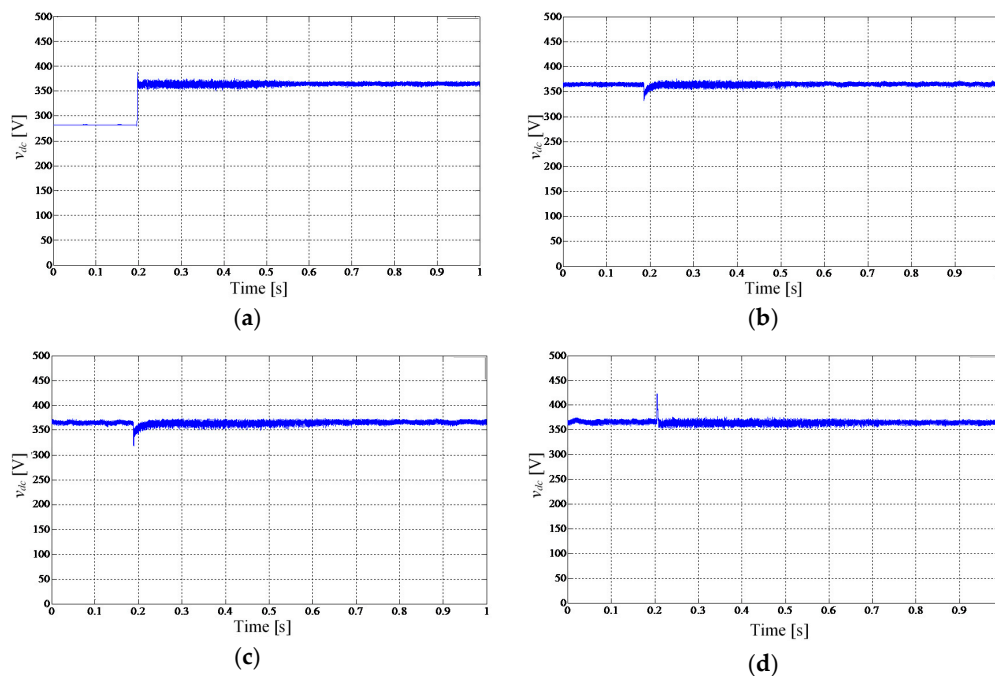
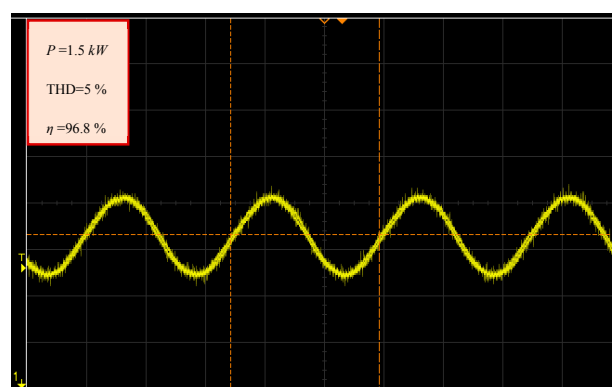


Figure 9. Behavior on the DC-Link voltage under different transient conditions: boost stage (a); 0 → 1.5 kW load step variation (b); 1.5 → 3 kW load step variation (c); 3 kW → 0 load step variation (d).



(a)

Figure 10. Cont.

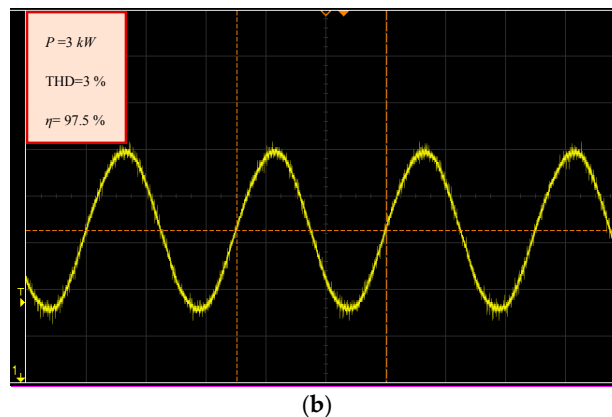


Figure 10. Line current behaviors in steady state condition: 1.5 kW (a) and 3 kW (b).

8. Conclusions

This work has been focused on the design and control of a SiC-based VSR converter.

The analytical model of the converter has been used to derive analytically the optimal values of the DC-Link capacitance C and boost inductance L with respect to both steady state conditions (low line currents THD) and transient operations (contained DC-Link voltage overshoot/undershoot).

The VSR control strategy has been coupled with a novel adaptive DC-Link PI controller, conceived with the aim of achieving sinusoidal and symmetrical line currents even under strong load/grid disturbances, while keeping the DC-Link voltage close the reference one even under strong load perturbations.

A set of simulations has been performed in order to validate the approach presented. The numerical results confirm the effectiveness of the sizing procedure and highlight the good performance of the proposed adaptive PI regulator.

Furthermore, an experimental campaign has been conducted on a 3 kW SiC-based PFC converter prototype. The experimental results have confirmed the simulated ones obtained under Matlab/Simulink™ environment, showing the capability of the system to take all relevant parameters under control: power factor, line currents THD and DC-Link voltage.

High level efficiency operations have been achieved in spite of the considerable target switching frequency as a result of the SiC technology employed. Indeed, it is worth noting that the total weight of the SiC-based prototype realized (boost inductors excluded) is around 1.1 kg, of which 0.6 kg are related to the heatsink. It should be pointed out that a comparable Si-based converter would require a much larger heatsink, resulting in a total weight exceeding 3 kg.

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List of Symbols

C/L	DC-Link capacitance/Boost inductance
$I_{s,R}/P_R/V_{dc,R}/V_{s,R}$	Line currents/Output power/DC-Link voltage/Grid voltages rated values
P	Mean active power absorbed by the grid
P_R	Converter rated power
p_L	Instantaneous power absorbed by the load
k_p, k_i	Proportional, integral components of the adaptive PI regulator
r_p	Rated power ratio

ε_v	Relative DC-Link voltage error
f_s/T_s	Switching frequency/Sampling time interval
k_b	Converter boost factor
$i_k/v_{c,k}/v_{s,k}$	Line current/Converter voltage/Phase voltage of the k^{th} phase
\mathbf{i}_s	Line currents space vector
i_{sd}, i_{sq}	Line currents space vector components in the synchronous frame
$s_{P,\max}$	Maximum power time derivative in the worst case condition
$v_{dc,us}$	Relative DC-Link voltage undershoot
$\mathbf{v}_c/\mathbf{v}_s$	Converter/Phase voltages space vector
$\tilde{\mathbf{v}}_s/\mathbf{v}_{s,p}^1$	Residual harmonics/Fundamental positive sequence of the phase voltages space vector
$v_{cd}, v_{cq}/v_{sd}, v_{sq}$	Converter/Phase voltages space vector components in the synchronous frame
ψ/ω	Instantaneous phase angle/Angular frequency of the fundamental positive sequence of \mathbf{v}_s

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