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Published in:
ACS Applied Materials & Interfaces

DOI:
10.1021/acsami.6b14934

Publication date:
2017

ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

Broadening of Distribution of Trap States in PbS Quantum Dot Field-Effect Transistors with High-*k* Dielectrics

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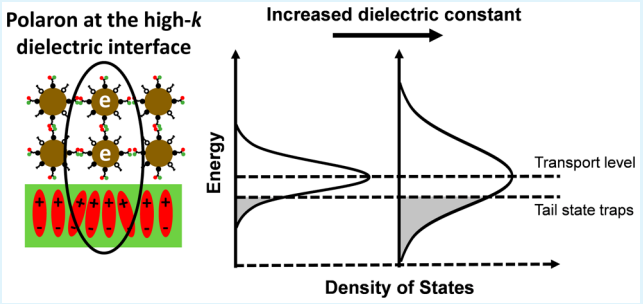
Supporting Information

ABSTRACT: We perform a quantitative analysis of the trap density of states (trap DOS) in PbS quantum dot field-effect transistors (QD-FETs), which utilize several polymer gate insulators with a wide range of dielectric constants. With increasing gate dielectric constant, we observe increasing trap DOS close to the lowest unoccupied molecular orbital (LUMO) of the QDs. In addition, this increase is also consistently followed by broadening of the trap DOS. We rationalize that the increase and broadening of the spectral trap distribution originate from dipolar disorder as well as polaronic interactions, which are appearing at strong dielectric polarization. Interestingly, the increased polaron-induced traps do not show any negative effect on the charge carrier mobility in our QD devices at the highest applied gate voltage, giving the possibility to fabricate efficient low-voltage QD devices without suppressing carrier transport.



KEYWORDS: *field-effect transistors, high-k, PbS quantum dots, polaron, trap states*

INTRODUCTION

Lead sulfide quantum dots (PbS QDs) have been demonstrated in recent years to be interesting semiconducting building blocks for the fabrication of solution-processable field-effect transistors (FETs) and other optoelectronic devices.[1−8] PbS QDs are dispersed in solution, as they are capped with long-alkyl chain ligands, which provide good solubility in most organic solvents.[9−11] Because of this solution processability, fabrication of QD-FETs is compatible with low-cost deposition technology such as blade-coating, dip-coating, roll-to-roll and inkjet printing.[1,3,12−14] As they are interfacial devices, in FETs the nature of the semiconductor/insulator interface is crucial: it influences the performance as well as the properties of the fabricated devices.[2,10,13−17] When SiO_2 is used as dielectric, dangling bonds due to hydroxyl (OH) groups on the dielectric surfaces act as carrier traps, which limit the performance of devices.[2,13,16,18−22] Moreover, SiO_2 gating in FET devices suffers from very high operating voltage due to its low capacitance, which is not compatible with practical applications.

Reducing the operating voltage of FETs is a necessary step to use them for a broader range of applications. A lower operating voltage can be achieved with the use of gate insulators with high dielectric constant (high-*k*).[13,23−27] In organic semiconductor FETs, however, energetic disorder and polaron relaxation are enhanced at the semiconductor/insulator interface when high-*k* insulators ($k > 3$) are utilized.[28−30] This disorder and polaronic-related interaction may modify the electronic structure, such as the nature of trap states, at the semiconductor/insulator interface and are responsible for the reduced charge carrier mobility in some reported high-*k* gated organic FETs.[28,31] While localized (trap) states with the use of high-*k* dielectrics have been intensively studied in organic FETs, little information is available for FETs based on PbS QDs. Since the trap states can strongly determine the performance of QD-FET devices, and at the same time dielectrics with higher *k* are

Received: November 21, 2016
Accepted: January 13, 2017
Published: January 13, 2017

DOI: 10.1021/acsami.6b14934
ACS Appl. Mater. Interfaces 2017, 9, 4719−4724

important in particular for low operating voltage, understanding the nature of trap states in PbS QD-FETs with increased gate dielectric constant is crucial.

In this paper, we perform an analysis of the trap density of states (trap DOS) in PbS QD-FETs employing several polymer gate dielectrics. These solution-deposited polymer gate insulators display dielectric constants ranging from 2 to 41. Using these insulators, we first find that the number of deep traps extracted from the subthreshold swing of our FETs increases with increasing dielectric constant of the insulators. To understand this behavior, we quantify the distribution of the trap DOS versus energy in the devices by simulating the device working mechanism. In agreement with the subthreshold swing result, we observe the increase and broadening of the trap DOS with increasing dielectric constant of the insulators. These results are rationalized in terms of increased disorder due to polaronic interaction at the semiconductor/insulator interface in PbS QD-FETs with increased dielectric polarization strength.

EXPERIMENTAL SECTION

Deposition of PbS semiconducting thin films was performed by spin-coating 10 mg/mL oleic acid-capped PbS solution in chloroform on SiO_2/Si substrates. To improve the film conductivity, we exchanged the long oleic acid ligands with shorter molecules, such as 1,2-ethanedithiol (EDT). The concentration of the EDT solution was 1% (v/v) with acetonitrile as a solvent. Deposition of PbS thin films, as well as ligand exchange, was performed via a layer-by-layer (LbL) spin-coating procedure. After each ligand exchange, pure acetonitrile was dropped on the films to remove unbound EDT and native oleic acid ligands. PbS layer deposition and ligand exchange were repeated 5 times until the desired thickness was reached. After deposition, the devices were annealed at 120 °C for 20 min to remove residual solvent and to promote coupling between QDs, thus improving conductivity without sintering the QDs. As gate dielectrics, we used four different polymer insulators: Cytop, poly(methyl methacrylate) (PMMA), poly(vinylidene difluoride)−hexafluoropropylene (PVDF-HFP), and poly(vinylidene difluoride)−trifluoroethylene−chlorofluoroethylene (PVDF-trFE-CFE). In this study, pure Cytop (CT-809M) was used without further dilution. PMMA was dissolved in ethyl acetate at a concentration of 80 mg/mL. To prepare PVDF-HFP solutions, we dissolved the polymer in dimethylformamide (80 mg/mL). The last dielectric, PVDF-trFE-CFE, was dissolved in cyclohexanone to form a solution with concentration of 60 mg/mL. All these polymers were used to vary the dielectric constant of gate insulators in the devices in the range between 2 and 41. Deposition of the polymer insulators was done by spin-coating on the previously deposited active layer of PbS QDs. The devices were then annealed at 95 °C for 1 h to remove the residual solvent. Finally, a thin layer of aluminum (50 nm) was evaporated as top gate electrode. All device fabrication was performed in an N_2-filled glovebox.

RESULTS AND DISCUSSION

The bottom-contact top-gate structure of the fabricated devices is shown in Figure 1a. When the gate voltage is applied on the devices, charge carriers are accumulated in the semiconductor at the interface with the insulator. The microscopic nature of this interface has great influence on the accumulated charge carriers as well as on their transport. Sirringhaus and co-workers[29,30] reported that dipolar disorder at the dielectric interface leads to the broadening of interface density of states (DOS) in polymer field-effect transistors. This dipolar disorder originates from Fröhlich polarons, which are caused by interaction of the charges with induced dipole moments and polarization of the dielectric, as shown in Figure 1b. With increasing dielectric constant of the gate insulator, strong

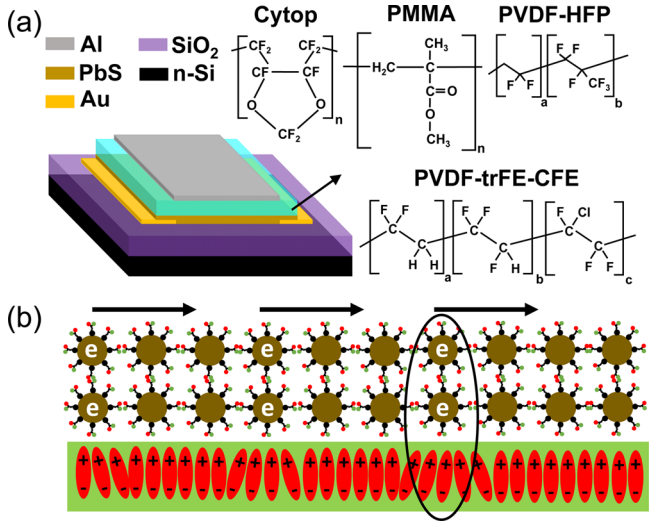


Figure 1. (a) Configuration of FET devices with given chemical structures of polymer dielectrics and (b) formation of polaron (black oval) due to the interaction between moving electrons and accumulated charge carriers at the semiconductor/insulator interface.

polaronic interaction can be responsible for the increased disorder and carrier activation energy in FETs.[29,30] In agreement with this, Morpurgo and co-workers[28] found that polaron binding energy increases with increasing dielectric constant of gate insulators. These polaronic interaction and the increased disorder also explain the origin of the reduced charge carrier mobility in some reported high-k gated organic semiconductor FETs.[28,31]

To understand the trap DOS in PbS QD-FETs with increasing gate dielectric constant, we utilize a series of polymeric insulators with dielectric constant ranging from 2 up to 41. The polymers used are free of hydroxyl groups, as shown in Figure 1a, which allows us to exclude the effect of interface traps due to dangling bonds on the dielectric surfaces. The interface traps given by these chemical groups have been known to influence the properties of the devices, which may affect the analysis of the results.[2] Following to this reason, we did not perform analysis on the charge accumulation using bottom SiO_2 gating. Furthermore, the bottom surface of the PbS films might have different properties than the top surface, which may influence our analysis.

As a first step, we characterized the polymer films, including film thickness (d) and capacitance (C), as shown in Table 1. Film thickness was characterized by use of a Dektak profilometer, whereas capacitance was measured by electrical impedance spectroscopy (EIS). To measure the film

Table 1. Polymer Insulator Characteristics and Electron Mobility in the Respective Devices

polymer	thickness (nm)	capacitance (nF·cm^{-2})	dielectric constant	mobility (cm^2·V^{-1}·s^{-1}) at similar n	mobility (cm^2·V^{-1}·s^{-1}) at max V_G
Cytop	650	2.7	2	0.12	0.12
PMMA	468	6.5	2.6	0.11	0.11
PVDF-HFP	308	26	10.5	0.09	0.14
PVDF-trFE-CFE	257	126	40.5	0.05	0.15

DOI: 10.1021/acsami.6b14934
ACS Appl. Mater. Interfaces 2017, 9, 4719−4724

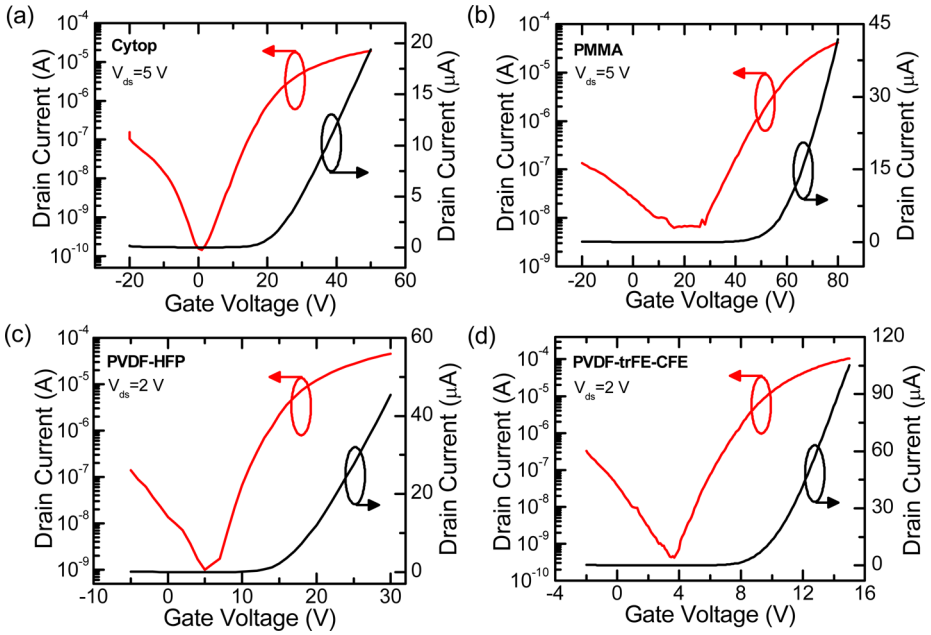


Figure 2. I_D-V_G transfer characteristics of devices with (a) Cytop, (b) PMMA, (c) PVDF-HFP, and (d) PVDF-trFE-CFE polymer gate dielectrics.

capacitance, we used a metal−insulator−metal (MIM) structure by sandwiching the polymer films with indium tin oxide (ITO)-coated glass substrates and thermally evaporated thin aluminum layer. The dielectric constant (k) of the polymer films was extracted by use of a standard parallel plate capacitor model. In Table 1, the terpolymer (PVDF-trFE-CFE) shows the highest dielectric constant with capacitance as high as 0.126 μF/cm^2, which allows us to induce high carrier density in the devices.

The I_D-V_G transfer characteristics of devices with different polymer insulators are shown in Figure 2. The devices show good current modulation in n-channel operation with on/off ratio of 10^4-10^5. In p-channel operation, a small hole current is observed. However, because of the weak hole current, we limit our analysis to n-channel operation. In addition, the devices also show some hysteresis in transfer characteristics. The full transfer characteristics in linear and semilogarithmic scales are presented in Supporting Information (Figures S1 and S2). From the measurements, the devices employing high-k insulators show smaller hysteresis than those with low-k insulators (Cytop and PMMA).

With the use of high-k polymer insulators, we obviously reduce the operation voltage of the devices. The operation voltage can be further suppressed by optimizing the film thickness of the high-k insulators. Electron linear mobility (μ) in the devices is extracted from eq 1:

$$\mu = \frac{L}{WC_iV_{ds}}\frac{\partial I_{ds}}{\partial V_g} \tag{1}$$

where V_{ds}, W, and L are source-drain voltage, channel width, and channel length. The channel length and width of the devices are 20 μm and 1 cm, respectively. By use of eq 1, we estimate the average electron linear mobility as high as 0.12 cm^2·V^{-1}·s^{-1} with Cytop at high gate voltage, as given in Table 1. Calculated mobility data in the devices with given standard deviation values are presented in Supporting Information (Table S1). With this low-k insulator, we are only able to accumulate carrier concentration up to 4.7×10^{11} cm^{-2}. By use of the high-k insulator PVDF-trFE-CFE, the carrier concentration can be improved by 1 order of magnitude (4.6×10^{12} cm^{-2}) at relatively low gate voltage (15 V). In PbS QDs, carrier traps mainly come from dangling bonds on the QD surfaces, which have a strong influence on carrier transport. In contrast to the case of organic semiconductor FETs, the increase of carrier density in PbS QD-FETs is expected to have great impact on charge carrier mobility, particularly due to filling of the surface traps.[12,32] However, we did not observe any significant change in charge carrier mobility with this increased carrier density (Table 1). With PVDF-trFE-CFE insulator, the average mobility is estimated to be 0.15 cm^2·V^{-1}·s^{-1} at maximum applied gate voltage, which is only a few percent higher than that measured with Cytop. Furthermore, we even observe a reduction in the mobility with the high-k dielectrics when we compare the mobility values at similar carrier density (4.2×10^{11} cm^{-2}). At this point, different phenomena are occurring when high-k dielectrics are used. The increase of interface disorder, which suppresses carrier transport, may be evoked. To further investigate this effect, we first estimate the number of traps (N_{traps}) in the devices by use of the subthreshold swing formula:

$$S = \frac{k_BT\ln 10}{e}\left(1 + \frac{e^2N_{traps}}{C_i}\right) \tag{2}$$

$$N_{traps} = \left(S\frac{e}{k_BT\ln 10} - 1\right)\frac{C_i}{e^2} \tag{3}$$

where e is elementary charge, k_b is the Boltzmann constant, and T is temperature. The capacitance of insulator (C_i) is shown in Table 1.

From our measurements (Figure 2), it is obvious that the subthreshold swing decreases with increasing gate dielectric constant, as expected from eq 2. However, if we analyze the subthreshold swing in more detail, we find that the actual values do not decrease as fast as we would expect when we consider the effect only of the dielectric, meaning that an additional

DOI: 10.1021/acsami.6b14934
ACS Appl. Mater. Interfaces 2017, 9, 4719−4724

effect comes into play at higher dielectric permittivity. The only unknown parameter in eq 2 is the number of trap states, which might increase due to an increase in dielectric permittivity. Figure 3 presents the number of electron traps (N_{traps})

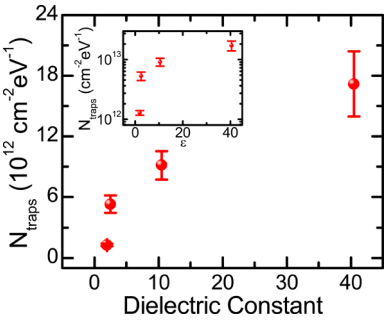


Figure 3. Number of electron traps in devices as a function of dielectric constant extracted from subthreshold regime. (Inset) Number of traps in semilogarithmic scale.

extracted from subthreshold regime by use of eq 3. It is obvious that the number of electron traps in the devices increases with increasing dielectric constant of the gate insulator. In the devices with Cytop gating, the number of electron traps is as low as 1.28×10^{12} $cm^{-2}\cdot eV^{-1}$, which is comparable to our previous report.[2] At increased gate dielectric constant, with the use of PVDF-trFE-CFE terpolymer, we observe a significant increase in number of electron traps by 1 order of magnitude (1.82×10^{13} $cm^{-2}\cdot eV^{-1}$). This increase in carrier traps can explain the reduction in mobility when we compare it at similar carrier density. In addition, this result also can be responsible for the mobility characteristics at maximum applied gate voltage with high-k dielectrics. Furthermore, the increase of carrier traps and the mobility characteristics in our devices with high-k dielectrics are an indication of the existence of polaronic-related interaction at the semiconductor/insulator interface, as observed in organic semiconductor FETs.[28−30]

To further understand the nature of the trap DOS in our devices with increasing gate dielectric constants, we perform a computer simulation on the I_D-V_G transfer characteristics of the fabricated devices. The simulation is performed by solving the drift-diffusion and Poisson equation for I_D-V_G transfer characteristics of the devices following a numerical model developed by Oberhoff et al.[33] This simulator is based on general principles and can be applied to study a wide range of semiconducting materials.[33−36] Using this simulation, we are able to analyze the distribution of density of charge carrier traps (localized states) close to highest occupied molecular orbital (HOMO)/lowest unoccupied molecular orbital (LUMO) levels in our FET devices.[2,34] Although eq 3 can estimate the number of carrier traps in the devices, it can quantify them at a certain energy level in the subthreshold regime only, whereas with the simulation we can study the number of traps in a broad energy range. With the help of this simulation, we could successfully prove the origin of a significant improvement in charge carrier mobility in our previously reported PbS QD-FETs with hydroxyl-free dielectric gating.[2] Figure 4a shows the analyzed density of trap states close to the LUMO level in our devices, fabricated with different polymer gate dielectrics. In agreement with the result in Figure 3, we observe an increase in carrier traps over a wide energy range close to the LUMO energy (electron traps) with increasing dielectric constant of the gate insulator. With this simulation, we are able to analyze the density of trap states up to 0.4 eV below the transport level (LUMO) of the charge carriers. As our devices show slight ambipolar characteristics, we have limited our analysis to this energy level to minimize the error due to minority charge carriers (holes), which may exist close to the off-state of the devices. In addition to the increase in trap DOS, we also observe the broadening of trap DOS with increasing gate dielectric constant as displayed in Figure 4a. The broadening of trap DOS with high-k dielectrics is shown schematically in Figure 4b. The origin of the increase and of the broadening is most likely a consequence of polaronic interaction at the semiconductor/dielectric interface, which modifies the already-present disorder. This analysis is supported by the fact that the polaron relaxation has great impact on the density of states in polymer semiconductor FETs employing gate insulator with dielectric constant (k) > 3, as confirmed by charge-modulation spectroscopy (CMS).[29,30] With these results, we can confirm that the polaronic interaction at the semiconductor/insulator interface also has an important effect on the behavior of PbS QD-FETs.

Finally, as we refer to the extracted mobility and the analyzed trap DOS, the increase of charge trapping is expected to greatly suppress carrier transport, and thus charge carrier mobility, in the devices. In line with this, the mobility decreases with increasing dielectric constant of the gate insulators when we compare the mobility values at similar carrier density as displayed in Table 1. Meanwhile, at respective maximum applied gate voltages with different dielectrics, the mobility slightly increases with increasing gate dielectric constant (see Table 1). In contrast to our results, the mobility in organic semiconductor FETs monotonically decreases with increasing

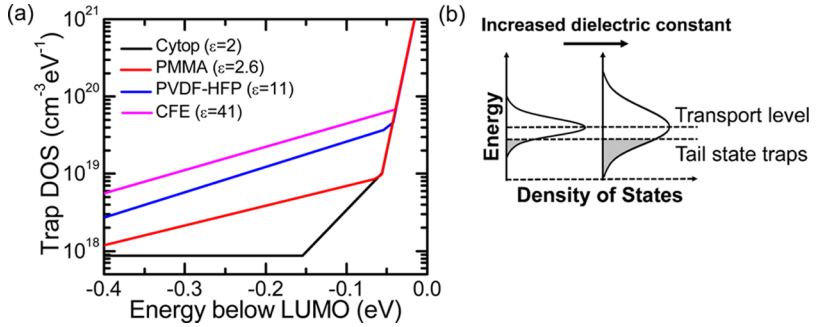


Figure 4. (a) Distribution of trap density of states (DOS) close to LUMO in devices with different dielectric constant of gate insulators. (b) Schematic of broadening of tail trap states with increased gate dielectric constant, where the transport level corresponds to the LUMO of the QDs.

DOI: 10.1021/acsami.6b14934
ACS Appl. Mater. Interfaces 2017, 9, 4719−4724

dielectric constant of the gate insulators over the entire range of applied gate voltages.[28] To understand these results, we propose that an interplay between charge trapping and trap-filling process might take place in our devices. As we increase the dielectric constant of the gate insulators, the increased carrier density is expected to fill the traps in the devices. Meanwhile, because the polaron-induced traps are increased at the same time, many gate-induced charge carriers are used to fill the trap states. Therefore, the effective free carriers with high-*k* dielectrics will be only slightly higher than in the devices with Cytop, leading to a small improvement of the charge carrier mobility. Another possible explanation for the less affected charge carrier mobility than in organic transistors at high gate voltage is the large separation between the polaron and the accumulated charge carriers in PbS QDs. In PbS QD-FETs, the top surface of the dielectrics is separated by cross-linking EDT ligands, which have length about 0.4 nm, while the radius of QDs is around 1.8 nm. As the accumulation of charge carriers in PbS QDs is assumed to be in the center mass of the QDs, therefore, the total separation distance between polaron and the accumulated charge carriers is around 2.2 nm. Moreover, some residual oleic acid ligands on the bottom side of QDs may also exist, which can increase the separation distance. This larger polaron separation distance than in the case of polymer semiconductors (~0.3 nm) may minimize the effect of polarons on charge carrier mobility in our devices.[29,30] However, despite the large polaron separation distance, the trap states are still greatly influenced by the polaronic interaction. Nevertheless, charge carrier mobility over the entire range of applied gate voltages is expected to be greatly affected by polaronic interaction at low temperature, which will be the focus of our future work.

CONCLUSION

In conclusion, we have performed a study on the trap DOS in PbS QD-FETs, employing several high-*k* polymer gate insulators. With increasing gate dielectric constant, we observe an increase in electron traps in the devices as extracted from the subthreshold regime. By using a computer simulation, we further analyze the detailed distribution of trap DOS in the devices close to the LUMO level of PbS QDs. We found a general broadening of trap DOS, which is attributed to increased disorder due to polaronic-related interactions at the semiconductor/dielectric interface. While the increased trap states effectively influence the mobility, compared at similar carrier density, the extracted mobility at maximum applied gate voltages is not significantly affected by the polaronic interaction, which is likely due to the interplay between trap filling and increased charge trapping as well as the large separation distance between polarons and free carriers in PbS QDs. Our results clearly show that, by careful choice of dielectrics, PbS QD FETs with low operating voltage can be built without reducing the charge carrier mobility, which is a fundamental insight into further utilizing colloidal QD systems in optoelectronic applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.6b14934.

Two figures showing hysteresis profiles of transfer characteristics in linear and semilogarithmic scales; one table listing statistical data on electron mobility and trap density (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was partly supported by the European Research Council Starting Grant (306983) Hybrid solution processable materials for optoelectronic devices (ERC-HySPOD). W.H. and M.S. gratefully acknowledge the use of the services and facilities of the Energie Campus Nürnberg and financial support through the Aufbruch Bayern initiative of the State of Bavaria. We thank Y. Yamashita and S. Z. Bisri for discussions. Finally, we acknowledge A. F. Kamp and R. Gooijaarts for technical support.

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DOI: 10.1021/acsami.6b14934
ACS Appl. Mater. Interfaces 2017, 9, 4719−4724