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Controlling of the surface energy of the gate dielectric in organic field-effect transistors by polymer blend

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In this letter, we demonstrate that by blending insulating polymers, one can fabricate an insulating layer with controllable surface energy for organic field-effect transistors. As a model system, we used copper phthalocyanine evaporated on layers of polymethyl metacrylate blended with polystyrene with different blending ratios and measured the field-effect mobility in transistors. We show that the highest field-effect mobility is achieved for identical surface energies of the dielectric and the semiconductor. This simple technique demonstrates the viability of using the blends of insulating polymers to systematically control the surface energy of the gate dielectric toward achieving better performances. © 2009 American Institute of Physics. [DOI: 10.1063/1.3086894]

In organic field-effect transistors (OFETs), the gate dielectric has a prominent role on the morphology, charge trapping, and the mobility of the organic semiconductor.[1–4] Many efforts have been focused on modifying the dielectric/semiconductor interface in order to decrease the gate leakage current,[5] to modify the surface energy of the gate dielectric[6,7] to promote the morphology of the semiconductor,[8] and to reduce the charge trapping at the gate hence improving the field-effect mobility. Although polymeric dielectrics are the first choice for the gate layer if OFETs are to go flexible, the focal point of the research has been mostly on silicon oxide gate dielectric and modifications to it by self-assembled monolayers.[9,10] Very recent reports have shown that blends of insulating polymers with small cross linking organic molecule are highly desirable for gate dielectrics.[11] However, controlling the surface energy of the polymeric gate dielectric in order to control the morphology of the semiconductor deposited on to it is still challenging.

In this letter, we present an approach based on blending the insulating polymers to tune the surface energy of the gate dielectric to such an extent that its surface energy becomes identical to the surface energy of the semiconductor. Polymer blends proved to be highly beneficial in the context of organic electronics, where beneficial properties of separate materials are combined in a single composite.[12–16]

Here we take the following strategy to tune the surface energy; we chose two insulating polymers such that surface energy of one is greater than the surface energy of the targeted semiconductor, while the surface energy of the other is lower than that of the semiconductor. Casting a film from the blend of these two polymers provides a layer with a surface energy that is between the limits given by the components of the blend. We used copper phthalocyanine (CuPc) as the semiconductor. As the gate dielectric we chose polymethyl metacrylate (PMMA) with a surface energy that exceeds that of CuPc, and polystyrene (PS) with a surface energy that is lower than that of CuPc. We found that upon blending

PMMA and PS with different blending ratios, the surface energy of the polymeric gate dielectric can be nicely tuned between the two limits provided by pure PMMA and PS layers. The highest field-effect mobility was achieved when the surface energy of the polymer blend gate dielectric was identical to the surface energy of CuPc, which we attribute to the preferred growth of CuPc on such surface. Studying the charge transport mechanism in more detail revealed that in OFETs with polymer blend, gate dielectric activation energy is lowered, which we explained in the framework of multiple trapping and release (MTR) model.

Devices were fabricated according to the following procedure. As substrate, we used heavily *n*-doped Si wafer (the gate electrode) with a thermally grown oxide layer of 420 nm. The wafers were ultrasonically cleaned with acetone, isopropyl alcohol, and de-ionized water, respectively. Solutions of PMMA, PS, and the blend with different blending ratios, with a concentration of 3 mg/ml were prepared and spin coated onto the substrate at 1500 rpm. The films were then dried at 50 °C for 2 h. Despite the low field-effect mobility, we chose CuPc for our experiments due to its high thermal and chemical stability and, most importantly, it is a cheap candidate for experimental purposes. Thermal deposition of 30 nm of CuPc was carried out at base pressure of $(2–4)\times10^{-6}$ Torr at a rate of 0.04–0.06 nm/s, while the substrate was kept at room temperature. Subsequently to make the source/drain electrodes, gold was evaporated at the rate of 0.02–0.03 nm/s via shadow masks. All the devices had a defined channel width of 2–3 mm and a channel length of 120 μm. Electrical characteristics of the transistors were measured in helium atmosphere with Hewlett–Packard (HP) 4145B semiconductor parameter analyzer. The capacitances of the dielectric layers were measured with Agilent 4284A at 1 kHz. Several devices were measured in order to test the stability and reproducibility of the transistors and to reach a statistical average for the mobility. We derived the surface energy of the different layers by measuring the contact angle of distilled water and ethylene glycol on the layer. Finally the morphology of semiconductor thin film was probed by

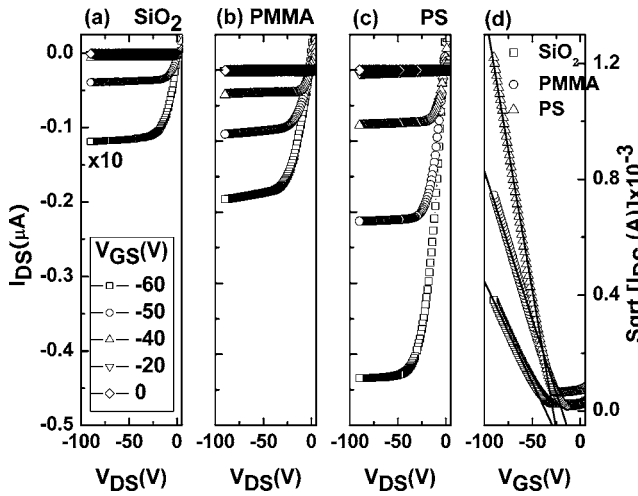a)Authors to whom correspondence should be addressed. Electronic addresses: j.gao@rug.nl and jbxu@ee.cuhk.edu.hk.

FIG. 1. Output and transfer characteristics of CuPc transistors on different gate dielectrics: (a) on bare SiO$_2$ magnified by a factor of 10, (b) on PMMA, and (c) on PS. (d) Transfer curve of all the devices in saturation regime with the linear fit to the square root of the current, the slope intercept of which is used to derive the mobility and threshold voltage, respectively.
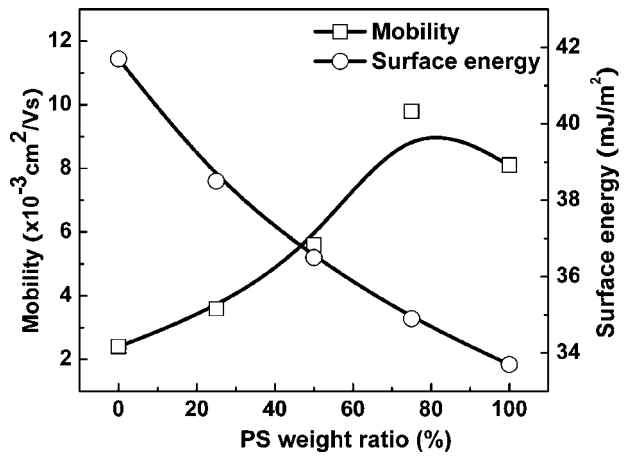

FIG. 2. Relationship between the blending ratio of PMMA:PS and the field-effect mobility of the devices in relation to the surface energy of the dielectric layer. The highest mobility is reached when the surface energy of CuPc and dielectric are similar (the B-spline line is drawn to guide the eye).

atomic force microscopy (Digital Instrument Multimode) in tapping mode.

As the first step we deposited CuPc on bare SiO$_2$. The output characteristics of the transistor, Fig. 1, showed a deteriorated performance with a low mobility of $(6-8) \times 10^{-4}$ cm^2 V^{-1} s^{-1}, comparable to the previous reports.[17] The appearance of the high threshold voltage of -40 V is a signature of high trap densities at the SiO$_2$ and CuPc interface[18,19] that hinders the performance of the device. In the next step, a layer of PMMA and PS was spin coated onto the SiO$_2$. Interestingly, the magnitudes of source-drain current, as shown in Figs. 1(b) and 1(c), in these devices were larger than those of the SiO$_2$ despite the fact that the capacitance of the dielectric is lowered by inserting an extra insulating layer, which was in the range of $6.2-6.5$ nF cm^{-2}. For the SiO$_2$/PMMA gate insulator, the increase in mobility is threefold, reaching 2.4×10^{-3} cm^2 V^{-1} s^{-1}, and the threshold voltage was reduced to -20 V, whereas for the SiO$_2$/PS, the mobility was increased even further to 8.3×10^{-3} cm^2 V^{-1} s^{-1}. We note however that roughness of the dielectric/semiconductor plays a crucial rule on the mobility of the charge carriers.[20] The roughness of the spin-coated polymer film in our case is apparently higher than that of the SiO$_2$ (roughness less than 1 nm) and the mobility achieved here for SiO$_2$/polymer layer is yet to be optimized by smoothing the polymer layer, which will result in even higher mobility.[21] Nevertheless, this is not our intention in this letter.

Small molecules grow differently on different surfaces due to variation in surface energies.[22–26] For better understanding of the mechanism of the enhanced mobility, we derived the surface energies using the contact angle measurement.[27] First the surface energy of 35.1×10^{-3} J m^{-2} was measured for CuPc. PMMA has a surface energy of 41.7×10^{-3} mJ m^{-2} exceeding that of CuPc, while that of PS amounts to 33.7×10^{-3} mJ m^{-2}, in accordance to the reported values.[28,29] In combination with the field-effect mobility of the CuPc, a trend was observed. The closer the surface energy of the dielectric layer to the surface energy of CuPc, the higher is the mobility.

In the next step, we blended PMMA and PS in a common solvent and spin casted a film wherein the composition of the layer is systematically varied from 100% PMMA to 100% PS. As the amount of PS in the matrix of PMMA increases, the surface energy of the blend layer (Fig. 2) showed a declining trend from that of the pure PMMA layer to pure PS. In a special case of PMMA:PS with 1:3 blending ratio, the surface energy was measured to be identical to the surface energy of CuPc. Subsequently we evaporated CuPc onto the layers with different blending ratios. The corresponding mobility (Fig. 2) showed an steady raise as the amount of PS is increased in the composite film up to 1:3 PMMA:PS blending ratio where indeed the highest mobility of 1×10^{-2} cm^2 V^{-1} s^{-1} was achieved.

Investigation of the morphology of the CuPc film prepared on different gate dielectrics showed a trend between the grain size and the surface energy of the dielectrics onto which CuPc was deposited. The closer the surface energy of CuPc to the surface energy of the dielectrics, the larger is the grain size. That is, less grain boundaries that is favored for better charge transport. The same trend has also been observed by Chou *et al.*[30]

In all devices with different gate dielectrics, the mean value of the mobility showed an Arrhenius behavior, which is the signature of a thermally activated charge transport. The activation energy is derived from the exponential fit to the experimental results in Fig. 3. Lower activation energy for the case of the 1:3 PMMA:PS blend can be explained in the frame work of multiple trapping and release model for charge transport in molecular materials.[31] Larger grains lead to less grain boundaries, which are known to act as charge trapping centers. Smaller grain boundaries therefore result in less trapping of the charge carriers and consequently higher field-effect mobility.

In conclusion, we demonstrated the viability of the blending technique of two insulating polymers in order to achieve a gate dielectric with a surface energy that can be systematically controlled by simply controlling the blending ratio of two polymers. We tuned the surface energy of the blend gate insulator to match with that of the organic semiconductor. In the case of CuPc and PMMA:PS, the performance of the OFETs showed strong dependence on the sur-
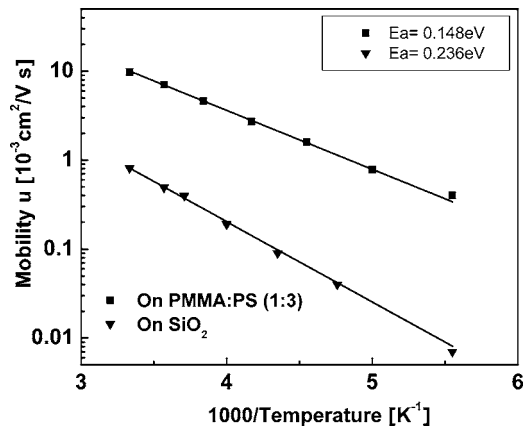
FIG. 3. Temperature dependence of the mobility on different dielectrics. The scatter dots are the average device mobility and the solid lines are the fitting results (Ref. 31). The activation energy of CuPc on different dielectrics is shown in the inset.

face energy of the blended gate dielectric. Applying a gate dielectrics with a surface energy that matches that of the CuPc, i.e., the blend layer of PMMA:PS with a 1:3 blending ratio, resulted the best FET performance among all devices measured. The enhanced performance is due to better morphology and favored growth of CuPc on this layer. The performance of the OFETs however remains to be optimized for the roughness of the blend dielectrics.

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