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We demonstrate thin-film ferroelectric transistors, made entirely from organic materials that are processed from solution. The devices consist of thin ferroelectric poly(vinylidene fluoride/trifluoroethylene) films sandwiched between electrodes made of conducting poly(3,4-ethylenedioxythiophene) stabilized with polystyrene-4-sulphonic acid. On top of this stack, an organic semiconductor is applied. The ferroelectric transistors, constructed using unipolar *p*- or *n*-type semiconductor channels, have remnant current modulations of $\sim 10^3$ with a retention time of hours. They can be switched in 0.1–1 ms at operating voltages less than 10 V. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2035324]

Thin film transistors based on solution-processed organic semiconductors are currently proposed for use in simple circuitry such as flexible displays[1,2] and identification tags.[3] The latter application requires nonvolatile data storage, preferably with memory elements that can be programmed, erased, and read electrically. Ferroelectric field-effect transistors (FeFETs) are attractive for this purpose due to fast nondestructive data readout and low-power consumption.[4] The simplest layout of a FeFET comprises a metal–ferroelectric–semiconductor layer stack (Fig. 1), in which the ferroelectric layer serves as the gate dielectric. The ferroelectric layer, because of its remnant polarization, can adopt either of two stable polarization states, which persist when no biases are applied. Switching from one polarization state to the other can occur by applying a sufficiently large gate bias. Depending on the orientation of the polarization, positive or negative charges are induced in the semiconductor at the semiconductor/ferroelectric interface, i.e., in the semiconductor channel. The induced surface charge density shifts the onset of channel accumulation towards either more negative or positive gate biases. Hence, a gate bias window, defined by the shifted onset voltages, exists wherein the drain current may have either of two levels depending on the actual polarization state of the ferroelectric gate dielectric. The corresponding drain current levels can be used to define Boolean "0" and "1" states of a nonvolatile memory with nondestructive readout.[4] This is illustrated schematically in Fig. 1.

Several groups have demonstrated memory effects in organic-based field-effect transistors using ferroelectrics, ferroelectric-like materials and electrets as gate dielectric.[5–10] We recently showed high-performance memory transistors with on–off ratio's as high as 10^4 using a random copolymer of vinylidenedifluoride and trifluoroethylene, P(VDF/TrFE), as ferroelectric gate dielectric,[11] in combination with a poly(*p*-phenylenevinylene) (PPV) semiconductor.[19] The high on–off ratio was attributed to the high remnant surface charge density, of 18 mC/m^2 induced in the semiconductor channel by poling the ferroelectric. In that work, as well as the other studies, metallic electrodes were used (and in some cases also the gate dielectric was inorganic). For cost reasons it is desirable to deposit all layers from solution by for instance spincoating or inkjet printing. Here, we demonstrate a 150 mm wafer scale technology to make all-polymer ferroelectric capacitors and transistors. The maximum processing temperature of 140 °C ensures compatibility with flexible plastic substrates.

Devices are prepared on 150 mm size silicon support wafers with a 1500 nm thick layer of SiO_2. First, a conducting layer of poly(ethylenedioxythiophene)–polystyrene–4–sulphonic acid (Baytron *P*, Bayer Corp.), PEDOT-PSS, was spincoated and patterned to form the gate electrode according to a literature procedure.[12] Then, a film of P(VDF/TrFE) with 80 mol % VDF (Solvay and Cie, Belgium) was spincoated from a 2-butanone solution with a thickness of either 150 or 550 nm. The second PEDOT-PSS layer was applied and patterned to give source and drain electrodes. After processing, the PEDOT-PSS sheet resistances are 1–2 kΩ/square. The wafers were heated to 140 °C for 1–2 h to increase P(VDF/TrFE) film crystallinity[11] after which the semiconductors, consisting of either poly(2-methoxy-5-(3′,7′–dimethyloctyloxy)–phenylenevinylene) (OC_1OC_{10}–PPV) or [6,6]–phenyl-C_{61}-butyricacidmethylester (PCBM), was applied from chlorobenzene solution.[13]

The ferroelectric properties of P(VDF/TrFE) sandwiched between PEDOT-PSS electrodes, are characterized by displacement *vs* electric field ($D-E$) hysteresis loops. The measurements were recorded in ambient atmosphere using a Sawyer–Tower setup and sinusoidal field scanning at 1 Hz. The saturated loops are symmetric and square with remnant polarizations of $|84|$ mC/m^2. The coercive voltages (V_c), i.e., where $D=0$, for 150 nm and 550 nm thick P(VDF/TrFE) films are found at $|8|$ and $|29|$ V, respectively. The coercive field (E_c) of ~ 53 MV/m is consistent with literature data[11,14] and indicates that abrupt well-defined interfaces are formed between the solution-deposited P(VDF/TrFE) and PEDOT-PSS layers.

Transistor characteristics were measured in N_2 and dark at room temperature using a HP4156B semiconductor parameter analyzer at a scan speed of 1 V/s. The transfer (I_D-V_G) characteristics of FeFETs with a 550 nm thick P(VDF/TrFE) layer, recorded at a drain bias of −5 V, are shown in Fig. 2.[15] We made unipolar *p*-type and *n*-type FeFETs using OC_1OC_{10}–PPV or PCBM as a semiconductor,

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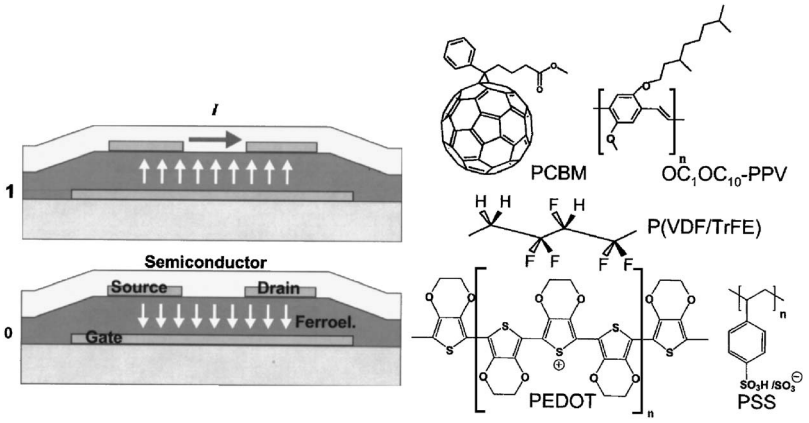

FIG. 1. Schematic representation of the all-polymer ferroelectric transistor and the chemical structures of the materials used. The arrows indicate the two remnant states of polarization in the ferroelectric layer. Readout of the polarization state occurs nondestructively by detection of the current level, I, between source and drain electrodes.

respectively. Both FeFETs show a drain current hysteresis that can be explained by the ferroelectric gate dielectric polarization. Polarization reversal occurs at gate biases comparable to the values of the coercive voltage.

Figure 3(a) shows the transfer characteristics of a OC_1OC_{10}–PPV FeFET with different channel lengths, recorded at a drain bias of −2 V. The device has a 150 nm thick P(VDF/TrFE) layer. The driving voltages are significantly reduced compared to the devices with the thicker 550 nm P(VDF/TrFE) layer; polarization reversal occurs already below 10 V. Switching voltages were found to be somewhat lower for small-channel devices. For transistors with channel lengths ranging from 20 to 2 μm, the on–off ratio was consistently higher than 10^3, with a maximum of 5×10^3 [Fig. 3(b)]. These values are superior to the remnant current modulations of 10–100 reported by other groups,[5–7] and close to the highest value of 10^4 reported.[10,19]

When the polarization switches from one state to another, charge is displaced across the ferroelectric insulator. The accompanying switching currents are observed as sharp features in the drain current [Figs. 2 and 3(a)] as well as gate current [see inset Fig. 3(a)]. Their presence confirms that the memory effect is driven by ferroelectric polarization, and that it is not due to injection of charges or ion migration.[10,16] Furthermore, so-called inner loops, I_D-V_G scans to V_G smaller than the switching values (not shown), are symmetrically positioned on the V_G axis within the outer loops. This demonstrates that the hysteresis results from switching between two approximately equal opposite polarization states that differ from the net zero polarization present in the pristine devices; when switching the device the semiconductor surface charge density within the channel changes from $-P_R$ to $+P_R$, or vice versa.

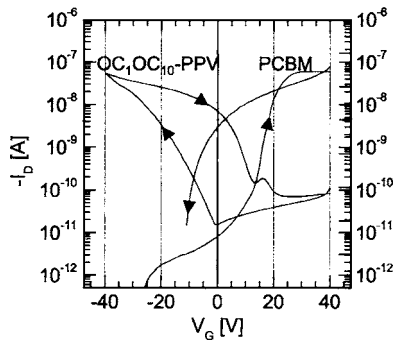

FIG. 2. Transfer (I_D-V_G) curves of all-polymer ferroelectric transistors with a 550 nm thick P(VDF/TrFE) gate dielectric layer and either OC_1C_{10}–PPV or PCBM semiconductor, respectively. The arrows indicate the directions of the hysteresis between the forward and backward scans recorded at drain biases of −5 V. The transistors have a channel length and width of 5 and 1000 μm, respectively.

Figure 3(c) shows the switching charge Q_{FE} for different channel lengths, as obtained by integrating the difference in gate current in forward (switching) and backward I_D-V_G sweep (non switching) direction and multiplying this value with the scan speed (1 V/s). A linear fit to the data yields an ordinate intercept ($L=0$ μm) of 3.6 ± 0.1 nC and a slope of 0.011 ± 0.001 nC/μm. The intercept value is determined by the induced charge between overlapping source-drain and gate electrodes, which is identical for all transistors, and parasitic charging effects outside the active channel. It is therefore strongly dependent on the transistor geometry used. The slope of the curve can be used to estimate the semiconductor surface charge density (P_R) within the channel. From the slope and channel width of 1000 μm, a switching charge per unit channel area of 11 mC/m^2 is calculated. If we assume that Q_{FE} equals $2P_R$, as suggested by the observation that the inner loops are symmetrically centered within the outer loops, the semiconductor surface charge density induced by ferroelectric polarization is determined to be ~6 mC/m^2. Measurements on other transistor series (with different channel widths and/or source–drain electrode configuration) yielded values within 25%. This value is smaller than the remnant polarization of 84 mC/m^2 found for our capacitors and the value of 18 mC/m^2 reported in the P(VDF-TrFE) transistors that have Au electrodes.[19] The latter value was estimated using the method of Miller and McWhorter.[17]

Data retention characteristics were examined by measuring the remnant drain currents ($V_G=0$ V) as a function of time after a 100 ms set pulse of +15 or −15 V [Fig. 4(a)]. The off state current remains more or less constant with time. Note that loss of ferroelectric polarization would have resulted in an increasing off-state drain current. The on-state current decreases steadily with time. After 1 h the ratio of the remnant currents has deteriorated to ~30% of the initial value. More information on the on state degradation mechanism was obtained by applying programming pulses on the "degraded" devices. Applying negative gate pulses to the devices that had been in the on state for 1 h did not result in an increase in on state remnant current. However, when these devices were first programmed to the off state and then switched back to the on state, recovery of the original on state current was observed. We found that recovery in the off state is completed within 1 h. Similar aging behavior was

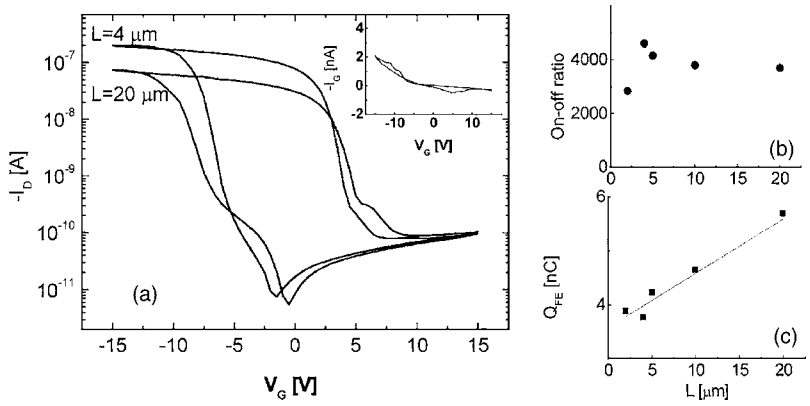

FIG. 3. Characteristics of OC_1OC_{10}–PPV ferroelectric transistors with a 150 nm thick P(VDF/TrFE) gate dielectric layer. (a) I_D-V_G curve of transistors with channel length 4 and 20 μm, recorded with $V_D=-2$ V. Inset: I_G-V_G curve of the 20 μm transistor; (b) ratio of remnant on- and off-currents, measured at $V_G=0$ V and $V_D=-2$ V for different channel lengths; (c) switching charge, Q_{FE}, for different channel lengths. The channel width was 1000 μm and the finger width of source and drain electrodes was 5 μm, so that the gate-to-source/drain overlap in all devices was identical.

observed in *n*-type FeFETs. Based on these observations, we attribute the degradation to ferroelectric domain pinning by ionic contaminations.[18] Because this degradation was absent in devices that have gold electrodes,[19] it is likely that the ionic contaminations stem from the PEDOT-PSS layers.

Further insight in device operation is gained with transient switching investigations of OC_1OC_{10}–PPV FeFETs with a 150 nm P(VDF/TrFE) layer [Fig. 4(b)]. Duration, magnitude, and polarity of the voltage pulse were varied. If we define switching time as the crossover point of the two curves, the switching time decreases from ~3 ms for pulses of ±10 V to 0.1 ms for pulses of ±25 V. Hence, especially for high fields the switching time is considerably larger than those of PEDOT-based ferroelectric capacitors of 40 μs,[20] suggesting that in the FeFETs the switching speed is dominated by the RC time constant of the semiconducting channel,[21] i.e., the product of the source–drain channel resistance in depletion and the gate capacitance.

Concluding, we demonstrated a potentially low-cost technology to make all-polymer ferroelectric transistors with promising switching characteristics and retention properties. The technology is amenable to downscaling of the dimensions of the transistor, both minimum feature size and layer thickness of the ferroelectric layer, as demonstrated by transistors with channel lengths of 2 μm that switch at voltages well below 10 V.

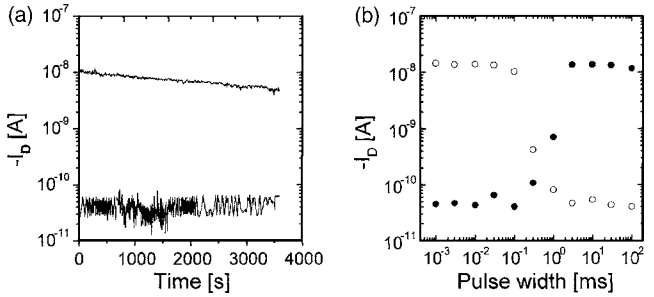

FIG. 4. Switching characteristics and retention times of OC_1OC_{10}–PPV ferroelectric transistors with a 150 nm thick P(VDF/TrFE) gate dielectric layer. (a) Time dependence of drain current (I_D) in the on-and off-state; (b) drain current (I_D) after application of gate pulse of + or −15 V with different pulse widths. In both (a) and (b), a 100 ms set pulse of + or −15 V was used to define the initial polarization state. V_D was kept at −2 V throughout the measurements.

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