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Technology for nanoelectronic devices based on ultra-high vacuum scanning tunneling microscopy on the Si(100) surface

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We describe two process steps in an STM-based fabrication technology for nanoelectronic devices. First, we have fabricated Co/Si metal lines on Si(100) surfaces by UHV-STM based nanolithography on a monohydride passivation layer. The STM tip was used to define depassivated lines (<10 nm in width) by electron-stimulated H desorption followed by Co deposition at submonolayer coverage. The resulting Co/Si wires show a granular structure with rough boundaries, but after anneal at 410 °C this changes into a compact structure possibly due to strong silicidation. Second, fabrication and analysis of tungsten contact metallization that will allow electrical transport studies along these metallic nanostructures has been performed.

1. INTRODUCTION

Scanning tunneling and atomic force microscopy (STM and AFM) have been proven to be unique tools for the fabrication of nanoscale structures [1,2]. For example, under normal scanning conditions the STM does not perturb the H-Si(100) surface, while by increasing the voltage between the STM tip and the sample H can desorb leading effectively to the possibility to pattern areas of any desired shape and size [2]. Metallization proceeds by means of Chemical or Physical Vapour Deposition (CVD, PVD) techniques [2-4] of metal adatoms which nucleate selectively on depassivated areas due to the increased density of reaction sites.

Although metallization techniques have been demonstrated recently for Fe and Al by CVD and PVD, respectively [2-4], Co merits special attention since it forms silicides with widespread applications in microelectronics (e.g., transistor gates, contacts, etc.), because they have low electrical resistivity, small lattice mismatch with Si at room temperature (RT) [5], and are metallic in nature [6]. On the other hand, Al/Si suffer from high temperature processing (≥400 °C) due to dissolution of Al into Si [7] leading effectively to degradation of metallic structures, while $FeSi_2$ is usually semiconducting (depending on the phase) [8].

Furthermore, for nanometer-scale devices, it is necessary to use a high-resolution conventional patterning technology to link the atomic scale to the measurement equipment. The first reports on such technology were given in ref. [9,10]. Here we will present details of electronic properties of such contact metallization.

2. EXPERIMENTAL PROCEDURE

We have separated the experiments in two series; one directed at patterning of nanostructures, on conventionally prepared substrates, the other directed at the contact metallization. All experiments presented here were performed on p-doped Si(100) samples of resistivity approx. 25 Ωcm.

For the nanostructure patterning samples were cleaned by resistive heating to 1200 °C and dosed with atomic H from high purity H_2 as described in ref. [11]. Co was e-beam evaporated at a rate ~0.0017 nm/sec. The samples were imaged and

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patterned *in-situ* with mechanically cut PtIr tips.
For the contact metallization, the liftoff technique to create tungsten patterns of 6 nm thickness with 30 nm resolution is described elsewhere [10]. Liftoff takes place in hydrofluoric acid (40% in water), which leaves the sample surface mostly hydrogen passivated. The sample is kept in dry nitrogen ambient as much as possible, and is immediately loaded into the UHV. A sequence of lengthy 400 °C degassing, hydrogen radical cleaning, and anneal at approx. 720 °C is used for the in-situ preparation. The last anneal takes place in a chamber with base pressure $5 \cdot 10^{-11}$ mbar; avoiding carbon contamination of the surface is crucial for this step. These samples are imaged with etched and sputtered W tips (radius of curvature 10 to 20 nm). The results presented here are for 24 Ωcm p-type wafers.

3. FABRICATION TECHNOLOGY OF Co/Si NANOWIRES

Fig. 1 illustrates the ability of a mechanically cut PtIr STM tip to form high-resolution patterns on a H-Si(100) surface by electron stimulated H desorption. Depassivated lines were written with varying current, sample bias V_b=5.5 V, and a writing speed of 200 nm/sec. In this case (V_b<7 V) H desorbs according to a vibrational excitation mechanism [2]. The lines appear higher than the rest of the H-Si(100) surface due to the increased density of states (H-free Si dangling bonds) for tunneling. It is clear that at these moderately high voltages it is possible with the mechanically cut tips to define depassivated lines of 2-3 dimer rows wide.
Submonolayer deposition of Co onto bare and passivated Si(100)2x1 surfaces at RT as well as elevated temperature, and the effect of subsequent annealing, is described in refs. [11 - 13]. On the bare surface, reaction occurs, in contrast to passivated surfaces, on which Co nucleates in sparse nonepitaxial islands.
Fig. 2 shows part of a depassivated line on a H-Si(100) sample after deposition of 0.13 ML of Co at RT. A dense concentration of Co in the depassivated area occurs due to reaction of Co with Si towards silicide formation even at RT [5], while on the monohydride areas it forms distinct islands [11]. The deposited Co atoms nucleate randomly even close to the wire without showing a significant depletion zone around the wire boundary. The wire width is approximately 8-9 nm which is comparable to the original depassivated line width.
It is possible to improve the structure of the metal patterns by further annealing treatments up to 470 °C (where H desorption commences [14]). Previous studies have shown CoSi and $CoSi_2$ formation to occur in the temperature range 375-500 °C [5,15]. Such a possibility is presented in Fig. 3 where Co was deposited at RT on a H-Si(100) surface with depassivated lines of about 5 nm wide, and further annealed at 410 °C for 20 sec. A more distinct and compact structure than that at RT is formed indicating strong silicidation in the wire area. The monohydride side remains intact even closely at the wire boundary (appearing even sharper than at

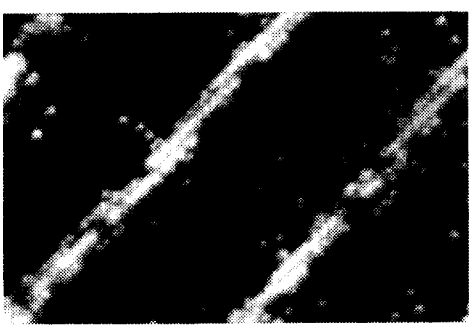

Figure 1. Depassivated lines on H-Si(100) surfaces created with STM at writing currents 3 and 4 nA (from top to bottom), and substrate bias voltage 5.5 V. Imaging at -2 V and 0.1 nA. Scan size 30x20 nm.

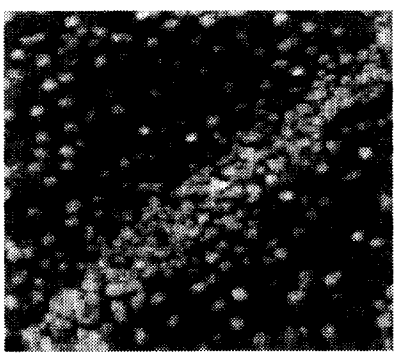

Figure 2. Co/Si wire formed after Co deposition at RT. Scan size 33x40 nm, Imaging at -1.8 V and 0.48 nA.

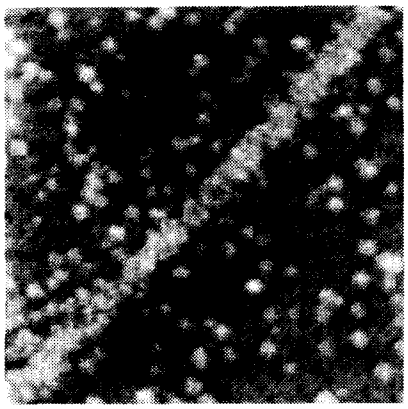

Figure 3. Co wire (5 nm wide) after Co deposition at RT and anneal at 410 °C for 20 sec. Scan size 45x45 nm. Imaging at -1.5 V and 0.28 nA.

RT) after the annealing process. Finally, we should point out that the presence of Co islands around the wire is not a potential problem for electronic transport experiments. Electron hopping from the wire to the nearest isolated islands is effectively suppressed because it leads to large charging energy [1, 16].

4. ELECTRICAL CONTACT TECHNOLOGY

An STM image of a contact structure resulting from the processing described in section 2 is displayed in Fig. 4a. Fig. 5 shows the current versus voltage of the *gap* in this pattern, i.e., the conductance through the tungsten silicide-silicon barrier and the silicon gap at a temperature of 4 K. The leakage current is below the noise level (about 1 pA) up to 3 V, and below 2 pA up to 5 V. Above 5.5 V the I(V) curve can be well fitted to Fowler-Nordheim emission. Using an electron microscope measurement of the gap size, 120 nm, the fit yields a barrier height of 0.5 eV. We expect the metallization is partly silicidized after the preparation, and the fitted barrier corresponds quite well to common silicide-silicon Schottky barriers [5]. Note that the gap is small enough to neglect curvature of the silicon bands due to space charge: the gap can be approximated by a square barrier for the conduction electrons, which is rounded at the edges due to the image charge potential.

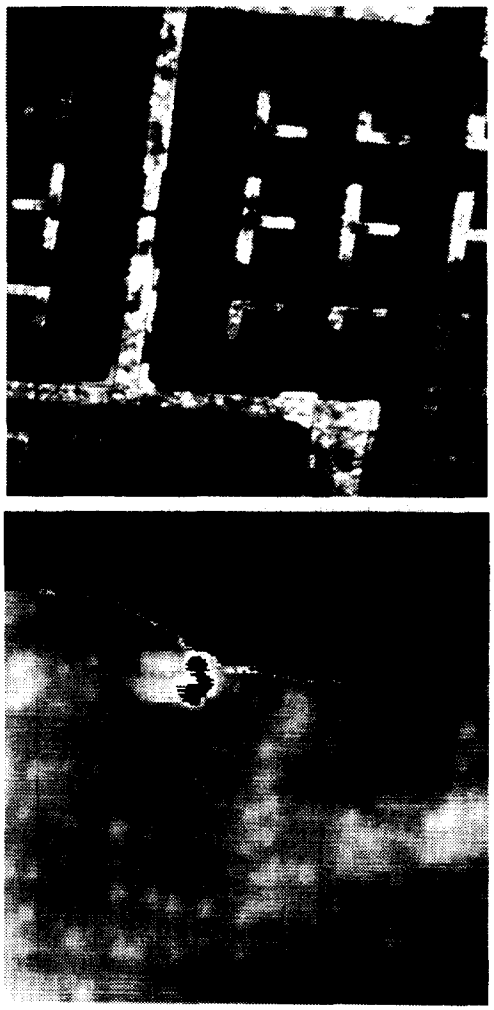

Figure 4. Central contact and marker pattern after cleaning as described in text. a) 4.5 micron view; b) detail of the area inside the gap, showing numerous terraces of the 2x1 reconstructed Si surface (25nm scan).

The silicon surface inside the gap is 2x1 reconstructed. Fig. 4b shows a detail of this surface. In general, the silicon has many terraces close to the W metallization. This becomes progressively worse as the final anneal temperature is increased above 720 °C. Nevertheless, after hydrogen passivation we have written patterns on this substrate, crossing the terraces and apparently running into the metallization. However, due to tip convolution there is a 'shadow' region around the metal which can not be imaged, so it is not verified that these patterns

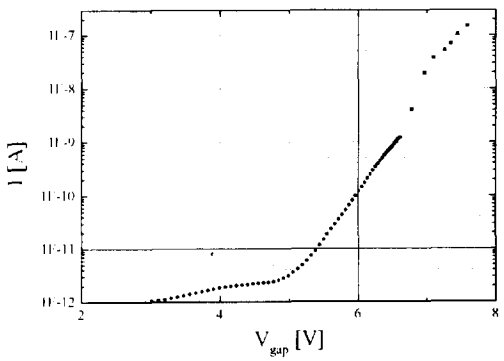

Figure 5. Current-voltage measurements through a structure closely similar to Fig. 4, with 120 nm gap. Temperature approximately 4 K.

actually connect to the metallization. Experiments are in progress for the resolution of this problem by employing thinner contacts and/or polishing techniques combined with alternative cleaning processes.

5. CONCLUSIONS

In comparison with former metallization studies, the Co/Si wires (especially the annealed ones) appear more compact than those by formed by CVD of $Fe(CO)_5$ [3] and PVD of Al [4] and with better defined boundaries. Thus, Co can be a potentially suitable candidate for future nanofabrication of metallic nanostructures due its strong reaction with the Si. Experiments are in progress to create metal nanostructures connected to macroscopic contacts.

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16. As is explained in ref. 1, envelope calculations indicate that for island sizes $\leq$10 nm the island charging energy $\sim e^2/C$ can overcome the thermal energy K_BT at RT ($T \approx 300$ K).