The FDM readout system for the TES bolometers of the SWIPE instrument on the balloon-borne LSPE experiment

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ABSTRACT

We present the design and first tests of a prototype readout for the SWIPE instrument onboard the LSPE balloon-borne experiment. LSPE aims at measuring the linear polarization of the Cosmic Microwave Background (CMB) at large angular scales, to find the imprint of inflation on the B-mode CMB polarization. The SWIPE instrument hosts two focal planes hosting 163 TES Au/Mo spiderweb bolometers each, cooled at 0.3 K for the detection of microwave frequencies of 140, 220 and 240 GHz.

To read all the detectors, a 16 channel frequency domain multiplexing readout system has been devised, consisting of LC resonators composed of custom Nb superconducting inductors and commercial SMD capacitors.

A set-up consisting of 14 LC resonators shows that we can accommodate 16 channels in the frequency range between 200 kHz and 1.6 MHz, since the necessary line-widths can be achieved. A preliminary firmware for the generation and read-out of the biasing frequency comb is also discussed.

Keywords: Cosmic microwave background, Frequency domain multiplexing, TES bolometers, superconducting inductors, LSPE, SWIPE.

1. INTRODUCTION

To obtain improved precision in measurements of cosmic microwave background (CMB), a new generation of mm-wavelength receivers with hundreds to thousands of transition edge sensor (TES) bolometric detectors must be exploited. This is due to TES detectors being close to the photon noise limit, which means that their noise performance is dominated by fluctuations in the arrival rate of the photons at the detector. Therefore, the strategy for the next generation of experiments to achieve a large increase in sensitivity is increasing the number of detectors.

Readout of large arrays of cryogenic detectors is a major instrumental challenge. In order to reduce the wiring complexity, the cost of per-channel readout components and the heat load delivered to the coldest stages by readout wiring, the readout of these arrays is multiplexed.

There are two complementary multiplexing techniques: time domain multiplexing and frequency domain multiplexing. In time domain multiplexing (TDM), a single readout channel is sequentially switched between each member of a set of n detectors. In frequency domain multiplexing (FDM), detectors are sinusoidally biased, so that they are separated in frequency space. In this way, a single readout channel simultaneously reads n detectors.

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2. THE LSPE EXPERIMENT

The Large Scale Polarization Explorer (LSPE) is a balloon-borne mission aimed at measuring the $B-$mode polarization of the CMB at large angular scales exploiting the reionization peak at $l \lesssim 10$.[1] Its primary target is to improve the tensor-to-scalar ratio limit down to $r = 0.03$ at 99.7% CL with a secondary goal to produce wide maps of foreground polarization generated in our galaxy by sinchrotron emission and interstellar dust emission. The angular resolution of the beam is roughly $1.5°$ FWHM and the experiment has a 25% coverage of the sky. The payload will fly, spinning in azimuth, in a 15 days long circumpolar balloon mission during the polar night.

The Short Wavelength Instrument for the Polarization Explorer (SWIPE) instrument[2] is composed of arrays of multi-mode bolometers to detect CMB at 140 GHz, 220 GHz and 240 GHz. Multifrequency detection is fundamental to achieve an efficient and reliable foreground evaluation. The system is cooled down to 300 mK, with optical components and filters cooled below 4 K to reduce the background on the detectors. The sky-scanning Stokes polarimeter uses a rotating half-wave plate and a steady polarizer to modulate the linear polarization of the incoming brightness.

3. SWIPE READOUT SCHEME

The CMB detectors in SWIPE are spider-web bolometers with TES thermistors.[3] Multi-mode horns are used to efficiently optically couple the optical stages of the detector with the TES bolometers, put in the backshort of the horns. SWIPE makes use of optically coupled sensors and not of antenna-coupled sensors, for the latter cannot allow a multi-mode detection because of throughput limitations.[4] The horns will be coupled to 12 modes for the 140 GHz band, 30 modes for the 220 GHz band and 34 modes for the 240 GHz band.

The readout of the detectors is achieved using the FDM technique, both for reduction of cost and implementation simplicity, by means of superconductive LC filters in series to each TES. TESs are voltage biased in AC from an external carrier generator. The cold LC filter has the double function of bandwidth-limiting the current noise from the resistive TES bolometers and allowing the n detectors to be biased with a single pair of wires. A comb of n bias frequencies is sent down this single pair. The tuned filter passes the appropriate bias carrier and suppresses the other $n - 1$. The n sensors with their series filters are connected in parallel and the currents are summed and readout with a single SQUID (see Figure 1), used as an extremely sensitive ammeter. Warm demodulation electronics separate and recover the individual detectors signals. SWIPE will use a 16-channel multiplexing, in the range of ~ 200 kHz $\div 1.6$ MHz with $14 \div 15$ channels used for biasing the TESs, and a 16th channel used for calibration purposes.

In the current design bolometer bias carriers are synthesized by an FPGA, which also performs demodulation and digitization of the bolometer outputs. The comb of the bias carriers is converted to analog through a DAC and then sent to the RLCs. The signal is amplified by a SQUID, after that active nulling is performed by sending an identical comb with a displacement of $180°$ at the SQUID input. In this way only the physics signal is amplified. After being digitized by an ADC, the FPGA demodulates the signal and sends it to the readout control computer via an Ethernet port. A simplified schematics of multiplexing and readout electronics is represented in Figure 1.
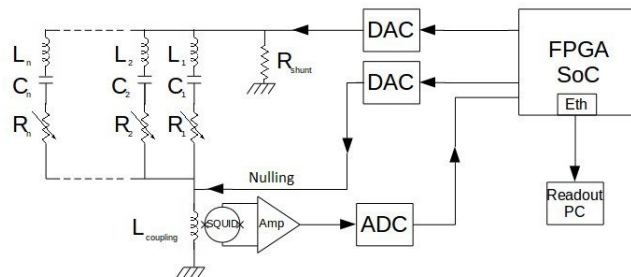

Figure 1. Sketch of the cold LC filters in series with each bolometer and the readout schematics.

3.1 Superconducting LC filters

The use of LC filters, consisting of a superconducting inductor and a capacitor, in series with each multiplexed sensor has three advantages: i) it allows the sensors to be biased with different frequencies, ii) the narrow bandwidth of the filters limits the Johnson current noise and prevent it from leaking to the other n channels in a multiplexed set, iii) it allows a comb of biases to be sent down a single pair of bolometer bias wires which greatly reduces the wire count to the sub-kelvin temperature stages, passing the appropriate bias frequency and suppressing the other $n - 1$.

The resonance frequency ν_r of a LC bandpass filter is given by

$$\nu_r = \frac{1}{2\pi\sqrt{LC}}, \tag{1}$$

where L and C are, respectively, the inductance and capacitance of the filter. The bandwidth is determined by the sum of all the dissipative elements in series with the filters. For an ideal LC filter in series with a TES bolometer with resistance R, the bandwidth (defined as the width of the resonance measured at 3 dB of attenuation) is given by

$$\Delta\nu = \frac{R}{2\pi L}. \tag{2}$$

In real measurements there is also a parasitic contribution R_p since the inductor and the capacitor are not ideal elements. The dissipative terms are summarized in the quality factor Q of the filter, defined as

$$Q = \frac{\nu_r}{\Delta\nu} = \frac{2\pi\nu_r L}{R + R_p}. \tag{3}$$

A bandwidth of ~ 10 kHz or less is desirable to minimize superposition between adjacent resonances.[9] Also, since the bandwidth depends only on L and not on C, the inductance should be the same for all the channels. Therefore, considering an operating TES resistance of ~ 1 Ω, a suitable inductance value is around $10 \div 15$ μH. The inductance in the bias circuit cannot be too large, due to electrical stability reasons.[5]

Capacitance values in the range 500 pF to 50 nF provide the correct span in frequency between 200 kHz and 1.6 MhZ. In LSPE an ensemble of commercial SMD C0G/NP0 capacitors, which show negligible dependence of capacitance and ESR with time, voltage, frequency and temperature, will be used.

3.1.1 Design

Since the LC filters are placed near the sensors, thus operating at sub-K temperatures, a natural choice is to use a superconducting coil to obtain the desired high Q. The standard inductor design for this applications is a superconducting coil deposited on and insulated from a square slit washer (see Figure 2).

For an n turn coil with inner diameter d, the inductance is close to[6]

$$L \approx 1.25 \ \mu_0 \ d \ n^2. \tag{4}$$

For its high critical temperature (~ 9 K), a standard choice is to use Niobium to fabricate the coil and the washer. SiO_2 is chosen as dieletric for the inductor.

We designed an 88 turns inductor coil (see Figure 2b), with a 1 mm large central hole, 5 μm large and 10 μm spaced tracks. According to Equation (4), this device has a nominal inductance of ~ 12 μH. We designed a photo-lithographic mask hosting a 6×6 matrix of inductors to be mapped on a 500 μm 2" polished Silicon wafer, with a 500 nm layer of thermal oxide.
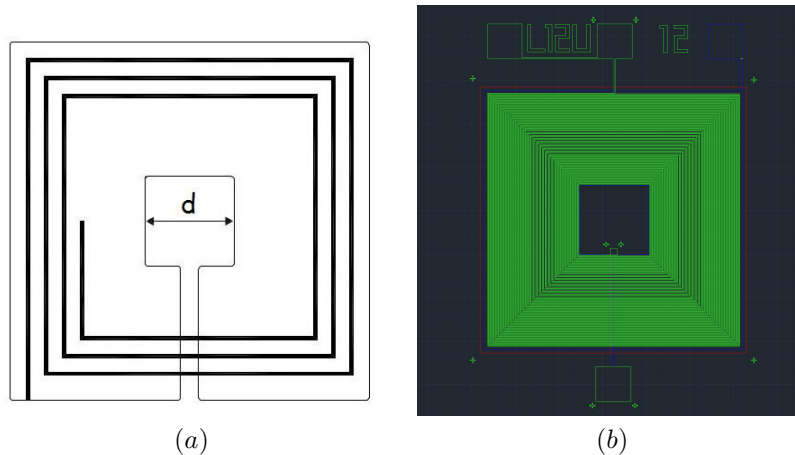
Figure 2. (*a*) Sketch (not to scale) of the square spiral inductor used for the LC filters. (*b*) A portion of the actual drawing for the inductor production mask.

3.1.2 Fabrication

The fabrication of the inductors is obtained exploiting optical lithography and sputtering processes in clean room environment.

The photolithography of the spirals is performed using a high resolution (0.9 μm) negative photo-resist. The wafer is preliminary baked on hot plate to reduce the presence of moisture that would compromise the resist adhesion on the SiO_2 substrate. After the wafer has returned to room temperature, the photo-resist is deposited on the substrate and spin-coated to reach a uniform 1.4 μm thick layer. Soft baking is then performed on hot plate to dry and harden the resist film, further increasing resist adhesion and reducing dark erosion during development.

The alignment and exposure is performed using a mask aligner in the UV spectral range. The radiation triggers a photo-chemical reaction, changing the chemical-physical properties of the exposed photo-resist, while leaving unaltered the areas covered by the patches of the mask. The amount of radiation dose supplied to the photo-resist is proportional to the exposure time. The correct value is calculated knowing the power supplied by the mask aligner and the radiation dose necessary to the resist to complete the crosslinking photo-reaction. An additional baking step (hard bake) is performed to further improve photo-resist hardening.

Since we use negative photo-resist, the development process removes the unexposed areas. To facilitate the lift-off step, we perform an over-development of about 30÷40% with respect to the nominal development time, to improve the undercut of the photo-resist.

After a cleansing step in Oxygen plasma to remove possible thin photo-resist films in the developed areas, the sample is put in the sputtering chamber. Niobium is deposited through DC sputtering. Vacuum is pumped to a level of $10^{-7 \div 8}$ mbar, then pure Argon is inserted to a controlled pressure of roughly 10 mbar. A DC-power is applied between the mechanical arm holding the sample and the metal plate holding the Niobium target, ionizing the gas and accelerating the Argon ions towards the target and breaking Niobium atoms out of it (see Figure 3*a*). A part of the atoms diffused in the chamber is deposited on the sample forming a thin film. The sputtering rate depends of the applied DC-power, the pressure of Argon gas and the distance between the target and the sample. We deposited a 120 nm thick film of Niobium with a sputtering rate of 30 nm/min.

The lift-off of the photoresist is achieved putting the sample in a bath with Acetone (see Figure 4). Figure 3*b* shows a schematic representation of the fabrication process while in Figure 5 some microscope views of a spiral inductor are presented.
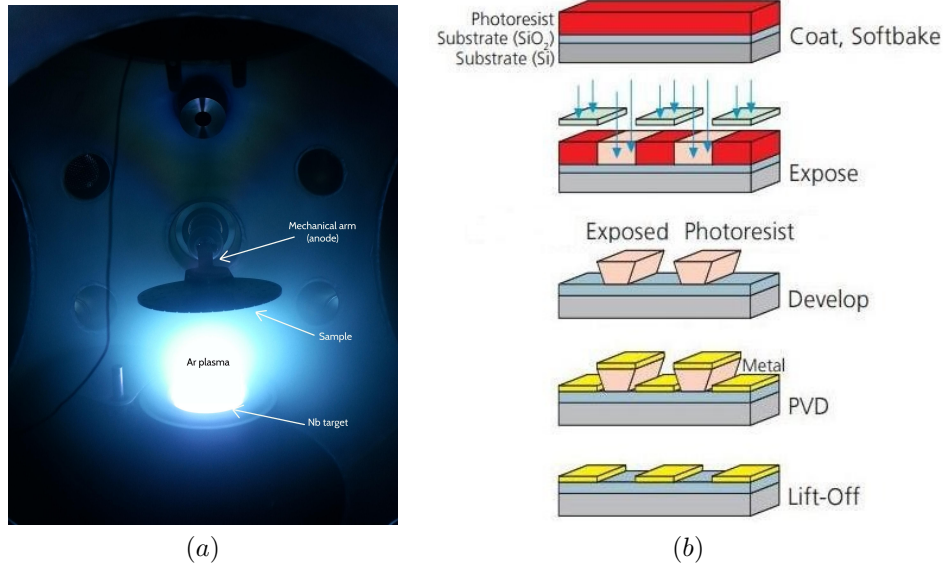
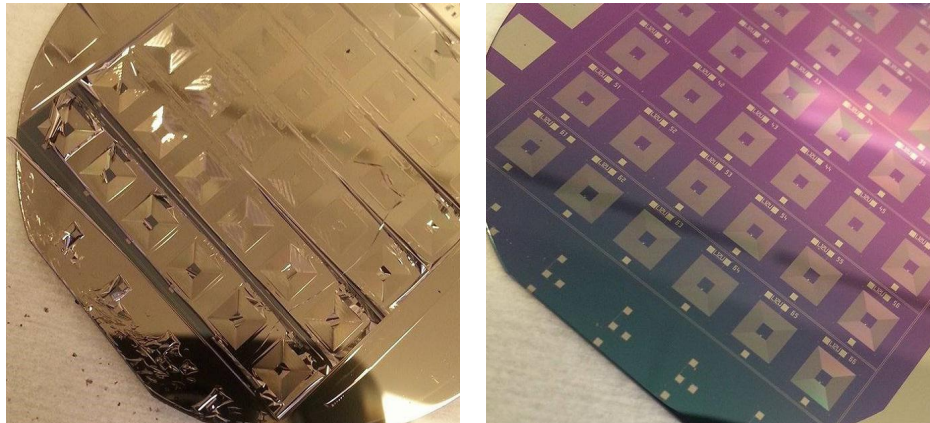Figure 3. (a) Niobium sputtering process. (b) Process schematics of the spiral inductors fabrication.[7]

Figure 4. Sample during and after lift-off. The wafer is put in a Petri dish with Acetone and stimulated in a sonic bath to favor the lift-off, exploiting the undercut of the photoresist. Finally, the wafer is cleaned with Isopropanol and Acetone.

3.1.3 Tests and results

We tested a 14-LC chain in our cryogenic facility at INFN Pisa.[8] To reach cryogenic temperatures, we used a two-stage pulse-tube cryocooler (PTC), composed by a first cold head (first stage) nominally reaching 50 K with a cooling power of 40 W and a second stage nominally reaching 4 K with a cooling power of 0.9 W. The two heads are hosted in a custom cryostat. The outer, room temperature, vessel is a steel vacuum chamber capable of reaching and maintaining a vacuum of $10^{-7 \div 8}$ mbar.

The first stage of the PTC is used to cool the intermediate 50 K stage, using a large copper plate, acting as a thermal break between room temperature and the 4 K stage. To reduce emissivity and radiation loading a cylindrical gold-plated copper radiation shield is suspended below the 50 K stage and encloses the 4 K stage. The second stage is the last and main stage of the PTC. With full thermal load, we could reach a temperature of 3.8 K. The temperature is monitored by a PT100 sensor on the first stage and a Si-diode sensor on the test PCB, on the second stage.

We realized a custom FR4 PCB to host three strips of six inductors, for a total of eighteen LC filters (see Figure 6). The LC filters were read in parallel, in a notch configuration, using a shunt resistance of 1.1 Ω. We
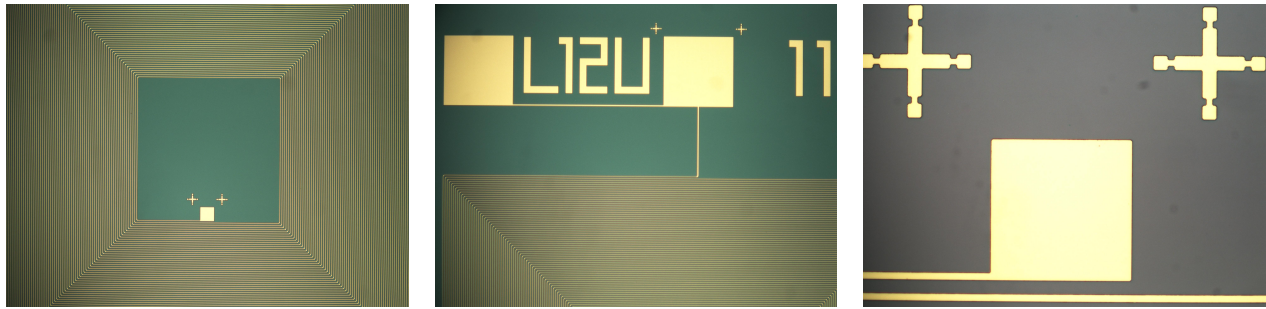
Figure 5. Microscope view of a spiral inductor: (left) large view on the central hole (5×), (middle) large view on the 500μm × 500μm bonding pads (5×), (right) detailed view of the 100μm × 100μm central pad with alignment crosses (50×).

used a Zurich HF2LI Lock-in amplifier to perform a frequency sweep from 100 kHz to 2 MHz and readout the cold resonators.
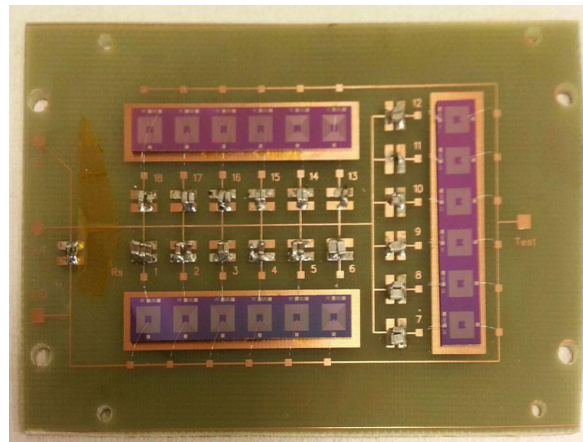

Figure 6. PCB hosting the LC chains, with micro-bondings connecting the inductors to the test circuit. Inductors 5 and 17 gave open resistance at room temperature, while all other inductors gave a room temperature resistance of ~170 kΩ. Chains 12 and 16 were not seen at a 3.8 K temperature.

The superconducting transition of the spirals occurred at ~ 8 K. We observed 14 resonances in the frequency range of interest (a possible 15$^{\text{th}}$ resonance may be superimposed to that at $\sim$ 950 kHz), with a bandwidth of roughly 4 kHz. We observed a high frequency rise, both in voltage and phase, which is interpreted as the parasitic contribution due to readout cables. We both simulated and measured this background and subtracted it from, respectively, the simulation and the data. In Figure 7 we show a comparison between simulation and data, which agree at a very good level. In the final multiplexing configuration the output of the LC chain will be sent directly to the SQUID input, so the background due to the cables will not contribute.

In Figure 8 the observed resonance frequencies as a function of the respective mounted capacitors are fitted with the expression

$$\nu_0 = \frac{1}{2\pi\sqrt{L_{\text{exp}}C}}, \tag{5}$$

yeilding $L_{\text{exp}} = 15.25 \pm 0.25$ μH. This value is suitable for our multiplexing scope, and is compatible with Equation (4), taking into account that these are not 3-layer inductors with a square slit washer, not yet implemented in this production, whose purpose is to exploit the Meissner effect to minimize the stray magnetic field, channeling the field lines into the central hole and minimizing mutual inductance between adjacent coils.
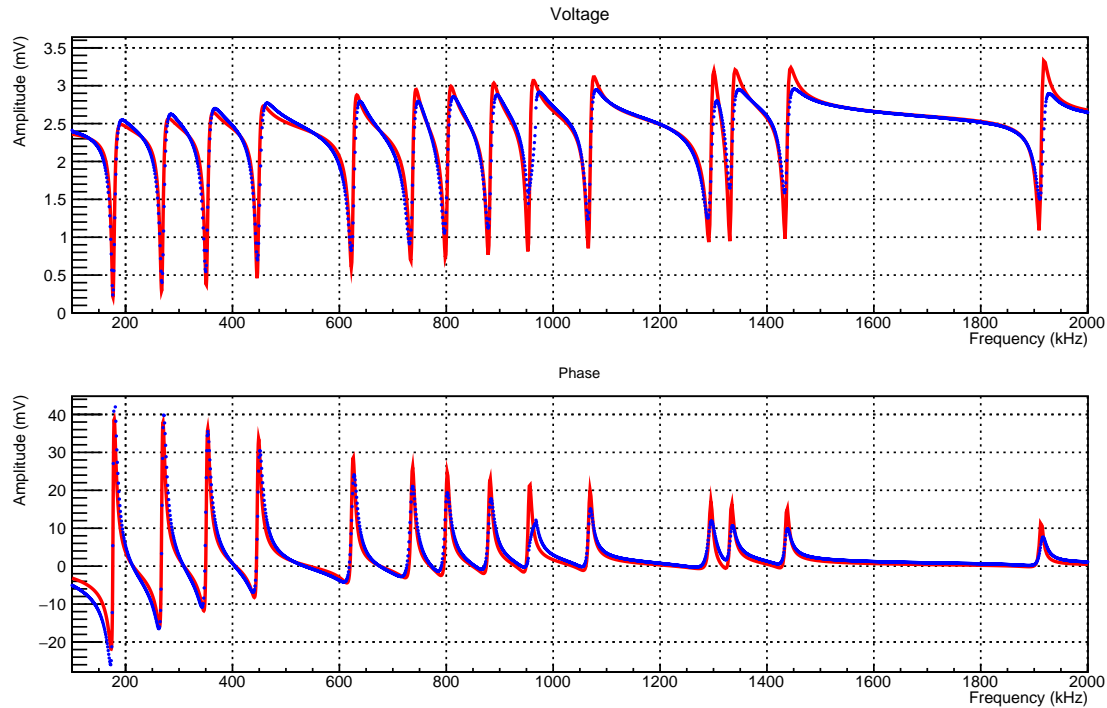
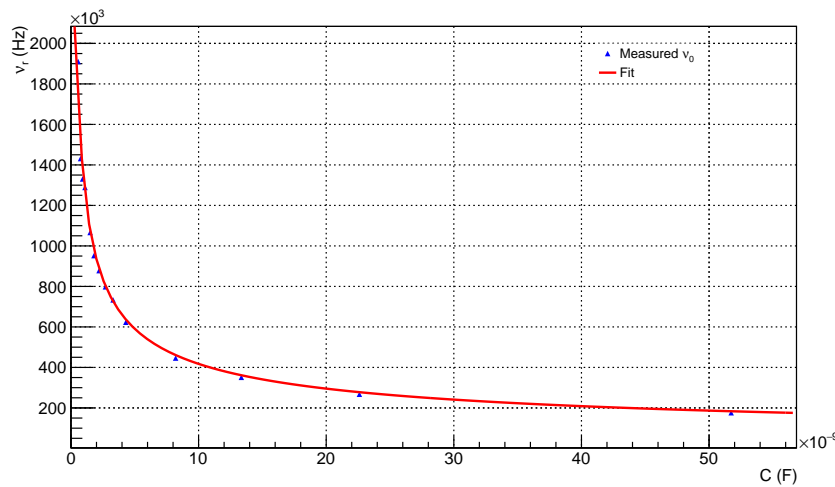Figure 7. Comparison between simulation (red line) and data (blue points).

Figure 8. Fit of the measured resonance frequencies to extract the inductance value.

3.2 Readout electronics

A custom board is being designed to read out the 16 resonator chains during LSPE flight. The core of the board is a System-on-Chip (SoC) device, Altera Cyclone V SoC model 5CSXFC6 which includes an FPGA with 110K logic elements and a powerful dual core ARM9 processor. The Cyclone V has been chosen because it offers good performances with very low power needs (as a reference it requires only 1.8 W for 4000 MIPS processing power).

In the current prototype only 2 DAC and one ADC are connected to the SoC device, allowing the control of a single chain but the final board will handle 4 chains. The chosen DAC (LTC1668) was selected for its low noise and low power properties, while the ADC will be an AD9266 with a sampling speed of 20 MHz. The SoC devices are a relative new entry in the digital electronics devices collection and appear to be the perfect choice

for data acquisition systems with moderate data input throughput but with a strong need of data reduction. At the firmware level the ADC and DAC protocol handling, the comb generation, the synchronous demodulation and the first data reduction will be handled by the FPGA fabric, then the remaining data will be transferred to the processors through the internal high speed bus. The processor will further reduce data and prepare data packets to be sent to the main DAQ computer through 100 Mbit Ethernet links.

To describe the FPGA firmware we decided to use the Visual DSP package from Altera. Visual DSP includes a rich set of DSP component libraries and it is interfaced with Matlab, allowing a very fast simulation of new demodulation algorithms and at the same time assuring that the logic is optimized in terms of speed and occupancy.

3.2.1 Generation

The board generates a comb consisting of 16 carriers one of which, for testing purpose, will be looped-back in order to measure and compensate the amplitude stability of the generator level.

The carrier and nulling generation are based on Numerically Controlled Oscillator (NCO) blocks which are used in multichannel mode at 20 MSPS. Frequency, amplitude and phase of each carrier are independently programmable. The frequency can be set with a resolution related to the Q factor of the TES RLC network, typically at the tens of Hz level, and the amplitude can be modified to span the TES dynamical range. Once amplitude and frequency are fixed, a set of relative phases is selected in order to minimize the output signal dynamic range.

A typical schematic of the synthesizer developed in DSP builder is represented in Figure 9 together with a typical Fourier spectrum of the carrier comb.
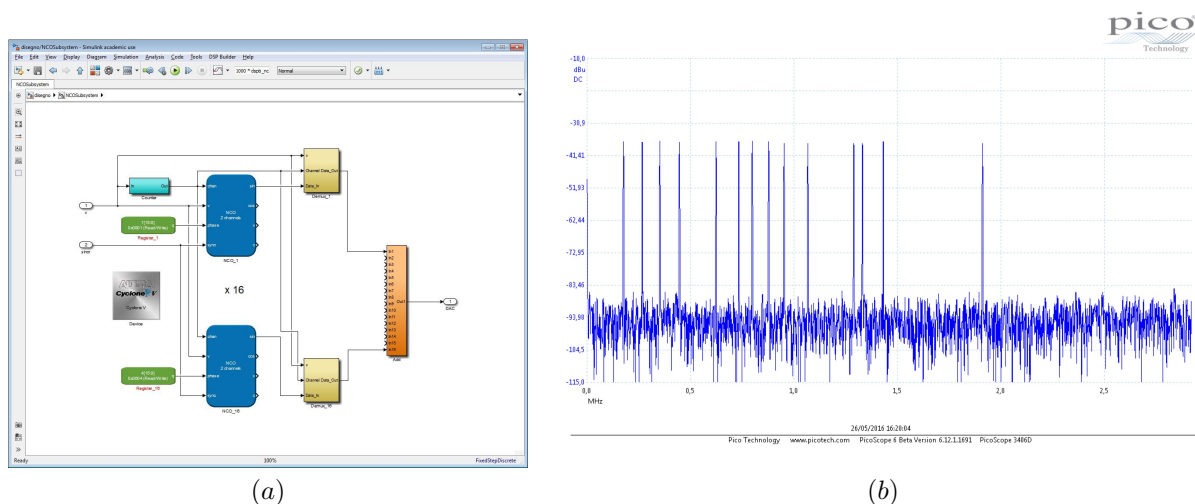

Figure 9. (*a*) An example of the implementation of a bias comb in DSPBuilder. (*b*) Example of Fourier spectrum of the output of our comb generator tuned to the frequencies measured in the present tests.

3.2.2 Demodulation

We have just started the firmware development of the demodulation phase, which is inspired by existing projects developed for similar experiments.[10,11] In the current implementation the digitized signals from the 16-bit input ADCs are mixed with the 16 sinusoidal carriers, decimated and filtered to get the demodulated output. This is in turn sent to the processor for recording a 100 Hz data stream of time-ordered data, sufficient to extract temperature variations induced by CMB temperature fluctuation on the rotating LSPE payload.

4. CONCLUSIONS

We are designing, fabricating and testing a 16-fold FDM system to read-out the TES bolometers of the SWIPE instrument onboard LSPE. First tests proved our ability to produce custom lithographed single-layer Nb inductors that allow to pack 16 frequencies between 200 kHz and 2 MHz. The cross-talk between adjacent inductors is estimated at the order of percent level, as confirmed by dedicated SONNET simulations. Direct measurements of the cross talk between neighbor inductors are planned in the near future, together with a test of an entire chain (bolometer, resonator chain and SQUID read-out) in a dedicated test facility that is being assembled at INFN Pisa.

ACKNOWLEDGEMENTS

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