Design and Analysis of a New Evaluation Circuit for Capacitors Used in a High-Power Three-Phase Inverter

Kazunori Hasegawa, Member, IEEE, Ichiro Omura, Member, IEEE, and Shin-ichi Nishizawa, Member, IEEE

Abstract—DC-link capacitors in power electronic converters are a major constraint on improvement of power density as well as reliability. Evaluation of the dc-link capacitors in terms of power loss, ageing, and failure rate will play an important role in design stages of the next-generation power converters. This paper proposes a new evaluation circuit for dc-link capacitors used in a high-power three-phase inverter, which is intended for testing power loss, failure rate, ageing, and so on. The evaluation circuit produces a practical ripple current waveform and a dc bias voltage into a capacitor under test, in which the ripple current is equivalent to that generated by the three-phase inverter on the dc link. The evaluation circuit employs a full-scale current-rating and downscaled voltage-rating inverter for producing the ripple current, so that the power rating of the evaluation circuit is much smaller than that of a full-scale current rating and full-scale voltage rating inverter. Theoretical analysis and simulated results verify the effectiveness of new evaluation circuit.

Index Terms—DC-link capacitors, high-power density, reliability, three-phase inverters.

I. INTRODUCTION

Power density of power electronic converters are continuously becoming higher and higher as their market size is getting larger and larger, which is accompanied by smaller power loss, lower volume, and lower weight in the converter. The market size growth also requires improvement of reliability not only in power semiconductor devices but also in passive components [1, 2]. Hence, the next-generation power converters will be designed with managing both power density and reliability.

DC-link capacitors in power electronic converters are a major constraint on improvement of power density [3, 4]. They tend to include a design margin of size or capacitance due to power loss. Thus, the minimum design margin of the capacitors is desirable, which should be considered in design stages of the converters. Furthermore, a lifetime of the capacitors is usually shorter than that of semiconductor devices or magnetic devices, which would degrade reliability of the power converters. Evaluation of the capacitors in terms of power loss, ageing, and failure rate will play an important role in design stages of the next-generation power converters [5-14].

Fig. 1 Basic concepts of an evaluation circuit for a high-power capacitor. (a) Using full-scale inverter. (b) Using full-scale current-rating and downscaled voltage-rating inverter.

Although nonlinear characteristics of the capacitors are usually evaluated by a single sinusoidal current such as 120 Hz, 1 kHz, and so on on [9, 10, 14-16]. There are some kinds of “ripple current tester” instruments that provide a sinusoidal ripple current as well as a dc-bias voltage into the capacitor [16]. Actual current flowing out of the converter into the capacitor contains multiple frequency components [17], so that characteristics of the capacitors cannot be exactly estimated. Although the so-called fast Fourier transform (FFT) can extract the multiple frequency components from the actual current, a power loss of the capacitor cannot be estimated using the multiple frequency components because power loss in general has a nonlinear characteristic. In addition, the dc bias voltage across the capacitor affects power loss and ageing [2, 7, 13, 14]. Thus, the power converters often employ more capacitors than necessary.

It is important to develop an evaluation circuit for component
testing of capacitors, which will be utilized in design stages or in tests before shipment of the converters. Note that the system should behave as an existing inverter in terms of the dc bias voltage and ripple current waveform of the capacitor.

This paper proposes a new evaluation circuit for dc-link capacitors used in a high-power three-phase inverter, which presents a practical ripple current waveform that is equivalent to that of the existing inverter. The circuit will be utilized for evaluating the capacitor by electric or thermal measurement such as the followings:

1. Electrical measurement of ESR and capacitance [8, 11].
2. Power loss measurement by electrical or calorimetric measurement [12, 18].
3. Accelerated aging [14].

Although this paper does not pay attention to measuring characteristics of the capacitor under test, it just focuses on design and analysis of the evaluation circuit. The following sections describes possible circuit configurations, intensive theoretical analysis, and power rating of the evaluation circuit.

II. BASIC CONCEPT

A. Evaluation circuit for capacitors

The most effective way to evaluate dc-link capacitors is measuring their characteristics with an existing inverter in operation. For example, references [6, 8, 11] discuss real-time monitoring for capacitor condition using equivalent series resistance (ESR) and capacitance. Therefore, a basic idea of the evaluation circuit would utilize the existing inverter. Fig. 1 (a) shows the basic idea of the evaluation circuit, in which a full-scale current-rating and full-scale voltage-rating inverter is connected to a capacitor under test, $C_{UT}$. The inverter provides a practical ripple current and dc bias voltage for the capacitor.

There are some special circuits that evaluate the capacitors [10, 14]. Reference [10] presents a simple circuit to evaluate an electrolytic capacitor, which consists of a combination of a dc-voltage supply providing a dc bias voltage, and a line-frequency transformer injecting a sinusoidal ripple current. Reference [14] presents a simple circuit configuration for accelerated aging of metalized film capacitors, which consists of a combination of a resonant inverter producing a sinusoidal ripple current and a dc voltage supply providing a dc bias voltage. Although both the two combinations contribute to reducing the overall power rating of the evaluation circuit, the ripple current waveform is different from the practical one generated by the inverter.

Fig. 1 (b) shows the basic concept of the proposed evaluation circuit that employs a small inverter, the capacitor under test, a bypassing capacitor, a choke inductor, and a high-voltage dc supply. The concept is similar to the circuits proposed in [10] and [14] in terms of a combination of a ripple current source and a dc voltage supply, whereas it presents a practical ripple current waveform, i.e., the same current waveform as that generated by the inverter. Current rating of the small inverter is full-scale, while voltage rating of that is downscaled. The high-voltage dc supply keeps the capacitor voltage a desired dc bias voltage. The bypassing capacitor is used for circulating the ripple current generated by the inverter through the capacitor under test. The choke inductor is used for blocking the ripple current, through which only dc current flows. Hence, the proposed circuit operates as a full-scale voltage-rating and full-scale current-rating inverter from the standpoint of the dc bias voltage and ripple current. Thus, power-rating of the small inverter is much smaller than that of the full-scale inverter.

B. Possible configurations of the small inverter

Candidates for the small inverter can be classified into the followings:

1. Single-phase current-source inverter (CSI) (Fig. 2 (a))
2. Single-phase voltage-source inverter (VSI) (Fig. 2 (b))
3. Three-phase voltage-source inverter (VSI) (Fig. 2 (c))

The evaluation circuit using the single-phase CSI behaves as a full-scale three-phase or single-phase inverter if it can provide the same ripple current waveform as the current generated by the full-scale single-phase or three-phase inverter, respectively. However, not only pulse width but also amplitude should be modulated to synthesize the ripple current waveform. In practice, therefore, quite complex control would be required for the CSI.

The single-phase VSI can be used for an evaluation circuit for the full-scale single-phase inverter. DC-link terminal of the VSI is connected to the bypassing capacitor and capacitor under test, so that the voltage across the bypassing capacitor is slightly lower than that across the capacitor under test by the dc-link voltage. Since instantaneous power in a single-phase circuit
fluctuates at double the fundamental frequency, a ripple amplitude of the dc-link voltage in the single-phase VSI tends to be large. It will be a constraint on the voltage rating of the VSI because the dc-link voltage should be larger than the ripple amplitude. The evaluation circuit consisting of the single-phase VSI would be applicable to capacitors of modular multilevel cascade converters (MMCC) [19], that are also referred to “modular multilevel converters (MMC)” or “cascaded H-bridge converters (CHB),” because they consist of single-phase full-bridge converters.

The three-phase VSI is a candidate for an evaluation circuit for the full-scale three-phase inverter. DC-link terminal of the three-phase VSI is connected to the bypassing capacitor and capacitor under test like the single-phase VSI. On the other hand, a ripple amplitude of the dc-link voltage in the three-phase VSI is much lower than that in the single-phase VSI because the instantaneous power of the three-phase inverter is constant in a steady state [20].

This paper introduces the three-phase VSI as the small inverter because of the following reasons:
1. The three-phase inverter is widely used.
2. Lower dc-link voltage allows smaller power rating.

3. General-purpose inverters are available as the small inverter.
4. No special control is required to the ripple current.

Note that the three-phase VSI has only to control its output voltage, i.e., open-loop PWM control is applicable.

## III. PROPOSED SYSTEM CONFIGURATION

### A. Circuit Configuration

Fig. 3 shows the proposed evaluation circuit consisting of the three-phase VSI, a low-voltage dc supply $V_{LV}$ with a choke inductor $L_{LV}$, the high-voltage dc supply $V_{HV}$ with a choke inductor $L_{HV}$, the bypassing capacitor $C_{bypass}$, and the capacitor under test, $C_{UT}$. The low-voltage dc supply is used for driving the three-phase VSI. The high-voltage dc supply provides a dc bias voltage to $C_{UT}$.

Fig. 4 shows current paths flowing out of the two dc voltage supplies and the three-phase VSI. The high-frequency ripple current generated by the VSI, $i_{HF}$ circulates through $C_{bypass}$ and $C_{UT}$ because it does not flow into the two choke inductors $L_{LV}$ and $L_{HV}$ as shown in Fig. 4(a). The low-voltage dc supply $V_{LV}$ provides a dc current $I_{LVdc}$ to the VSI through $L_{LV}$ as shown in Fig. 4(b). The high-voltage dc supply charges $C_{UT}$ and $C_{bypass}$ to their operating voltages, and then supplies a small amount of leakage dc current of the capacitors, $I_{HVdc}$ as shown in Fig. 4(c). Hence, the power rating of the high-voltage dc supply is quite small.

### B. Power rating of the small inverter

Since the current rating of the small inverter is the same as that of the full-scale inverter, the relation between the power rating of the small inverter, $P_{small}$ and that of the full-scale inverter, $P_{FS}$ is given by

$$\frac{P_{small}}{P_{FS}} = \frac{V_{DClink-S}}{V_{DClink-FS}} \times \frac{V_{LV}}{V_{HV}}$$

where $V_{DClink-FS}$ and $V_{DClink-S}$ are dc-link voltages of the full-scale inverter and the small inverter, respectively, and $P_{FS}$ is the power rating of the full-scale inverter. As the dc-link voltage of the small inverter, $V_{DClink-S}$ contains ripple voltages of $C_{UT}$ and $C_{bypass}$, the dc mean of $V_{DClink-S}$ should be designed to be more than the ripple voltages. The low-voltage dc supply should provide the dc mean voltage according to the ripple voltages. Since the instantaneous power of the three-phase
TABLE I RATINGS AND CIRCUIT PARAMETERS OF THE PROPOSED CIRCUIT USED IN ANALYSIS AND SIMULATION.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power rating of the system</td>
<td>1 MVA</td>
</tr>
<tr>
<td>Power rating of the inverter</td>
<td>100 kVA</td>
</tr>
<tr>
<td>AC current rating</td>
<td>I_o</td>
</tr>
<tr>
<td>AC voltage rating</td>
<td>V_o</td>
</tr>
<tr>
<td>Low-voltage dc source</td>
<td>V_Lv</td>
</tr>
<tr>
<td>High-voltage dc source</td>
<td>V_Hv</td>
</tr>
<tr>
<td>Load inductor</td>
<td>L_sw</td>
</tr>
<tr>
<td>Load resistor</td>
<td>R_sw</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>f_sw</td>
</tr>
<tr>
<td>Output frequency</td>
<td>f_o</td>
</tr>
<tr>
<td>High-voltage choke inductor</td>
<td>L_HV</td>
</tr>
<tr>
<td>Capacitor under test</td>
<td>C_UT</td>
</tr>
<tr>
<td>Unit capacitance constant of the capacitor under test [25]</td>
<td>H</td>
</tr>
<tr>
<td>Bypassing capacitor</td>
<td>C_bypass</td>
</tr>
<tr>
<td>Leakage resistance of capacitors</td>
<td>R_dk</td>
</tr>
<tr>
<td>Equivalent series resistance of capacitors</td>
<td>R_es</td>
</tr>
<tr>
<td>Damping resistor</td>
<td>R_damp</td>
</tr>
</tbody>
</table>

(1) is based on 1 MVA, 2 kV, and 300 A
(2) is based on 100 kVA, 200 V, 300 A, and 50 Hz

inverter is constant, dc-link voltage of the three-phase inverter contains only switching ripple component. Thus, one can pay attention to the switching frequency, the current rating, and capacitance of C_UT. In practice, however, attention should also be paid to imbalance of the three-phase load of the inverter because it would cause ripple voltage on the dc link.

Note that, accelerated ageing tests, especially for highly accelerated life tests (HALT), are often accompanied by over voltage or current ratings, so that the ripple voltages would get large. It would be a constraint on reducing the power rating of the small inverter in the accelerating tests.

This paper introduces a condition that the dc-link voltage of the small inverter is 1/20 to 1/10 of that of the full-scale inverter.

C. Design of Choke Inductors

Reactances of the two choke inductors should be much larger than that of capacitors C_UT and C_bypass:

$$\omega L_{\text{choke}} \gg \frac{1}{\omega C_{\text{dc}}}$$  \hfill (2)

where $$\omega = 2\pi f_{\text{sw}}$$, $$f_{\text{sw}}$$ is the switching frequency of the inverter, $$L_{\text{choke}}$$ indicates a choke inductor of $$L_{\text{HV}}$$ or $$L_{\text{LV}}$$, and $$C_{\text{dc}}$$ stands for C_UT or C_bypass. The current rating of $$L_{\text{choke}}$$ is determined by the leakage dc current of $$C_{\text{dc}}$$. Since volume of inductor is in proportion to 3/4th power to the maximum stored energy of

TABLE II RATINGS AND CIRCUIT PARAMETERS OF THE FULL-SCALE INVERTER USED IN SIMULATION.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power rating</td>
<td>1 MVA</td>
</tr>
<tr>
<td>AC current rating</td>
<td>I_o</td>
</tr>
<tr>
<td>AC voltage rating</td>
<td>V_o</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>V_dk</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>f_sw</td>
</tr>
<tr>
<td>Output frequency</td>
<td>f_o</td>
</tr>
<tr>
<td>Load inductor</td>
<td>L_o</td>
</tr>
<tr>
<td>Load resistor</td>
<td>R_o</td>
</tr>
</tbody>
</table>

(1) is based on 1 MVA, 2 kV, 300 A, and 50 Hz

IV. ANALYSIS OF THE CAPACITOR CURRENT

This section makes a theoretical analysis of the capacitor current against the current flowing out of the inverter so as to indicate equivalency to the full-scale inverter in terms of capacitor current waveform.

A. Transfer function for the capacitor current

Fig. 5 shows an equivalent circuit that focuses on the transfer function between the ripple current flowing out of the inverter $$I_{\text{HF}}$$ and the capacitor current $$I_C$$, where $$I_{\text{HF}}$$ is depicted as a high-frequency ac current source. $$Z_1$$, $$Z_2$$, $$Z_3$$, and $$Z_4$$ are impedances of the high-voltage choke inductor, bypassing capacitor, capacitor under test, and low-voltage choke inductor, respectively. $$Z_1$$ and $$Z_4$$ consist of inductances $$L_{\text{HV}}$$ and $$L_{\text{LV}}$$, and series resistances $$R_{\text{UV}}$$ and $$R_{\text{LV}}$$ that stand for equivalent series resistances and/or intentionally-installed damping resistors, respectively. $$Z_2$$ and $$Z_3$$ contain capacitances $$C_{\text{bypass}}$$ and $$C_{\text{UT}}$$, equivalent series resistances $$R_{\text{ES2}}$$ and $$R_{\text{ES3}}$$, and leakage

$$\frac{1}{2} LI^2$$ [21], the volumes of the choke inductors are quite small.

D. Example of practical use

Low-voltage (200 or 400 V) general-purpose inverters are available to the small inverter, so that medium-voltage capacitors are suitable for the proposed circuit. The current rating of the general-purpose inverters are up to 1000 A [22, 23]. Thus, the proposed circuit using the general-purpose inverter can evaluate capacitors used in a high-power inverter with a power rating up to 1-10 MVA.
resistances $R_{\text{leak}1}$ and $R_{\text{leak}2}$, respectively. The impedances $Z_1$ to $Z_4$ are given by the followings:

$$Z_1(s) = sL_{HV} + R_{HV}$$  \hspace{1cm} (3)

$$Z_2(s) = \frac{R_{\text{leak}2}}{1 + sC_{\text{bypass}}R_{\text{leak}2}} + R_{ES2}$$  \hspace{1cm} (4)

$$Z_3(s) = \frac{R_{\text{leak}3}}{1 + sC_{UT}R_{\text{leak}3}} + R_{ES3}$$  \hspace{1cm} (5)

$$Z_4(s) = sL_{LV} + R_{LV}.$$  \hspace{1cm} (6)

$I_C(s)$ can be calculated by $Z_1$ to $Z_4$ and $I_{HF}(s)$. Thus, the transfer function $G(s)$ between $I_{HF}(s)$ and $I_C(s)$ is expressed as

$$G(s) = \frac{I_C(s)}{I_{HF}(s)} = \frac{Z_1Z_4}{Z_1Z_2 + (Z_1+Z_2)(Z_3+Z_4)}$$  \hspace{1cm} (7)

B. Analytical Result

Table I summarizes the rating and circuit parameters of the proposed circuit used for this analysis as well as simulation described in section V. Reactances of $L_{HV}$, $L_{LV}$, $C_{\text{bypass}}$, and $C_{UT}$ under a switching frequency of 1 kHz are given by

$$\omega L_{HV} = \omega L_{LV} = 6.3 \, \Omega$$  \hspace{1cm} (8)

$$\frac{1}{\omega C_{\text{bypass}}} = \frac{1}{\omega C_{UT}} = 53 \, \text{m}\Omega$$  \hspace{1cm} (9)

Thus, reactances of choke inductors are adjusted to be much larger than those of the capacitors. Note that $R_{HV}$ corresponds to the damping resistor $R_{\text{damp}}$ described in section V, and $R_{LV}$ is set to be zero.

Fig. 6 provides a bode plot of the transfer function $G(s)$ with different capacitors of $C_{UT} = 3 \, \text{mF}$ and 1.5 mF. The gain of $G(s)$ stays 0 dB and the phase of that does 0 degrees in a range over the switching frequency of 1 kHz, which indicate that the capacitor current $I_C$ is equivalent to the ripple current flowing out of the inverter $I_{HF}$.
Fig. 7(a) shows the full-scale three-phase inverter, where a dc voltage source is connected instead of the capacitor under test on the dc link. Sinusoidal pulse-width modulation (SPWM) is applied to the inverter. The inductive load with a small equivalent series resistance of 1% is connected, so that the inverter drives almost only reactive power. Although the ripple current waveform somewhat changes according to the power factor of the inverter output power, it always contains high-frequency ac components that result from the switching frequency and a dc current that synthesizes an active power. Hence, the inverter does not have to drive active power when it operates as a ripple current source. Note that the inverter can also drive active power in return for increased power rating of the dc voltage source.

Table II summarizes the ratings and circuit parameters of the full-scale inverter.

![Graphs](image-url)

Fig. 8 Simulated waveforms of the capacitor current $i_C$. (a) Full-scale inverter. (b) Proposed circuit under Condition 1. (c) Proposed circuit under Condition 2. (d) Proposed circuit under Condition 3.
B. Proposed circuit

Fig. 7(b) illustrates the proposed evaluation circuit used for simulation. The capacitors $C_{UT}$ and $C_{bypass}$ include equivalent series resistances and leakage resistances. Power dissipations of the equivalent series resistances and that of the leakage inductances are assumed to be 0.05% of the rated power of the circuit because a dissipation factor of dc-link capacitors used in a high-power inverters is around 0.1%. The damping resistor $R_{damp}$ prevents an oscillation caused by the capacitors and the choke inductors. The power consumption of the damping resistor is only 0.1% of the supplied power from the high-voltage dc supply. Note that the proposed circuit can also supply a ripple current in case the load power factor is changed although the low-voltage dc supply has to provide an amount of active power to the small inverter.

This section discusses validity of the proposed circuit with different power ratings and different capacitors as the followings:

- **Condition 1:** Power rating is 1/10 of the full-scale inverter, and $C_{UT} = C_{bypass} = 3 \text{ mF}$.
- **Condition 2:** Power rating is 1/20 of the full-scale inverter, and $C_{UT} = C_{bypass} = 3 \text{ mF}$.
- **Condition 3:** Power rating is 1/10 of the full-scale inverter, and $C_{UT} = 1.5 \text{ mF}$ and $C_{bypass} = 3 \text{ mF}$.

The ratings and circuit parameters of the condition 1 are shown in Table I. Condition 2 employs a low-voltage dc source of $V_{LV} = 175 \text{ V}$ and the same current rating as the condition 1. Condition 3 uses the same parameters of the condition 1 except for $C_{UT}$.

C. Simulated results

Fig. 8 shows simulated waveforms of the capacitor current $i_C$. In addition, Fig. 9 illustrates frequency spectrums of the capacitor current extracted by the Fast-Fourier Transform (FFT). All the waveforms of the proposed circuit almost agree with that of the full-scale inverter from the standpoint of time domain as well as frequency domain.

Fig. 10 shows the voltage across the capacitor under test, $V_{CUT}$ in the proposed circuit. They stay at 3.5 kV that is the dc bias voltage applied by the high-voltage dc supply.

Fig. 11 shows the dc-link voltages of the small inverter in the proposed circuit, $V_{dclink}$. Since the peak-to-peak ripple amplitude of $V_{dclink}$ is determined by $i_{HF}$ and the capacitors, the amplitude in the condition 1 is equal to that in the condition 2, which is 64 V. This is only 18% of the nominal dc-link voltage of 350 V, and so it would have room for reducing the nominal dc-link voltage, i.e., reducing the power rating of the proposed circuit. On the other hand, the amplitude in the condition 3 are larger than that in the condition 1 and 2 because smaller $C_{UT}$ is employed.

**Conclusion**
This paper has proposed a new evaluation circuit for dc-link capacitors used in a high-power three-phase inverter. The proposed circuit is characterized by combining a small three-phase inverter and a small voltage supply. Although the power rating of the small inverter is less than 1/10 of that of a full-scale three-phase inverter, the proposed circuit is equivalent to the full-scale inverter in terms of the capacitor current and dc-bias voltage. Theoretical analysis has confirmed that the small inverter presents the same ripple current waveform as that of the full-scale inverter. Simulation using a software package of the “PLECS” has confirmed the viability and effectiveness of the proposed circuit, verifying that the proposed circuit presents the same ripple current waveform and dc bias voltage as those of the full-scale inverter to the capacitor under test.

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**REFERENCES**


**Fig. 10** Simulated waveform of the voltage across the capacitor under test, $v_{\text{CUT}}$, in the proposed circuit. (a) Condition 1. (b) Condition 2. (c) Condition 3.

**Fig. 11** Simulated waveform of the dc-link voltage of the small inverter in the proposed circuit. (a) Condition 1. (b) Condition 2. (c) Condition 3.
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