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PLATFORM-BASED DESIGN, TEST AND FAST VERIFICATION FLOW FOR MIXED-SIGNAL SYSTEMS ON CHIP

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“The field is lost, everything is lost!

The Black One has fallen from the sky and the towers in ruins lie

The enemy is within, everywhere! And with him the Light… Soon they will be here…

Go now, my lord, while there is time… There are places below”

“And you know them too... I release thee! Go! My servant you'll be for all time”

“As you command, my king”

“I had a part in everything. Twice I destroyed the Light and twice I failed.

I left ruin behind me when I returned, but I also carried ruin with me…

She, the mistress of her own lust”

J.R.R. Tolkien

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INTRODUCTION

In the last few years, automotive field has become one of the most dynamic but even complicated manufacturing sectors in the world. It pointed out how the increase of sophisticated and leading-edge emerging electronic technologies can be rapid. Car companies consider electronic development as the key point to meet very heterogenic requirements such as high-safety, comfort, infotainment, gas emission reduction, power saving, low cost and short time to market. For these reasons the expectations on the electronic automotive systems are very high and nowadays this sector seems to be one of the most innovative, challenging and competitive of all the market fields. If we take a look to some numbers, we can easily have an idea of the current situation: the 80% of technology innovation in cars is made of new electronics, the 20% of a vehicle's cost is related to electronics devices, the 15% of micro processor systems are absorbed by automotive and, in a car, there are more than 100 sensors and micro processors systems. We have to consider that all these numbers are still growing fast.

Following this trend, latest refinements in photolithography techniques has featured an increasing shrinking of dimension of sensing elements up to the development of Micro Electro Mechanical Systems (MEMS) and Micro Opto Electro Mechanical Systems (MOEMS) in which mechanical and optical elements, sensors, actuators and electronics are integrated on a common silicon substrate. If in the last decades the diffusion of measurement systems was limited by high costs, large size and low reliability, the new generations of MEMS sensors guarantee remarkable savings in cost, area and power consumption, featuring a fast and deep market penetration.

The scenario has evolved to a complex mixed-signal chip to be designed in a very short time, due to the low time-to-market, guaranteeing a high level of reliability and a strong fail-safe policy.

Of course, costs must be reduced to the minimum, avoiding re-design phases and further silicon runs.
Taking into account all the aspects mentioned above, this research is then providing methodologies to enhance the design phase from architectural space exploration and system study to verification of the whole mixed-signal system. At the beginning of the work, some innovative digital IPs have been designed to develop efficient signal conditioning for sensor systems on-chip that has been included in commercial products. After this phase, the main focus has been addressed to the creation of a re-usable and versatile test of the device after the tape-out which is close to become one of the major cost factor for ICs companies, strongly linking it to model's test-benches to avoid re-design phases and multi-environment scenarios, producing a very effective approach to a single, fast and reliable multi-level verification environment. All these works generated different publications in scientific literature.
The compound scenario concerning the development of sensor systems is presented in Chapter 1, together with an overview of the related market with a particular focus on the latest MEMS and MOEMS technology devices, and their applications in various segments.
Chapter 2 introduces the state of the art for sensor interfaces: the generic sensor interface concept (based on sharing the same electronics among similar applications achieving cost saving at the expense of area and performance loss) versus the Platform Based Design methodology, which overcomes the drawbacks of the classic solution by keeping the generality at the highest design layers and customizing the platform for a target sensor achieving optimized performances. An evolution of Platform Based Design achieved by implementation into silicon of the ISIF (Intelligent Sensor InterFace) platform is therefore presented. ISIF is a highly configurable mixed-signal chip which allows designers to perform an effective design space exploration and to evaluate directly on silicon the system performances avoiding the critical and time consuming analysis required by standard platform based approach.
In chapter 3 we describe the design of a smart sensor interface for conditioning next generation MOEMS. The adoption of a new, high performance and high integrated technology allow us to integrate not only a versatile platform but also a powerful ARM processor and various IPs providing the possibility to use the platform not only as a conditioning platform but also as a processing unit for the application. In this chapter a description of the various blocks is given, with a particular emphasis on the IP developed in order to grant the highest grade of flexibility with the minimum area occupation.

The architectural space evaluation and the application prototyping with ISIF has enabled an effective, rapid and low risk development of a new high performance platform achieving a flexible sensor system for MEMS and MOEMS monitoring and conditioning. The platform has been design to cover very challenging test-benches, like a laser-based projector device. In this way the platform will not only be able to effectively handle the sensor but also all the system that can be built around it, reducing the needed for further electronics and resulting in an efficient test bench for the algorithm developed to drive the system.
The high costs in ASIC development are mainly related to re-design phases because of missing complete top-level tests. Analog and digital parts design flows are separately verified. Starting from these considerations, in the last chapter a complete test environment for complex mixed-signal chips is presented. A semi-automatic VHDL-AMS flow to provide totally matching top-level is described and then, an evolution for fast self-checking test development for both model and real chip verification is proposed. By the introduction of a Python interface, the designer can easily perform interactive tests to cover all the features verification (e.g. calibration and trimming) into the design phase and check them all with the same environment on the real chip after the tape-out. This strategy has been tested on a consumer 3D-gyro for consumer application, in collaboration with SensorDynamics AG.

Chapter 1
SENSOR AUTOMOTIVE APPLICATIONS

1.1 Introduction

Today, electronics in automotive fields, like car sector, is knowing a incredible fast growing period. Automotive innovation and development is strictly correlated to electronic. Recent statistics show that about the 90% of innovation in new cars are electronic based, with global industry analysts forecasting that by 2010 electronic content will account for 40% of cost of a typical mid-sized. Moreover the world market for non-entertainment automotive electronics was estimated at US$36.8 billion in 2005 and is forecast to reach US$52.1 billion by 2010 that represents an increase of about the 40% in only five years. This incredible and fast growing will be possible thanks to the introduction of new products in quite all of the four main areas of the automotive electronic reported for simplicity in figure 1-1. While powertrain sector, accounted up to now to cover about the 32% of global market, will remain stable, safety, driving assistance modules and infotainment will show a dramatic increase. The request of new products in these fields is coming from two main different subjects. First of all governments are introducing continuously new laws to improve safety and reduce CO_2 emissions. Reinhard Schulte-Braucks, head of the automotive unit of the Enterprise and Industry Directorate-General of the European Commission, says car makers will have to reduce CO_2 emissions to reach the community target of 120g/km by 2012 and enhance road safety through crash-avoidance technologies.

Powertrain & Safety

Engine Management
Electronic Suspension
Drive by Wire
Braking Systems
Power Steering
Airbags
Gearbox

Comfort/Convenience & Vehicle Controls

Dashboard/Instrument Cluster
Lights/Seats
Climate Control
Voice Recognition
Remote Keyless Entry
Security Alarm Systems
Wiper/Window Control

Driver Assistance

Night Vision
Lane Departure Warning
Adaptive Cruise Control
Collision Warning
Park/Reverse Assist
Tire Pressure Monitoring
Heads Up Display

Infotainment & Communications

Telematics
Navigation/GPS
Multimedia Systems
Audio Systems
Rear Seat Entertainment
Games Consoles
Tuners (SDR)

Figure 1-1: Automotive Electronic segments [source: Bosch]

The requirements are detailed in the CARS 21 (Competitive Automotive Regulatory System for the 21st Century) strategy being promoted by the European Commission.
Another key factor for automotive companies is represented by the requirements coming from mature markets, such as the European and USA ones. Customers are looking for more and more comfort and security as well as an increasing number of entertainment systems. Such requests range from the basic control of climate, lighting, and humidity to the automatic setting of seat, rear view mirrors, steering wheel position according to the driver's physique, improved navigation assistance and infotainment products.
This scenario is representing a big challenge for semiconductors companies and automotive manufacturers. During these years

these companies have been going through a period of significant change and consolidation, a trend which is expected to continue and across all tiers of the industry. Recent examples include Continental's acquisition of Motorola's automotive electronics business and the acquisition of Siemens VDO automotive AG; Valeo's acquisition of Johnson Control's engine controls business; and Siemens VDO's acquisition of DaimlerChrysler's Huntsville Electronics. Contemporaneously systems and components suppliers are looking to reduce costs by moving production in the South-East Asia to lower cost locations. These changes and consolidations are done in order to improve productivity and give a proper answer to actual and future automotive market challenges.
From a more technical point of view, automotive manufacturers are under continuous pressure to fulfil market and governments requirements and they all agree that electronic is the key to solve in time the tensions between these different requirements and meet low cost production.
Anyway, these requirements are pushing towards an increase of complexity of electronics into cars. In today's luxury cars, up to 2500 signals (i.e., elementary information such as the speed of the vehicle) are exchanged by up to 70 Electronic Control Units and this trend continues to grow very fast. Many safety applications such as Anti-lock Braking System (ABS), vehicle stability control and occupant protection, so far independent, will have to communicate with each other for optimal safety. In addition, new driver assistance systems such as autonomous cruise control, lane departure warning, night-vision and blind-spot monitoring will be introduced, requiring semiconductor-based sensors and high-performance processors and memory resources. Moreover automotive experts agree on the fact that in the next few years "X-by-Wire" will play a key role on the growing of electronics in car and will completely change some important fields of the automotive industry.
In this scenario the performances of microcontroller units (MCUs) play a key role on the achievement of the aforementioned goals. They first entered the automobile for purposes of engine control in 1970s and since then, MCU computing performances have multiplied by 20. A recent agreement between Freescale and Continental has been signed to develop the first triple-core 32-bit microcontroller for next generation electronic braking systems (EBS). The multi-core approach is promising to increase performances, reduce power consumption and combine different functions in a single ECU (figure 1-2).

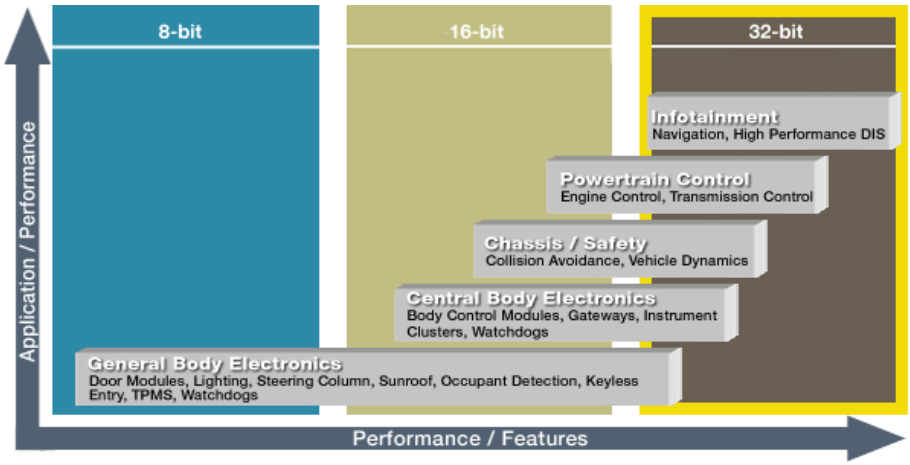


Figure 1-2: MCUs performances versus applications [source: Freescale]

1.2 Automotive electronic applications

In this paragraph we will see in much more details some of the most important automotive electronic applications. In particular we will focus on actual system solutions and on future trends. The target is to understand what the electronic world is expected to do in the automotive field and consequently which are the most industrial relevant research activities in this area.

i. Chassis & safety

Safety is certainly a driving factor for automotive since governments laws and customers are strongly requiring a continuous evolution. In this scenario modern chassis systems play an increasingly important part in autonomous safety and also in efficient vehicle operation. In figure 1-3 are reported some of the main actual technologies enabling modern and efficient chassis.
Anti-Lock Braking Systems (ABS) are designed to maintain driver control and stability of the car during emergency braking. Locked wheels will slow a car down but will not provide steering ability. ABS allows maximum braking to be applied while retaining the ability to "steer out of trouble". The operation of ABS can slightly reduce stopping distance in some cases like on wet road surfaces, but it can increase the stopping distance in others, as may be the case in deep snow or gravel.

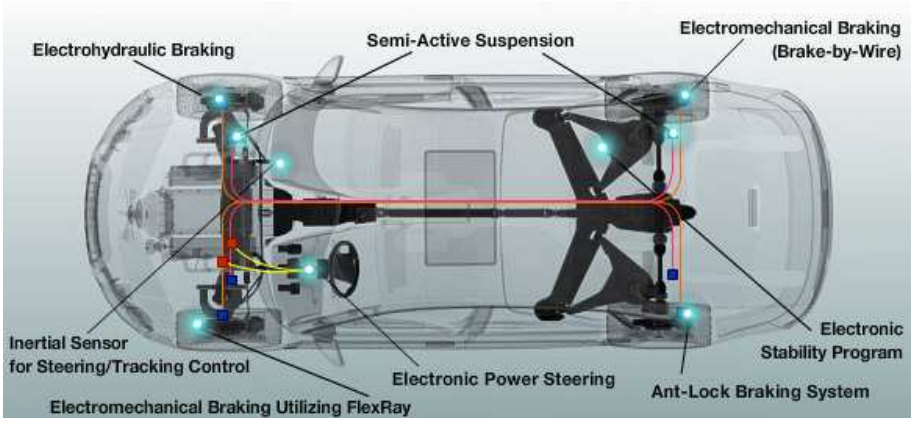


Figure 1-3: Technologies enabling modern chassis.

An ABS system monitors four wheel speed sensors to evaluate wheel slippage. Slip can be determined by calculating the ratio of wheel speed to vehicle speed, which is continuously calculated from the four individual wheel speeds. During a braking event, the function of the control system is to maintain maximum possible wheel grip on the road - without the wheel locking - by adjusting the hydraulic fluid pressure to each brake by way of electronically controlled solenoid valves. For passenger car applications, the majority of ABS components are often housed together in a single, under-hood mounted module. ABS systems make use of modern Micro Electro-Mechanical Sensors (MEMS) and in particular of gyroscopes and accelerometers.
MEMS are widely used in safety applications since they allow very sensitive and reliable solutions while lowering dramatically area occupation and overall costs. For example they are used to build electronic stability program (ESP) systems. They consist in the detection of a difference between the driver's control inputs and the actual response of the vehicle. When differences are detected, the system intervenes by providing braking forces to the appropriate wheels to correct the path of the vehicle. This automatic reaction is engineered for improved vehicle stability, particularly during severe cornering and on low-friction road surfaces, by helping to reduce over-steering and under-steering. Since ESP is an evolution of ABS, additional sensors must be added to the "old" ABS system. A steering wheel angle sensor is used to detect driver input with a yaw rate sensor and a low-g accelerometer sensor that measure the vehicle response. Some ESP systems include a connection to the powertrain controller of the vehicle to enable reductions in engine torque when required.

In the near future ESP, ABS, Traction Control System (TCS), powertrain and navigation modules will have to communicate each other to really improve the level of safety. This will require a higher computational power as previously underlined (see figure 1-2) and also improved MEMS and electronic solutions. In fact one of the main targets for the future is the realization of compact, reliable and cost efficient Inertial Measurement Units (IMUs). An IMU works by detecting the current rate of acceleration and changes in rotational attributes in the X, Y and Z-axis (see figure 1-4Figure 1-4).

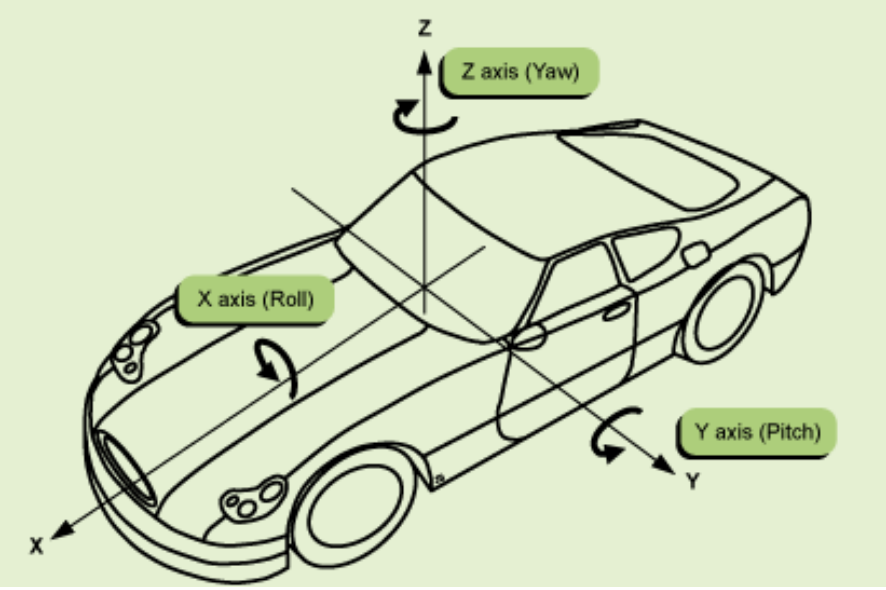


Figure 1-4: IMUs work by detecting changes in pitch, roll, and yaw.

It consists of three accelerometers and three gyroscopes used in combination to provide a complete control on vehicle movements. Many companies such as Continental, Freescale and SensorDynamics AG are investing so much in the IMU development since it would bring many safety modules - such as the aforementioned ABS, ESP and TCS - and navigation modules in a single one, thus leading to an evident advantage in terms of cost, area occupation and performances.
MEMS find another important application in airbag systems. Basic systems that serve as frontal collision protection for front seat occupants are being replaced by intelligent, high-end airbag systems that also include side protection for both the front and rear passengers and supplementary systems for additional head

and knee protection. For example while the detection of the passengers and their motion can be performed by a seats-based MEMS X-Y accelerometer, the airbag system can be positioned differently in a car, allowing multiple information determination such as identification of type of collision, its direction and the g-force impact; in this way a specific and dedicated airbag reaction can be guaranteed. As a consequence airbag algorithms are becoming significantly more complex requiring greater computational performances. In addition modern solutions implement one more inertial sensor signal linked to a watchdog MCU used to double-check that the "crash" has really happened.

Another important application in chassis & safety is the Electric power assisted steering (EPS). EPS uses an electric motor to provide directional control to the driver. Most EPS systems have variable assist, which provides more assistance as the speed of a vehicle decreases and less assistance from the system during high-speed situations. This functionality requires a delicate balance of power and control that has only been available in recent years. In the event of component failure, a mechanical linkage such as a rack and pinion serves as a back-up in a manner similar to that of hydraulic systems. In the next future many experts agree on the fact that EPS will completely replace electro-hydraulic power steering systems (EHPS). In fact the benefits of EPS compared to EHPS are numerous: it enhances safety, increases fuel economy, provides varying levels of "road feel", and allows car designers more flexibility. The main challenge is the power management because in the biggest vehicles the current required to actuate electric motors is very high.

Electrohydraulic braking (EHB) systems are designed to allow electronic control of vehicle braking while retaining a reduced hydraulic system. The hydraulic system functions as a reserve in the event of a failure in the electronic control. The EHB control unit receives inputs from sensors connected to the brake pedal. In normal operation, a backup valve is closed and the controller activates the brakes of the wheels through an electric motor driven hydraulic pump. When the controller goes into a fail-safe mode, the backup valve is opened, which allows the brakes to be controlled through a conventional hydraulic circuit. The trend on braking system is to completely remove hydraulic systems moving to new solutions called Electromechanical Braking (EMB) or Brake-By-Wire. EMBs replace conventional hydraulic braking systems with a completely "dry" electrical component system. This occurs by replacing conventional actuators with electric motor driven units. This move to electronic control eliminates many of the manufacturing, maintenance, and environmental concerns

associated with hydraulic systems. Furthermore an all electric solution enables simpler integration of such higher-level functions as TCS and Adaptive Cruise Control (ACC). One of the main challenges for this new system is again power management as mentioned for EPS. Quite all experts think that a switch to 42V power supply will be needed to deliver more power. Moreover an electric system needs a high level of safety and this means that EMB components merit higher level of analysis, design and verification, they must be networked using high-reliability bus protocols that ensure comprehensive fault tolerance and chip redundancy must be granted.
EMB is not yet in industrialization but quite all automotive companies are investing on that. The expectations on these new systems are enormous (figure 1-5) especially in the sector of small vehicles. By 2010 the market is expected to have a volume of EUR 1.1 billion, while for 2015 EMB could reach a market penetration of 20/25 %. In fact many producers such as Fiat, Renault and Volkswagen are likely to fit their small and middle range cars with EMB to enhance profitability.

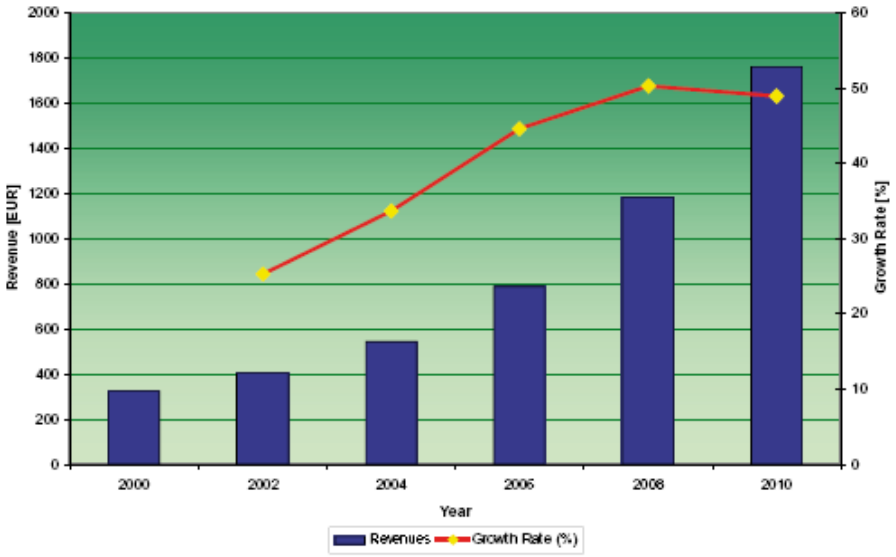


Figure 1-5: Revenue and grow rate forecast for X-by-wire systems in Europe.

ii. Powertrain

Powertrain represents for sure the core of automotive. Electronic has appeared in this field since the 1970s when the stringent automobile emission regulations introduced in the United States

immediately showed that a completely mechanical automobile couldn't give an efficient solution. Now electronic powertrain has the crucial role to reduce fuel emission meeting new requirements of CO_2 emissions while maintaining or increasing engine power as requested by customers. In figure 1-6 are sketched some of the main electronic features of powertrain. Probably the most known electronic powertrain application is the engine control. It first came out in 1978 and since then it has changed dramatically.

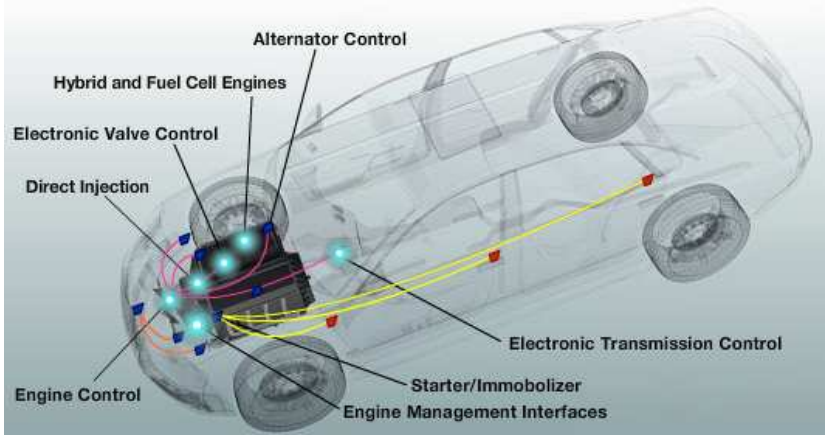


Figure 1-6: Powertrain technologies.

Modern electronic control systems are designed to meet legislative mandated exhaust emission levels, to provide competitive fuel economy, to meet customer quality expectations and to enhance the "fun to drive" factor. All system are based on a powerful microcontroller that is in continuous communication with many different devices that can interface with the harsh world of the engine and its complement of electro-mechanical sensors, solenoids, relays, injectors, coils, motors, actuators and other power managing devices. These systems always implement a high level of safety recurring to additional safety microcontrollers that continuously monitor the status of the engine, implementing failure and diagnostic routines. Consequently engine MCUs have to deal with a lot of input and output analog and digital signals to be processed in real time and coming from different parts of the car: cam position controller, wheel speed detector, temperature sensors, battery management unit, mass air flow system, throttle position system, oxygen sensors, relays, cam, throttle and fan control, injector system and so on. The system must survive in the harsh engine compartment environment thus satisfying strict

specifications such as reverse battery, load dump, inductive load spikes, over current, over voltage and high temperatures.
Now it's clearer that around the engine control ECU there are a lot of devices, each one related to a particular application. For this reason now we focus only on some of the most relevant from a research point of view.
The need to improve engine performance, reliability while reaching environmental targets is leading to the wide utilization of sensors. Nowadays all cars utilize mass air flow sensors to determine the mass of air entering a fuel-injected engine. The data from the sensors are used by the engine ECU to calculate and deliver the correct fuel mass to the engine. These kind of sensors can be implemented recurring to different solutions like hot wire sensors or "coldwire" sensors.
Crankshaft and camshaft sensors are used to control the mechanical movements of the engine. In modern automotive systems the data from these two sensors are used together to monitor the relationship between pistons and valves and to increase the efficiency of the engine. Moreover they are used for the measurement of the engine speed in revolutions per minute. These sensors typically consist of magnets and an inductive coil or they can be based on the Hall Effect.
Pressure and temperature sensors based on many different technology solutions are extensively implemented to monitor the correct functionality of the engine.
Battery Management Systems (BMSs) are gaining relevance since car power budget continues to increase thus pushing 14V automotive standard to crisis. Automotive BMS is highly complicated because it has to interface with a number of other on board systems and it has to work in real time in rapidly changing charging and discharging conditions as the vehicle accelerates and brakes (figure 1-7). It typically consists of a Battery Management Unit (BMU) and a Battery Control Unit (BCU). BMU is based on a microprocessor that has to manage many functions: one of the most important is the battery model function that consists in the continous monitoring and logging of the State Of Charge (SOC) of the battery. This is very important to coordinate the activity of the battery, calculating the maximum charging and discharging energy. The BCU contains all the BMS power electronic circuitry and it takes the inputs from the BMU to control battery charging and to switch the power connections to individual cells. Moreover it implements faulty routines to isolate the battery in case of alarm or fault conditions. Electric motors are used to implement many functions in a car (e.g. engine cooling fan, water pump) and in the

near future they are expected to be much more employed to replace mechanical or hydraulic actuated systems.
We already spoke about brake-by-wire and electric power assisted steering, but the X-by-wire technology finds other important applications. One of the most important in the powertrain sector is the electronic valve control (EVC) that is replacing the mechanical camshaft with single actuators for each valve for time independent driving. These actuators are typically electric motors controlled by the engine ECU.

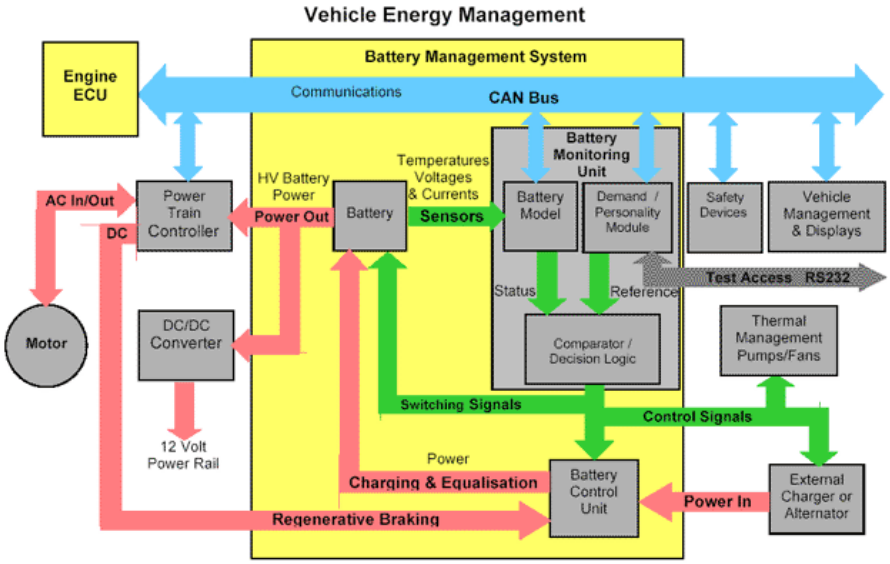


Figure 1-7: Typical Battery Management System diagram.

The advantages of this solution are numerous: increase of the engine power and fuel economy; features like adaptive cruise control, TCS and ESP become easier to be implemented. On the contrary valve control becomes much more power consuming if compared with mechanical solutions.

iii. Infotainment

Consumer demand for innovation continues to drive the rapid evolution of infotainment into cars. People wants to view movies, watch television, play video games, experience high-quality audio and have intelligent and fast navigation systems. Obviously automotive infotainment gets a lot of innovation from other industrial domains that are growing and progressing in the technology race at a very fast rate. Moreover while power saving is in common with the other automotive fields, the environment

characteristics such as the temperature are less restrictive thus leading to a fast technology growing. In figure 1-8 is sketched a diagram of entertainment and information system into a modern vehicle.

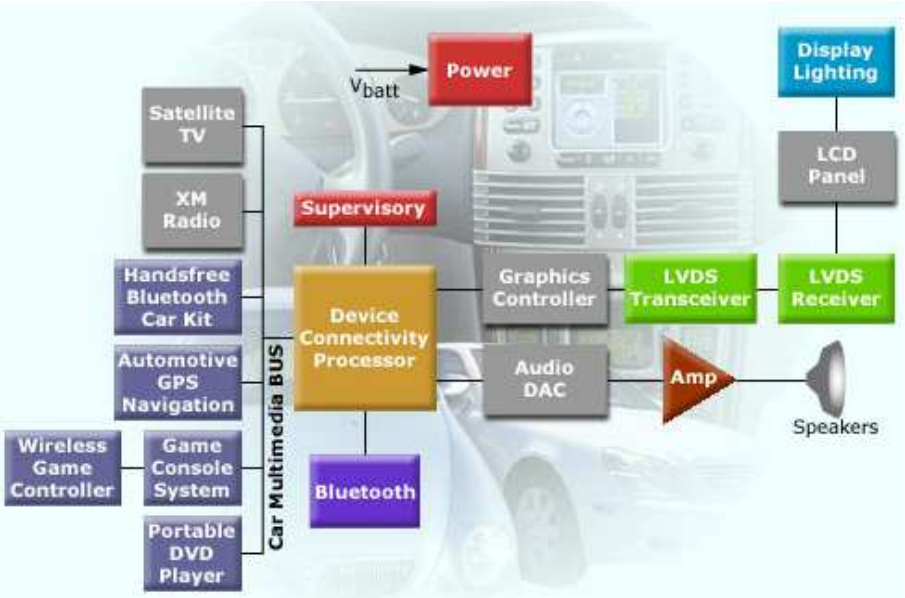


Figure 1-8: Automotive entertainment system.

There are many examples of infotainment applications: cellular communication, audio and video systems, intelligent navigation systems based on Global Positioning System (GPS), vehicle diagnostics and so on. The use of hard drives or flash drives in vehicles that could hold entire music libraries, games and movies for back-seat passengers is coming out on the market. Control of a device with voice commands will be possible in the near future using hybrid architecture that combines a MCU with a digital signal processor (DSP). A recent market research [1] shows that one of the major trends in the market is the realization of multi-featured systems that are expected to increase from 76M units in 2005 to 97M units in 2012 representing a CAGR of 3% per year. In the next few years this market will be most significantly impacted by new digital audio products that play 'soft' music files, digital broadcast technologies, connectivity to digital music players and stored files and emerging display based entertainment systems.

1.3 MEMS sensors in automotive

i. MEMS market analysis

In the last few years the density of electronic devices has exponentially grown thanks to the recent technological advances. Moreover the new progresses of micro-mechanical technology have featured the miniaturisation of sensing elements achieving complete sensor systems on a common substrate of silicon with the conditioning electronics. The new potentialities of MEMS devices have opened the way for a broad diffusion of sensing and actuating systems in a wide range of application fields. In fact, if in the last decades the diffusion of sensors and complete measurement systems was limited by the costs, the size and the low reliability, the new generations of MEMS sensors achieve high reduction of costs, area and power consumption. These systems have proven to be a key enabling technology of developments in areas such as transportation, telecommunications and health care, but the range of MEMS applications covers nearly every sector. According to latest updated technical market research report (a comprehensive new market research from SEMI and Yole [2] July 18, 2007), the global market for MEMS devices and production equipment reached $40 billion in 2006, and is expected to rise to $56 billion by 2009 and $72 billion by 2011, for a compound annual growth rate (CAGR) of about 12% over the five-year.
The MEMS devices at the heart of these systems overall amounted to $5.9 billion in 2006, and are forecast to grow to $10.8 billion in 2011, with a compound annual growth rate (CAGR) of 13 percent (refer to figure 1-9), pushed by the emerging employment in consumer electronics. MEMS devices are defined as die-level components of first-level packaging and comprise: pressure sensors, micro-resonators devices, accelerometers, gyroscopes, micro-RF devices, microphones, digital mirror displays, anemometers, etc.

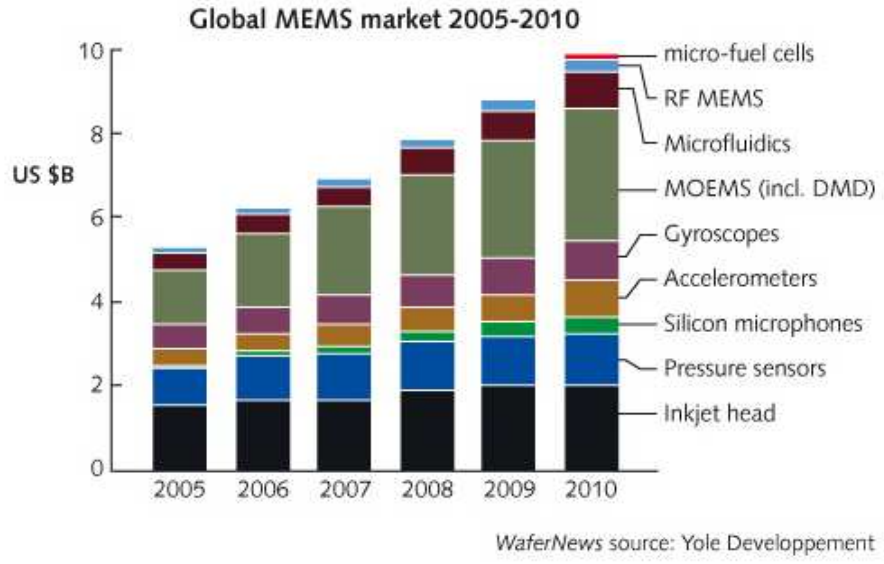


Figure 1-9: Global MEMS market 2005 2010

MEMS materials market can be partitioned into substrates and chemicals and other materials: together these markets consisted in $433 million in 2006 and are forecast to reach $806 in 2011. All materials are expected to be subject for five-year to a CAGR of 13% up to 2011 pushed by a demand driven by substrates, (representing more than 70% of the market), packaging coatings and emerging employment of chemical mechanical planarization (CMP). The MEMS equipment worldwide market amounted to $646 million in 2006, and is forecasted to achieve $838 million in 2009 and $999 million in 2011 with a five-year CAGR forecast for of 9%. Demand for MEMS equipment and materials also is poised for solid growth thanks to the increasing employment of etching technologies (notably deep reactive ion etch) by MEMS manufacturers, as well as for wafer-level bonding equipment in MEMS system packaging (see table 1-1).

Markets	2006	2011	Compound Annual Growth Rate
MEMS Materials	$433 million	$806 million	13%
MEMS Equipment	$646 million	$999 million	9%

MEMS Devices	$5.9 billion	$10.8 billion	13%
MEMS Systems	$40 billion	$72 billion	12%

Table 1-1: Global Markets and Forecasts for MEMS Systems, Devices, Materials and Equipment (Yole Development).

The world MEMS sensors market is fuelled by the increasing demand from different application fields, such as automotive and consumer electronics. The outstanding success of electronic stability control (ESC) and electronic safety active assistance systems joined with regulations passed by the worldwide safety authority that impose a growing adoption of security control in automobiles, are pushing the growth of the automotive segment. Furthermore the automotive technology has opened the way for the adoption of inertial sensors for adding functionality and safety in devices such as mobile phones, gaming devices and notebooks, determining a vertical growth in the consumer segment.
MEMS-based systems are also estimated to have a considerable potential in market segments such as life sciences, defence and environmental monitoring and protection, leading to continued commitment by government authorities and governmental agencies for this technology. The US and the European Union are promoting increasing investments in the employment of MEMS technology for a wide range of applications.
Furthermore funding from venture capitalists (VCs) is also expected to play a key role in the growth of the world MEMS sensors market.
Although the MEMS market is currently fragmented, both in terms of the types of devices being produced and the companies producing them (see figure 1-10). The latest projection [3] states that in the upcoming future over the next ten years, MEMS components trend will follow an increasing integration into single modules that will replace existing electronics systems. Moreover MEMS manufacturing will be absorbed by mainstream semiconductor companies. Nowadays it is a matter of fact that MEMS technology is replacing a growing number of non-silicon devices and the global sensor market is migrating from the component sensors to integrated devices. For example, several leading companies, (including Bosch, BEI Technologies, Invensense, and Honeywell) are focusing on MEMS-based inertial measurement systems to substitute non-silicon accelerometers and gyroscopes not only for automotive applications but also for a

wide range of other fields, and even companies such as Knowles and Akustica are merging silicon microphones into acoustic devices. Furthermore, companies oriented to consumer applications are pushing the demand for integrating MEMS devices into modules aimed at replacing optical auto-focus and zoom functions in mobile phones [4].

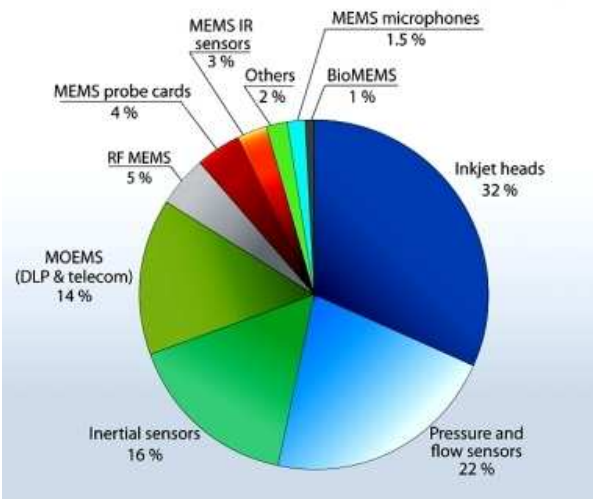


Figure 1-10: Global MEMS market 2006 (source WtC) [5].

As a result of this trend a high level of interest has arisen around MEMS technology from twofold directions: business one and technical one. On business side MEMS systems are proved to be increasingly attractive because multiple emerging markets for MEMS devices promise large financial gain and this potential for growth is confirmed by a growing amount of venture capital industry investment into MEMS based companies. On the other hand technical attractiveness is determined by multiple factors: the cost of the single sensor device is directly related to its size and, as it does for ICs, it scales down with the upcoming technologies.
The MEMS devices display excellent mechanical properties, which are guaranteed by an extremely pure crystalline structure. Silicon features a perfect fitting material for sensors devices thanks to the removal of mechanical fatigue and hysteresis phenomena. In single crystal form, silicon is an almost perfect Hookean [2] material, thus when it is flexed there is virtually no hysteresis and hence no consequent energy dissipation. Moreover silicon perfectly fits applications in which repeatable motions are required since it

suffers very little fatigue, featuring lifetimes in the range of billions to trillions of cycles without breaking. Its mechanical properties are comparable to steel (see table 1-2).

	Steel	Silicon	Units
Yield strength	< 4.2	7.0	1010 dyne/cm2
Young`s Modulus	2.1	1.9	1012 dyne/cm2
Density	7.9	2.3	Gram/cm3
Thermal conductivity	0.97	1.57	W/cm°C
Mechanical hysteresis	Yes	No	
Sensitivity to stress	Low	High	
Fabrication resolution	10	0.01	µm
Fatigue failures	Yes	No	

Table 1-2: Mechanical properties of steel versus silicon [2].

We can resume the main advantages as follows:

- Technology infrastructures for developing MEMS are already available and quite well established, comprising: batch-wafer processing, cutting-edge IC processing equipment, complicated diagnostic equipment, design and simulation tools and high-volume IC packaging technologies, even though new technology progresses always require a continuous research for new development and design strategies for facing the growing market demand.

- System on a chip can be created embedding conditioning electronic on the same silicon substrate (system on a chip) or at least on the same package (system on package) for

developing low-cost integrated mechanical, optical, and biological systems.

- The pool of educated silicon processing technologists is available even though the market demand requires always new forces.

- MEMS can be used as a packaging vehicle for nano devices, suggesting synergy with nanotechnology.

Furthermore there is now a widely shared vision among chip designers, suppliers, as well as original equipment manufacturers (OEMs): a clear commitment for improving the use of the technology in a wide range of market segments. In addition the growing popularity of novel features related to sensing introduction in the final user's applications is expected to spur the use of sensor system in particular fields such as consumer and automotive (e.g. the increasing demand for advanced safety systems as well as driver infotainment systems on chips in automobiles, see figure 1-11).

Figure 1-11: Sensor Systems in Automotive (source WtC) [4].

ii. MEMS automotive applications

Since MEMS devices got their start in the automotive industry in the 1960s, the motor vehicle industry has gradually introduced electronic technology to perform many of the control functions previously performed mechanically or by hydraulic actuators and today's high-end vehicles feature up to 100 different sensors

among which about 30 these are now MEMS, and the percentage is forecasted to grow. The market is composed by accelerometers, gyroscopes, pressure and flow sensors. Latest applications comprise IR sensors for air quality, micro-mirrors for displays. According to [2] the automotive segment is accounted for $1.6 billion, making this the second biggest opportunity after IT peripherals and inkjet print heads. By 2011 the market will top $2.2 billion, with a CAGR of roughly 7% (see figure 1-12).

Figure 1-12: Market for Automotive MEMS sensor (source wtc-consult).

Hereafter we depict some of the main sensing applications in the automotive sector:

- Active safety represents the most important requirement in modern vehicles. The MEMS accelerometers and gyroscopes are both sensors which can perfectly fit active safety requirements in the automotive domain [5]. The well known ABS (Anti-lock Braking System) prevents the wheels from locking while braking, Cornering Brake Control (CBC) performs stabilisation during partial braking while cornering. Traction control system (TCS) is designed to prevent loss of traction. Furthermore sensor systems are employed in the correction of drive trajectory: Electronic (Dynamic) Stability Control (ESC, ESP) compares the driver's intended direction to the vehicle's response via lateral acceleration, rotation (yaw) and individual wheel speeds. ESC then brakes individual front or rear wheels and/or reduces engine power as needed to get correct under steer or over steer. Some systems feature anti-collision detection like Adaptive

(Active, Intelligent) Cruise Control (ACC, ICC) which uses either a radar or laser setup to slow the vehicle when approaching another vehicle and Lane Departure Warning system (LDW) which warns the driver when the vehicle begins to move out of its lane.

- Intelligent Light Positioning is gaining relevance in high end cars and is expanding down to more market segments. MEMS sensors like accelerometer and gyroscope can lead to a new generation of head lights enhancing road illumination and guaranteeing safer driving conditions. Thanks to motion detection and assisted by GPS systems, the alignment of head light to various road conditions (e.g. asphalt, curves, uphill, downhill) and depending on vehicle condition (e.g. speed type pressure, suspensions, number of occupants) can be automatically performed.

- Intelligent Airbags care to soften impact for passengers during car crashes can also be efficiently performed. Since the airbag system must act at the right instance and also with the proper force toward the car occupants, the identification of type of collision, its direction and the g-force impact assume critical importance. The adoption of MEMS accelerometer, thanks to their high integration capability and accuracy, can lead to detection system of new generation replacing standard electromechanical system, achieving enhanced passenger care. Since the instant of the impact cannot be predicted in advance, it is extremely important to detect for each passenger the seat position and if in the crash the occupant is lifted from the seat. The MEMS accelerometer can determine the correct positioning of car occupants to dose the force of airbags bang.

- Vehicle Monitoring is devoted to check up the car condition to anticipate the detection of any malfunctioning. The tire correct condition can be determined through tire pressure sensors, and MEMS sensors, thanks to the compact size and high accuracy, embody optimal candidates. Furthermore the monitoring of machine vibrations can avoid excessive power consumption and accelerated wearing on bearings, seals and foundations. Vibrations can be detected by accelerometer systems for measuring vibrations frequency, amplitude (strength) and spectrum (signature) to identify the particular vibration.

- Satellite navigation systems in vehicles can determine the position of the car anywhere on the world by radio signals from Global Positioning System (GPS) satellites. Nevertheless, data from satellite is not sufficient to constantly determine the correct positioning since the satellite signal could not be always available due to shadowing by buildings and overpasses, especially in crowded urban areas. In this scenario, a dead reckoning GPS system can replace the navigation system continuing tracking movements during the time when satellite signals are not available. MEMS-based gyroscope and a magnetometer can path the motion direction and together with an accelerometer can implement complementary tracking system to GPS.

- Enhanced Antitheft System can take advantage of accelerometers and inclinometers to sense the inclination of the car or motorbike versus the ground. As a drag truck is used to steal a vehicle, when the car is lifted the accelerometer can notice the change in inclination, activating the alarm and all the related security systems.

1.4 MOEMS applications

Micro-Opto-ElectroMechanical systems represent a subset of the MEMS family that has been developed since the ’90s for fiber optics telecommunication applications [3]. However, the sudden crisis in 2001 has changed the landscape, as most of the companies developing or manufacturing optical MEMS for telecom have shut down. Historically, optical MEMS have been successfully used for TV and projection systems (this is the case of TI DLPs technology). Following the telecom downturn, some companies have succeeded to explore several new applications that are widespreading the use of optical MEMS. Despite the difficulties that global market has encountered in the last part of the 2008, MOEMS market has increased from 2003 to 2008 with an outstanding Compound Annual Grow Rate (CAGR) of more than 30% passing from 780 million dollar in 2003 to more than 3 billion dollar in 2008 as shown in figure 1-13.

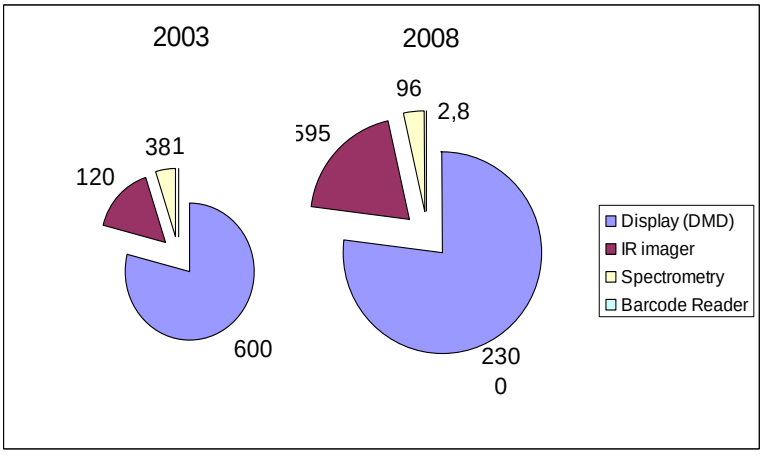


Figure 1-13: MOEMS Market grow from 2003 to 2008.

Actually the most important fields were MOEMS are employed include:

- Displays (DMD)
- Spectrometry
- IR imaging
- Barcode Readers
- Picoprojectors

i. Display (DMD)

Digital Micromirror Device (DMD) is a spatial light modulator developed at Texas Instruments that is the core of Digital Light Projection (DLP) technology, and was invented in 1987.
A DMD chip has on its surface several hundred thousand microscopic mirrors arranged in a rectangular array which correspond to the pixels in the image to be displayed [6]. The mirrors can be individually rotated ±10-12°, to an on or off state. In the on state, light from the projector bulb is reflected into the lens making the pixel appear bright on the screen. In the off state, the light is directed elsewhere (usually onto a heatsink), making the pixel appear dark.
To produce greyscales, the mirror is toggled on and off very quickly, and the ratio of on time to off time determines the shade produced (binary pulse-width modulation). Contemporary DMD chips can produce up to 1024 shades of gray.

The two main application of DLP systems are front projectors (small standalone projection units) and DLP rear projection television.
Projectors can be equipped with a single DMD chip or with three chips. The first solution employs a spinning colour wheel between the light source and the DMD. The colour wheel is usually divided into four sectors: the primary colours (red, green and blue) and an additional clear section to boost brightness. Since the clear sector reduces colour saturation, in some models it may be effectively disabled and in others it is omitted altogether. Some projectors may use additional colours (for example, yellow).
The DMD chip is synchronized with the rotating motion of the colour wheel so that the green component is displayed on the DMD when the green section of the colour wheel is in front of the lamp. The same is true for the red and blue sections. The red, green, and blue images are thus displayed sequentially at a sufficiently high rate that the observer sees a composite "full colour" image. In early models, this was one rotation per frame. Later models spin the wheel at two or three times the frame rate, and some also repeat the colour pattern twice around the wheel, meaning the sequence may be repeated up to six times per frame [3].
A three-chip DLP projector uses a prism to split light from the lamp, and each primary colour of light is then routed to its own DMD chip, then recombined and routed out through the lens. Three-chip DLP projectors can resolve finer gradations of shade and colour than one-chip projectors, because each colour has a longer time available to be modulated within each video frame; furthermore, there won't be any flicker or rainbow effect like with the single chip solution. Like three-tube CRT projectors, the optics for some three-chip DLP projectors must be carefully aligned. But it's more common to use a prism which makes it necessary for only one optic, instead of three, and therefore removes the problem of colour separation.

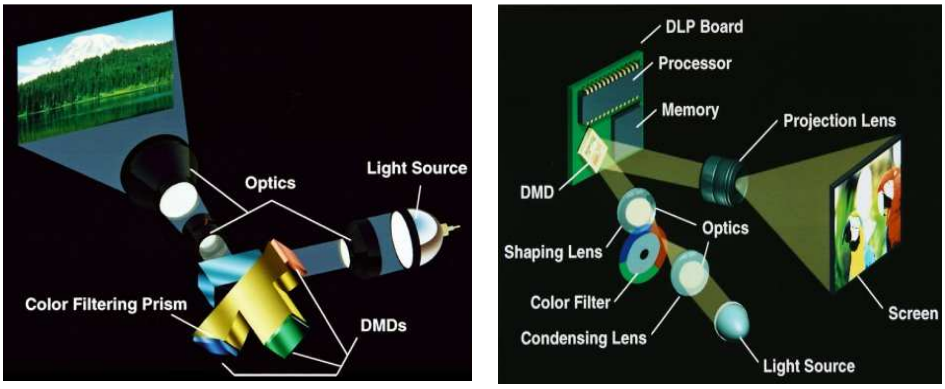


Figure 1-14 - 1-15: Triple DMD DLP projector and single DMD DLP projector.

The three-chip projectors used in movie theatres can produce 35 trillion colours, which many suggest is more than the human eye can detect. The human eye is suggested to be able to detect around 16 million colours, which is theoretically possible with the single chip solution. However, this high colour precision does not mean that DLP projectors are capable of displaying the entire gamut of colours we can distinguish (this is fundamentally impossible with any system composing colours by adding three constant base colours).

ii. Spectrometer

A spectrometer is an optical instrument used to measure properties of light over a specific portion of the electromagnetic spectrum, typically used in spectroscopic analysis to identify materials [7]. The variable measured is most often the light's intensity but could also, for instance, be the polarization state. The independent variable is usually the wavelength of the light, normally expressed as some fraction of a meter, but sometimes expressed as some unit directly proportional to the photon energy, such as wavenumber or electron volts, which has a reciprocal relationship to wavelength. A spectrometer is used in spectroscopy for producing spectral lines and measuring their wavelengths and intensities. Spectrometer is a term that is applied to instruments that operate over a very wide range of wavelengths, from gamma rays and X-rays into the far infrared [8]. If the region of interest is restricted to near the visible spectrum, the study is called spectrophotometry.

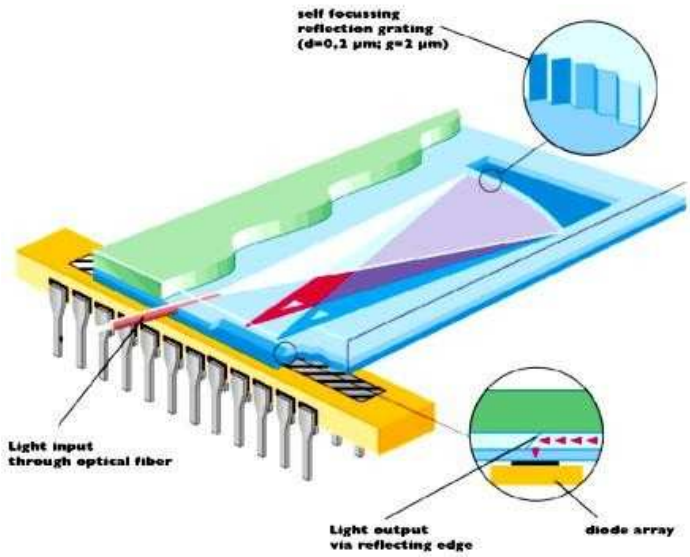


Figure 1.16: An example of MOEMS spectrometer.

By using the microspectrometer shown in figure 1-16 as key component, has been possible to develop an analytical apparatus for non-invasive, early detection of jaundice in new-born babies.
After placing the hand-held device on the skin of the baby's forehead, the measuring operation starts. The instrument exposes a small area of the skin to white light and measures the specific intensity of the reflection. The concentration of bilirubin in the blood can thus be determined exactly and within a very short time. The measurement is independent of both skin colour and the exact age of the babies. An example of this instrument is shown in figure 1-17.

Figure 1-17: Non-invasive Bilirubin detector based on MOEMS spectrometer.

iii. IR sensors

IR integrated sensors are also called InfraRed Focal Plane Array (IRFPA). IRFPAs are a subset of the active pixel sensor (APS) family. An APS is an image sensor consisting of an integrated circuit containing an array of pixel sensors, each pixel containing a photodetector and an active amplifier. There are many types of active pixel sensors including the CMOS APS used most commonly in cell phone cameras, web cameras and in some Digital Single-Lens Reflex Cameras. Such an image sensor is produced by a CMOS process (and is hence also known as a CMOS sensor), and has emerged as an alternative to charge-coupled device (CCD) imager sensors.
The term active pixel sensor was broadly defined by Eric Fossum in a 1993 paper [9].
Image sensor elements with in-pixel amplifiers were described by Noble in 1968 [10], by Chamberlain in 1969 [11], and by Weimer et al. in 1969 [12], at a time when passive-pixel sensors – that is, pixel sensors without their own amplifiers – were being investigated as a solid-state alternative to vacuum-tube imaging devices. The MOS passive-pixel sensor used just a simple switch in the pixel to read out the photodiode integrated charge [13]. The first IRFPA designs were able to operate only at cryogenic temperatures in the infrared spectrum. This devices were composed by two chip: one chip contain detector elements made of InGaAs or HgCdTe, and the other chip was typically made of silicon and was used to readout the photodetectors. The exact date of origin of these devices is classified, but they where in use from the mid 1980's only.
Due to the very low temperature needed, these type of IRFPA never reach the consumer market nor they were investigated for large-scale application. Almost ten years ago the first prototype of uncooled IRFPA where presented giving new opportunities to the IR field of applications. Compared to cooled technology, the uncooled detector offers many interesting advantages: high reliability and lower cost, whereas the performance is high enough for a lot of applications where the "targeting" range is relatively close to the sensor (typical range around 1km). Some examples are: thermography application, automotive and military, such as thermal weapon sight and low altitude Unmanned Aerial Vehicle (UAV) detection.
Uncooled IRFPA are based on an array of MOEMS used to measure the energy of incident electromagnetic radiation. In this way it is possible to detect variation in the range of tens of milliKelvin at 60 Hz [14]. Such sensors are widely employed for thermography,

predictive maintenance, security, medical imaging, night vision, veterinarian and fire fighting. An example is shown in figure 1-18.

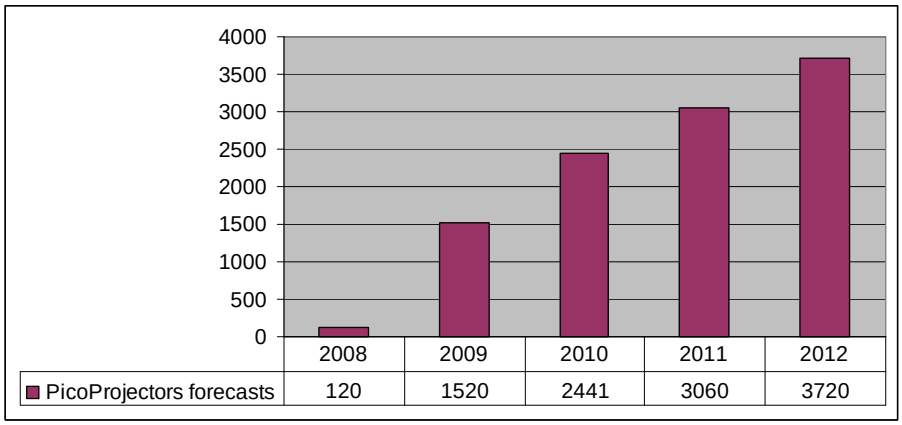
Figure 1-18: Using an IR sensor it is possible to detect people otherwise not visible at night.

iv. Barcode scanner

The bar code scanners are available in various types; the basic principle of all the types is to project light to the bar code to identify the width of each bar, basing on the quantity of reflected light [15][16][17]. This bar code scanning can be done by either of the following two methods. One of the method is such that a fine beam spot is sent perpendicularly to code bars one after one and the reflected light from each bar is scanned by a single photodetector element. The other method is to projecting light evenly to the bar code surface and scanning the reflected lights from the code bars simultaneously by a photodetector or CCD (character coupled device) image sensor composed of a plural photodetector elements provided correspondingly to the code bars. In both cases an optical system is needed to handle the scanning beam or the reflected light. Due to the size reduction and high integration of this system MOEMS are the best choice for this type of optical system.

v. Picoprojector

Today, the need for thinner TVs, portable electronics devices and more compact optical devices requires innovative optical technologies to shrink the light management module at the heart of many applications such as Rear Projection Televisions (RPTVs).
Mixing MOEMS technology with solid state lighting (LEDs, HBLEDs and/or laser diodes) is a new, unique solution to achieve a potential low cost and compact light engine. The successful development of a compact and low cost light engine will improve existing products (DLPRPTV) and drive new market such as picoprojectors or smaller head-up.
The aim of picoprojectors is to realize low size, high performance portable projectors for notebooks or palm PCs and or handheld devices, such as cell phones or digital cameras [18]. This is a very promising market, as it is possible to see from the forecasts. In fact, figure 1-19 shows that the market will raise to 3720 million dollar in 2012, with a CAGR of 135%. The companies predict that the first pocket-sized projectors, available in volume within the next two years, will probably be stand-alone accessories priced at $300 to $900 (consumer price and professional price) but the ultimate goal is to fit them inside handhelds. And with camera phone owners snapping photos by the thousands (manufacturers will ship an estimated 1 billion camera phones by 2008) a built-in projector that displays photos in larger formats could be a big draw for cellular customers (figure 1-20).



	2008	2009	2010	2011	2012
PicoProjectors forecasts	120	1520	2441	3060	3720

Figure 1-19: Picoprojectors market forecasts.

However mixing solid state lighting and MOEMS require innovative solutions mixing optics, thermal management, electrical power conversion, electronic drive circuitry. Although there are many

open technical issues to be solved regarding packaging, thermal management, cost/performance ratio, green laser lifetime and market access the first picoprojectors suitable for use in a mobile phone has been demonstrated by US firm Microvision at the Global press Summit Conference in San Francisco in April 2008.

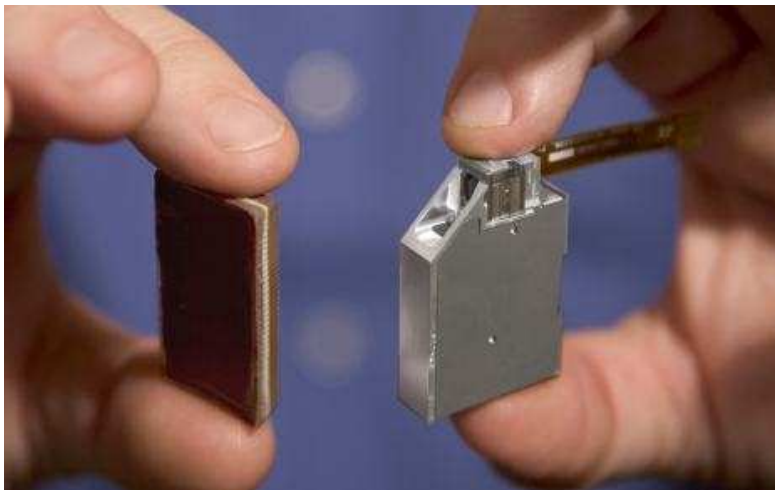


Figure 1-20: Microvision Picoprojector.

Chapter 2
THE PLATFORM BASED DESIGN APPROACH TO A SENSOR INTERFACE

2.1 Introduction

Complexity of SoC (System on a Chip) design, especially in sensor interfacing and conditioning applications, has been dramatically increased over the last years thanks to recent advances in integrated technology while time-to-market requirements has strongly decreased. Cost reduction and performance enhancement of sensors are pushing the introduction of new electronic applications to an increasing variety of fields ranging from monitoring of industrial processes to automotive.

The designer of electronic devices for sensing applications has to provide complex and effective sensor interfaces in a continuously evolving and competitive market. The critical aspects that have to be overcome to achieve final success reside in facing the latest technology facilities, exploiting the recent advances for designing high performance products which combine optimal features with high reliability, answering the market craving for short time to market. A key aspect is also represented by the safety and reliability features that a platform interface has to assure and the need for flexibility to guarantee successive upgrading. The design effort for achieving an optimized sensor interface (with regard to area, performances and low power) on one side and the market aggressive demand for low cost and short development cycle on the other, has lead to a different series of approaches tailored to the specific application.

2.2 Universal Sensor Interface

During last years, to save development time and reduce design risks, several solutions have been presented, among which the Universal Sensor Interface (USI) [5]. While a full custom ASIC requires considerably design efforts and features higher development costs (both time and money), a more generic and flexible sensor interface can match the market requirements by addressing several similar applications and reducing its costs with a longer production life. This single chip solution has the main advantage to be compatible with a wide range of sensors, but it not tended towards optimal solution for a target sensor. In figure 2-1 the leading idea of the universal sensor interface is described.

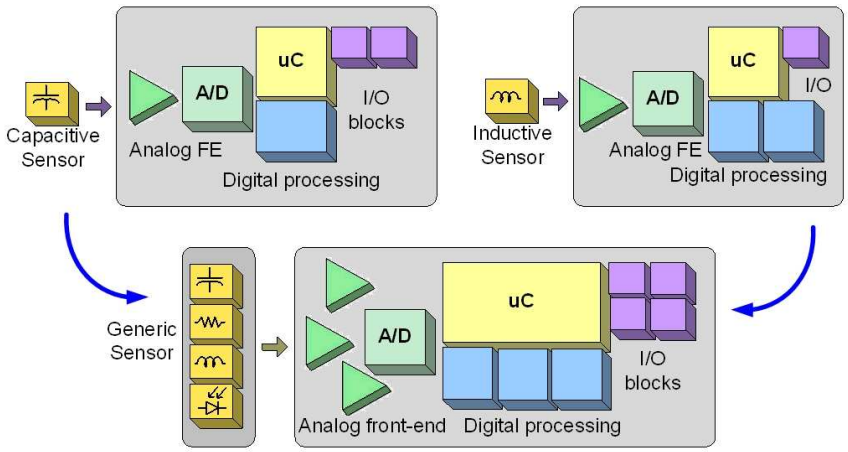


Figure 2-1: Building a Universal Sensor Interface

USI has as drawbacks high power consumption and area occupation, while it features not optimized performances if compared to a chip tailored for a target sensor.
The USI in [19] is implemented with high performance sensor signal acquisition stages, capable of acquiring different typologies of signals (e.g. capacitive, inductive, and resistive). The interface adopts an analog to digital converter based on voltage-to-period technique and processes the data acquired in the digital domain thanks to the presence of a microcontroller and a hardware DSP structure. This interface achieves considerable cost reduction by sharing evaluation resources between different acquisitions from sensors analog interfacing circuits and the actuators[20].
On the other hand, this system does not tend in the direction of any forecasting for a possible customization determined by specific sensor for specific sensor requests. The USI proposed result indeed

achieves good performances but not suitable for the strict requirements of demanding application fields like the automotive one.

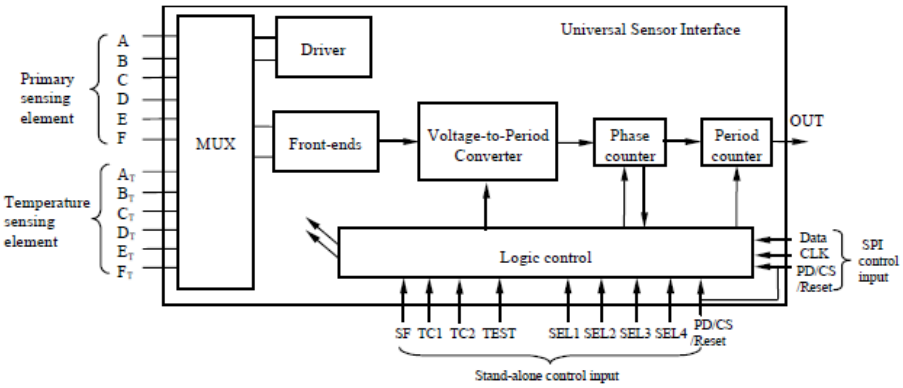


Figure 2-2: Block diagram of the USI [19].

In literature we can find other solutions such as the Universal Micro-Sensor Interface (UMSI) [21][22] which expands the capability of the USI circuits featuring a sort of sensor bus for connecting the sensor read-out channels to evaluation nodes and embedding standard interface for communication (UART, SPI). In addiction more UMSI can be connected together for achieving an easy implementation of a sensor network. However this approach has the drawback of providing not performing acquisition channel to answer the strict requirements of market demands especially in fields like industrial process monitoring and automotive and aerospace applications

The interfaces implemented in [23] represent an industrial solution for a wide spectrum of sensor applications: piezo-resistive, ceramic-thickfilm, steel-membrane-based (metal-thinfilm), strain-gauge, magneto-resistive bridge sensors. The solutions proposed in [24] refer to a generic analog conditioning channel suitable for more typologies of sensor and a digital architecture based on general purpose digital blocks handled by microcontroller. This work provide a good flexibility although can handle application which do not require a high degree of complex algorithm for sensor conditioning.

The mentioned approach displays the advantages of interfacing a wide class of sensors to be suitable for many different applications thanks to a little overhead in terms of added circuitry, but find its weak point in the sub-optimal architecture which can not guarantee excellent performances and answer the market demands for low power consumption and low area occupation.

2.3 Platform Based Design

The increasing complexity of integrated circuits has lead to a dramatic requested enhance for architectural analysis and design space exploration. The continuous progress of EDA (Electronic Design Automation) tools allows users to speed up the design process but can hardly handle the whole system complexity.
In literature we can find a series of approaches towards the integration of methodologies for achieving the complete design and verification of integrated circuits and to answer the market demand for sort development time. To handle the system complexity the most acknowledged approaches reside in the IP-Design and Reuse methodology [25][26] System Level Design [27][28], and above all Platform-Based Design approach [29]. All the above mentioned methodologies have been developed to deal with the key issues of modern ASIC design:

- Manufacturing cost: it depends mainly on the area size of the device, optimized by the development a dedicated architecture for a target application.

- NRE (Non-Recurrent Engineering) cost: it is related to the design itself and to the set of masks of the silicon foundry. The cost of masks is growing rapidly as going to reduced geometries. Moreover testing issues related to modern complex mixed signal ICs are becoming one of the major factor of cost for IC factories.

- Design cost: it is dramatically rising due to the increased complexity of the new ICs and the challenges caused by distributed physical effects for deep sub-micron technologies. Furthermore design productivity is not keeping the rush with respect to the technology advances making almost impossible to develop the new products facing the increasing complexity and, at the same time, matching the reduced time to market constraints.

The platform based methodology [30] defines the design of electronic systems from concept to implementation as a sequence of different layer of abstractions in the design flow: each layer can be considered as a platform for which the underlying, subsequent design flow steps are abstracted [31] (see figure 2-3).
Platform based design exploits rigorously and exhaustively the concepts of design reuse, of design flexibility (the blocks are

programmable and are specified at low level), and of correct-by-construction assembly, since modules are pre-characterized and pre-designed (not complete full-custom design). Therefore the platform based methodology features a good cope with manufacturing, NRE and design costs, with little design performance loss.

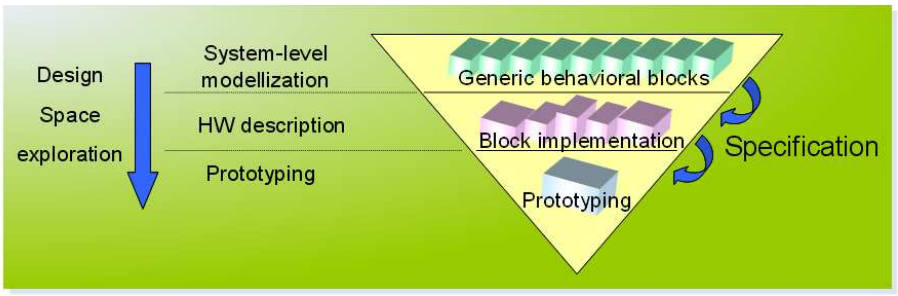


Figure 2-3: System platform layer and design flow. From system level modeling to prototyping through different layers

For embedded system designs, a platform is composed by a library of (preferably configurable) pre-implemented modules, interfaces, services and software routines that can be assembled to generate a design at that level of abstraction. Each module is provided with a characterization regarding performance and supported features. A platform instance is a set of modules selected from library according to the constraints and to the needs specified by the target specifications. Hence this methodology can quickly fulfill a generic class of applications.
Each platform layer can models the upper layers of the platform and, in addition, it is possible to estimate performance and physical attributes of lower layers in the design flow.
Platform-based designs found the most important achievement in the definition of the layers, defining the design space exploration through regular structures, resulting into the elimination of large loops of re-design.
On the other hand, a critical pace of the platform-based design process is the definition of intermediate platforms to support predictability, to guarantee an higher-level optimization and a design space exploration at an high level of abstraction, but conditioning the whole architecture development.

2.4 Limitations of Platform Based Design flow

The Platform Based methodology represents a powerful strategy for managing complex design with strict constraints, subject to development time determined by industrial aggressive markets. However this approach features some weak points with respect to thigh designs imposed by particular application fields, (e.g. critical industrial, aerospace, automotive) that have to be resolved in order to answer the market demand for low cost, low area, high reliability and high performance products.
The key issues of the platform based design are inherent to the architectural design exploration at high design level. The architectural decisions have to be taken with care since all the design will be critically affected by these choices not only for general architecture but also for preliminary block specifications and partitioning. This critical aspect recurs also in all top-down design approaches. Therefore comprehensive study and exhaustive simulations have to be performed at this highest level of abstraction: the system has to be modelled and even a target sensor has to be taken into account for getting the best possible architecture for the conditioning sensor interface. The critical aspects reside in the unavoidable lack of details by which the system level is affected and little inaccuracies can result in final wrong conditioning chain implementation and in poor specifications for critical blocks. Another killing issue for this approach is determined by unforeseen phenomena in the first level of the design phase which came to light only at the final stage of the design process in the prototyping phase.
All these design issues can determine to a final prototype affected by significant design inaccuracy leading to necessary re-design cycles with a consequent rising of costs and time to market inflation.
Likewise, the missing information details at top system level can lead to a device whose physical implementation does not perfectly match the specification required at the first stage of the design phase, this may occurs, for example, from not accurate simulations (due to the complexity of the product) for performances extraction.
At the extreme consequences, the top-down approach is demonstrated to be critical for all those platform customizations which would require a dedicated feasibility study.

2.5 SD400

The requirement for developing high performances sensor interfaces with optimal area occupation and low power consumption has pushed towards the research of a new approach for developing platform design methodologies: a new strategy has been developed by the University of Pisa in collaboration with SensorDynamics AG [31][32].
The SD400 is the first platform developed following the Intelligent Sensor InterFace (ISIF) approach. The ISIF approach has been conceived to overcome the issues related to top-down design methodologies.
ISIF provides a set of programmable analog and digital IPs directly on silicon that have been developed taking into account the wide-ranging signal conditioning electronics for different sensors. These IPs feature flexible interconnection structure and can be empowered by software routines which can substitute hardware dedicated blocks by emulating the hardware IPs. With the ISIF platform the optimum architecture can easily be derived from direct evaluation of the target sensor connecting the sensor itself to the platform and performing the analysis directly on silicon. Adopting this approach a various typologies of applications can be easily evaluated with a consequent speeding-up of the design space exploration phase.
Moreover this approach with the ISIF platform for performing the design space exploration does not exclude a traditional approach to run in parallel: MATLAB™ modelling and system level simulations can be performed to achieve a further investigation and possible cross check between the two approaches for system design refinement.
The most important concept that resides in ISIF design flow is represented by the drastic reduction of time needed for performing the design architectural space exploration, which in a traditional platform based design should have been carried out with the utmost care in a time consuming and error prone process. In place of long time simulations, with ISIF the application can be directly evaluated on the real silicon (thus a prototype of the target application is indeed possible before its actual design). Furthermore accurate feedback information coming from IPs already on silicon can be of crucial importance, since we can observe phenomena impossible to be foreseen in a traditional design simulation. Also a correct evaluation of the real parasitic elements can be developed, allowing designers to reach a really

accurate estimation of the performance of the device for an exact match with the specifications of the final product.

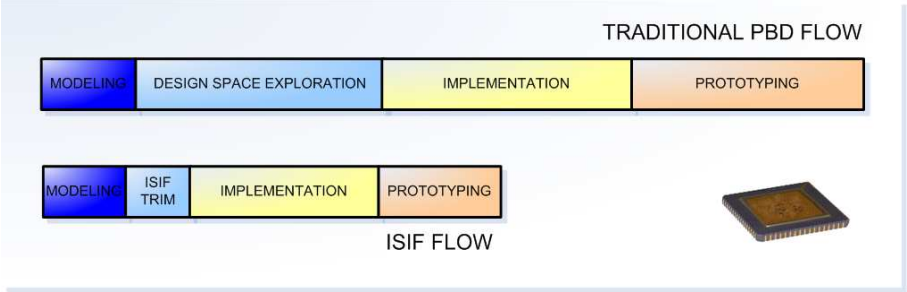


Figure 2-4: comparison between design time for a traditional Platform Based and the ISIF flow.

The key aspect to achieve the ISIF concept reside in a twofold feature: the particular care for providing high performance IPs both for analog read-out stage and for digital conditioning path and the extreme flexibility of the whole structure. In fact not only each single IP can be fully configured but also the routing and the connection map among different IPs can be modified and adjusted, including also the possibility to emulate physical IPs with a library of software routines which perform the same functionalities with the right timing and the necessary data-paths limitations. Although ISIF presents some similarities with the Universal Sensor Interface (as it aims to conditioning a wide class of sensors) described in section 2.2, it is not tended towards a final product for any target application, its aim is indeed to provide designers a powerful and complete interface for a quick development of a final product with reduced risks and short development time in order to achieve the highest performances and the lowest overheads. This fact entails that only the required analog/digital components are integrated onto the final silicon for production, resulting in minimized area and power overheads. ISIF IPs are in fact tailored not for area optimization but to implement the platform based design approach keeping the configurability options as wide as possible.
In this way the architecture space exploration can be rapidly carried out, reaching a prototype of the target architecture by simple acquiring the signal by an analog conditioning channel trimming the conditioning path with the desired analog IPs (it is possible also to skip some IPs) and then apply complex and ad-hoc algorithm thanks to the hardware DSP structure and to the emulation of software IPs. The target sensor can be driven by

several typologies of DAC driver in order to apply a proper feedback implementation.

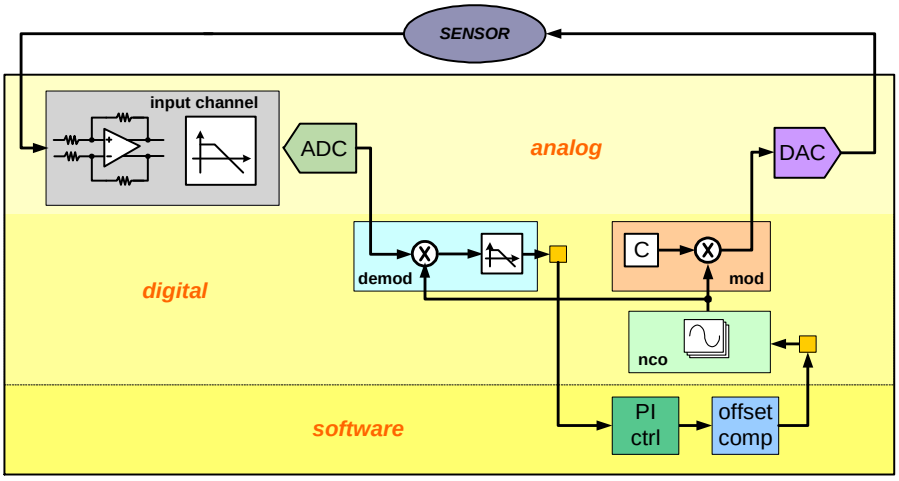


Figure 2-5: example of partitioning of a DSP chain within ISIF platform between analog, digital and software processing blocks.

ISIF platform has been studied to provide an interface for capacitive and resistive sensors, allowing measurements of voltages and low currents and many other applications. In the following paragraph, the platform will be presented.
In figure 2-6 ISIF structure is depicted: an analog front end featuring a wide range of IPs for sensor signal acquisition, driving and basic analog conditioning such as DACs, ADCs, amplifiers, filters, and current/voltage sources; a digital DSP section based on LEON core; some peripherals for communication with external devices, memories and buses (AMBA APB/AHB). ISIF platform has been developed by SensorDynamics AG in collaboration with Pisa University.

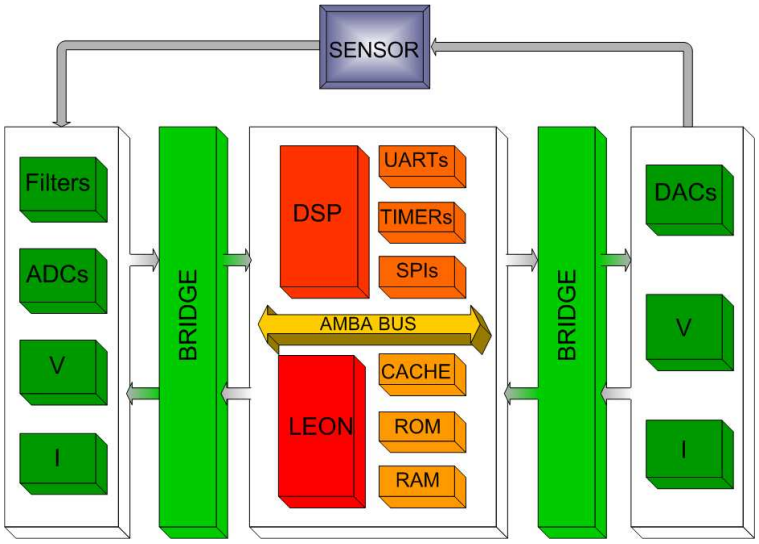


Figure 2-6: ISIF block diagram.

i. Analog section

ISIF analog section features 4 dedicated input channels for sensor signal acquisition (see figure 2-7). The readout stage is composed by an operational amplifier that can be programmed to implement a charge amplifier, a trans-resistive stage or an instrument amplifier, covering a wide range of sensor typologies. Further stages perform signal analog processing, signal recovery, and low-pass filtering for anti-aliasing purpose. Eventually the signal is converted by a 16 bits Sigma Delta ADC. Service circuitries provide voltage/current references, and oscillation for clock generation.
The sensor driving stage of the platform is provided by set of configurable 12 bit and 10 bit thermometer DACs. The driving section has been tailored also for creating sinusoidal signals needed for driving a generic sensor. The sine wave is generated by a DAC to create a digitalized wave which can be afterwards filtered with a low pass filter in order to get rid of the spurious harmonic generated by the quantization procedure. DAC references and low pass filter gain can be modified for amplitude and offset selection.
The bias section is composed by two regulators, one for the analog 5V supply and one for the 3.3V supply of the digital section, by a bias current generator (developed by a Proportional-To-Absolute-Temperature) and a current reference.

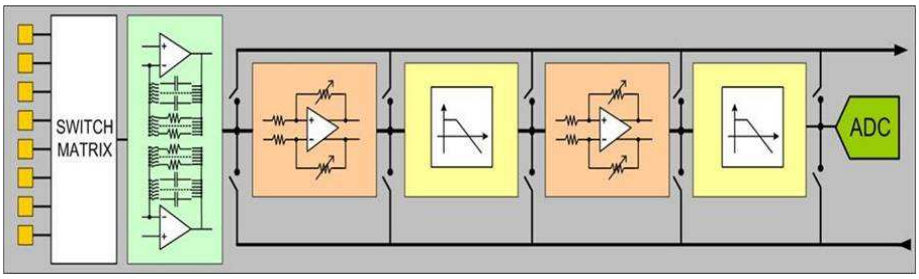


Figure 2-7: ISIF input channel.

An input/output test bus is provided to supply stimuli and to probe output signals for each block: the test bus represents a key feature for an effective and quick debug of the signal conditioning path.
A peculiarity of ISIF analog section is the design accurateness for improving the noise margin. The biasing structure is composed by separated analog and digital power to minimize noise couplings and particular attention has been applied to the design of the analog IPs that perform sensor signal readout (which is the most critical operation for the sensitivity of the whole system).
To improve the noise margin, this system features also a JTAG-like approach to handle the digital bits used for analog block configurations, guaranteeing safe communications between digital and analog sections since programming is performed by shifting the configuration bits through shift registers, to overcome clock skew issues.

ii. Digital hardware section

The digital hardware section is based on the LEON core CPU, with related peripherals and dedicated IPs for digital signal processing (see figure 2-8).
LEON core is a 32-bit RISC SPARC-V8 compliant architecture conforming to the IEEE-1754, which features hardware multiplier and divider, interrupt controller, timers, watchdog and memories (ROM, RAM and data/instruction caches); LEON core is freely distributed by European Space Agency under LGPL license, together with standard peripherals for communication with external devices (UARTs, SPIs), and buses (AMBA APB/AHB).
The digital signal processing section is composed by dedicated IPs optimized for low power consumption, comprising modulator and channel demodulators, 6 DAC controllers, filters (FIR and IIR) and a Numerical Controlled Oscillator (NCO) capable of providing up to 16 different sine waves with selectable phase with 3 different frequencies.

These IPs feature a flexible interconnection architecture: they are hardware interconnected but they also can be accessed at their input/output by software, allowing the designer to implement complex and ad hoc algorithms for the target sensor exploiting the high configurability of DSP section and LEON CPU potentiality. As example, a digital PLL has been fully implemented and tested on a fast prototyping board [32].

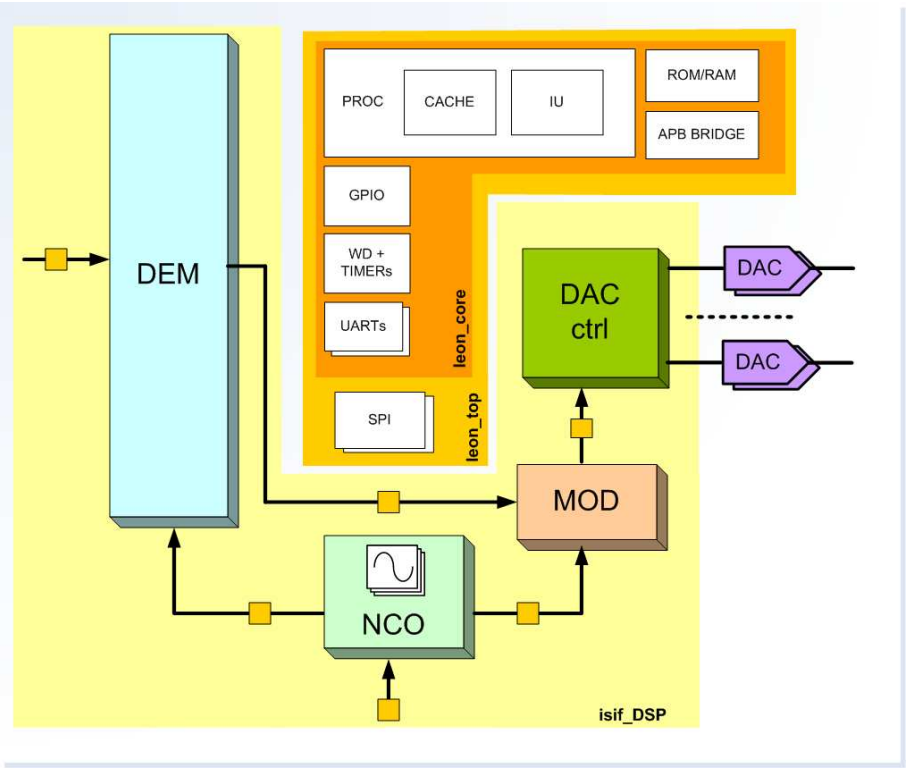


Figure 2-8: ISIF digital section.

LEON processor is involved in system monitoring. It manages signal processing and handles the communication with external devices (such as a PC during the prototyping phase) through available interfaces. The core part of the software is included in ROM (boot and few utility functions) and the functional routines can be downloaded at the start-up phase via UART, or can be stored in an external SPI EEPROM to be directly downloaded ate every boot. The additional EEPROM can hold different kind of software to be downloaded in order to speed up trimming procedures for achieving an optimized trimming phase, moreover measurements data can be stored to log results.

By using firmware routines the designer can modify interconnections between physical IPs and general settings of each analog and digital IP for free exploration of design space in the investigation for optimal conditioning architecture. In addiction, firmware utilities can handle the communication with external devices (for debug, monitoring).

iii. Software section

The industrial requirements are pushing towards hardware solutions, especially for safety applications, but, on the other hand, digital IPs require detailed and exhaustive analysis to guarantee complete reliability and proper parameter settings, in order to achieve high performances with reasonable area (reduced number of trimming bits). Furthermore the presence of non-linearities and of parasitic elements, often invalidate the design exploration making a right-first-time silicon difficult to achieve.
To meet these requirements ISIF platform includes a library of software peripherals (e.g. filters, controllers) with an exact matching with hardware devices. The LEON CPU, thanks to its advanced signal processing features, guarantees high flexibility and low computational power for real-time software IPs implementation.
The most common functionalities, which are not physically implemented in the ISIF platform, are modelled by software routines (with the same behaviour of the original DSP library IPs). The DSP software environment features data acquisition from the hardware digital IPs by routines, and inputs data back in further hardware IPs after elaboration just as the data processing was completely hardware-implemented.
These features help the designers to carry on a quick and exhaustive design space exploration changing analog settings, interconnecting digital IPs and even instantiating new ones to find the fittest solution in interfacing a target sensor, both in term of area and performances.
It is worth noticing that ISIF platform is not tended towards a solution with best performances but aims to provide an accurate emulation of a complete hardware interface optimized for the target sensor. In the final ASIC device, software routines can be quickly replaced by corresponding hardware IPs with low risks and costs for redesign, minimizing the time to market.

2.6 SD400 physical implementation

SD400 platform has been implemented in a 0.35 μm Bipolar CMOS DMOS (BCD6) technology to perform exhaustive tests on single IP and to check the correct functionality of platform configurations for particular industrial applications.
The main problem in physical implementation has been the analog layout synthesis and the top assembly. A way for speeding up and releasing physical implementation and prototyping phase has been achieved in ISIF platform adopting a modular approach also at the layout level.
Each module is designed and afterward implemented to perform a particular function in the whole sensor interface with the requirements picked-up directly from the platform. An interface for a particular class of sensors, can be designed applying only minor changes to fit the final implementation. However, if necessary, area occupation can be reduced simply cutting a part of the digital programmability which is no more useful since the single cell can be optimized for the target application.
Figure 2-9 shows the physical implementation of the ISIF platform while in figure 2-10 the final version of ASIC layout is depicted. The whole chip area occupation amounts to 72 mm^2.

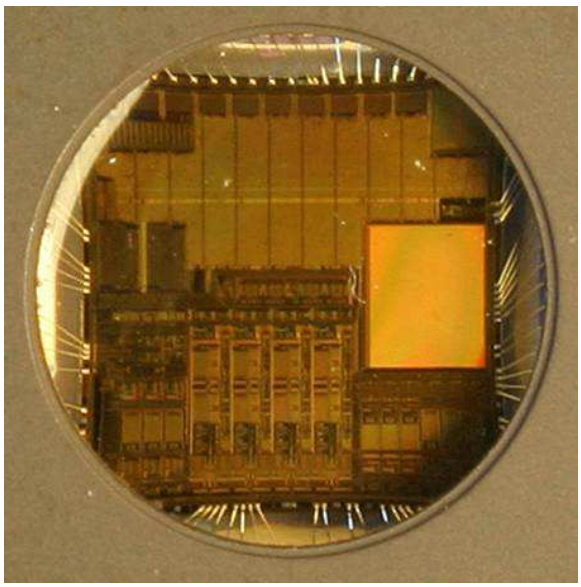


Figure 2-9: SD400 Physical implementation.

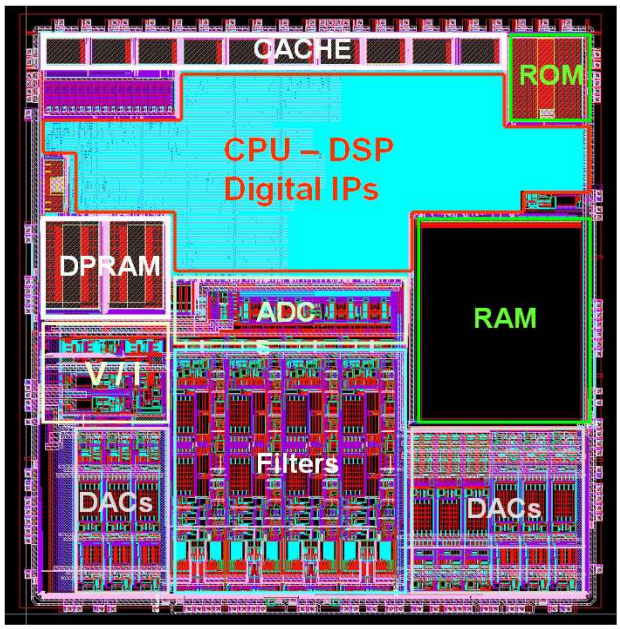


Figure 2-10: SD400 Layout.

2.7 Limitations of SD400

While the ISIF approach results as a good way to overcome the issues related to top-down design methodologies, the SD400 suffers of some limitations mainly due to the technology chosen.
The BCD6 technology has been used because of its integration of bipolar, CMOS and DMOS devices [33]. This feature has caused a degradation of the performance that mainly affected the digital section.
When the SD400 was has been designed, the BCD6 technology was the only one available to grant this kind of integration. Nowadays a new BCD technology in 0.18 μm is emerging and it provides the possibility to realize a more performing interface [8].
The introduction of a new technology could allow us to overcome of many of the limitations of the SD400. First of all, it is possible to integrate a more performing digital section, with a more powerful processor. Then, for the analog section, it is possible to introduce new input and output channels, focused on the emerging MEMS and MOEMS technologies, which have more strictly constraints.
In fact, while the SD400 can be employed to interface with a wide range of sensors, from inertial ones (like accelerometers and

gyroscopes) to flow sensors [9][10][11][12][31][32], it can't drive some kind of MOEMS which can require higher frequencies at higher driving voltages than our platform is able to handle.
From the experience inherited from the SD400, a new platform in BCD8 technology has been designed, the SD4k.

2.8 The SD4k

As previously explained, the SD4k was conceived in order to overcome the main limitations of the SD400, implementing a new technology which allows the designer to integrate a more flexible structure.
The main changes in the SD4k are:

- A greater number of analog input channels
- A greater number of output channels that will be able to handle high voltage or high speed actuation
- A new processor
- An higher performances DSP chain for sensors close loop control
- A fast embedded memory, able to store high quantity of data
- A fast and flexible interface to connect the SD4k with an external FPGA

Our first test bench for this platform will be the realization of a complete projection system, featuring a laser and a scanning Micromirror.

Chapter 3
SD4K PLATFORM

3.1 Description and Block Diagram

As previously stated, the SD4k inherits the ISIF design methodology from SD400 and share the same concepts of the previous platform: high flexibility in order to fast prototype state-of-art sensors. However, due to the twist introduced by the new technology, it is also possible to increase both digital and analog sections of the platform, allowing the SD4k to handle not only sensors but also complex environment used for the application, like the driving of a micromirror coupled with a laser-based projection system.
Obviously a platform it is not appreciable by the market, due to the great amount of area occupied by structures not relevant for the application. One of the aims of the SD4k is to prove the efficiency of the algorithm proposed to design complex systems, in order to target a tailored application specific integrated circuit that will be able to handle the system in the same way the SD4k has been able. The policy of IP reuse grants not only minimum development time for the tailored ASIC, but also enhance the probability of first silicon success, due to the extensive tests performed by the SD4k on the application [5][34].
This flexibility must be guaranteed both in analog and digital sections. In the first a great amount of switch, capacitance, resistance and multiplexer has been introduced, trying to foresee the possible configurations that will be need. For the digital section a powerful processor of the ARM 9 family has been chosen, coupled with an hardware structure for the phase locking loop of the micromirror resonance frequencies. The loop is for the great part in hardware but also has a software proportional-integral

controller. This grants high flexibility to the PLL, allowing a change in the controller parameters at run-time, following application and environment constraints.

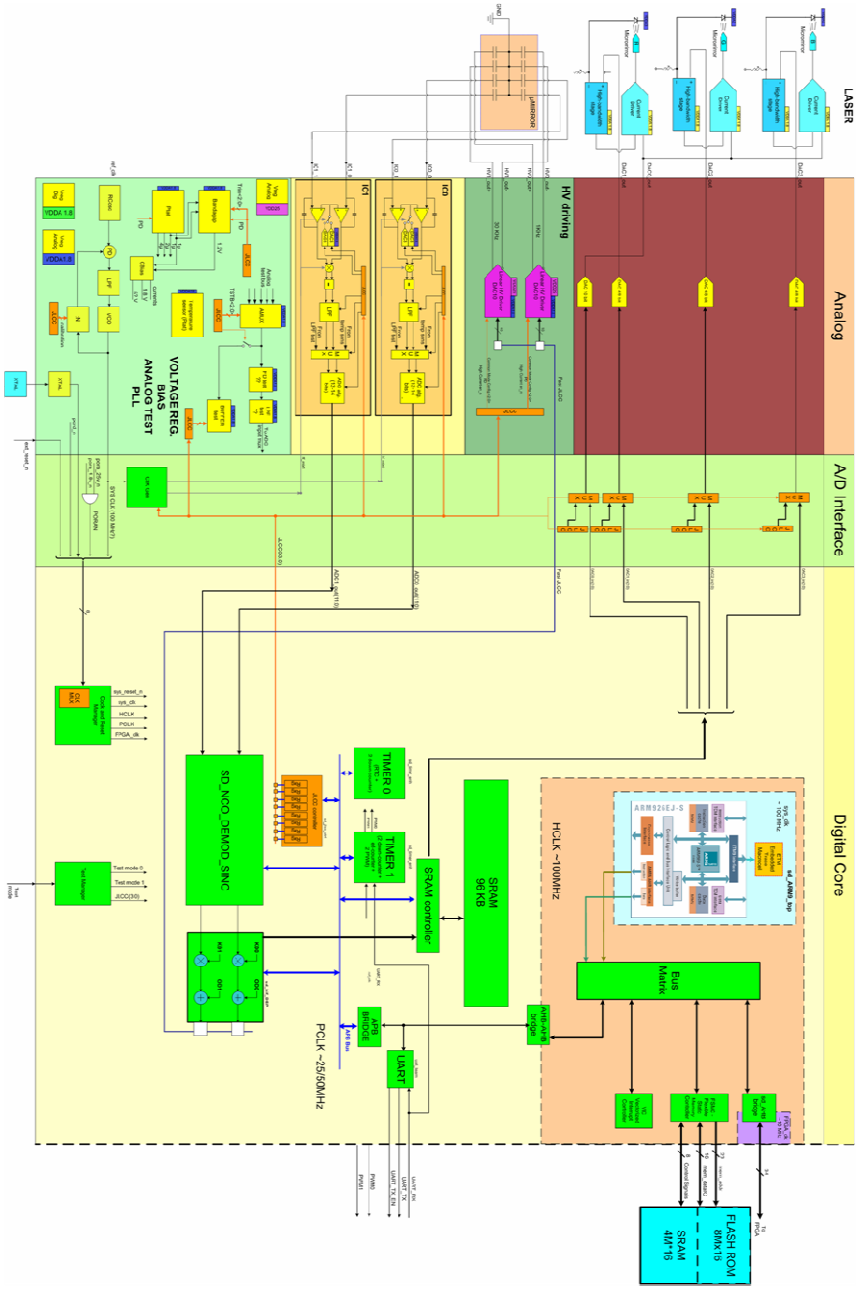


Figure 3-1: SD4k Simplified Block Diagram

Figure 3-1 shows a simplified Block diagram of SD4k, highlighting the different sections and internal division. The analog section (on the left of the figure) is divided into four sub-sections, from top to bottom:

- A low power and high speed output section, featuring three high speed output channels, which in our application are dedicated to the laser driving.
- A high voltage output section, used to driving MOEMS or MEMS with voltages up to 30 Volts and frequencies up to 100 kHz.
- The input channel section, used to sense the capacitance variation.
- An auxiliary section, which contains regulators, temperature sensor, clock generator, test structures, etc.

The central section is the Analog/Digital Interface, which contains the JTAG-like test structures and the clock generator for the input and output channels.
The digital section is divided in a high speed section, where the ARM9, the external memory controller and other high speed IPs reside and a low speed section, for the APB and all the peripherals connected to that bus. The decision to put an IP on a low or high speed bandwidth comes from its requirements and from its use in the application. The system study shows that the hardware involved in the phase locking loop of the resonance frequency of the mirror does not need an high frequency (around 100 MHz), so, to reduce power dissipation and design complexity this part has been moved on the APB bus where a lower frequency (selectable among 25 and 50 MHz) is used. On the other hand, the ARM9 high performances allowed us to feed it with a 100 MHz clock to implement heavy software routines up to a little operating system, like a Real-Time Linux [35].

3.2 Overview of Analog section

The analog section is composed by two fully differential input channels for signal acquisition, with a programmable gain from 2.78 to 121, bandwidth of 25 KHz, and a common mode input range of 0.2V-2.2V with maximum differential input of ±300mV.

Furthermore each channel has its own bandgap that can be trimmed (see figure 3-2).

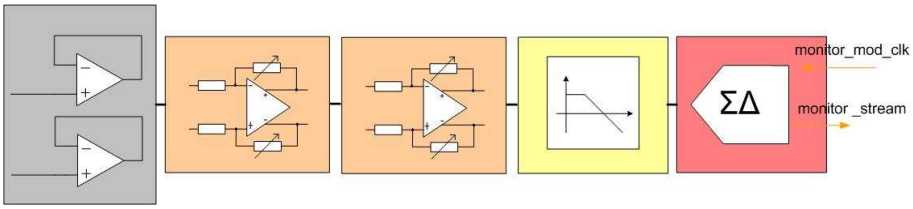


Figure 3-2: Input channel

One of the aims of this platform is to project a QVGA image with full colour option and high level of brightness and contrast. The implementation of a QVGA format implies many important specifications. An acceptable QVGA laser based system must guarantee at least 50 frame/sec. Consequently pixels are drawn each 65 ns (16 MHz). Since pixel generation must be done in combinations with many other routines such as video memory access, laser driving and control, a system clock of 100 MHz is mandatory. Moreover, full colour option implies that the platform must provide control for Red, Green and Blue (RGB) laser sources with a proper analog feedback control to correctly trim the optical power for pixel generation. Since the average clock for drawing a pixel is 16 MHz, the analog laser control system band must be one order bigger (160 MHz) to guarantee high quality video projection.
In addition to the high speed RGB laser drivers, the analog platform will include many IPs such as two 1.8V voltage regulators for the digital and for the analog section, DACs, ADCs and bias blocks (bandgap and PTAT). Besides, the system must provide ad-hoc actuation and sensing for a two-axis electrostatically actuated scanning micromirrors used to project RGB laser beams on the screen. This type of MOEMS requires high voltage driving up to 20 V while scan angle detection (sensing) is not strictly necessary to drive the mirror. Anyway the platform must include an analog readout channel to sense the capacitance variations due to the mechanical deflection of the two micromirror axis in order to implement a Phase Locked Loop (PLL) control necessary to achieve high quality display projection.

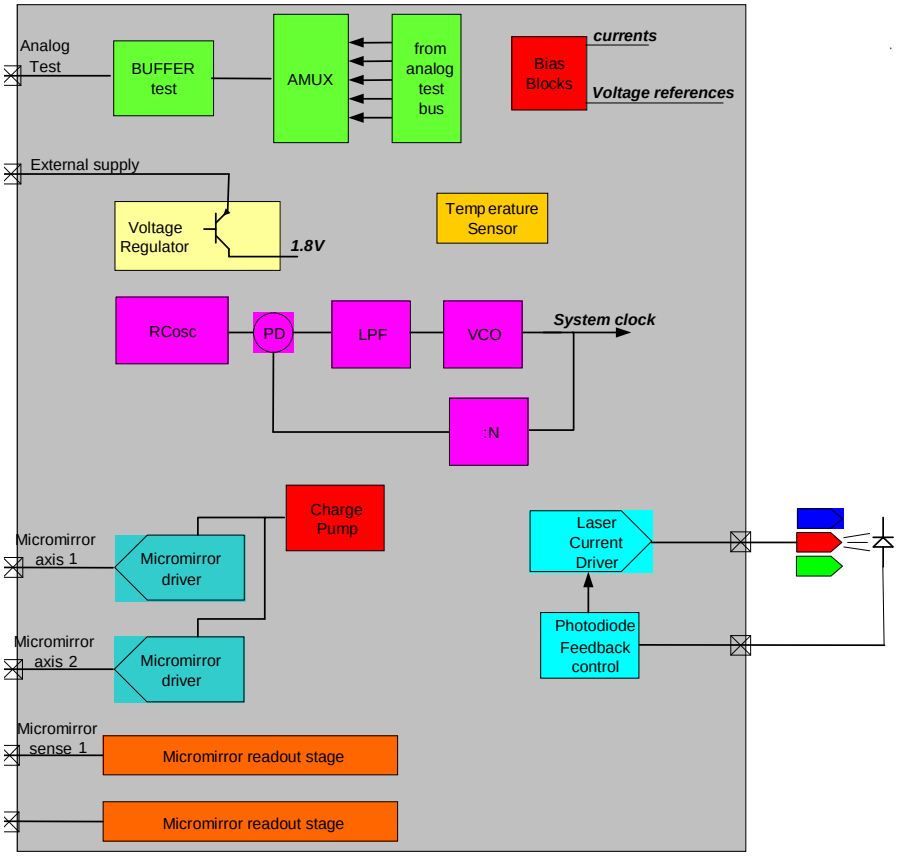


Figure 3-3: Simplified Block Diagram of the analog section

The analog section (figure 3-3) will be designed following the design for testability approach already used for the previous version of the platform: analog test buses will grant accessibility at the input and at the output of each block for characterization and debug purpose. Moreover a JTAG-like approach allows complete programmability of the analog blocks in order to exploit platform potentiality and flexibility.

3.3 Overview of ARM9 section

High speed and a high level of computation require a powerful processor. For the new platform the ARM926EJ-S has been chosen [36]. It features a 32-bit RISC CPU, flexible size instruction and data cache, memory management unit and separate instruction

and data AMBA AHB interfaces. The processor is about 250 kgates and has to be run at 100 MHz as previously underlined.
The ARM processor features an optional but very interesting IP called Embedded Trace Macrocell (ETM) whose purpose is to trace in real-time the CPU activities for debug purpose [37]. It occupies about 40 Kgates (< 1 mm^2) and requires about 15 pins but it is quite essential in a platform to have a powerful debug and trace system.
If an Operating System must be inserted there is a need for an external memory containing it. A little OS requires about 4 Mbyte of RAM while an 8 bit QVGA video system needs about 80 Kbytes.
For our applications it is important to remark how some of the features implemented by the ARM926 will affect the overall performances of the system.
First of all the ETM will grant a real-time debug of the firmware and software running on the processor. This will be very useful during the debug of the platform and of the application but at the cost of a minimum area increasing.
The ARM implements a Harvard architecture to separate instruction and data bus, in order to speed up operation and prevent CPU stalling while waiting instructions. Due to the higher speed of the processor in respect of the typical memory access time, two cache memories and their memory management units (MMU) are integrated with the CPU, allowing the download of the page of the external memory where the instructions or data requested reside.
The ARM 926 handles also a double master AHB Lite controller, to manage the instruction and data buses independently [38].
The ARM926 uses AHB Lite protocol that is a reduced version of the AMBA AHB. The AHB Lite is a multi-layer single master high speed high bandwidth protocol; the choice to drop the multimaster feature from the AHB protocol has reduced drastically the complexity of both master and slave IP and has introduce some arbitration structures that are used only to control those IP that are common to the various layer, such as the memory controller.
Figure 3-4 shows the block diagram of the ARM processor, highlighting the Harvard architecture, with the separate cache structures and the doubled AHB Lite master outputs

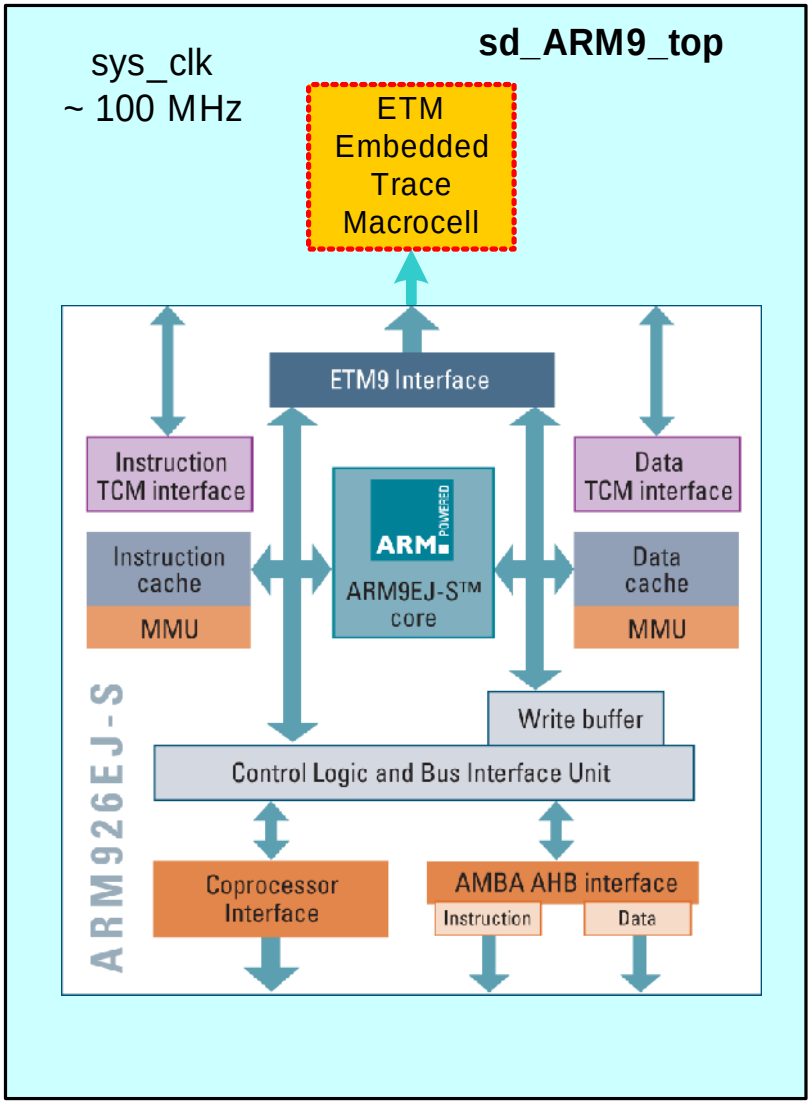


Figure 3-4: Simplified Block Diagram of the ARM core

3.4 Analysis of Digital section

As previously stated not all the system needs to be feed by a high speed clock around 100 MHz. Great part of the digital system can work at a slower frequency, so a bridge between the more performing AHB bridge and the APB is introduced, allowing some IP to reside on the latter bus [39].

First of all, the SD4k must provide quite all the digital hardware IPs integrated in the native ISIF system to maintain the old application space and to exploit all its demonstrated powerful capabilities even for the platform system:

- UART communication;
- modulators, demodulators and NCO necessary to implement a closed loop control on the micromirror;
- Timer and Watchdog;
- Accessibility at the input and at the output of each IPs;
- Added to this structure the system requires also a RGB laser video controller to correctly interface the high-speed analog laser driver for the laser projection. This IP will be highly programmable, as requested by the platform approach: the number of bits for each pixel will be programmable between 8 and 16; the clock speed could be adjusted to meet QVGA constraint;

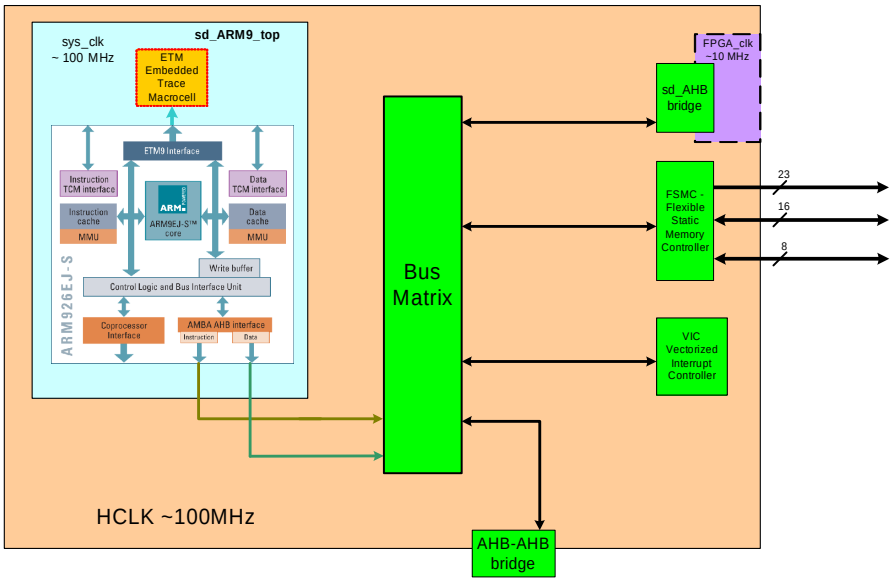


Figure 3-5: High Speed structures of the digital section of the SD4k

Figure 3-5 shows the structures fed by the high frequency clock, it comprehend the Vectored Interrupt Controller (VIC), the Flexible Static Memory Controller (FSMC) and the AHB to FPGA bridge.
The VIC provides a software interface to the interrupt system [40]. In a system with an interrupt controller, software must determine the source that is requesting service and where its service routine is loaded. A VIC does both of these in hardware. It supplies the starting address, or vector address, of the service routine corresponding to the highest priority requesting interrupt source. This IP is very useful to enhance the performance of the software when an interrupt is requested and it is a fundamental to equip the SD4k of an operating system.
The Flexible Static Memory Controller is an AHB-compliant memory controller able to interface a wide range of memories, like SRAM, NOR and NAND flash and cellular RAM. With a single controller it is possible to access to various type of memories reducing the area occupation and the pinout of the system. This comes at the cost of some latency introduced when both instruction and data bus tries to access to the external memory. In this case the Bus Matrix (highlighted in figure 3-5) allows the access following the priority imposed by design.
The AHB to FPGA bridge is an IP designed to transmit data from the processor to an external FPGA at a lower frequency (around 10 MHz) [41]. The utility, feature and trade-offs of this IP will be treated in more detail later in this section.
Figure 3-6 shows the IPs that reside on the APB bridge. Apart from the typical structure like UART and timers we can see the PLL chain: demod, NCO and modulator. The latter receive inputs from the NCO but also from the firmware running on the processor, realizing a mixed hardware/software PLL as we have discussed above.
The SRAM on this clock domain contains information about the image to be projected, in fact the controller can be fed with information from the processor or directly from the modulator, allowing the memory to be read exactly in the same way as the mirror is driven (except for a phase shift).
The I2C/SPI is a communication IP that has been developed to allow a greater flexibility among the serial protocols, reducing at the same time the area occupation [42]. Also about this IP there is a deeper description below.
The orange IP are those that are in some way related to the test of the system. The JTAG-like controller handles all the JTAG chains of the system, allowing the processor to vary the parameter of the analog front-end at run time. In this way it is possible for the user

to program the firmware and to test various configurations of the analog input channel without restarting the application.
The other structure is a clock multiplexer, inserted inside the Clock and Reset Management Unit. This multiplexer allows fast and glitch-free transition of the system clock from one source to another [43]. In this way it is possible to switch from the RC clock to the Quartz clock or to an external clock source. This IP will be deeply covered in the next section.

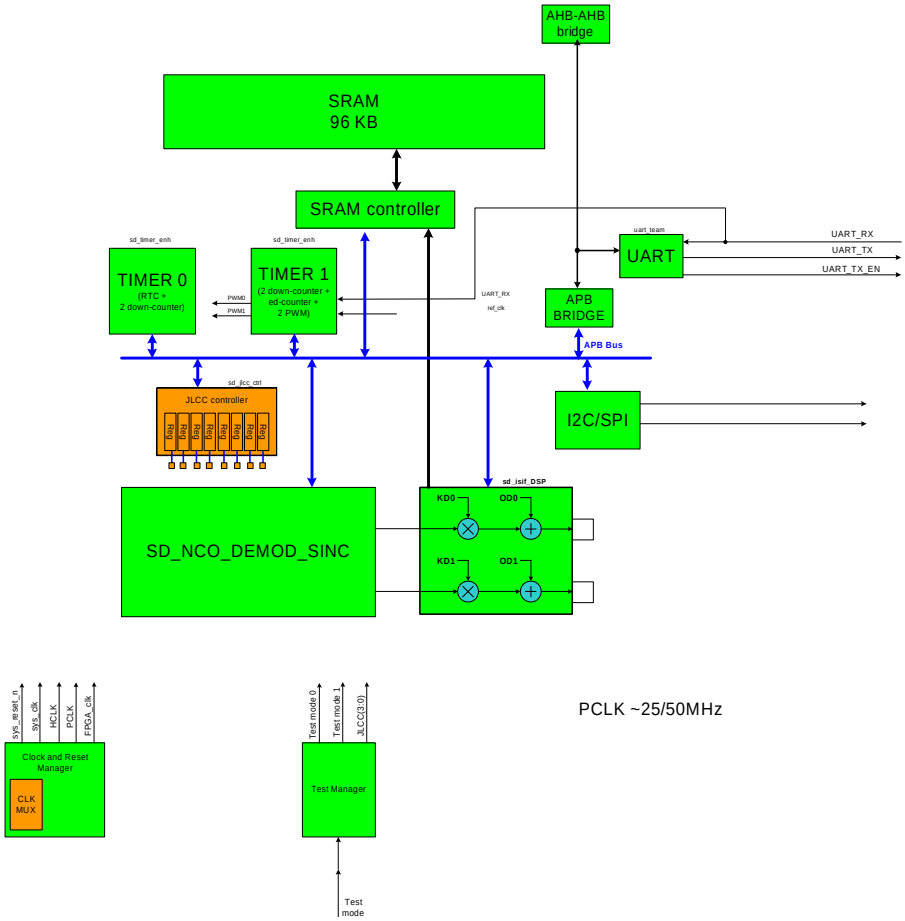


Figure 3-6: Low Speed structures of the digital section of the SD4k

Hereafter we propose a deeper analysis of some of the IP blocks of the SD4k platform. The choice has fallen upon those IPs completely developed by our team in order to grant the flexibility needed by our platform. Every IP is highly configurable and low

power oriented and, where needed, a standard interface is provided, granting a high level of reusability of the IP itself.

i. Clock Multiplexer

Currently the most used architectures that generate the clock signal are RC and quarts oscillators, widely described in literature [44][45]. Both architectures have their own benefits: RC oscillators are fully integrable, low cost and characterized by a short startup time. The principle of an RC oscillator is usually quite simple: a capacitance is charged by a constant current to generate a voltage ramp; hence this voltage is compared with a reference voltage via a comparator to generate the clock signal. This leads to an immediate start of the oscillator as soon as the current is provided. One of the main drawbacks of these kinds of oscillators is the wide spread of the produced signal frequency. Quartz oscillators exploit external quartz to provide the oscillation: the resonance frequency of the quartz becomes the frequency of the clock signal. These oscillators have a high Q factor, which allows a stable and precise oscillation. Unfortunately they introduce a large delay between the oscillator power-up and the oscillation stability. Power consumption is another crucial drawback of this type of time reference generator.
In a platform, where the flexibility of the structure grants a wider solution space exploration, the possibility to change the clock source from an internal to an external source can give the designer an additional grade of freedom while projecting the final application. For these reasons a clock multiplexer structure [43] has been added to the SD4k platform.

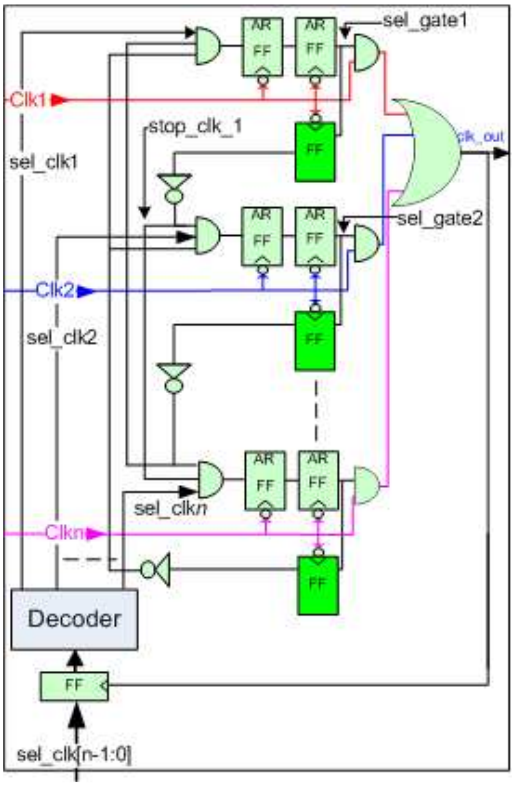


Figure 3-7: Clock Multiplexer block diagram

The figure 3-7 shows the structure of the clock multiplexer for a generic number n of clock cycles. The decoder enables only a branch at time and the enabled branch disables all the other branches so only the selected clock drives the output. The flip-flop at the end of each branch is used to introduce a delay on each enable line of the other branches, so no conflict happens in case of dynamic-switching.
This structure guarantees that there is no clk_out pulse during T_{switch} shorter than minimum clk_in pulses, and so no glitches on clk_out may occur. To clarify this concept the relevant timing diagram is reported in figure 3-8, showing the time interval when the multiplexer switches from clk1 to clk2. The selection signals change synchronously with clk1, disabling clk1 branch and enabling clk2 one. Two clk1 cycles are needed to propagate this change, and then the stop_clk_1 signal rises at the third clk1 falling edge, enabling the clk2 input. The enable signal of clk2 is propagated on the falling edge of clk2. The stop_clk_1 signal is asynchronous for clk2 so there is a risk of setup or hold times

violation. Two flip-flops in series are used to avoid the propagation of the possible metastability.

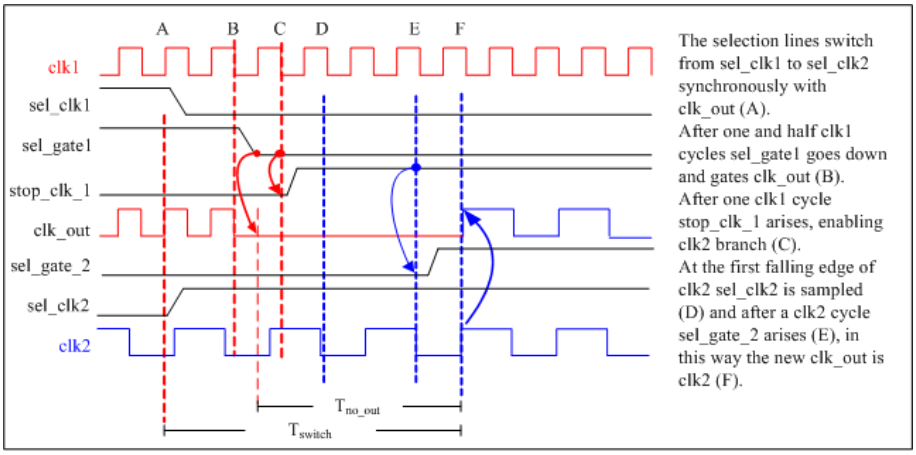


Figure 3-8: Timing Diagram

The switching from clk1 to clk2 is referred T_{switch} in figure 3-8. This time is calculated from the transition of sel_clk signal to the rising edge of clk_out, driven by clk2. The upper and lower limit of T_{switch} can be seen in the timing diagram. The results are derived form the following expression:

$$2.5\,t_1 + 1.5\,t_2 \leq T_{switch} \leq 2.5\,t_1 + 2.5\,t_2 \quad (3.1)$$

where t1 and t2 are respectively the period of clk1 and clk2 signals.
It is possible to estimate also T_{no_out} which is the period to force clk_out to ground:

$$0.5\,t_1 + 1.5\,t_2 \leq T_{no\_out} \leq 0.5\,t_1 + 2.5\,t_2 \quad (3.2)$$

It is worth nothing that the stop of the clock, which is forced low by our architecture for some cycles during the clock switching, doesn't represent a problem for a synchronous ASIC. The whole system is sensible only at the edge of the clock, so the stop of the clock signal can be see like a delay in the normal behavior of the system.
The typical clock gating structure shown in figure 3-9 guarantees that no glitches can be found on output if proper timing constraints are met. In case the path of the clock from the flip-flop to the logic port is not well designed there is the possibility of clock clipping [46].

Clock clipping is a distortion of the clock signal at the gated clock output because the data input was changing or controlling the gate during the time when the clock signal was not controlling the gate.
A timing diagram is shown in figure 3-10, assuming that the logic port is an AND or NAND one.
While the clock signal is controlling the output, the DATA signal can change its value but must go stable T_{setup} before the rising edge of the clock and must remain stable T_{hold} after the falling edge. If these constraints are satisfied, the clock is gated correctly and no glitch is generated. On the contrary, an error occurs. Of course the designer has to put special attention also to the interconnection delays by given proper logic synthesis constraints.

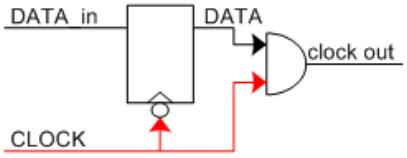


Figure 3-9: Clock gating structure

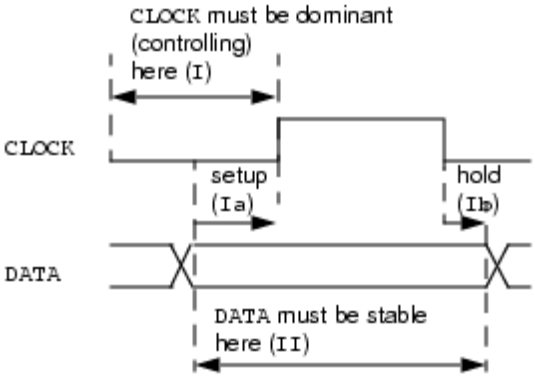


Figure 3-10: Clock Gating Timing constraints

ii. I2C/SPI interface

In telecommunications, consumer and industrial electronics the general trend is to integrate all the components on a single System on Chip (SoC) that collects all available blocks. All the integrated components must be connected each other and every

SoC must be linked each other in an efficient way for a fast and error-free communication. In industrial and automotive environment the realization of networks of electronic control units (ECU) is becoming even more crucial to handle the high quantity of data requested by actual applications; the communication among SoC is the key to grant high performances: the most used solution for interconnecting SoC is a serial bus that presents great advantages in terms of costs. Using few wires to link different devices means few occupied area and consequently minor costs for the producer. A large number of serial protocols are actually used, so if a designer wants to create a SoC that can communicate using various protocols he must equip his system with a large number of interfaces, despite the fact that when the SoC is on the field usually only few of the supported protocols will be used. This means that a large amount of area remains unused and on the system bus are appended various useless structures. At the same time, if there is not a pad sharing, a large number of pads remain unused. Moreover a high number of pads leads to a pad-limited structure that implies packaging problems and increased product cost.

We have developed an IP macrocell that can be used with different serial protocols. The idea is to merge two different interfaces: a Serial Peripheral Interface (SPI) and an Inter-Integrated Circuit (I2C) one [47] in a unique software programmable structure. Taking pin reduction as a priority, the pads are shared between the two modules. The proposed IP cell was equipped with an AMBA APB (Advanced Peripheral Bus) bus [39] interface. The choice of an APB interface is due to the fact that both SPI and I2C protocols work with a frequency lower than 5 MHz, so an APB interface will be enough to handle the communication.

This I2C/SPI interface is a software programmable device, working as I2C or SPI interface whose internal registers are accessible through the AMBA APB bus. A configuration bit allows the host CPU to switch from one protocol to the other one. System clock division allows wide range of bit rates for both communication protocols. The design is fully synchronous and low power oriented. I/O pads and internal registers are shared between I2C and SPI.

The block diagram of the device is shown in figure 3-11. It is possible to see that the APB interface and the pins are shared between the I2C and SPI modules. In this way the amount of unused area is reduced to the minimum. SPI protocol uses more pin than I2C (at least 4 instead of 2) so some pins are SPI-dedicated while the others are shared between the two modules.

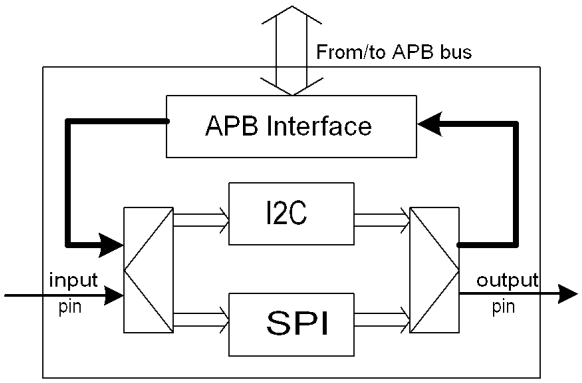


Figure 3-11: I2C/SPI IP Simplified Block Diagram

iii. AHB to FPGA bridge

During the last years, one of the trends in the design of systems for sensor interfacing and conditioning was to combine a platform-based design with a reconfigurable system. The opportunity to have reconfigurable systems that are adaptable to a large set of sensors makes these solutions more preferable during the first steps of the study of new sensors, to speed up the comprehension of the system before developing ad-hoc architectures [10][11][12].

Whereas a solution completely on FPGA could be considered the best in versatility and reconfigurability (at the expense of area occupation and power dissipation) for fully digital systems, for the reading and the driving of sensors is necessary to have a mixed-signal structure. In this case, ASICs are better than FPGAs in terms of performance because they allow a better integration of analog and digital circuits, loosing in terms of programmability and reconfigurability.

On the basis of these considerations, we chose to develop an architecture to allow an ASIC platform to be interfaced with an FPGA. In this way the FPGA can be used, if necessary, as a further resource for data processing or for particular applications that were not taken into account during the ASIC design phase. The communication between ASIC and FPGA, indeed, usually becomes a critical task, especially for IC: on the one hand for the short available number of pins (unless it's used expensive solutions, as Ball Grid Array, BGA), on the other for the necessity to reduce frequencies going out from chip, to reduce the currents managed by pads. In fact, high frequency digital signals induce high currents

into the capacitors introduced by the pads: these currents flow from voltage supply to substrate that is common to analog and digital part, consequently injecting a high level of noise into signals involved, for example, in sensors read out operations.
These problems carried us to develop an IP that could be integrated on silicon and allows communication between a CPU on the ASIC and the architecture implemented on FPGA.
The solution adopted is based on bi-synchronous First-In First-Out (FIFO) structures for frequency conversion, using a custom protocol provided of priority paths managing. High effort has been spent in order to grant high programmability of the module, both during the implementation phase and at run-time execution. The size and number of locations of the FIFOs can be chosen during the implementation time, while the output frequency can be modified at run-time.
Due to the high bandwidth that can be involved in this communications, the interface of this IP is AHB-Lite compliant, granting a high-speed communication between the processor and the IP.

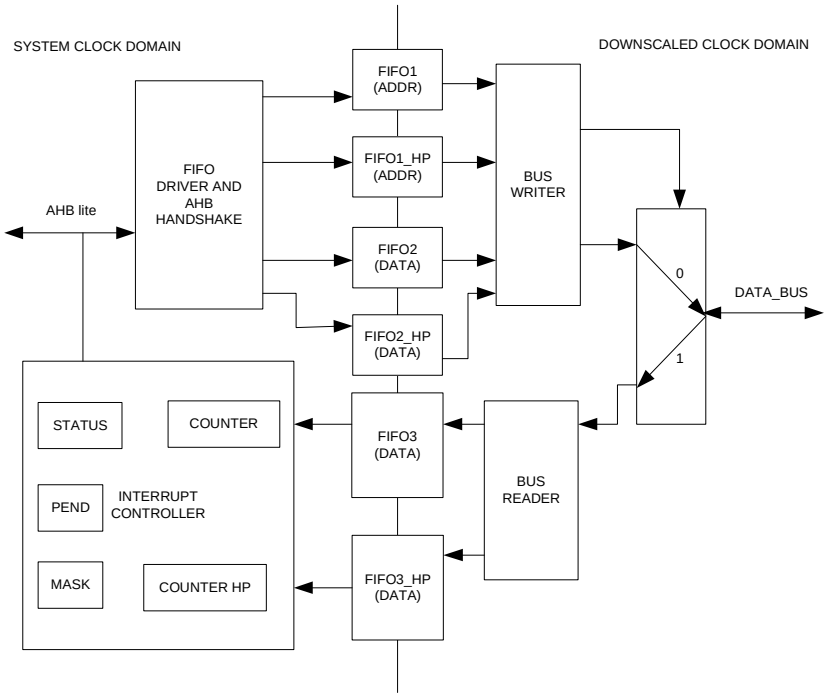


Figure 3-12: AHB to FPGA bridge Simplified Block Diagram

Figure 3-12 shows a simplified block diagram of the AHB to FPGA IP. It is possible to see how it is divided in two sections, one at the system clock frequency, the other at a downscaled frequency that will be used to transmit data out of the chip. The FIFOs are divided in normal and High Priority FIFO, to offer the CPU the opportunity to manage high priority transfers. In this case, a high priority request for transfer can be served immediately at the end of the current transaction.
This kind of structure allows the communication of the processor with an FPGA. In this way it is possible to implement on the FPGA some IP whose use can not be foreseen when the SD4k has been designed.

Chapter 4
MULTI-LEVEL TEST ENVIRONMENT

4.1 Introduction

In the last years electronic market trend has pushed towards the development of products with lower cost and smaller size. This, combined with the decreasing "economic life time" of electronic products (a short time-to-market has became crucial for the success of a new product) has resulted in the need to put entire systems, having both analog and digital functions, on a single chip [48]. Applications for these mixed-signal circuits are numerous, covering an immense segment of the electronics market. Computers and peripherals incorporate mixed-signal chips into multimedia, audio and video and networking functions. Additional uses include wireless communication devices, cellular phones, pagers and GPS receivers. High-demand consumer applications include set-top boxes, DVD players, video game consoles, high-definition TVs and also automotive applications. For example for the SoCs for automotive application we typically have a sensor producing an analog output, an analog section for signal conditioning and a digital one for signal elaboration. As a matter of fact, the following figure shows that now the number of SoCs that have critical analog/mixed-signal content is almost 80%.

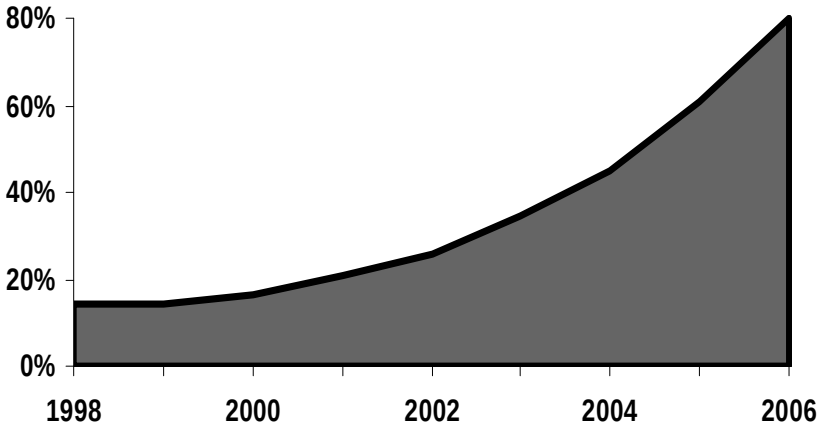


Figure 4-1: Mixed Signal on overall SoC(%). Source Industry analyst IBS Corporation

All of this illustrates the pressure on designers to achieve first-pass silicon and the need for improved design verification methodologies.
The traditional approach for such kind of systems is partitioning the design at the beginning of its development cycle: digital and analog portions are then designed and verified separately. The digital design flow is typically top-down, thus allowing a continuous verification of the matching between specification and simulation results. Instead the analog flow is more frequently bottom-up and this makes hard to feedback information from the bottom level simulations to the design top level, being almost impossible SPICE simulations of the whole system (due to the excessive simulation time, convergence troubles and computational effort). This kind of mixed-signal separated flow can easily lead to a final assembly which is not sufficiently tested (such strategy cannot provide the designer with much confidence that digital and analog portions will interface correctly) and thus it's extremely difficult to debug (see figure 4-2): any fault due to a wrong interaction between the analog and the digital section, or just inside the analog section can result in very expensive production delays [49][50][51]. For these reasons it is mandatory to have a whole system simulation immediately before tape-out, able to verify common top-assembly bugs not covered by the traditional flow (e.g. wrong/missed connections, swapped busses, references exchanged, wrong levels

and connections between analog and digital part), and the adoption of a Mixed Signal Hardware Description Language (MSHDL) [52][53], such as VHDL-AMS [54][55][56][57] or Verilog-AMS [58], becomes therefore crucial since it allows the designers to simulate the whole system (analog and digital section with the same simulation tool) during its own development. Some works can be found in literature attempting to formalize a methodology to verify mixed signal circuits using a MSHDL [59][60] however not suitable to verify very complex mixed signal SoC.

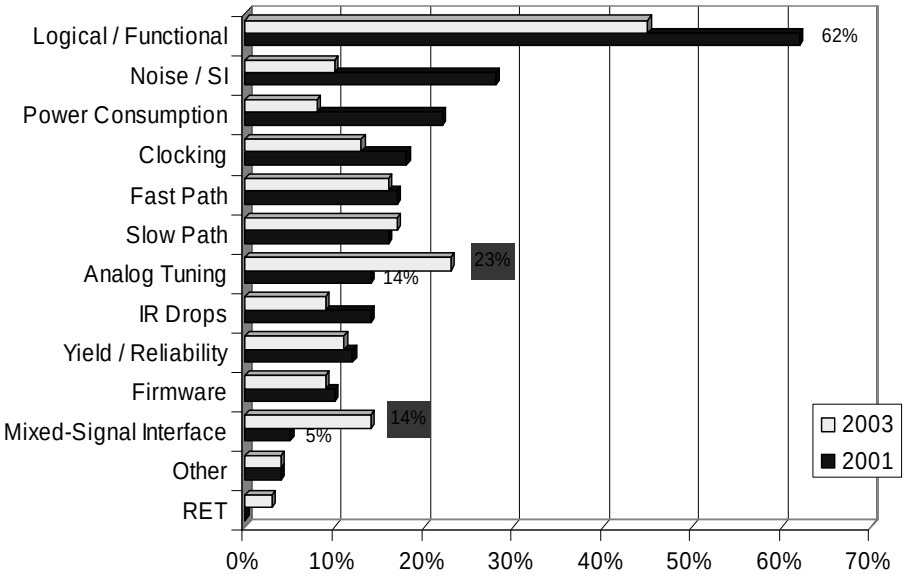


Figure 4-2: Most Common Causes of Silicon Failure

In fact modeling (for system verification) of mixed signal SoC involving several hundreds of macro-blocks features three main challenges:

- the requirement of modeling the macro-blocks with the minimum set of details for fast top level functional simulation;

- the coherency of pinout and connectivity between the model and the real system;

- the need to perform these steps in a easy, quick and safe way.

In order to meet these requirements, a semi-automatic verification flow has been developed: it bases on the behavioural VHDL-AMS modelling of the whole analog section of a generic mixed-signal IC.

4.2 System Verification Flow

The proposed system verification methodology is depicted in figure 4-3. Starting from full-custom schematics, VHDL-AMS models template can be automatically extracted by means of a set of scripts, guaranteeing the coherency between model and schematic pin-out. A behavioral model for the whole analog system can then be obtained with a flow that reads the Cadence™ top schematic and changes it into a verilog hierarchical netlist containing all the VHDL-AMS models. This model is used for top level system verifications, together with synthesizable VHDL code (regarding the chip's digital section), verilog PAD models and VHDL-AMS model of sensor.
The behavioral model of an analog macroblock is an abstract, simulatable representation that exhibits the characteristics of most interest to the designer while suppressing physical detail irrelevant for top level behavioral simulation [61]. Anyway, if on one side suppressing details speeds up simulations, on the other the VHDL-AMS model accuracy must still be suitable for system level simulation and for detecting common top level connection bugs. Therefore, to reduce the analog complexity and the required designer's effort to customize the model, we have decided to use a model template that is common for all the analog cells, yet suitable to be tailored to match the system requirement. The model used (in figure 4-4 it is shown in a simplified version for an amplifier) is a circuit's equivalent of the original transistor-level block, where the designer can modify properly the value of internal parameters and functions.

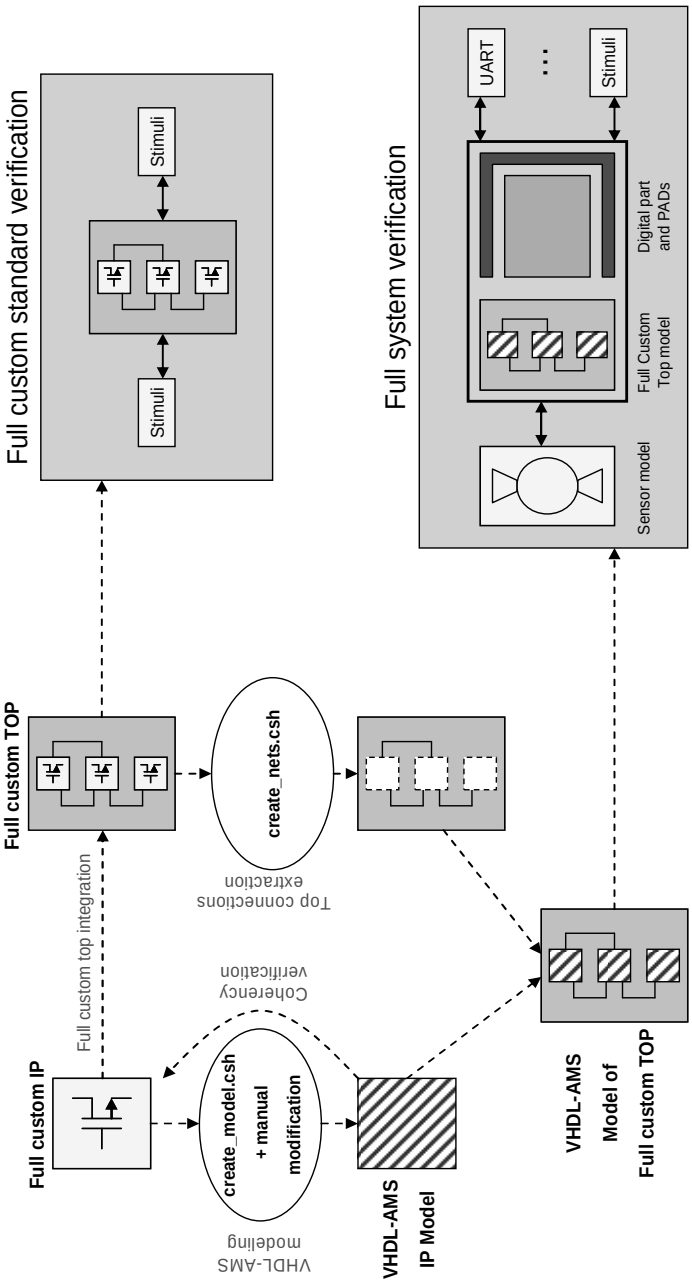


Figure 4-3: System Verification Flow

In order to ensure the pin out coherency between the model and the original block, for all the analog cells, the models have been

created semi-automatically, by means of a set of scripts, and then customized by the designer according to real behaviour of the analog cells.
The consistency of the model can be cross-validated with the original analog design, by exchanging the cell-view and running the same test-bench used to validate the transistor-level block or creating a VHDL-AMS smart test-bench that generates the stimuli and performs a self-check test comparing analog outputs of the real cell with those of its behavioural model. This feedback process increases mixed-signal simulations efficiency, allowing more comprehensive system verification. At this point the models must be interconnected in a consistent way with the actual top netlist. To reduce the possibility of mismatch with the real netlist, a CSHell script has been created to obtain an automatic extraction of top connections.

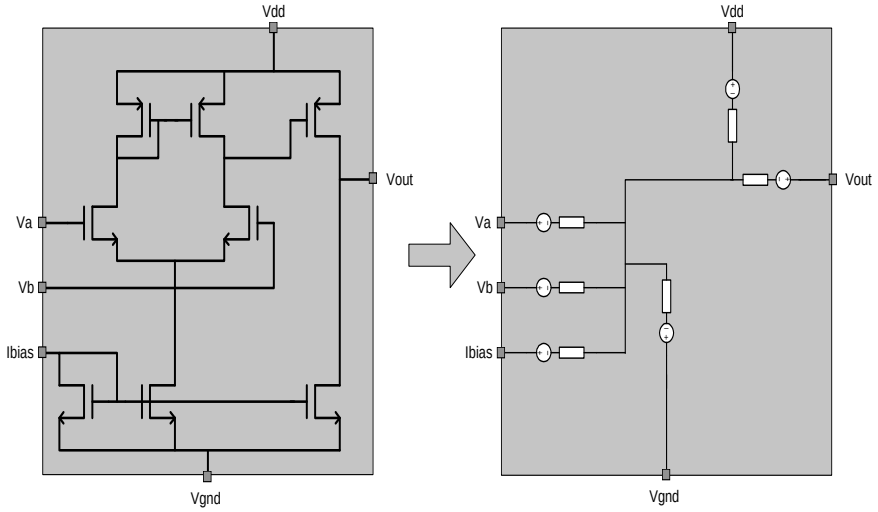


Figure 4-4: Generic Analog Block and its Simplified VHDL-AMS Model

4.3 VHDL-AMS modeling

The high system complexity and the requirement of reliability, in terms of coherency between VHDL-AMS model and relative schematic pin-out, have pushed towards an automatic model generation flow.
In fact this approach has appeared to be mandatory since the mixed-signal SoC (for which this behavioural verification has been adopted) has several models, each one with a long list of

connections, and it is extremely risky and time-consuming to create manually all the models for such complex system.

i. Modeling Flow

In order to satisfy this need for consistency, we have decided to use the Cadence™ Virtuoso command "create cellview from cellview" [62] to obtain, starting from the original schematic, a text file containing the pins' names. This command is executed by a CSH script that needs as input just the name of the analog cell to be modelled. The text file generated by the tool is then post-processed with a C++ program (create_model_engine in figure 4-5) that transforms it into a VHDL-AMS template ready to be compiled and simulated, plus a Verilog wrapper that simply instantiates the model, restoring pinout names case as it is on the schematic (to overcome the fact that VHDL is intrinsically case insensitive, while the Verilog is case sensitive). The C++ program runs in a interactive way asking the user if the pin of the analog cell is analog or digital (if the pin is analog it is declared inside the VHDL-AMS model as a electrical terminal, while if the pin is digital, for instance a power down or a configuration bit, it is declared as a std_logic pin). At the end of this pins' type selection phase, the user can select the ground terminal (if it exists) to which every other analog terminal is referred.
To be able to use VHDL-AMS models, either for analog or digital or mixed-signal simulations, and to prevent sources duplication issues (the environment used for design and simulation of analog cells is normally different from the digital one), a CSH script has been realized that copies the VHDL-AMS model and the Verilog wrapper both in the analog and in the digital database, and creates the right links between these files, in order to have only one version of each source file.

ii. Model Template

The generated template is divided in several sections and only a few of them (sections highlighted in figure 4-6) have to be modified by the designer (specifying internal parameters and functionalities) in order to make the model behave like the original transistor-level block.

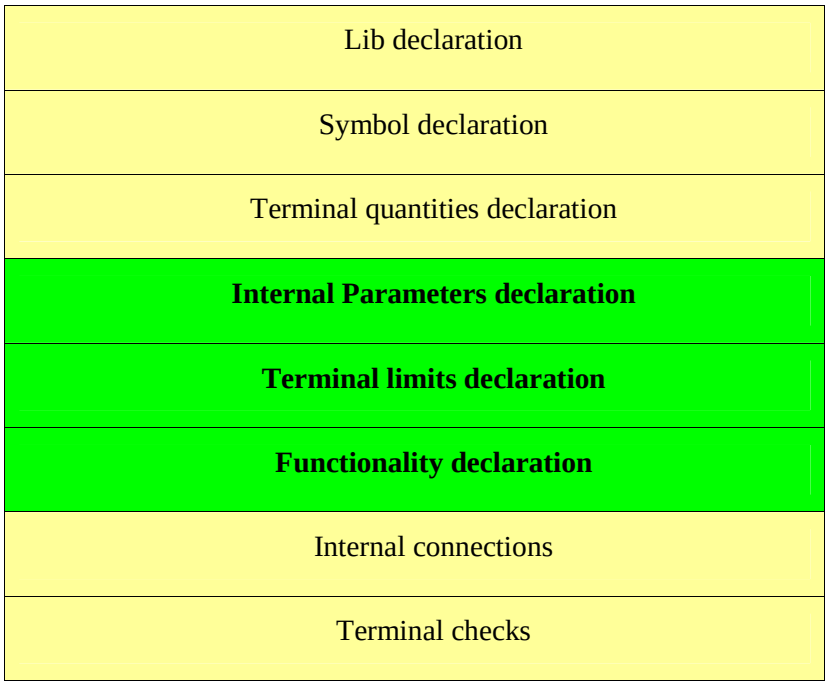


Figure 4-5: Template sections

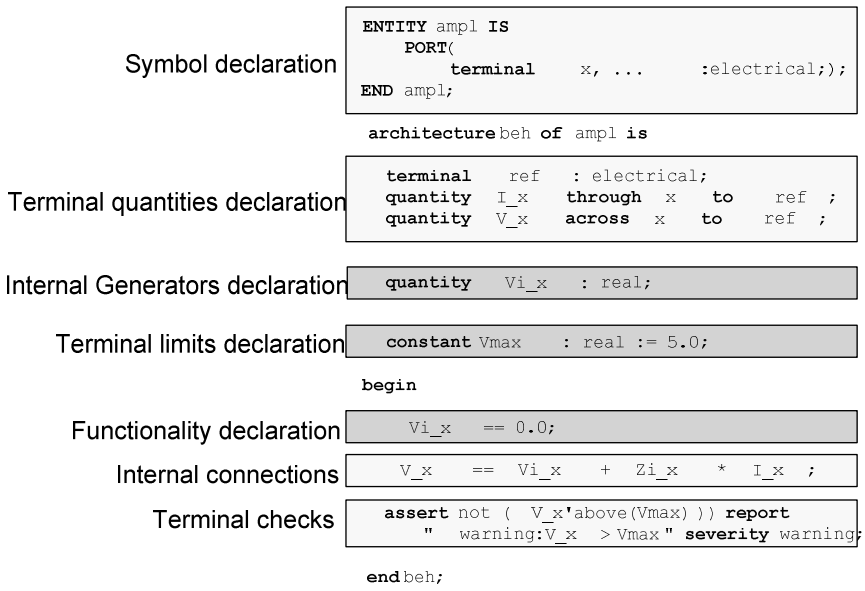


Figure 4-6: Template description

The first section (Lib declaration) is common for all the analog models and includes the IEEE libraries for the electrical system package and some others common libraries for mathematical operations. The second section includes the entity and the port declarations (as already mentioned the analog pins of the cell are defined as electrical terminals, while the digital ones are declared as std_logic). In the third section the branch quantities are defined:

- Across quantities (voltage between two electrical terminals).
- Through quantities (current flowing through two electrical terminals).

For any electrical terminal "<terminal_name>" the branch quantities are defined as depicted in figure 4-7:

- I_<terminal_name>: current through the terminal.
- V_<terminal_name>: voltage across terminal and cell reference terminal.

The Terminal limits declaration section allows the designer to specify voltage and current limits for every terminal of the cell (as depicted in figure 4-6): if during simulation voltage and/or current of a terminal exceeds limits fixed by the designer, a warning message is issued. This self-diagnostic check allows detecting very dangerous top assembly bugs like shorts or unconnected power-wires not easy to be discovered with the traditional visual inspection of the analog waveforms, especially for a design with thousands of wires just for the top level interconnections of analog macroblocks. Inside the Functionality declaration section, values for internal voltage generators (Vi<x> in figure 4-7) and impedances (impedance Zi<x> between terminal x and the reference terminal in figure 4-7) can be specified. This section as well as the previous two is initially fulfilled with default values that are to be fixed with the proper ones by the designer after the model is created by the script. Inside the sections Internal connections section the constitutive electrical equations of the model are specified as follow:

$$V\_term\_name = Z\_term\_name \times I\_term\_name$$

The last section includes the statements for the terminal voltage and current checks. These check are performed using the VHDL construct assert and the VHDL-AMS function above as in the following example:

assert not (V_term_name'above(Vmax))) report "Warning: V_term_name > Vmax" severity warning;
When the across quantity V<x> exceeds the voltage limit value V<x>_max fixed by the designer the warning message "V<x> > V<x>_max" is issued.

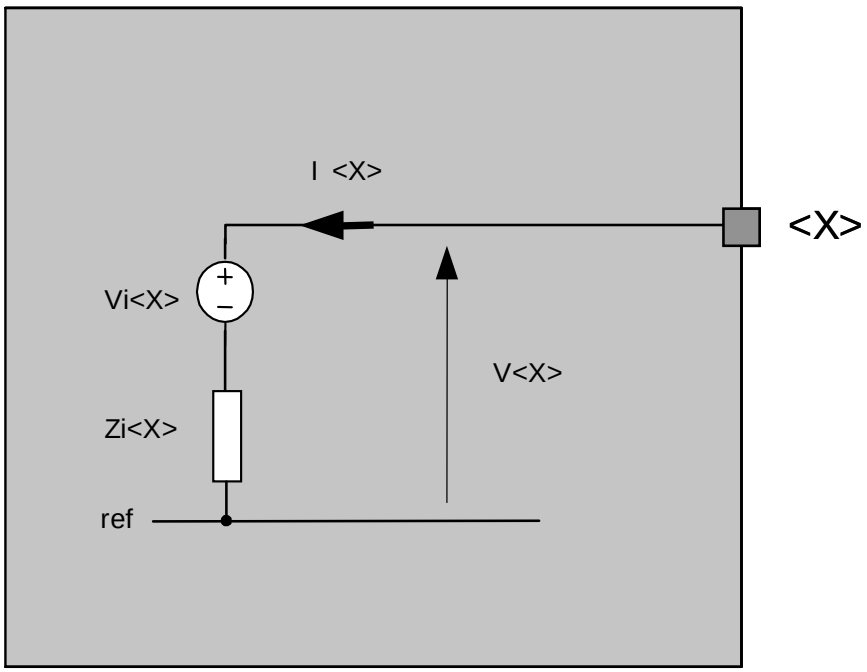


Figure 4-7: Terminal check

iii. Model Trimming

To validate models with high complexity and many pins a VHDL-AMS self-checking test-bench is created, as shown in figure 4-8 for a 16bit DAC.
The consistency of the model can be cross-validated with the original analog design, as mentioned before, employing the same test-bench used to validate the transistor-level block: the model behaviour should be visually inspected in order to check the

matching with the real cell behaviour (of course this approach only fits very simple cells).

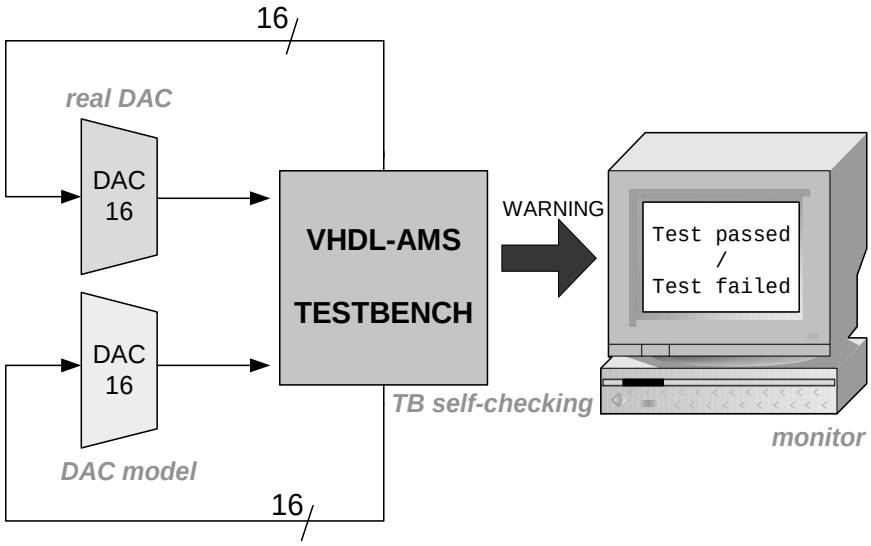


Figure 4-8: Self-checking Test Bench

The VHDL-AMS test-bench, in this example, generates proper inputs for the two DACs (model and real cell) and, after the settling time of the transistor-level DAC, samples both DAC outputs, issuing a warning message if they differ more then one LSB.

4.4 Automatic Extraction of Netlist

Once all the VHDL-AMS model are available and checked, the top level simulation can be performed: this kind of verification is effective only under condition that interconnections between the blocks in the verilog netlist are the same as those of the original analog schematic.

i. Netlisting Flow

In order to keep unaltered this amount of connections, a CSH script called create_nets.csh has been developed. It sweeps recursively the entire analog hierarchy, and by means of the

Cadence™ "AMSdirect" engine [63] extracts a verilog netlist coherent with the analog database structure.

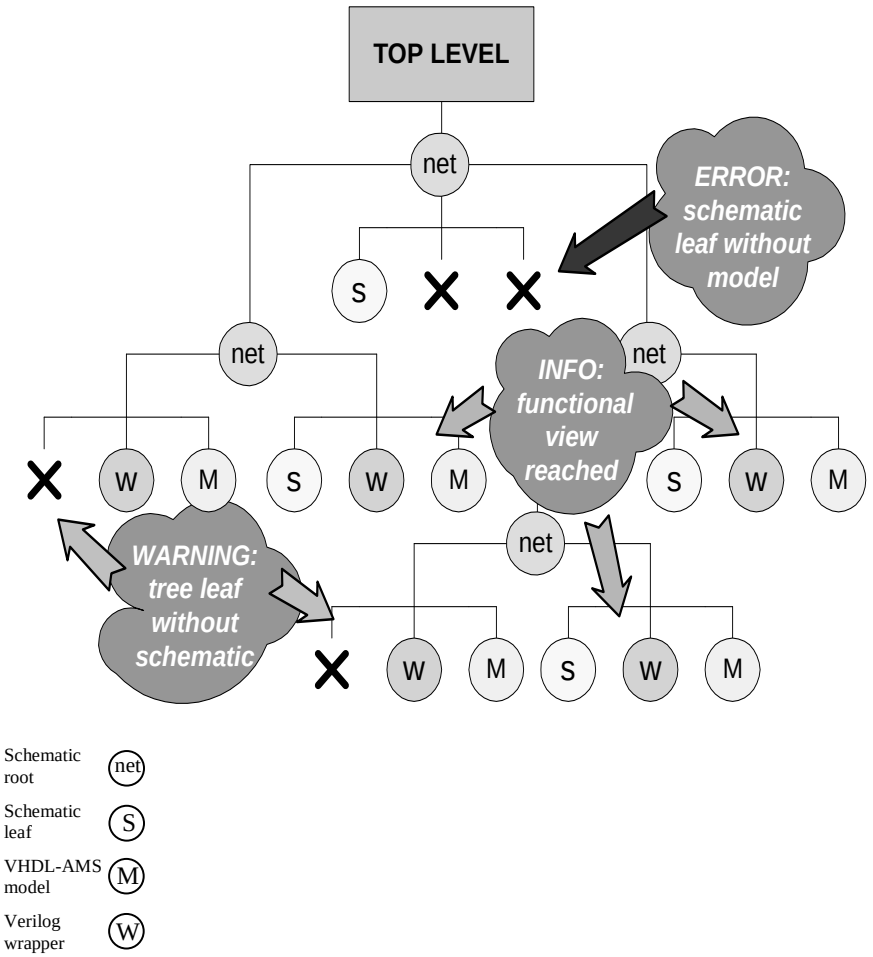


Figure 4-9: Netlist Extraction Flow

Referring to the example picture shown in figure 4-9, this script runs through the hierarchy and stops when a tree leaf is correctly detected (when a cell node database features schematic, wrapper and VHDL-AMS model), issuing an INFO message stating that the functional view has been reached for that cell. Otherwise a WARNING message is issued, in case of a node with a functional view but without the corresponding schematic, while if any leaf

lacks the model or the wrapper an "ERROR" message is signaled. In this way potentially dangerous situations are immediately pointed out, easing debug phase and thus global simulation time.
All the instantiated nets, models and wrappers can be automatically compiled by the AMS simulation tool, as the create_nets.csh script generates several log files that are directly sourced by the AMS compiler:

- The Verilog netlists of all hierarchical levels, up to those containing only VHDL-AMS blocks.
- A file containing the list of all extracted nets.
- A file containing the list of all the VHDL-AMS models to be compiled.
- A file containing the list of all the Verilog wrappers to be compiled.

ii. Connection Modules Insertion

Together with the above mentioned nets, models and wrappers are compiled the connection elements needed to convert analog signals in logic value and vice versa. These connection elements are written in Verilog-AMS, in fact, while VHDL-AMS requires manual or netlister based insertion of these connection elements, Verilog-AMS with its additional automatic insertion of connect elements during the design elaboration phase gives the user more flexibility [64]. The user just specifies the rules defining what connect modules should be used for the possible cases of inter-connection (Analog-to-Digital or Digital-to-Analog) creating a connect_rules file as in the following example.

```
connect_rules ConnRules_5V;
        connect  logic_to_elect;
        connect  elect_to_logic ;
endconnect_rules
```

Figure 4-10: Connection Modules Insertion Rules

During design elaboration the disciplines get resolved and based on that the connect elements get inserted following the above mentioned connect rules. In the D-to-A case (in the following

example connect_module logic_to_elect) the connection element detects the state of the digital drivers at the input of the connection element and applies the voltage to the analog output net accordingly.

```
connect_module logic_to_elect(cm,el);
        input cm;
        output el;
        logic cm;
        electrical el;
    analog begin
        V(el) <+ transition((cm == 1) ? 5.0 : 0.0);
endmodule
```

Figure 4-11: Logical to Electrical Connection Module

In the D-to-A case (in the following example connect_module elect_to_digital) the connection element reads the analog voltage level and applies the appropriate logic state to the digital receivers.

```
connect_module elect_to_logic(cm,el);
        input cm;
        output el;
        logic cm;
        electrical el;
        reg kout;
    analog begin
        always @( above( V(el)-2.5) ) kout=1'b1;
        always @( above( 2.5-V(el)) ) kout=1'b0;
        assign cm = kout;
endmodule
```

Figure 4-12: Electrical to Logical Connection Module

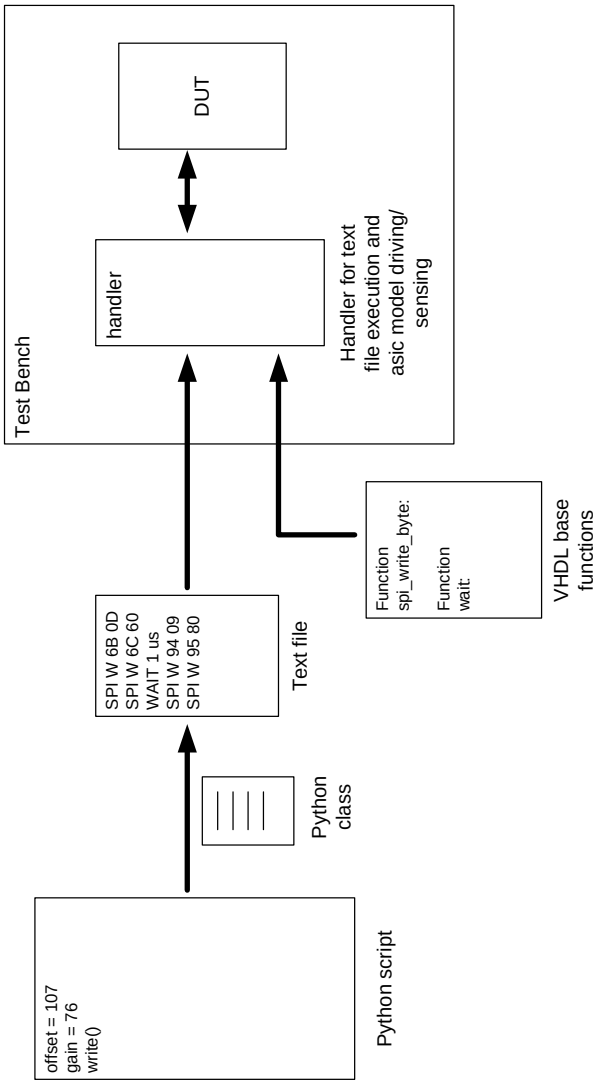


Figure 4-13: Introducing Python scripts into test environment

4.5 Full System Simulation and Results

The presented VHDL-AMS methodology has been used to validate the mixed signal SoC designed in collaboration with Sensordynamics AG and described in the previous chapter.
This semi-automatic model generation flow has made possible the whole system modelling (featuring about 100 different models) in only four man-weeks. This approach also allowed the designers to

detect top assembly bugs which are usually very difficult to discover with traditional bottom-up validation flows. An example of this kind of bugs is related to the huge number of system configuration switches, whose combined effects are very hard to be checked, in a comprehensive way, by visual inspection. The analog section of the SoC, described in the previous chapter, is actually provided with hundreds of bits, used to configure the JTAG-like serial chain used to monitor and control filters, amplifiers and converters: they lead to thousands of possible configuration states, among which a few can result in unexpected high-current paths, potentially harmful (or even killer) for system integrity. The VHDL-AMS validation flow let us discover a control signal pattern (out of the hundreds present) which would have caused a short at system start-up, and that could have never been discovered otherwise (unless running a SPICE top-level simulation).
VHDL-AMS modelling has also allowed reducing simulation time: with the presented flow it has been possible to speeds up the simulation up to two/three thousands times faster than SPICE simulation; actually one msec of full chip simulation (with analog and digital sections, pad models and software) requires only two hours and thanks to this, it has been feasible to simulate chip start-up, execution of boot, power-down, etc….

4.6 Environment Upgrades

i. Python script and text file

After the creation of the model for analog part, we optimized our test environment by introducing Python scripts to give the user the opportunity to create simulations in an easier and faster way.
This environment is based on 4 main elements:

1. PYTHON TEST: script made of mnemonic names with all the sequential operations to be done;

2. LOW-LEVEL INSTRUCTION FILE: An automatically generated text file containing the command sequence to be executed as a list of low-level instructions;

3. HANDLER: instance for command text interpretation managing, using a dedicated package call;

4. DUT: Verilog model driven and sensed by the handler;

By using an Excel list of all the mnemonic names of the modifiable parameters contained into the project, they are translated into the right physical memory location. A Python dedicated class, substitutes mnemonic names into user simulation script and translates all the assignment into one or more write operations at the right addresses. For example:
gain_1 = 157
"gain_1" is the mnemonic name for the VHDL parameter "closed_loop_gain_x" that is an 8 bit register, physically partitioned as follows:

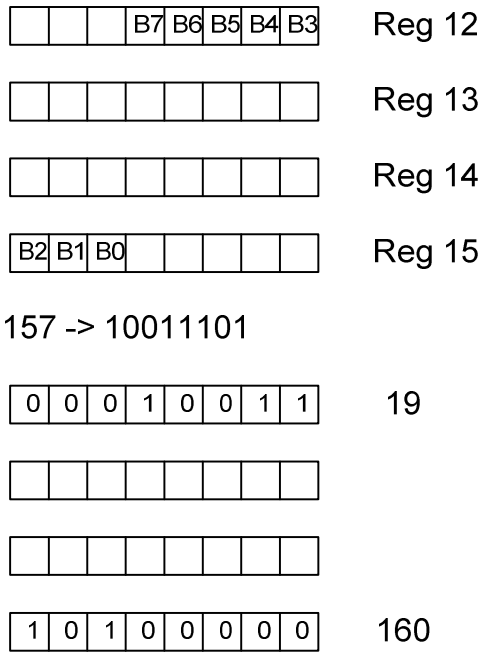


Figure 4-14: Example of parameter split into two not adjacent registers

The system automatically performs 2 write operations, writing '19' at register 12 and '160' at register 15. In this way, the user can easily create simulation files, without knowing how parameters are physically mapped into device memory resources. The class is build to keep information of the entire memory resource state to avoid accidental overwriting due to the fact that a location contains parts of different parameters.
This approach makes the test phase creation faster, keeps an high level of abstraction, could be adapted to any device by changing the mnemonic names list and, by adapting the communication

Python class, could guarantee the re-usability of the scripts also to test the real chip. Instead of text file creation, operations can be directly send to the real device by a dedicated driver. We have some weak points too, such as the text file bridging that in VHDL language involves slow routines and the fact that there is no interactivity because of the use of a list of sequential statement that has to be created before the simulation run.

ii. Full Python environment

Considering the previous analysis, we tried to create a better environment, as shown in figure 4-15.

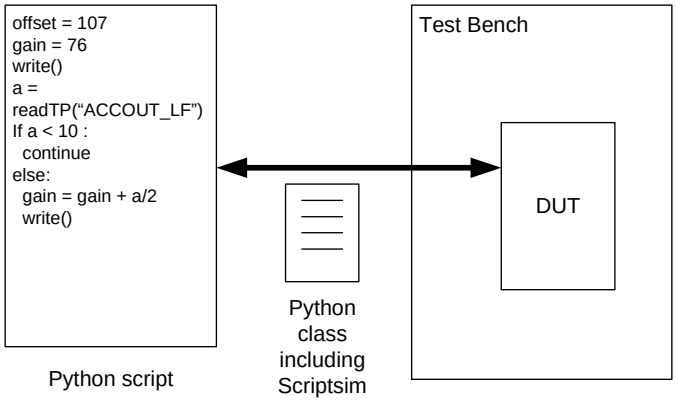


Figure 4-15: Advanced Python co-simulation environment

In this way we can avoid the introduction of the text file, decreasing simulation time and making our test completely interactive. This passage has been made possible by the introduction of ScriptSim, a free PLI bridge to simultaneously run a Python script that directly manages Verilog model's signals [65]. Running as separated processes, the full capability of both languages can be used.
ScripitSim must be instantiated as a normal Verilog function having as arguments the python script path and all the signals needed, e.g.:

$scriptsim("./dir_path/my_prog.py",signal1,signal2,signal3 ...);

With this simple statement, all the passed signals could be recalled, forced and read into Python script. This is the only line to add to Verilog model code (it creates a simulator object). For everything concerning compilation and elaboration scripts, the only

change to provide is to start the ScriptSim server and the elaboration of the pli.so library. Into the script responsible of top elaboration, it must be added the following lines (example for Cadence NCSim tool):

/*install_path*/ss_server
ncelab *tbench_lib.tbench_name:module* -logfile ./*your_log_file.log* -snapshot snapshot_name *your_ncelab_options* - loadpli1 /*install_path*/scriptsim/bin/ss_pli.so:cver_bootstrap -pliverbose

No other change is needed.
ScriptSim consists of two main objects (called modules):

- Simulator - basic object for all interaction with the simulation. It is returned by the scriptsim.Simulator() function. There is only one simulator object and repeated calls to scriptsim.Simulator() always return the same object. The simulator object is immutable.
  Invoked into Verilog code:
  $scriptsim("ss_python.py", dtest, csn, miso_addr, mosi_sda, scl, scl_int);
  Referenced into Python class:
  self.sim = scriptsim.Simulator()
  Note that signals are the arguments of the object:
  dtest, csn, miso_addr, mosi_sda, scl, scl_int =
  self.sim.argv[1:]

- Display - you get the display object with the python command scriptsim.Display(). This display is the Tk display of the display server. The display server is a python process which creates a display usable by all python agents. One python agent is created for every $vepthon() command in the Verilog code, but only one display server is present. If no programs use the display object, no Tk windows are created.
  Referenced into Python class:
  sys.stdout = scriptsim.Display().console

There are two other (side) objects:

- VVO - refers to any object in the Verilog simulation which has a value. The arguments of the Verilog $scriptsim() function call are VVOs, but you can create additional VVOs for any Verilog valued object anywhere in the Verilog design.

Assignment:
variable=sim.vvo("signal_name")

- Sim_time - it holds a value representing simulator time. Internally it is stored as a 64-bit unsigned number in units matching the simulator time_precision. It is created by the simulator method time(). When it is created, it can be initialized to any desired value, or by default it is initialized to the current simulation time.

Assignment:
t1=sim.time('1us')#t1=1us

Used in a check as a condition:

```
t2=sim.time('10ms')
if (sim.time() < t2):
    break
```

Each one of these objects has some attributes that can be read or modified. To know something more, please refer to ScriptSim documentation [65]. There are only two ways to involve time into user Python script:

- Sim_time: as seen before, it is absolute and indicates the time that passes by into simulation.

- Event on one or more of the passed signals: more "VHDL-like", synchronizing to a sort of clock as minimum time division.

The handler has been replaced with two ScriptSim functions call: a dynamic link to python script is been specified each time during NCSim call, depending on the simulation has to be performed. One script acts on supply voltages and the other on SPI interface.
Complete SPI functions setup for operations on DUT have been written: they are defined into a dedicated class where the SimScript object is called (they are based on single write, single read and multiple read low-level functions that can be found into scriptsim_basic_func.py file).
Inheriting previous environment SPI class, a complete interface for mnemonic/physical parameters conversion is provided.
These functions the user can invoke into his test script Python code are:

- Wait(num) : wait an arbitrary number of events of a specified signal change.
- Write() : write all the modified registers of the whole memory.
- ReadByte(add) : read a single byte at a specified address.
- ReadTP(name) : read the specified (by mnemonic name) 16 bits output of test bus, called "test point".
- readFromDevice() : complete memory download.

With those function we can perform all the basic SPI functions, having a complete control of the DUT. By using a Simulink™ bit-true model of the system, as normally made for feasibility study, output verification can be automatic, using the same stimuli on both the design top-level and the reference.

4.7 Test case: 3D consumer gyro X axis gain calibration

We tested our environment, developing some tests for a 3D gyroscope consumer ASIC, in collaboration with SensorDynamics AG. This project stores some blocks key parameters into an on-board RAM memory 256x8. Due to the large amount of different lenghts, most of them are not word-aligned, as explained before. A programmable insertion test bus, stores the requested 16 bit value into two 8 bit registers, called test_points (one for each of the possible 5 channels – 3 axis plus driving and sensing signals). Here will follow a brief extract of a simple example of calibration of a parameter.

```
imss04.g1_X_gain=100
let=0
x_vals=[]
good=0
for l in range(0,100):
  imss04.sim.resume_and_wait_for_event()
  for j in range (0,20) :
    imss04.Wait(100)
    let = imss04.ReadTP('XOUT_LF')
   if (let > 32767) :
        let = let-65536
    x_vals.append(abs(let))
```

```
    if (max(x_vals) > (2**14)):
      good=1
      break
    else:
      x_vals=[]
      imss04.g1_gain+=1
      imss04.write()
if good==1:
    print("\n")
    print("Gain for X has been trimmed! Gain value is")
    print("\t")
    print(str(imss04.g1_gain))
    print("\n")
  else:
    print("\n")
    print("No trimming possible!")
    print("\n")
  print("END OF OPERATIONS!")
   imss04.sim.close()
```

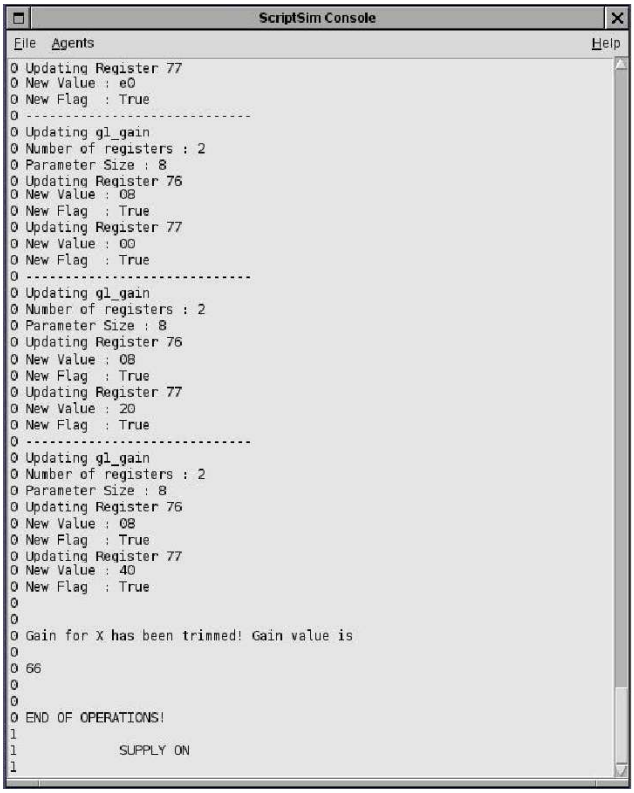


Figure 4-16: Simulation console snapshot

This script simply reads the 16 bit value of x axe test point in 2's complement notation for 20 times every 100 ns and stores all the values in a vector. If the maximum element absolute value is lower than 214, it increment the gain parameter value and performs this operations another time. When the value is higher than 214, it stops and print the value of the gain. A snapshot of the user window (the SimScript Display object) is shown in figure 4-16.

4.8 The complete environment use

In this chapter we described a complete environment for mixed-signal ASIC testing. From the simulations of the whole system by introducing a semi-automatic VHDL-AMS models design flow, with fault-free netlist automatic extraction, we developed a test strategy to use Python scripts for fast simulation bring-up, fully re-usable for both HDL level and real chip simulations. This environment allows the user to fast develop test scripts, to perform fully-interactive simulations in a more powerful, easy-to-use, Python environment with real-time processing features, completely re-usable for lab tests on real chip. We developed a high-level of versatility because this environment can be adapted to every device by modifying only an Excel document on mnemonic names. The needed Python files are automatically generated. We tested our environment with a 3D gyroscope ASIC for consumer applications, providing a complete self-checking policy that is immediate by using python scripts and can be performed even by introducing as the standard approach, a Simulink™ bit-true model as reference. We detected a strong reliability and an high level of versatility to perform a fast developing simulation environment for all the verification levels of a complex mixed-signal chip [66].

CONCLUSIONS

In this research a complete analysis of sensor interface development techniques has been carried out. Starting from the state of the art analysis, a complete overview on MEMS and MOEMS sensor-based ASICs has been presented, focusing on applications for automotive field. A significant result has been pointed-out proposing an evolution of the Platform Based Design Flow with the ISIF platform. ISIF platform is indeed a powerful tool for achieving a fast and effective prototyping of the sensor interface, overcoming the critical and time consuming system simulations needed in standard approaches at the highest system level for architectural space exploration, making the designers find the best conditioning architecture in a short time and directly on silicon, thus improving time-to-market and final ASIC performances.

The first complex mixed-signal platform designed with ISIF concept was developed by the University of Pisa in collaboration with SensorDynamics AG and featured a comprehensive set of high performance and fully programmable analog and digital IPs for interfacing a wide spectrum of sensor typologies. This platform presented some restrictions, primarily connected to the technology used. With the BCD8 evolution, and due to the positive result of the first ISIF device, a new platform has been design to overcome the limit imposed by technology and to be able to drive the last generation micro machined sensors, like MEMS and MOEMS.

As comprehensive case of study, a complete sensor system based on the electrostatic actuated, bi-dimensional raster scanning micromirror has been presented. The ISIF approach has featured a fast and effective evaluation of the whole sensor system achieving an optimal architectural definition. Furthermore, since ISIF platform allows the design space exploration to be carried out

directly on silicon, also phenomena related to the specific sensor and the optic environment have been brought to light, allowing designers to study and to apply proper counteractions.
We come to the description of the SD4k architecture, highlighting pros and cons of the various architectural choices, focusing on the primary function of the various sections. First the analog section has been described, highlighting the performances of the output channels and the flexibility of the input channels. Due to needed of the application three high speed output channels where integrated to drive the laser sources.
We have also explained the functionality of the ARM9 processor embedded in the system. The powerful embedded processor allows not only a fast execution of the software routines needed to the application but also to embed an Operating System, inserting a more user friendly software layer.
A deeper analysis of the digital section has then been carried out, focusing on some more representatives IPs. Those IPs have been chosen among the others because they were completely developed by our team in order to enhance the flexibility needed by our platform. The chosen IPs, in fact, affect the system clock, allowing the choice at run-time of different clock sources or structures used to communicate with the external environment in a fast and effective way.
Laser-based video projection systems are expected to find a wide utilization for the realization of new generation automotive head up displays thanks to the recent advance of Micro-Opto-Electromechanical Systems (MOEMS) and visible laser sources. The thesis has described in details this topic focusing especially on the design of a prototyping platform able to drive state of the art of MOEMS and laser sources. The conditioning system has been studied and widely simulated, in order to highlight those application issues that the conditioning electronic must face. The simulation has been also very useful to test the algorithm implemented to overcome these issues, ranting the possibility of a first silicon success for our platform and the target application [67][68].
Finally a complete multi-level test environment has been presented. A significant problem into a full ASIC design flow is represented by the need of a reliable and flexible test environment able to perform verification steps during all the different phases, guaranteeing a fast implementation to avoid re-design, so drastically reducing development costs. After the introduction of a semi-automatic VHDL-AMS design flow to test the whole system (both the analog and the digital parts connected together), a Python environment has been included into HDL simulation,

allowing mnemonic names parameters recall by an automatic physical addresses remapping, offering the flexibility of a software script, acting directly on Verilog top-level. This environment can be used also for laboratory verification on silicon prototypes by changing only the Python class call but using the same scripts as into the design test phase. The main advantages are represented by the high speed of implementation of new tests, the opportunity to perform recursive procedures such as calibration or communication interfaces stress. The whole verification platform has been implemented for a consumer 3D gyro in collaboration with SensorDynamics AG.

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