Comprehensive Investigation on Remedial Operation of Switch Faults for Dual Three-phase PMSM Drives Fed by T-3L Inverters

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***Abstract*—In this paper, the remedial operation of switch faults will be investigated comprehensively for T-type three-level (T-3L) inverters fed dual three-phase motor drives. The open-circuit switch faults in multiple phase legs are discussed at first. The faulty conditions are classified into five categories. Different remedial strategies, namely Type-I to Type-V schemes are proposed for different faulty conditions. In particular, three kinds of Type-III fault-tolerant control schemes are proposed by using medium voltage vectors to synthesize small voltage vectors, in such a way that mid-point voltage in DC link can be stabilized well. Then, the short-circuit faults in both clamping switches and half-bridge switches are investigated. By analysis, their operation conditions are equivalent to conditions loss of both P and N voltage levels and open-phase faults, respectively. Thus, the corresponding remedial strategies can be applied accordingly. Particularly, a voltage compensation control method is proposed for conditions where open-switch faults coexist with open-phase operation induced by short-circuit faults in half-bridges switches. The validity of all of theoretical analysis and proposed remedial strategies have been verified by experiments.**

***Index Terms*—Dual three-phase PMSM drive, T-type three-level inverters, remedial operation, switch faults, space vector modulation.**

I. INTRODUCTION

RECENTLY, with increasing demands of high reliability and large capacity for electric drive systems, multiphase drives have been widely applied in various fields such as elevator, aerospace, electric vehicle, ship propulsion, etc [1-2]. The main advantages of multiphase motor drives over three-phase ones can be summarized as low torque pulsations, low current stress, low DC link current harmonics, high power density and high fault-tolerant capability [3-4]. On the other hand, the multilevel converters fed drives become an important solution for high-power drives. By using multilevel techniques, the rated voltages of drives are increased. Besides, the multilevel converters fed drives provide better harmonic performance in output voltages, which facilitates low switching-frequency operation of high-power drives [5]. Today, more and more attentions have been paid to fault-tolerant operation for multilevel converters due to their redundant voltage vectors [6]. As a kind of multilevel inverter, the T-type three-level (T-3L) inverters become popular in applications such as photovoltaic (PV) power generation and electric vehicle traction systems recently [7-8]. The T-3L inverters could generate three-level output voltages by adopting two series-connected power switches to clamp output terminal of each phase to mid-point of DC link. Furthermore, the T-3L inverters have been verified to offer small conduction and switching losses [9]. Particularly, the T-3L inverters are verified to be most efficient during operation with switching frequencies in range of 4-30 kHz compared to two-level inverters and diode neutral-point-clamping (NPC) three-level inverters [10]. By adopting T-3L inverters to supply multiphase motor drives, high-performance and high-reliability operation can be used for high-power low-voltage applications such as electric vehicle tractions systems [8].

Fault-tolerant control have been studied intensively for both multiphase drives and multilevel inverters. For multiphase drives, almost all fault-tolerant control schemes are focused on open-phase faults in power inverters or armature windings of electrical machines, since redundant phases are available for multiphase drives compared to three-phase systems. The remedial strategies of multiphase drives under open-phase faults can be classified into three categories: The first category has been developed with field-oriented control schemes, where the armature currents are decomposed and controlled aligning with a rotating synchronous frame of rotor flux [11-14]. The proportional-integrator (PI) controllers are usually used for current regulation. The second category is to decompose components of natural frame onto torque-generation subspace, harmonics subspaces and zero-sequence subspace based on vector space decomposition (VSD). The resonant controllers, hysteresis controllers and model-based predictive controllers can be used to track the periodic current references on those orthogonal subspaces [15-17]. The third category is with direct

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torque control, where the current controllers are omitted. Under faulty conditions, the remaining switching voltage vectors are used to synthesize desired voltage components on torque-generating subspace, which are generated by stator flux and torque comparators. The current component on an additional dimension is also considered to achieve a circular stator magnetic motion force (MMF) and make copper loss minimum [18-19]. However, all of these study are limited to two-level inverters fed multiphase drives.

On the other hand, previous study on fault-tolerant control schemes of multilevel inverters, in particular for NPC three-level inverters are focused on three-phase systems. The remedial strategies include reconfiguration of power circuit with additional hardware and modification of switching strategies with remaining switching vectors [6, 9, 20-21]. In [22-23], the impacts of missing voltage vectors are analyzed for open-circuit fault in each switch of three-phase T-3L rectifiers and inverters. Different remedial strategies have been proposed and compared for the single-switch open-circuit fault, in particular for neutral-point-clamping switches of T-3L rectifiers and inverters. Different from them, the purpose of this paper is to analyze and propose remedial strategies for faults in semiconductor switches of T-3L inverters fed dual three-phase motor drives comprehensively. Compared to two-level inverters fed systems, study on fault-tolerant control of multilevel multiphase drives are very few due to complexity in their voltage synthesis. In [24], remedial schemes are studied for T-3L inverters fed six-phase induction. In [25], the investigation has been presented for open-switch faults in T-3L inverters fed dual three-phase permanent magnet synchronous motor (PMSM) drives based on VSD. The switching vector synthesis is achieved with remaining switching voltage vectors under open-switch faults. This method is suitable for multiphase drives with any phase number. But the remedial strategy in [25] is only used for single-switch open-circuit fault since the processes of reconstructing voltage vectors are complex.

It should be noted that effective fault diagnosis is very important for fault-tolerant operation, since proper remedial measures can be taken after detection of fault. In [26], twenty one diagnostic methods are studied for open-circuit faults and ten methods are evaluated for short-circuit faults of two-level inverter. These diagnosis methods have been summarized based on their performance and implementation efforts. Different current patterns are analyzed for NPC inverters under different open-switch faults in [27]. Additionally, the radius of current patterns and the current angles are used to identify the location of faulty switches in the inverter. In [9], an open-switch diagnostic method is presented for T-3L inverters by using average of the normalized phase current and the change of the neutral-point voltage. Furthermore, an open-switch fault detection method is proposed for the T-3L rectifier with unity power factor, and only currents are used for fault detection in [28]. In [29], a fast on-line diagnostic method is presented for detecting open-circuit switch faults in T-3L inverter. The principle is based on monitoring abnormal variations of DC bus neutral-point current in combination with existing information on instantaneous switching states and phase currents. The deviations of line-to-line voltages and capacitor voltages are used to identify the faults since DC-link capacitor voltages and line-to-line output voltages will be changed after occurrence of switch faults [30]. The emphasis of this paper is to study post-fault remedial strategies, which are to be taken after effective fault detection. So, the concrete methods of fault diagnosis will not be discussed in details in this paper.

Different from previous work, the contributions in this paper are: Firstly, the impacts of switch faults and the related remedial operation of T-3L inverter fed dual three-phase PMSM drive will be investigated comprehensively. Both open-circuit faults and short-circuit faults in power switches will be studied. Furthermore, not only single-switch but also multiple-switch faults will be investigated in this paper. Secondly, different remedial operation strategies, namely Type-I to Type-V schemes are proposed for the drives depending on fault types. In particular, three Type III remedial schemes are proposed for some severe multiple-switch faulty conditions. The medium voltage vectors are incorporated for voltage synthesis to mitigate negative impacts from redundant small voltage vectors. Besides, two upgraded remedial strategies, namely Type III-1 and Type III-2 are proposed for severer fault conditions based on this idea. Dynamical adjustment of dwelling time of remaining voltage vectors and closed-loop control of mid-point voltage are incorporated in the two strategies. Thus, the distinct deviation and fluctuation in mid-point voltage of DC link are suppressed. Thirdly, a voltage compensation method is presented for the condition where some phase legs are removed due to short-circuit faults in half-bridge switches. By compensating terminal voltages of remaining windings, smooth torque can be kept even open-circuit faults occur in other phase legs. Although voltage vector analysis and synthesis of the proposed fault-tolerant strategies are designed for dual three-phase PMSM drives in this paper, the similar remedial strategies can be designed and applied for two independent three-phase PMSM drives.

The organization of the rest of this paper is listed as following: The configuration and control structure of T-3L inverters fed dual three-phase PMSM drives in this paper are described in section II. Then, the remedial strategies of open-circuit switch faults are studied comprehensively in section III. According to types of faults, the remedial strategies are classified into five categories. In section IV, the remedial strategies of short-circuit switch faults are investigated. The coexistence of short-circuit and open-circuit faults is also discussed in section IV. The experimental verification of the proposed remedial schemes is given in section V. Finally, conclusions are drawn in section VI.

II. Configuration and Control

Fig. 1 shows the configuration of the T-3L inverters fed dual three-phase PMSM drives. The electrical machine has two three-phase windings, with 30-degree shifted angle between them. The windings are fed by two separate T-3L inverters, which share a common DC link. Fig. 2 shows block diagram of control structure in this paper. The VSD is adopted to achieve decoupled control of torque and harmonics. The vector predictor is used to generate α-β voltage reference components U_α and U_β on torque-generation subspace based on perturbation angle $\Delta\delta$ deriving from closed-loop torque controller, stator flux reference ψ_{ref} and feedback of stator currents $i_{s\alpha\beta}$. The closed-loop current controllers (proportional resonant, PR) are incorporated to generate *x*-*y* voltage reference components U_x and U_y on harmonic subspace. Thus, both fast torque response

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and good harmonic performance will be provided. In this paper, the double three-phase SVM strategy is applied for modulation in dual three-phase T-3L inverters. Owing to that, design of modulation strategy becomes much more convenient under fault-tolerant operation compared to utilization of VSD method in [25].

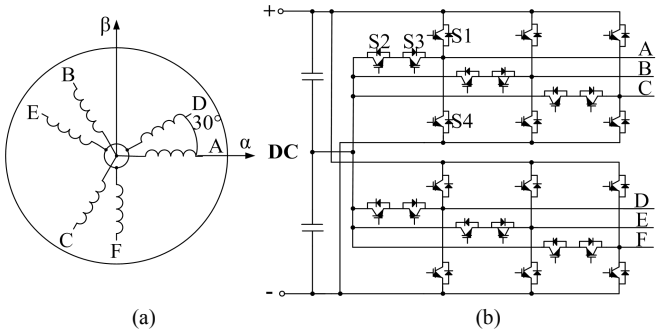


Fig. 1. Dual three-phase PMSM drive: (a) winding arrangement; (b) T-3L inverter

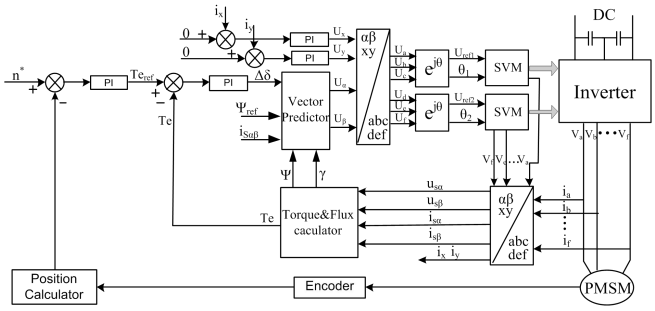


Fig. 2. Block diagram of double SVM based control for drive system.

As aforementioned, the T-3L inverter fed dual three-phase motor drives have high fault-tolerant capability due to the redundant voltage vectors and more phase legs. Thus, more controllability is available in fault-tolerant operation and suppression of mid-point voltage fluctuation in DC link. Different types of switch faults and the related remedial strategies will be investigated comprehensively. In this paper, the remedial strategies will be achieved only by modulation reconstruction, and the control scheme in Fig. 2 is unchanged under faulty conditions even with open-phase faults.

III. Remedial Schemes of Open-circuit Faults

A. Change of Current Paths

To clarify the impacts of open-circuits faults in power switches, Fig. 3 is used to show current paths in one phase leg under typical different current directions and operating states. Since the output phase could be clamped to the mid-point of DC link through switches S_2 and S_3, the T-3L inverter can output three voltage levels of $+U_{dc}/2$, 0 and $-U_{dc}/2$, which are expressed as P level, O level and N level respectively. The switches S_1 and S_2 are turned on to generate P level. Under this condition, the switches S_3 and S_4 must be turned off to avoid short-circuit fault. The switches S_2 and S_3 are turned on to generate O level, and the switches S_1 and S_4 must be turned off under this condition. The switches S_3 and S_4 are turned on to generate N level, and the switches S_1 and S_2 must be turned off under this condition. Fig. 3(a), (b) and (c) represent the current paths when the phase current i flows outside. In Fig. 3(a), the red route represents the current path of P level under normal condition, and the green route represents the current path when S_1 is with open-circuit fault. Thus, the P level is forced to O level under the fault condition. In Fig. 3(b), the red route represents the current path of O level under normal condition, and the blue route represents the current path when S_2 is with open-circuit fault. The level is forced to N level under the fault condition. Fig. 3(c) represents N level with current flowing outside phase leg, where S_3 and S_4 are turned on. It is observed the current path is same under normal condition and open-circuit fault in S_4. Both of them are marked red in Fig. 3(c). On the other hand, Fig. 3(d), (e) and (f) plot the current paths of P, O and N levels when the current flows inside phase leg. Also, the red routes represent the normal condition. In Fig. 3(d), the current path is not changed when S_1 is with open-circuit fault since the current flows through the diode D_1. Differently, the current path under normal condition will be changed to the blue route when S_3 is with open-circuit fault in Fig. 3(e), where the original O level is forced to P level. In Fig. 3(f), the current path of N level under normal condition will be changed to the current path marked with orange when the open-circuit fault is with S_4. So, the voltage level is changed from N level to O level.

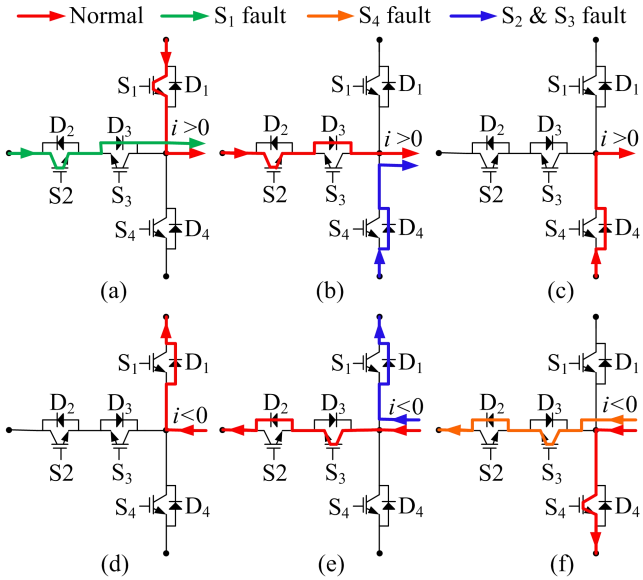


Fig. 3. Current paths in normal state and different faulty states according to the current direction and operating state. (a) i >0,P level: S_1, S_2 =ON, S_3, S_4 =OFF; (b) i >0,O level: S_2, S_3 =ON, S_1, S_4 =OFF; (c) i >0,N level: S_3, S_4 =ON, S_1, S_2 =OFF; (d) i <0,P level: S_1, S_2 =ON, S_3, S_4 =OFF; (e) i <0,O level: S_2, S_3 =ON, S_1, S_4 =OFF; (f) i <0,N level: S_3, S_4 =ON, S_1, S_2 =OFF.

B. Faults in One Phase Leg

Table I shows changes of voltage levels when faults occur in one phase leg. When clamping switches, namely S_{A2} or S_{A3} is with open-circuit fault, O level will be missed in phase A. The remaining voltage vectors are shown in Fig. 4(a), where the missing voltage vectors are shaded with grey color. For remedial operation, the P level and the N level are used to synthesize the missing O level according to the volt-second balance principle. For example, the dwelling time of P level, O level and N level of phase A leg within one switching period are defined as T_P, T_O and T_N under normal operation. With the aforementioned fault-tolerant strategy, the dwelling time of P level, O level and N level are modified as $T_P+T_O/2$, 0, $T_N+T_O/2$. This solution is defined as Type-I scheme. By replacing the missing O level by P level and N level, the switching strategy will be converted from three-level modulation to two-level

modulation. For the proposed Type-I scheme, the dwelling time of the missing O level is distributed by P level and N level equally in faulty phase based on volt-second balance principle. The transition actions between P and N become more frequent and the output voltage harmonics will become larger slightly. But the voltage change within one sampling interval would be attenuated by filtering effect of motor inductances. The synthesized vectors under normal operation and fault-tolerant operation have same effects on magnetic field of motor. The control structure is also unchanged during the process. With Type-I remedial operation, the drive performance will be improved except that the inverter harmonics increase slightly in the sectors where O level is missing. The maximum modulation index and torque ability of the drive system are unchanged. Thus, the system performance will not be defected except that more switching actions occur between P and N levels in phase A. It is noted here that the same countermeasures will be taken for loss of O level under other conditions in the following of this paper. Due to limited length, they will not be mentioned again.

When P level is missing under open-circuit fault in S_{A1}, the space vector diagram is plotted in Fig. 4(b). Since some large and medium voltage vectors are missing, the modulation index has to be decreased inside the inner hexagon. There are still quite a few redundant small voltage vectors remained. So, the fluctuation of mid-point voltage in DC link can be mitigated well. This solution is defined as Type-II scheme.

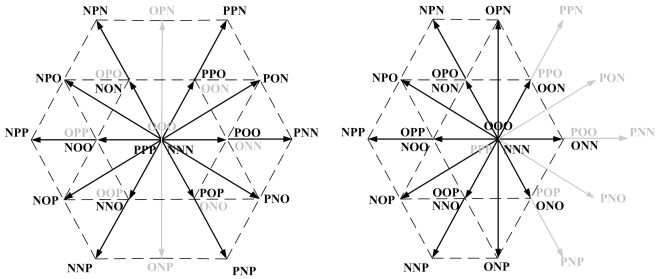


Fig. 4. Space vector diagram: (a) faults in S_{A2}/S_{A3}; (b) faults in S_{A1}.

TABLE I OPEN-SWITCH FAULTS IN ONE PHASE LEG

Missing Levels	Remedial Scheme
O	I
P(N)	II
P and N	III
others	IV

Fig. 5(a) shows distribution of voltage vectors when both P and N levels are missing, and only O level is left for phase A. Similarly, the drive system will operate with reduced modulation index after losing large and medium voltage vectors. As shown in Fig. 5(a), the mid-point voltage of DC link will suffer from distinct fluctuation inevitably since all small voltage vectors lose their redundant voltage vectors in the faulty inverter. To mitigate this problem, some medium voltage vectors are used for voltage synthesis instead of small voltage vectors. For example, small voltage vector OON is synthesized by medium voltage vector OPN and another small voltage vector ONN. Thus, the chance of using small voltage vectors becomes less and oscillation in mid-point voltage of DC link will be mitigated. The red color is used to mark voltage vectors used actually. This solution is defined Type-III scheme.

When both P and O levels are missing in phase A, the space vector distribution of the inverter becomes asymmetric and phase A must be removed. The remedial solution of this open-phase operation is defined as Type-IV scheme. With this scheme, the phase currents become asymmetrical to avoid torque oscillation in the drive system.

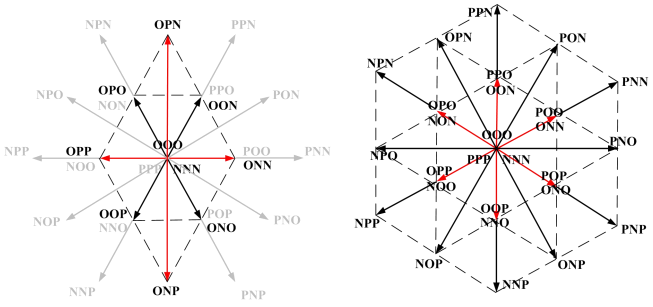


Fig. 5. Space vector diagram with faults in both S_{A1} and S_{A4}: (a) inverter 1; (b) inverter 2.

C. Faults in Two Phase Legs

Table II presents categories of voltage vectors when open-switch faults occur in two phase legs, and they are located in different inverters. The first condition considered here is that P level is missing in one inverter while N level is missing in the other inverter. For instance, P level is missing in phase A and N level is missing in phase D when S_{A1} and S_{D4} are with open-circuit faults. As shown in Fig. 6, the modulation index has to be reduced for these two inverters, and only small voltage vectors are used for voltage vector synthesis. Since the P-type small voltage vectors and the N-type small voltage vectors are missing in two different inverters, their impacts on mid-point voltage in DC link could be compensated by each other. The type of remedial scheme is classified as Type-II scheme.

TABLE II OPEN-SWITCH FAULTS IN TWO PHASE LEGS OF TWO SEPARATE INVERTER CHANNELS

Missing Levels of Phase Leg 1	Missing Levels of Phase Leg 2	Remedial Scheme
P(N)	N(P)	II
P(N)	P(N)	III-1
P and N	P(N)	III-1
P and N	P and N	III-2

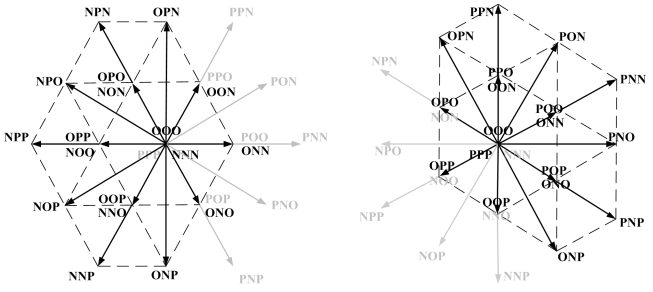


Fig. 6. Space vector diagram with faults in both S_{A1} and S_{D4}: (a) inverter 1; (b) inverter 2.

The second condition in Table II is that P level is lost in two phase legs located in two inverters. For instance, the P levels are missing in phase A of the first inverter and in phase D of the second inverter when open-switch faults occur in S_{A1} and S_{D1}. The actual voltage vectors used are marked red in Fig. 7. However, the missing Type-P small voltage vectors in the two inverters are both distributed in the right plane, which will cause DC deviation in mid-point voltage of DC link. Besides, both two inverters lose Type-P small voltage vectors, and there will be large oscillation in mid-point voltage of DC link. So, medium voltage vectors are adopted for voltage synthesis to

save using small voltage vectors. The medium voltage vector OPN and small voltage vector ONN are used to synthesize OON, and medium voltage vector ONP and small voltage vector ONN are used to synthesize ONO. Taking sector I as an example, the dwelling time of vectors OOO, ONN/POO and OON/PPO are T_0(OOO), T_1(ONN/POO) and T_2(OON/PPO) under normal operation. Under fault-tolerant operation, the vectors OOO, ONN and OPN are used instead and the corresponding dwelling time are calculated by:

$$\begin{cases} T_1^*(\mathrm{ONN}) = T_1\ (\mathrm{ONN/POO}) + T_2\ (\mathrm{OON/PPO})/2 \\ T_2^*(\mathrm{OPN}) = T_2\ (\mathrm{OON/PPO})/2 \\ T_0^*(\mathrm{OOO}) = T_0\ (\mathrm{OOO}) \end{cases} \quad (1)$$

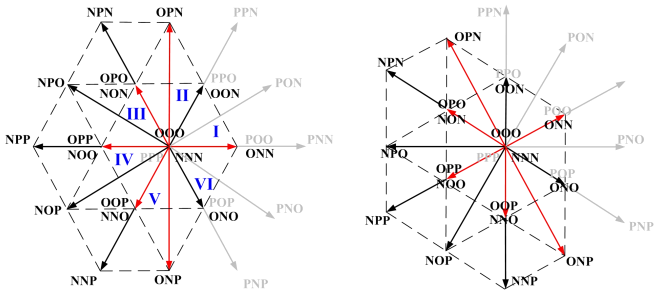


Fig. 7. Space vector diagram of open-switch faults in S_{A1} and S_{D1}: (a) inverter 1; (b) inverter 2.

The DC deviation in mid-point voltage may result in lower usage of DC link voltage. To enhance the output voltage capability, two measures are taken: The first one is to adjust dwelling time of P and N levels dynamically to compensate unbalance in output voltage. The criteria are as follows:

$$T_P = T_P^* \cdot \frac{U_{dc}}{2u_{Cupper}} \quad (2)$$

$$T_N = T_N^* \cdot \frac{U_{dc}}{2u_{Clower}} \quad (3)$$

where T_P^* and T_P are dwelling time of P level before and after adjustment, respectively, and T_N^* and T_N are dwelling time of N level before and after adjustment, respectively. u_{Cupper} and u_{Clower} are real values of the upper and lower DC capacitor voltages. U_{dc} is the total voltage of DC link.

The second measure is to introduce a closed-loop controller for average value of mid-point voltage in DC link. The principle is shown in Fig. 8. u_{mid} is average value of 10 maximum sampling values and 10 minimum sampling values of mid-point voltage in DC link within each fundamental period. By using a PI controller, the adjustment voltage Δu_{mid} is generated. By adding Δu_{mid} to $U_{dc}/2$, the mid-point voltage reference u_{mid}^* is obtained. In Fig. 7, the remaining three pairs of small vectors of each three-phase inverter can be utilized to adjust the mid-point voltage in DC link by comparing values of u_{mid}^* and $U_{dc}/2$. If the mid-point voltage reference u_{mid}^* is larger than $U_{dc}/2$, the voltage vectors ONN, OPN, OPO, OPP, OOP and ONP are used for voltage synthesis. Otherwise, the voltage vectors ONN, OPN, NON, NOO, NNO and ONP are used for voltage synthesis. The mid-point voltage in DC link will be controlled by remaining redundant small voltage vectors together with medium voltage vectors. Since this strategy uses additional countermeasures, it is called Type III-1 scheme. The third condition in Table II is that both P and N levels are missing in one phase of the first inverter, and P level is missing in one phase of the other inverter. For example, P and N levels are missing in phase A with faults in S_{A1} and S_{A4}, while P level is missing in phase D with fault in S_{D1}. As shown in Fig. 9, the P-type small voltage vectors are lost on right plane of both two inverters. So, Type III-1 scheme is used to avoid causing large deviation in mid-point of DC link.

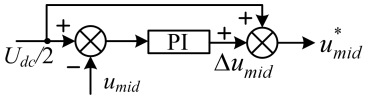


Fig. 8. Closed-loop controller for adjustment of mid-point voltage reference in remedial scheme III-1.

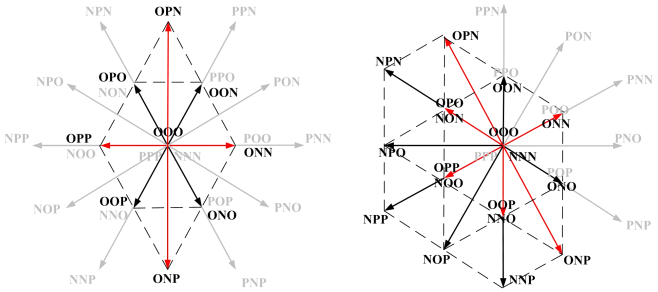


Fig. 9. Space vector diagram of open-switch faults in S_{A1}, S_{A4} and S_{D1}: (a) inverter 1; (b) inverter 2.

The fourth condition in Table II is that both P and N levels are missing in one phase leg of the first inverter, and both P and N levels are missing in one phase leg of the other inverter. Fig. 10 shows the voltage vector distribution when open-switch faults occur in S_1 and S_4 in both phase A and phase D. It is observed that all redundant small voltage vectors are missing in the two inverters. Besides, the same types of small voltage vectors are almost distributed within the same half plane. So, the controllability of small voltage vectors for mid-point voltage in DC link is very limited and more difficult compared to the second condition in Table II. To avoid DC deviation of mid-point voltage, a specific strategy is proposed as shown in Fig. 11. There will be two schemes of voltage synthesis in each sector. In each sector, there are totally N_{s1}+N_{s2} switching cycles. The number of switching cycles of scheme 1 is N_{s1} and the number of switching cycles of scheme 2 is N_{s2} for each sector. A closed-loop compensation is designed to generate value for N_{s1}, as shown in Fig. 12. The voltage vector selection for voltage synthesis is plotted in Fig. 13. For scheme 1 in sector I, medium voltage vector OPN and small voltage vector ONN are used to synthesize OON, which will be used together with ONN to synthesize voltage reference if $u_{mid} \le U_{dc}/2$. Otherwise, small voltage vectors ONN and OON are used directly to synthesize voltage reference in scheme 1. For scheme 2 in sector I, OPN and ONN are used to replace OON no matter what value of u_{mid}. For scheme 1 in sector II, ONN and OPN are used to synthesize OON, which in turn works together with OPO for synthesizing voltage reference if $u_{mid} \le U_{dc}/2$. Otherwise, OPN and OPP are used to synthesize OPO, which turn works with OON for voltage synthesis in scheme 1. For scheme 2 in sector II, ONN and OPN are used to synthesize

OON, and OPN and OPP are used to synthesize OPO. Then, the two newly synthesized voltage vectors are used for synthesis of reference voltage.

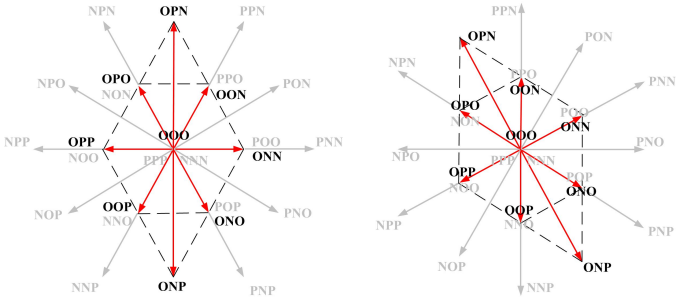


Fig. 10. Space vector diagram of open-switch faults in one phase leg: (a) faults in S_{A1} and S_{A4} of inverter 1; (b) faults in S_{D1} and S_{D4} of inverter 2.

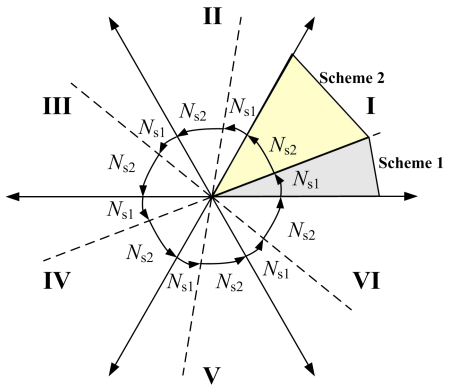


Fig. 11. Description of split regions for Type III-2 remedial scheme.

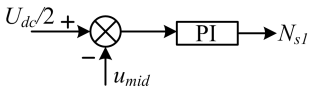


Fig. 12. Closed-loop controller for adjustment of mid-point voltage reference in remedial scheme III-1.

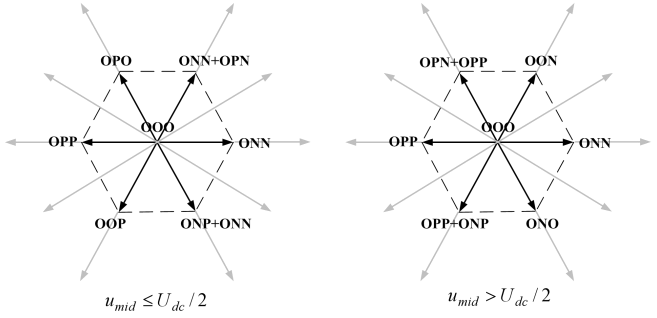


Fig. 13. Vector selection of Scheme 1: (a) $u_{mid} \le U_{dc}/2$; (b) $u_{mid} > U_{dc}/2$.

Table III shows the distribution of voltage vectors when open-switch faults occur in two phase legs, which are located in one inverter. As shown in Fig. 14(a), when S_{A1} and S_{B1} are with faults of the first inverter, P levels are missing in both phase A and phase B. The modulation index is to be reduced. The redundant small voltage vectors will compensate fluctuations in mid-point voltage of DC link with remedial scheme II. Under other conditions, the faulty phase legs have to be removed from system. For example, when P level in phase A and N level in phase B, the voltage vector distribution is shown in Fig. 14(b). The whole faulty inverter must be cut off and the other healthy inverter still works as a three-phase system. This solution is defined to be Type-V scheme.

TABLE III OPEN-SWITCH FAULTS IN TWO PHASE LEGS OF ONE INVERTER

Missing Levels of Phase Leg 1	Missing Levels of Phase Leg 2	Remedial Scheme
P(N)	P(N)	II
Others		V

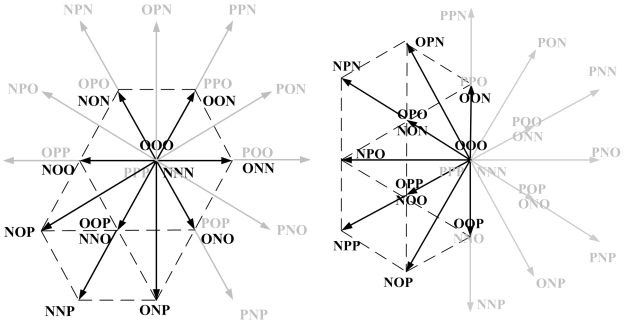


Fig. 14. Space vector diagram of open-switch faults in two phase legs of one inverter: (a) inverter 1 with faults in S_{A1} and S_{B1}; (b) inverter 1 with faults in S_{A1} and S_{B4}.

D. Faults in Three Phase and More Phase Legs

Table IV presents categories of voltage vectors when open-switch faults occur in three phase legs. Fig. 15 shows the voltage vector distribution when P levels are missing in the first inverter while N level is missing in the second inverter. The drive system can use the remaining small voltage vectors inside inner hexagon. Since two inverters lose different types of small voltage vectors, the fluctuation in mid-point voltage of DC link caused by missing small voltage vectors can be compensated by redundant small vectors of the other inverter. The remedial scheme is classified to be Type-II remedial scheme. Under other conditions, same types of small voltage vectors may be lost and distributed in an overlapping area in two inverters. Alternatively, three phase legs in one inverter may suffer from loss of P or N levels. Large oscillation may appear in mid-point voltage of DC link. Therefore, the inverter with faults in two or more phase legs has to be removed from the system. The other inverter will work as a three-phase system with remedial scheme V. It should be noted that when P or N level is missing in one phase leg of remaining inverter, the three-phase four-switching operation can be used [31].

TABLE IV OPEN-SWITCH FAULTS IN THREE PHASE LEGS

Missing Levels of inverter 1	Missing Levels of inverter 1	Missing Levels of inverter 2	Remedial Scheme
P(N)	P(N)	N(P)	II
Others			V

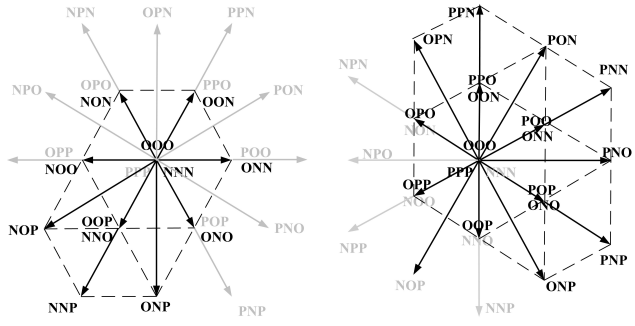


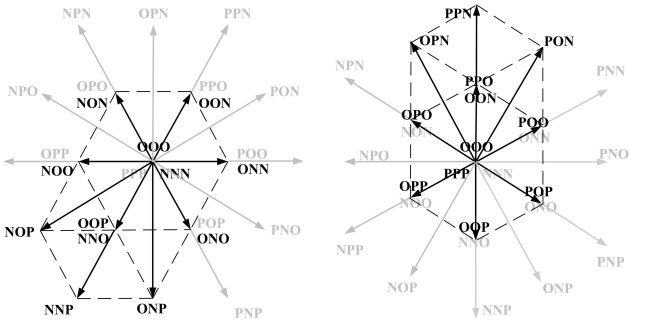
Fig. 15. Space vector diagram of open-switch faults in S_{A1}, S_{B1} and S_{D4}: (a) inverter 1; (b) inverter 2.

Similar to faulty conditions in three phase legs, the remedial operation with faults in four phase legs becomes very difficult. As shown in Table V, there is only one condition available for

remedial operation, where P levels are missing in two phase legs of the first inverter and N levels are missing in two phase legs of the second inverter. The two inverters lose different types of small voltage vectors, and the fluctuations in mid-point voltage of DC link can be compensated by small voltage vectors of the other inverter. The voltage vector distribution is shown in Fig. 16. The modulation index must be reduced, and the remedial strategy is Type-II scheme. When faults occur in three phase legs of the first inverter and in one phase leg of the second inverter, the first inverter should be removed, and the second converter can keep operation with Type-V scheme. Also, the three-phase four-switch operation is adopted when P or N level is missing in the second inverter. When faults occur in two phase legs of the first inverter and two phase legs of the second inverter, both of the two inverters must be stopped. When open-circuit faults occur five or more phase legs, the drive system must be stopped due to too many lost voltage vectors.

TABLE V OPEN-SWITCH FAULTS IN FOUR PHASE LEGS

Missing Levels of inverter 1	Missing Levels of inverter 1	Missing Levels of inverter 2	Missing Levels of inverter 2	Remedial Scheme
P(N)	P(N)	N(P)	N(P)	II
Missing Levels of inverter 1	Missing Levels of inverter 1	Missing Levels of inverter 1	Missing Levels of inverter 2	Remedial Scheme
Any	Any	Any	Any	V



(a) (b)

Fig. 16. Space vector diagram of open-switch faults in S_{A1}, S_{B1}, S_{D4} and S_{E4}: (a) inverter 1; (b) inverter 2.

IV. SCHEMES OF SHORT-CIRCUIT FAULTS

A. Fault-isolation Circuit

Five different fault-isolation schemes have been presented and reviewed in [32]. For those schemes, additional hardware such as fuses, semiconductor-controlled rectifier (SCR), and relay could be combined to isolate short-circuited power switches. Thus, the short-circuit fault can be converted into the open-circuit fault. If fault-isolation circuits are used for each power switch, there will be a large number of additional hardware for the four power switches in one phase. This paper is to make full use of remaining switching states for fault-tolerant operation while using simple fault-isolation circuits. Fig. 17 shows the fault-isolation circuit for strategies in this paper, where F_{u1} and F_{u2} present two fast fuses connected to S_1 or S_4 in series, and R presents the relay at output side of the phase leg. The fault-isolation circuit is simple without using semiconductor-controlled rectifier (SCR) and the related triggering signals.

When S_1 is with short-circuit fault, and the relay R is tripped off and the phase leg is removed from the system. Under this condition, S_2, S_3, and S_4 are kept off. When S_4 is with short-circuit fault, the similar solution can be used. When both S_1 and S_4 are with short-circuit faults, fast fuses F_{u1} and F_{u2} will be burned out, and they are isolated from the system. It is mentioned that the fault-isolation solution is also suitable for hybrid switching faults in one-phase leg. For example, when S_1 is with short-circuit fault and S_2 is with open-circuit fault, the phase leg can be removed by tripping off relay R. When S_2 is with short-circuit fault and S_3 is with open-circuit fault, the phase leg can be removed by tripping off relay R.

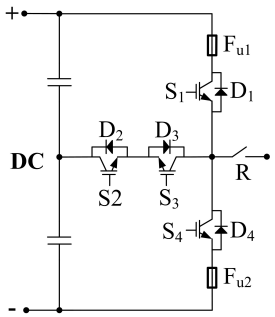


Fig. 17. Fault-isolation circuit.

B. Short-Circuit Faults in S_2 or S_3

When S_2 or S_3 switch fails in short-circuit fault, the corresponding phase leg must be clamped to O level by turning on switch signals of the other switch in clamping route. On the other hand, the half-bridge switches S_1 and S_4 in the faulty phase leg must be turned off in order to avoid short-circuit current. Thus, the faulty phase leg is converted to the conditions where P and N levels are missing. The conditions can be classified to the third condition in Table I, and the third and the fourth condition in Table II. The corresponding remedial schemes in Table I and II are valid for those conditions.

C. Short-Circuit Faults in S_1 or S_4

When S_1 or S_4 switch is with short-circuit fault in one phase leg, this leg is removed. The reason lies in that both O and N/P levels are prohibited in this phase leg. Thus, fault-tolerant control of open-phase condition has to be used. This remedial scheme can be classified as Type-IV scheme in section III. In [25], a fault-tolerant control is proposed for open-phase faults in dual three-phase PMSM drive with VSD. Based on modeling of electrical machine, the voltage perturbation is derived and compensated for terminal voltages of remaining phase legs directly. Thus, torque oscillation will be suppressed without changing the switching strategy of remaining voltage vectors. In this paper, this method is newly designed based on the double three-phase SVM modulation, which is in turn applied for fault conditions where both short-circuit faults and open-circuit switch faults occur simultaneously. It is convenient to implement for faulty conditions where short-circuit faults and open-circuit faults occur in switches simultaneously. In this method, while analyzing voltage vectors on space vector diagram, the removed phase leg is assumed to still exist. Instead, the voltage compensation will be added to voltage references of remaining phase legs. Thus, Type-IV remedial scheme can be converted to Type-I and Type-II remedial schemes.

For example, when S_1 or S_4 is with short-circuit fault in phase F, the phase leg of phase F has to be removed by using protection measures. Meanwhile, S_1 is with open-circuit fault in phase A. Phase F is assumed to be still exist in the drive. Thus, the voltage vectors distribution in faulty inverter will be similar

to that in Fig. 4(b). The remedial scheme will become Type-II scheme. Based on mathematical modelling, the phase current constraints $i_A + i_B + i_C = 0$ and $i_D + i_E + i_F = 0$ and terminal voltage constraints of windings $u_A + u_B + u_C = 0$ and $u_D + u_E + u_F = 0$ are still valid under open-phase conditions. Thus, the terminal voltage of phase F, u_F is derived as [24]:

$$\begin{aligned} u_F &= -R_s(i_D + i_E) - \frac{d}{dt}(\psi_D + \psi_E) \\ &= -\frac{\sqrt{3}}{3}[u_{BC} - R_s(i_B - i_C) - L_{ls}\frac{d}{dt}(i_B - i_C)] \end{aligned} \tag{4}$$

Different from the VSD based modulation in [25], the compensation of terminal voltages on double three-phase windings are derived based the double three-phase SVM in this paper:

$$\begin{bmatrix} u_{\alpha 1} \\ u_{\beta 1} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} = \begin{bmatrix} \frac{2}{3}u_{AB} + \frac{1}{3}u_{BC} \\ \frac{\sqrt{3}}{3}u_{BC} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} u_{\alpha 2} \\ u_{\beta 2} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{3}u_{DE} \\ -u_F \end{bmatrix} \tag{6}$$

The voltages on α-axis are not changed before and after faults. After fault, the voltage component on β-axis of the first inverter $u_{\beta 1}$ is still equal to $\sqrt{3}u_{BC}/3$. But $u_{\beta 2}$ is changed from $\sqrt{3}u_{BC}/3$ to $-u_F$ after fault, as shown in Eq. (6). To keep the total value of voltage components on β-axis namely $u_{\beta 1} + u_{\beta 2}$ same as that before fault, the voltage reference $u_{\beta 1}$ of healthy winding has to be modified to compensate the change in $u_{\beta 2}$. Thus, the compensation on $u_{\beta 1}$ is derived to be:

$$\Delta u_{\beta 1} = \frac{\sqrt{3}}{6}[R_s(i_B - i_C) + L_{ls}\frac{d}{dt}(i_B - i_C)] \tag{7}$$

By adding the voltage compensation $\Delta u_{\beta 1}$ to voltage reference of the healthy winding, the drive can provide smooth torque without changing modulation strategy. But it is noted that the phase currents become asymmetric with the proposed control method.

V. Experimental Verification

The experiments have been carried out on a laboratory prototype of T-3L inverter fed dual three-phase PMSM drive to verify the effectiveness of the proposed schemes. In the experiments, the DSP (TMS-F28335) performs the control algorithm and generates the PWM signals. A PM generator is coupled to the dual three-phase PMSM machine to act as the electric load. The load value is set by using the load control system. The real rotor position is measure by photoelectric encoder, so that the accuracy can be guaranteed. In the experiments, open-circuit faults of power switches are achieved by forcing the driving signals on specific IGBT devices to be low. On the other hand, short-circuit faults of power switches are constructed by forcing the driving signals on the corresponding IGBT devices to be high all along. The system parameters are shown in Table VI.

TABLE VI Parameters of Experimental Setup

Name	Value
Pole pair number	3
q-axis inductance	6.21 mH
d-axis inductance	6.21 mH
PM flux (amplitude)	0.2 Wb
Resistor	0.21 Ω
DC link capacitors	1000 uF
DC link voltage	200V
Given speed	1000 rpm
Load Torque	10 Nm
Switching frequency	5 kHz

Firstly, the performance of the proposed fault-tolerant control is verified when open-circuit faults occur in one phase leg. When switches S_{A2} or S_{A3} is with open-circuit fault, the level O is missing in phase A. As shown in Fig. 18, the phase current waveforms suffer from distorted waveforms and there is slight oscillation in torque waveforms. It can be observed in Fig. 18(a) that, the amplitude of the current in faulty phase decreases and zero current values occurs for a short period of time. The reason is that the O level is forced into other levels in the states shown in Fig. 3(b) and Fig. 3(e), and then the average amplitude of output voltage will be decreased. Under normal operation, the output voltage changes between P level and O level in each switching period, when the phase current i_a is larger than zero. If S_{A2} is with open-circuit fault, the O level is forced to N level, as shown in Fig. 3(b). Since the output voltage changes between P level and N level in each switching period, the amplitude of output voltage will be decreased and the amplitude of current will be reduced accordingly. Therefore, the phase current i_a will decrease to zero value for a short period. On other hand, the phase current i_a is negative, and the switching actions between O level and N level will be forced to switching actions between P level and N level, as shown in Fig. 3(e). Thus, the phase current will be increased to zero for a short period. By using P and N levels to synthesize the missing O level with Type-I scheme, the phase currents become symmetric and the torque becomes smooth. In Fig. 18(d), the fluctuation of mid-point voltage in DC link is ΔU_c, which is expressed by $\Delta U_c = U_{Clower} - U_{Cupper}$.

Then, the performance is investigated for the condition in Fig. 19 where S_{A1} is with open-circuit fault. It can be observed in Fig. 19(a) that the amplitude of the current i_a remains zero in positive half cycle. Under normal condition, the output voltage changes between P level and O level in each switching period within the positive half cycle. But if S_{A1} is with open-circuit fault, the P level is forced into O level, as shown in Fig. 3(a). Therefore, the output voltage of phase A remains to be O level in positive half cycle, which results in the zero current value. As analyzed before, the Type-II remedial strategy is used. The phase currents and the torque are also controlled well. However, it can be observed from Fig. 19(d) that the oscillation of mid-point voltage becomes larger with Type-II scheme. To evaluate control performance of mid-point voltage of DC link, an indicator u_{mid_D} is defined as percentage of maximum deviation value of mid-point voltage of DC link to half of the total DC link voltage. In Fig. 19(d), the value of u_{mid_D} increases from 6% to 8% after using fault-tolerant control. The reason is due to that the missing small voltage vector will be forced into another vector without fault-tolerant control, which has similar impact on fluctuation of mid-point voltage in DC link. As shown in Fig. 3(a), missing of P-type small voltage vector PPO forces another P-type voltage vector OPO valid

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without fault-tolerant control. However, the location of vector OPO is different from that of the vector PPO in vector distribution of Fig. 4. So, there will be distinct torque ripples and distorted phase currents in Fig. 19(a) and (b) without fault-tolerant control. On the other hand, the redundant small voltage vector OON replaces the missing vector PPO with Type-II remedial strategy. Thus, the circular trajectory will be provided by using the proposed fault-tolerant strategy. The torque ripple is reduced and the phase currents become sinusoidal and symmetrical with fault-tolerant control in Fig. 19(a) and (b). But the vector OON has negative impact on mid-point voltage of DC link. So, larger fluctuation appears in mid-point voltage of DC link with fault-tolerant control, as shown in Fig. 19(d). Fortunately, owing to controllability of redundant small voltage vectors in the healthy inverter, the mid-point voltage of DC link can still be controlled well with Type-II scheme.

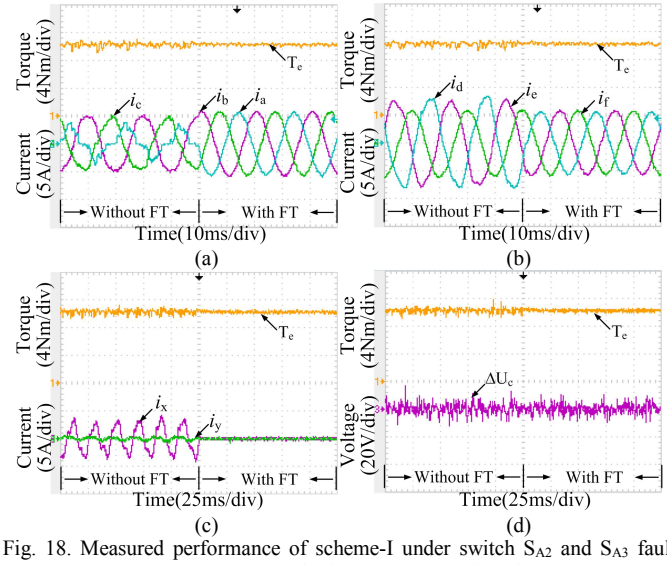

Fig. 18. Measured performance of scheme-I under switch S_{A2} and S_{A3} fault (1000rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage deviation in DC link.

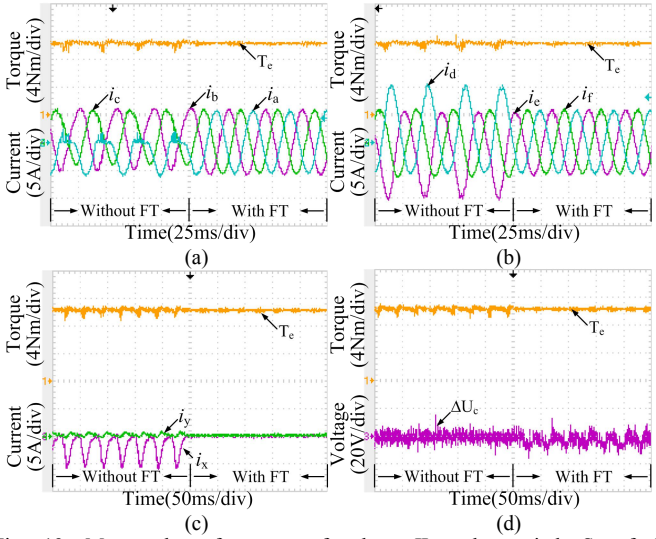

Fig. 19. Measured performance of scheme-II under switch S_{A1} fault (600rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage deviation in DC link.

When S_{A1} and S_{A4} are with open-circuit fault, both P and N voltage vectors are missing, and the experimental results are shown in Fig. 20. Since all redundant voltage vectors are missing, there exist clear ripple and distorted phase currents without fault-tolerant control. It can be observed in Fig. 20(a) that the amplitude of the current i_a almost remains zero under the faulty condition. Under normal operation, the output voltage changes between P level and O level in positive half cycle and changes between O level and N level in negative half cycle. If both S_{A1} and S_{A4} are with open-circuit fault, the P level and N level will be forced to O level as shown in Fig. 3(b) and Fig. 3(e), respectively. Therefore, the output voltage of phase A remains to be O level, which results in the zero current. As mentioned in section III, the Type-III scheme is used for fault-tolerant operation. The red voltage vectors in Fig. 5(a) are used to synthesize the voltage reference, where two medium voltage vectors participate in voltage synthesis. The torque ripple and distorted phase currents are mitigated effectively. Similarly, in Fig. 20(d), the oscillation in mid-point voltage in DC link is larger with fault-tolerant control since the redundant voltage vectors have negative effects in controlling mid-point voltage. By adopting medium voltage vectors to save use of redundant small voltage vectors, the oscillation in mid-point voltage of DC link is suppressed smaller. But the value of u_{mid_D} still increases to 8% after using fault-tolerant control in Fig. 20(d). As mentioned in Section IV, when S_{A2} or S_{A3} is with short-circuit faults, S_{A1} and S_{A4} must be switched off. Thus, output voltage of phase A must be forced as O level. The similar performance can be obtained as shown in Fig. 20.

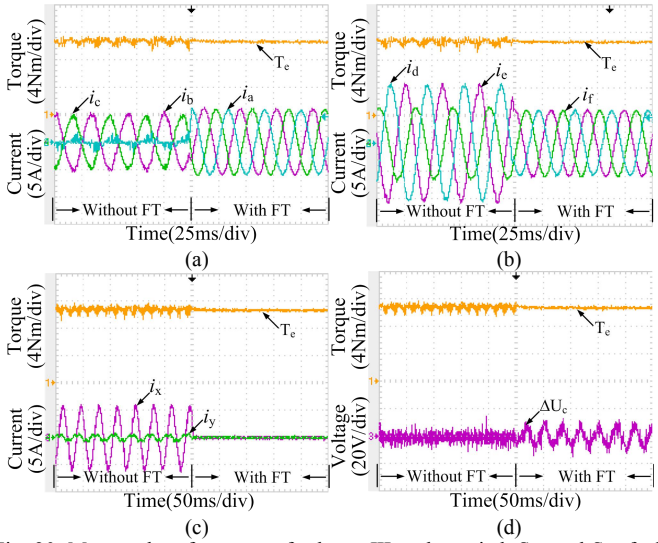

Fig. 20. Measured performance of scheme-III under switch S_{A1} and S_{A4} fault (600rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage deviation in DC link.

Secondly, the performance of the proposed fault-tolerant control is investigated for open-circuit faults in two phase legs. When S_{A1} and S_{D1} are with open-circuit faults, P voltage vectors are lost in both phase A and phase D. As shown in Fig. 21(a), the mid-point voltage in DC link not only has clear oscillation but also is deviated to the lower end. By using medium voltage vectors, the fluctuation in mid-point voltage of DC link can be mitigated, and the torque ripple becomes smaller, as shown in Fig. 21(b). It should be noted that the torque fluctuations in Fig. 21(a) and Fig. 21(b) under fault-tolerant operation are both caused by unexpected oscillations of DC-link voltage. Therefore the distortion of phase currents can be further mitigated by dynamical adjusting dwelling time with Eqs. (2-3). Thus, the torque ripple is further reduced in Fig. 21(c) even with similar fluctuation in mid-point

voltage as Fig. 21(b). However, there still exist deviation in mid-point voltage of DC link, which reduces maximum modulation index of inverter. Finally, the introduction of closed-loop control in Fig. 8 helps moving average of mid-point voltage u_{mid} to $U_{dc}/2$ in Fig. 21(d), in such a way that not only torque ripple is suppressed, but also the fluctuation and deviation in mid-point voltage of DC link are mitigated. It should be noted that the transition actions between P and N become more frequent and the output voltage harmonics will become larger slightly by using medium voltage vector to participate in voltage synthesis. But the voltage change within one sampling interval would be attenuated by filtering effect of motor inductances. With four different fault-tolerant schemes, the corresponding values of u_{mid_D} are 27%, 21%, 21% and 15%, respectively. When S_{A2} or S_{A3} is with short-circuit fault and S_{D1} are with open-circuit faults, the same remedial strategy can be used, and the same performance can be obtained as shown in Fig. 21.

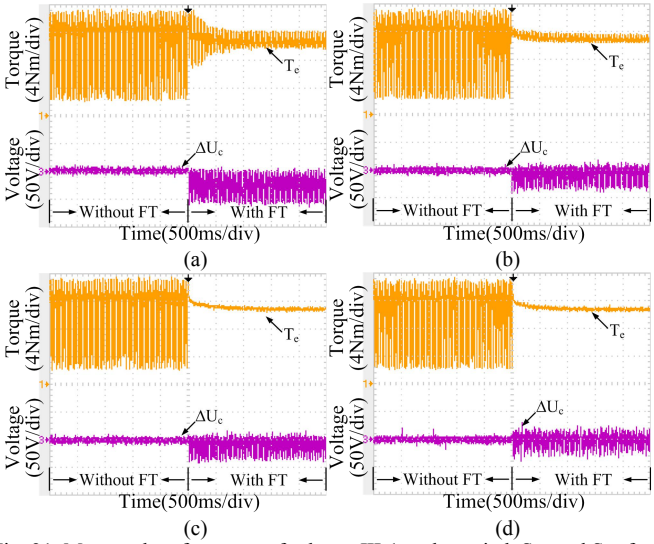

Fig. 21. Measured performance of scheme III-1 under switch S_{A1} and S_{D1} fault (600rpm-10Nm): (a) conventional scheme; (b) only using medium voltage vectors for synthesis; (c) with medium voltage vectors and dwelling time adjustment; (d) with medium voltage vector, dwelling time adjustment and closed-loop control of average of mid-point voltage in DC link.

Fig. 22 shows the measured performance of Type III-2 remedial scheme for the condition where S_1 and S_4 are with open-circuit faults in both phase A and phase D. As expected, it can be observed in Fig. 22(a) and Fig. 22(b) that the amplitudes of the currents i_a and i_d are around zero when S_1 and S_4 are with open-circuit fault in both phase A and phase D. The faulty phases have a 30-degree shifted angle and their interactions with other phases are different. Thus, i_a and i_d exhibit different waveforms. By using the proposed Type III-2 scheme in Fig. 11-13, the smooth torque is obtained and oscillation of mid-point voltage of DC link is suppressed effectively in Fig. 22. The value of u_{mid_D} is controlled below 23%. Instead of ΔU_c, the mid-point voltage of DC link U_{Clower} is plotted in Fig. 22(d) since the fluctuation in mid-point voltage of DC link is very large. Besides, the phase currents are controlled symmetric. Similarly, when S_{A2} or S_{A3} is with short-circuit fault and S_{D2} or S_{D3} is with short-circuit fault, both P level and N level will be lost in phase A and phase D. The scheme III-2 could also be used, and the same performance will be provided as shown in Fig. 22.

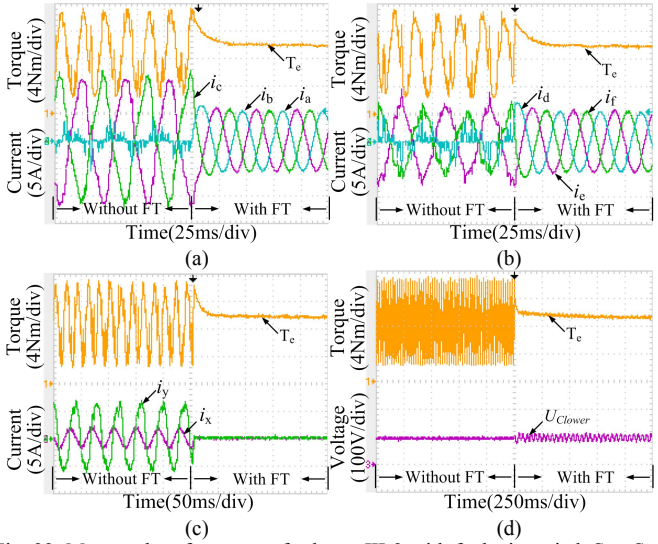

Fig. 22. Measured performance of scheme III-2 with faults in switch S_{A1}, S_{A4}, S_{D1} and S_{D4} fault (500rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage in DC link.

Fig. 23 verifies the drive performance when S_{A1}, S_{B1}, S_{D4} and S_{E4} are with open-circuit faults. The P levels are missing in phase A and phase B, while the N levels are missing in phase D and phase E. So, it can be observed in Fig. 23(a) and Fig. 23(b) that the amplitudes of the current i_a and i_b are around zero in positive half cycle and the amplitudes of the current i_d and i_e are around zero in negative half cycle. As aforementioned, the Type-II remedial strategy is used. By reducing modulation index, the good operation performance is provided in the drive. The value of u_{mid_D} is 9% in Fig. 23(d).

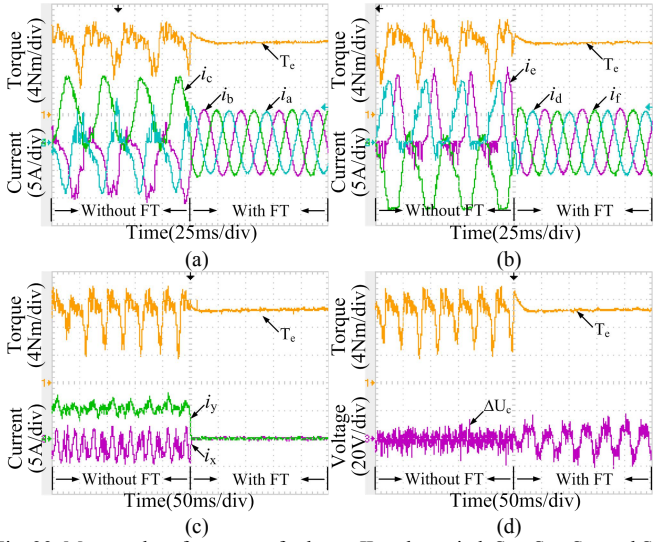

Fig. 23. Measured performance of scheme-II under switch S_{A1}, S_{B1}, S_{D4} and S_{E4} fault: (600rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage deviation in DC link.

Finally, the proposed voltage compensation control method is validated for the condition where short-circuit faults occur in S_{F1} and S_{F4} and open-circuit fault occur in S_{A1} simultaneously. Under this condition, phase F has to be removed and open-phase operation should be used. Fig. 24 shows the drive performance. In Fig. 24(a), the amplitude of the current i_a is around zero in positive half cycle because of open-circuit fault in S_{A1}. In Fig. 24(b), the amplitude of the current i_f is zero because phase F is removed from the system. It can be observed that the torque ripple is suppressed effectively after using voltage

compensation deduced in Eq. (6). It should be noted that the remedial Type-IV scheme for open-phase operation can be simplified to Type-II scheme by using the proposed method. Under open-phase conditions, it is observed that the phase currents are controlled asymmetric with the proposed remedial strategy. Since the DC link capacitor values and load torque are unchanged in post-fault operation, the DC-link voltage will not increase under post-fault operation despite of slight fluctuation in mid-point voltage of DC link.

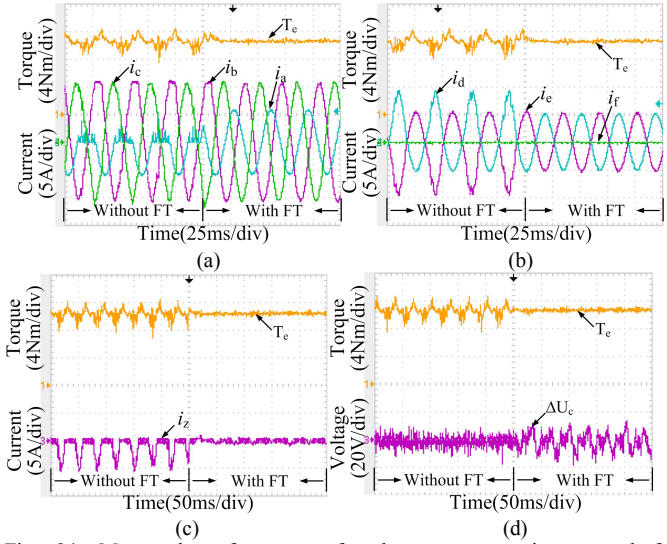

Fig. 24. Measured performance of voltage compensation control for open-circuit fault in S_{A1} and open-circuit fault in phase-F simultaneously: (600rpm-10Nm): (a) torque and phase currents; (b) phase currents; (c) harmonic currents; (d) mid-point voltage deviation in DC link.

VI. Conclusion

This paper investigated different switch faults and the corresponding remedial strategies for T-3L inverters fed dual three-phase PMSM motor drives comprehensively. Both open-circuit faults and short-circuit faults of power switches are discussed. According to fault severity, the open-switch faults are classified into five categories, and their remedial strategies are defined as Type-I to Type-V schemes, respectively. The suppression of torque oscillation and stabilization of mid-point voltage in DC link are main challenges for fault-tolerant control. For Type-I schemes, the maximum modulation index and load ability are unchanged. Instead, the maximum modulation index has to be reduced for Type-II schemes due to loss of some large and medium voltage vectors. For Type-III schemes, quite a few small voltage vectors are lost in two three-phase inverters, and the controllability of mid-point voltage in DC link becomes less. Hence, the medium voltage vectors are adopted to reduce the usage of small voltage vectors with negative impacts on mid-point voltage in DC link. While loss of small voltage vectors become severe under some conditions, two modified versions, namely Type III-1 and Type III-2 are proposed to improve the performance in mitigating both DC deviation and oscillation of mid-point voltage in DC link. The Type-IV schemes are defined as conditions where faulty phase legs are removed, and the Type-V schemes are conditions where one three-phase inverter is removed totally.

On the other hand, short-circuit faults in switches are classified into faults in clamping switches of S_2 and S_3 and in half-bridge switches of S_1 and S_4. The former conditions are equalized to open-switch conditions where both P and N voltage levels are missing. For the later condition, the related phase leg must be removed. A voltage compensation control method is proposed to derive voltage perturbation on remaining phase legs to mitigate torque oscillation induced by asymmetric operation. The switching modulation is unchanged by ignoring removal of phase leg. The remedial strategies for simultaneous occurrence of short-circuit and open-circuit faults in switches are thus obtained. It should be mentioned that control structure of the proposed fault-tolerant strategies is unchanged, which is same as that of normal condition. The reconstruction of voltage synthesis could be implemented by adjusting triggering signals for power switches. The experiments have been taken to verify validity of theoretical analysis and the proposed schemes.

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