# A 100-145 GHz Area-Efficient Power Amplifier in a 130 nm SiGe Technology

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***Abstract*—A 6-stage, 8-way combining power amplifier (PA) in a 130 nm SiGe BiCMOS technology is designed and measured. This PA has an output power of 12.5 – 15.5 dBm in a frequency range from 100 GHz to 145 GHz, when the input power is about 2 dBm. The small signal gain is 19 dB and the maximum DC power consumption is 480 mW with a supply voltage of 1.87 V. The peak power added efficiency (PAE) is 6.4% in D-band. T-junctions are utilized to combine and divide millimeter-wave power. To reduce the PA's loss and chip area, neither a Wilkinson power combiner/divider nor a balun is applied. The chip size is 0.53 mm$^2$.**

***Keywords—D-band, Power amplifier, SiGe, BiCMOS***

## I. INTRODUCTION

The progress of silicon based technologies allows for the design of circuits operating beyond 100 GHz. These SiGe circuits are able to build high-data communication systems, radar sensors and imaging systems. The performance of these millimeter-wave systems are often limited by the related low output power due to the scaling down in the transistor size and lowering of the breakdown voltage.

To get a large output power, circuit designers often use several amplifier units and combine their outputs via an *n*-way power combiner (*n* is the number of units). Taking a state-of-the-art PA as an example [1], 20.8-dBm output power is obtained by combining 8 amplifier units in-phase. The input power is 10.8 dBm, which is fed into the amplifier units by a network comprising a Wilkinson power divider, transmission lines, and T-junctions, as shown in Fig.1. Another 8-way combining PA in [6] consists of differential amplifier units, where baluns are used to combine and divide millimeter-wave power. The PA in [6] has an output power of 22 dBm, driven by a 17.6-dBm input power. The peak power added efficiency (PAE) of the PA in [6] is 3.6%, which is less than 7.6% for the PA in [1], partly because the balun's loss is larger than that of a Wilkinson power divider.

As shown in Fig. 1, the PA [1] arranges 4 vertical-align amplifier units on both sides of the power combiner, to shorten the length of the transmission lines connecting amplifier units and a point of converging "o" thus minimizing the loss. Unfortunately, such arrangement needs a "bulk" power distribution network. Two 1.6 mm long transmission lines at input alone contribute at least 2-3 dB loss, because a 50-Ω transmission line on a Silicon has a loss of 0.9-1.2 dB/mm in 100-150 GHz [1].

In this paper, a compact 8-way combining power amplifier is designed, aiming for large output power and high PAE, as well as a wide bandwidth. In the designed PA, the millimetre-wave is divided and combined via T-junctions and impedance matching networks without using a Wilkinson power divider or a balun.

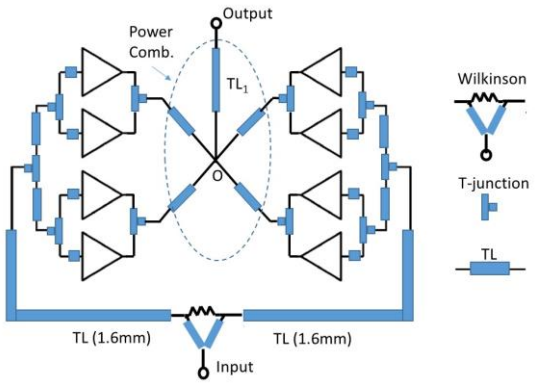


Fig. 1. Schematic of a 8-way combining power amplifier [1]

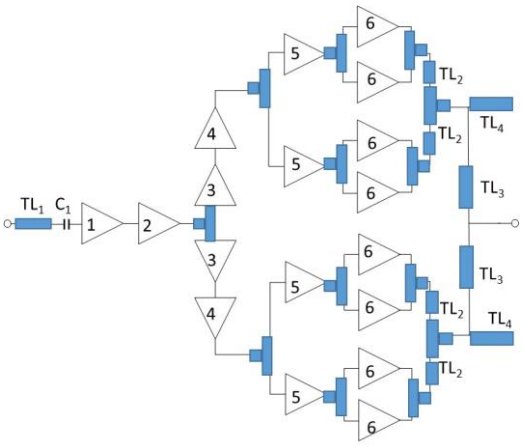


Fig. 2. Schematic of the 6-stage and 8-way combining power amplifier.

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## II. Circuit Topology and Design

### A. Circuit topology

The schematic of the presented PA is shown in Fig. 2. Both the 1st stage and the 2nd stage consist of a single amplifier unit. The 3rd stage and the 4th stage have two identical amplifier units. The 5th stage consists of four identical amplifier units, and the 6th stage consists of 8 identical amplifier units. Amplifier units at different stages have the same circuit topology, but their components have different parameters. The schematic of the amplifier unit is shown in Fig. 3(c).

The input port is connected to the 1st stage via an impedance matching network comprising $TL_1$ and $C_1$. Then, the millimeter-wave power is divided by several "T-junctions". A T-junction has less loss and occupies a smaller chip area than a Wilkinson power divider used in the PA [1]. The cascaded stages are connected by interstage matching networks.

At the last stage, 8 amplifier units are aligned vertically. The outputs of 4 amplifier units on the top are combined by using two T-junctions and two transmission lines, TL2 (140 µm), then connected to the output port via an impedance matching circuit consisting of $TL_3$ (114 µm) and an open stab $TL_4$ (116 µm). The outputs of other 4 amplifier units on the bottom are combined in the same way.

### B. Interstage matching network

The most commonly used interstage matching networks are: (a) L-type, (b) π-type, and (c) T-type, as shown in Fig. 3. In this design, the interstage matching network is also used for the connection between stages. The only suitable one is the T-type matching network, where two transmission lines ($TL_1$ and $TL_2$) separate the input and output with certain distance.

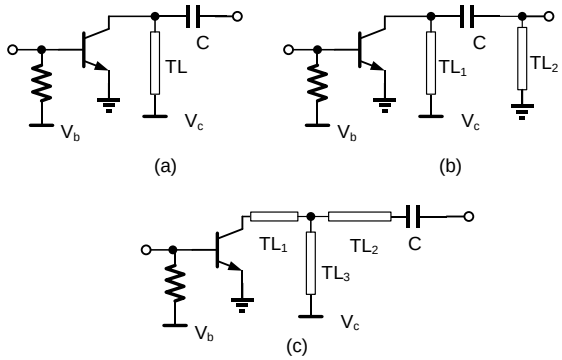


Fig. 3. Schematic of amplifier unit including interstage matching network (a) L-type, (b) π-type, and (c) T-type.

As an example, the layout of the 3rd and the 4th stages is depicted in Fig. 4. Those stages split a single input into 4 vertical-aligned outputs. Two amplifier units at the 3rd stage separate the outputs in the vertical direction. In the 3rd stage, the length of $TL_1$, $TL_2$, and $TL_3$ are 110 µm, 14 µm, and 34 µm, respectively. In the 4th stage, the length of $TL_1$, $TL_2$, and $TL_3$ are 140 µm, 20 µm, and 40 µm, respectively. The length of the TLs in the matching network are optimized for high output power and frequency bandwidth. If the TLs are too long, they can be folded. However, if the TLs are too short, an extra amplifier stage has to be added. Furthermore, the advantage of the T-type matching network is the potential for designing a wider bandwidth PA, which has been investigated in [7].

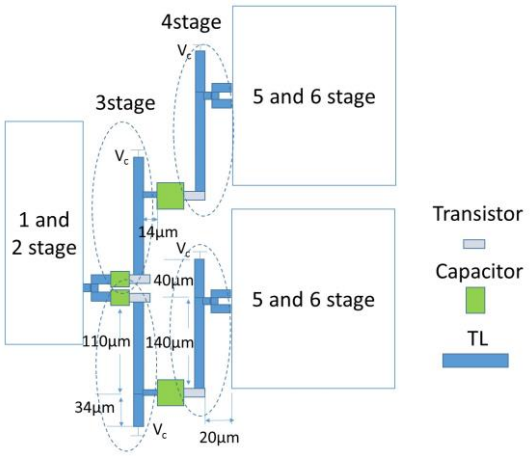


Fig. 4. Layout arrangement

### C. Circuit design

In the design, the transistors' size, base bias voltages, as well as sizes of the capacitors and the length/width of TLs in the matching networks are selected by simulations in Cadence. Optimization is carried out in the simulation, targeting the following: large output power, high PAE, as well as a good impedance matching at the input/output port.

In the optimization, the capacitor model and the TL model provided by foundry are used. For improved accuracy, EM simulations using Sonnet are carried out for all transmission lines and capacitors. The length/width of TLs, as well as the size of capacitor are modified further based on the simulation results.

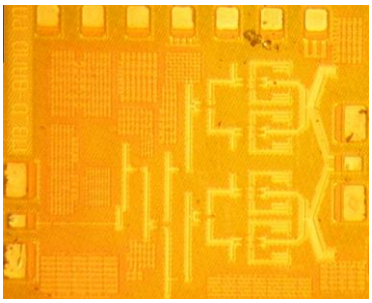

Fig. 5. Chip microphotograph of the power amplifier, size 0.81x0.66mm$^2$ (without pads 0.50x0.53 mm$^2$)

The designed circuit is fabricated in a 130 nm SiGe BiCMOS process provided by Infineon Technologies AG. The chip microphotograph is shown in Fig. 5. The chip area is 0.53 mm$^2$ (0.26 mm$^2$ without pads).

## III. Measurements

Characterization of the PA was done by on-wafer measurements. The measurement setup is shown in Fig. 6. S-parameters and output power are measured by a PNA-X

network analyzer (N5247A) from Keysight. Moreover, WR-10 and WR-6.5 extenders from Virginia Diodes, Inc. are used for W-band and D-band measurements, respectively.


Fig. 6. Measurement setup

For the large-signal S-parameters measurements, a 15 dB attenuator is connected in front of the extender at the chip's output side, in order to prevent saturation of the extender. For the small-signal S-parameter measurements, the attenuator is removed, avoiding overly reducing the reflection signal..

The measured small-signal S-parameters are plotted in Fig. 7. The PA has a maximum S21 of 19.0 dB, and a 35 GHz 3-dB bandwidth from 101 GHz to 136 GHz. The output port reflection coefficient, S22, in D-band (>110GHz) is less than -10 dB, and the input port reflection coefficient, S11, is less -4 dB in D-band. The discontinuity of S11 and S22 at 110 GHz is due to the different measurement setup (WR-10 or WR-6.5 extender) and different RF probes.

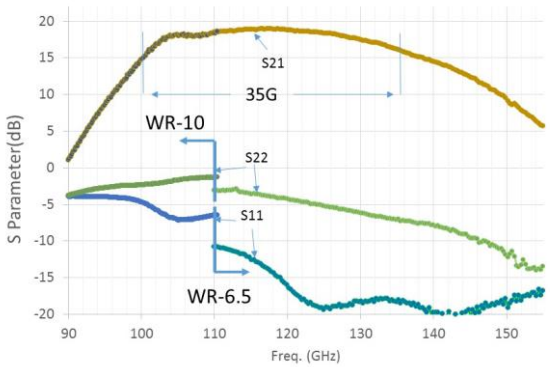


Fig. 7. Measured S-parameters versus frequencies.

For large signal measurements, the input power is kept around 2 dBm, and the frequency is swept from 90 GHz to 155 GHz. The measured output power is plotted in Fig. 8. Variation of the input power gives rise to ripples in the output power in D-band. It can be seen that, in the frequency range from 100 GHz to 145 GHz, the output power varies between 12.5 dBm and 15.5 dBm. Thus, at a large input signal, 3-dB bandwidth is 45 GHz, which is 10 GHz larger than 3-dB bandwidth of S21 at small input signal. This is because of the frequency dependence of the gain compression.

When the input power is swept from -23 dBm to 2 dBm, the output power, and DC power consumption are measured at 110 GHz, 125 GHz, 140 GHz, and 145 GHz, respectively. The measurement results are plotted in Fig. 9 - Fig. 11. Gain compressions at 2 dBm input power are 4.1 dB, 5.4 dB, 1.8 dB, 1.0 dB, at 110 GHz, 125 GHz, 140 GHz, and 145 GHz, respectively. Except at 110 GHz, the output power is not saturated. Unfortunately, in D-band, 2 dBm is the maximum available power in our Laboratory. The maximum DC power consumption of the PA is 480 mW from a 1.87-V supply voltage. The peak PAE is 6.4%.

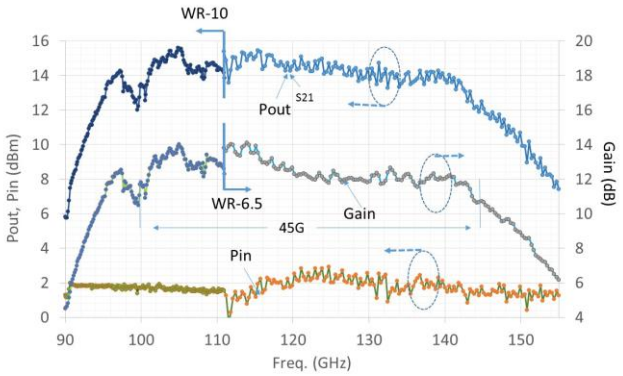


Fig. 8. Measured input/output power and gain versus frequencies at input power around 2 dBm.

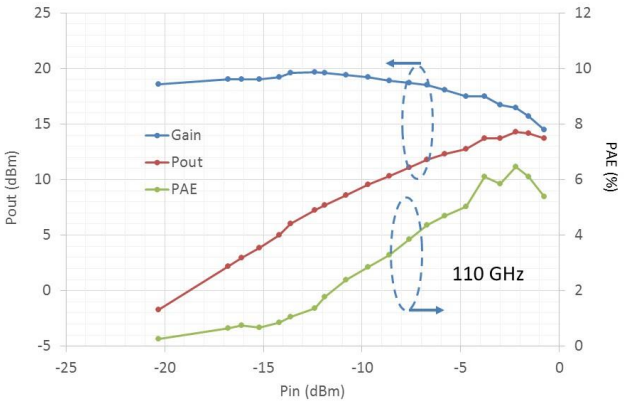


Fig. 9. Measured output power, gain, and PAE versus input power at 110 GHz.

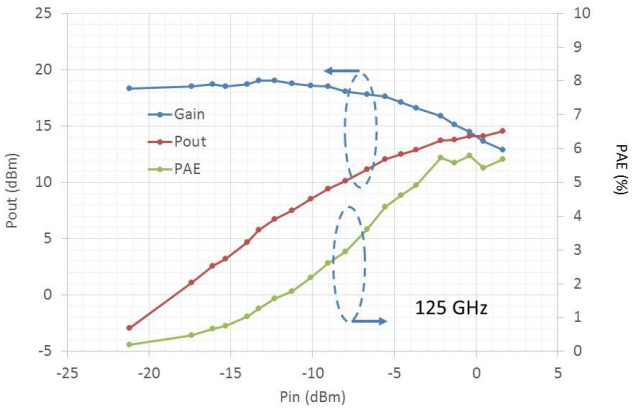


Fig. 10. Measured output power, gain, and PAE versus input power at 125 GHz.

TABLE I

SUMMARY OF SIGE PAS' PERFORMANCE (FREQUENCY>100GHZ)

| Ref. | Process | freq. (GHz) | $BW_{-3dB}$ (GHz) | $S_{21\ max}$ (dB) | $P_{sat}$ (dBm) | PAE (%) | $P_{DC}$ (mW) | Chip Size ($mm^2$) | $P_{sat}$/Aare $mW/mm^2$ | Topology |
|---|---|---|---|---|---|---|---|---|---|---|
| [1] | 90 nm | 122 | 24 | 15 | 20.8 | 7.6 | 1520 | 1.29 | 9.3 | 4-stage, 8-way comb. |
| [2] | 130 nm | 130 | 20 | 24.3 | 7.7 | 6.8 | 84 | 0.30 | 19.6 | 3-cascode stage, 2-way comb. |
| [3] | 130 nm | 160 | 10 | 32 | 10 | -- | -- | 0.39 | 25.6 | 3-cascode stage, 2-way comb. |
| [4] | 130 nm | 152 | 35 | 17 | 8 | 1.6 | 320 | 0.57 | 11.0 | 3-cascode stage, 2-way comb. |
| [5] | 120nm | 120 | 16 | 22.5 | 17.5 | 3.6 | 560 | -- | -- | 3-cascode stage, 2-way comb. |
| [6] | 90 nm | 130 | 35 | 7.7 | 22 | 3.6 | 2220 | 0.62 | 254 | 2-cascode stage, 8-way comb. |
| [7] | 180 nm | 140 | 80 | 24.8 | 11 | 5 | 262 | 0.42 | 29.9 | 4-cascode stage, 2-way comb |
| [8] | 180 nm | 115 | 13 | 20.3 | 6.7 | 1.1 | 403 | 0.40 | 11.6 | 5-comm. base stage, 2-way comb. |
| **This work** | **130 nm** | **120** | **35/45*** | **19** | **15.5** | **6.4** | **480** | **0.53** | **66.9** | **6-stage, 8-way comb.** |

*large input signal

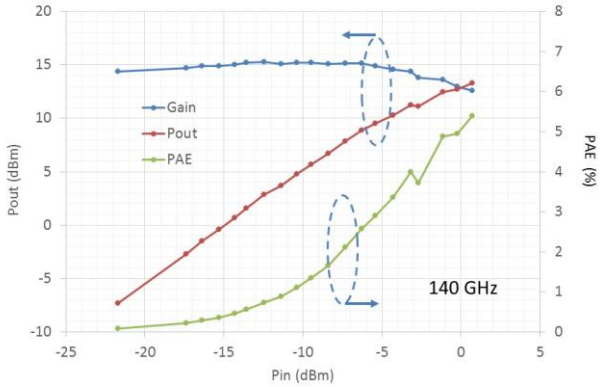


Fig. 11. Measured output power, gain, and PAE versus input power at 140 GHz.

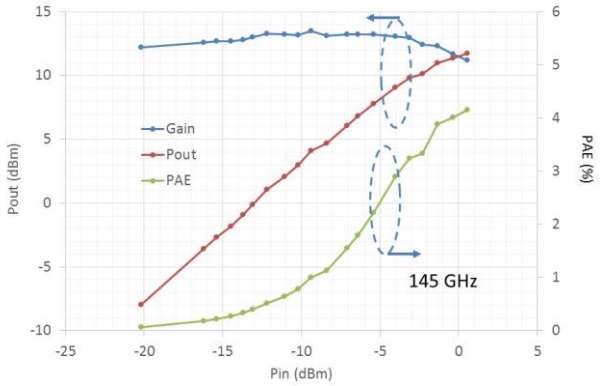


Fig. 12. Measured output power, gain, and PAE versus input power at 145 GHz.

The performance of the PA in SiGe technologies in the literature is listed in Table I. Those PAs operate at frequencies higher than 100 GHz. The presented PA achieves a relatively high output power with a moderate input power, a good PAE, and a wide frequency bandwidth. The chip size is the smallest among 8-way combining PAs. The output power per unit die area is 66.9 $mW/mm^2$, which is the second highest recorded in silicon technology.

## IV. CONCLUSIONS

An 8-way combining PA in 130 nm SiGe BiCMOS technology is designed, where T-junctions and impedance matching networks are used to combine/divide millimeter-wave power without either a Wilkinson power divider or baluns. This compact power amplifier is a suitable building block for a 16-way or even a 32-way combining PA, to increase the output power.

## ACKNOWLEDGMENT

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