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# Conductive atomic force microscopy studies of thin $SiO_2$ layer degradation

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The dielectric degradation of ultrathin (~2 nm) silicon dioxide ($SiO_2$) layers has been investigated by constant and ramped voltage stresses with the conductive atomic force microscopy (CAFM). CAFM imaging shows clearly the lateral degradation propagation and its saturation. Current-voltage characteristics, performed at nanometer scale, show the trap creation rate in function of the stress condition. The critical trap density has been found. © *2006 American Institute of Physics*.
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Silicon oxide is a material of crucial importance for the overwhelming majority of today's active electronic devices. It is chemically stable, it has excellent passivating and dielectric properties and its quality can be consistently controlled during production.[1] The properties of thin $SiO_2$ layers ($\geqslant$2 nm) are well known from many macroscopic measurements, including current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements, internal photoemission, etc.[2,3] In these measurements the microscopic properties are averaged over large areas. With the ongoing miniaturization of electronic devices, the atomic scale feature of the materials used may soon be comparable with the size of the device features themselves, and will affect the performance of the devices. It is, therefore, crucial to investigate the properties of thinner layers of this material at the microscopic level. In this way, scanning probe microscopy based techniques can be useful tools due to their very high lateral resolution. Scanning tunneling microscopy (STM),[4,5] ballistic electron emission microscopy (BEEM),[6,7] and conductive atomic force microscopy[8,9] (CAFM) have already been used to electrically characterize $SiO_2$ films at nanometer scale. Although BEEM and STM may be more spatially resolved than atmospheric AFM techniques, from the experimental point of view they show some drawbacks, such as a specific sample preparation and/or ultrahigh vacuum conditions. In contrast to STM based techniques, when an AFM is provided with a conductive tip (CAFM), electrical and topographical informations can be simultaneously and independently measured on insulating surface with a typical lateral resolution of ~10 nm using a quite simple experimental setup.

The reliability of ultrathin $SiO_2$ ($\leqslant$2 nm) layers in metal oxide semiconductor (MOS) structures is one of the issues of major concern in microelectronic technology. For this reason, one of the most discussed arguments on the characterization of ultrathin dielectric layers is the trap creation in the dielectric and how the charge injection triggers dielectric breakdown (BD).[10] In this letter we want to demonstrate that CAFM is a powerful tool for the investigation of the degradation and its propagation of ultrathin $SiO_2$ layers. In literature several works studied the dielectric degradation and its propagation using microscopy, most of them need to compare different techniques.[11–14] Indeed, the mechanisms involved in the dielectric degradation and in the BD still focus the attention of the scientific community. For these reasons, studies at nanometer scale are required.

In this work, electrical stress tests—constant voltage stress (CVS) and ramped voltage stress (RVS)—are applied to ultrathin $SiO_2$ films using a CAFM to analyze the electrical properties of nanometric oxide areas. Moreover, the propagation or spreading of the damaging during stress has been studied at nanometer scale. The results presented in this work will demonstrate the capabilities of the CAFM to discern the local mechanisms involved in the degradation and eventually breakdown of the thin gate oxides.

The studied wafer has been fabricated in the following way: a 2 nm thin $SiO_2$ layer has been obtained by thermal oxidation in dry oxygen ambient of an *n*-type (100) silicon substrate. After the thermal oxidation, a 100 nm thick layer of poly-silicon has been deposited to protect the $SiO_2$ surface from contamination. Before measuring, each piece of wafer has been prepared as follows. First of all, the native oxide grown on the poly-Si layer has been removed by dipping in diluted HF (10%) for 5 s. Secondly, the 100 nm of protective poly-Si has been removed using a selective KOH (10%) etch for 20 min. Data obtained on these samples have been compared with those obtained on samples without the protective poly-Si layer. Results are similar, this means that cleaning processes do not produce changes in the $SiO_2$ layer.

The electrical measurements were carried out with an AFM from Digital Instruments (contact mode, working in air) equipped with a conductive tip (acting as gate electrode) and a picoampere amplifier with an overall amplification of $10^{12}$ V/A.[15] In this work, silicon tips coated by a metallic layer of Pt/Ir have been used.

In our experiments, electrons were always injected from the substrate (positive tip polarity) due to several advantages compared to the injection from the tip. First of all, with a negative tip polarity, anodic oxidation processes can be triggered.[16,17] As a result, an oxide layer can be grown which would modify the oxide thickness. Secondly, the bare oxide surface could contain contaminates that may modify the barrier height, leading to erroneous results. When injecting from the substrate, however, the barrier height is perfectly defined by the $Si/SiO_2$ interface. This experimental setup allows to obtain two different kinds of information. The first one is the morphological image of the sample and the opportunity to compare with the current maps when a constant bias voltage is applied between sample and tip. The second one is the opportunity to perform current-voltage (*I-V*) characteristics

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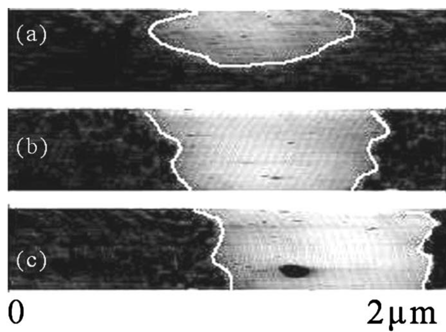


FIG. 1. Current maps at 4 V of $2\times0.5$ $\mu$m after CVS in four points at 4.5 V for (a) 30 s, (b) 60 s, and (c) 120 s.

at a given location on the oxide surface by applying a voltage ramp.

The possibility to study degradation effects in $SiO_2$ layers with the CAFM has been evaluated. We performed a CVS at 4.5 V for different times on four different points at the vertices of a square having a side of 250 nm in order to get a stressed region big enough for the CAFM lateral resolution. The stress processes have been followed by a scan on the stressed region looking for any changes in the current map of $SiO_2$. Figure 1 shows the current maps obtained at constant bias voltage of 4 V on different regions after CVS at 4.5 V for 30 s (a), 60 s (b), and 120 s (c), respectively.

The current maps present dark and bright zones. The first ones represent the typical behavior of a common 2 nm thick $SiO_2$ layer under a constant applied bias voltage of 4 V. The bright regions are zones with lower current compared with the dark zones. These bright regions indicate the areas affected by the stress. We think that during the CVS additional traps have been created. They trap electrons and play a relevant role in the conduction mechanism of the stressed region. In fact, it is reasonable to believe that electrons are trapped at the $Si/SiO_2$ interface and in the $SiO_2$ bulk, modifying the flat band voltage of the metal (tip) oxide semiconductor (MOS) structure. Consequently, the conduction mechanism is affected by trapped electrons and the effective oxide barrier height increases while the tunnel current flowing through the oxide decreases. Moreover, in Fig. 1 it is possible to note the stress changes in function of different stress times, i.e., smaller stress times correspond to smaller stressed regions [Fig. 1(a) and 1(b)]. If the stress time was large enough, the area of the stressed region did not change further but sometimes breakdown could be triggered (one of the four stressed points broke down) in the stressed region. This is shown by the big black spot (high breakdown current) inside the bright/stressed area in Fig. 1(c).

As these measurements prove that CAFM is an appropriate tool to study degradation effects in thin dielectric layers, also the effect of RVS have been studied. A single point was stressed by performing sequential voltage ramps from 0 to 4.5 V. In this case the stress parameter taken in consideration was the number of ramps performed on a single point. The actual stressed area is the contact region between the $SiO_2$ surface and the tip, and we can estimate this area to be a few hundreds of $nm^2$ at most.

Figure 2 shows current maps of regions after different numbers of RVS. From top to bottom, the current maps collected after 10, 20, 40, and 60 voltage ramps are depicted. The more stress ramps, the larger is the area affected by the stress. This is a direct observation of how the damaging effect "spreads" in the dielectric. In fact, the dimension of the stressed region is always larger than the contact area of the metallic tip on the surface. This spreading effect can be partially due to a little hysteresis of the piezoelectric material, responsible for the motion of the tip, which causes a drift movement on the surface and the increasing of the stressed area. However, it is reasonable to assume that this phenomenon is negligible compared with the lateral spread shown in Figs. 1 and 2. Note that drift would not impose a circular stress zone as the drift is usually in one particular direction. In fact, after several number of ramps there is no more increasing in the dimension of the stressed region. Moreover, analyzing also the data from Fig. 2, it is clear that the increase of the stressed area is a function of time until the reaching of a maximum value of the diameter of about 350 nm. In Fig. 2, this maximum lateral propagation diameter is reached between the 40th and the 60th ramp.

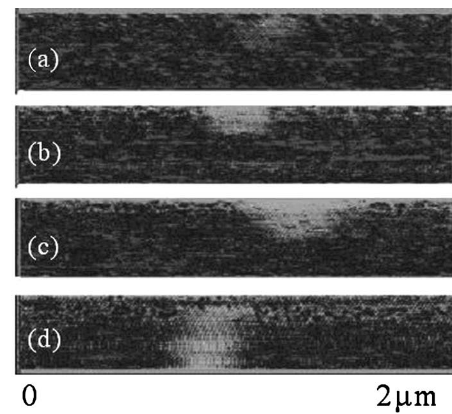


FIG. 2. Current maps at 4 V of $2\times0.5$ $\mu$m after RVS in one point from 0 to 4.5 V for (a) 10 times, (b) 20 times, (c) 40 times and (d) 60 times.

The *I-V* curves recorded during the RVS are shown in Fig. 3(a). It is possible to note that the threshold voltage (defined as the voltage where the current exceeds the noise level) shifts to higher voltage values especially in the initial three curves. This observation and the growth of the stressed regions after a different number of voltage ramps indicate a direct relation between the voltage shifts and the trap creation rate. After the first ramps the threshold voltage tends to reach a fixed value and the difference between the 50th and the 60th ramps is practically zero. The slope of all the curves is the same and it is possible to suppose that it is still Fowler-Nordheim injection[18] conditions. At the same time, it is possible to assume that the created traps produce a shift in the flat band voltage,

$$\Delta V_{\mathrm{FB}} = \frac{Q_t}{C},$$

where $Q_t$ is the trapped charge and $C$ is the capacitance of the nanocapacitor tip oxide silicon. In this way it is possible to estimate the density of created traps $N_t$,

$$N_t = \frac{\varepsilon_0 \kappa \Delta V_{\mathrm{FB}}}{et},$$

where $\varepsilon_0$ is the permittivity of vacuum, $\kappa$ is the relative dielectric constant of $SiO_2$, $t$ is the oxide thickness, and $e$ is the electron charge. Using the voltage shift between the 1st and the 60th ramps the trap created density has been calcu-

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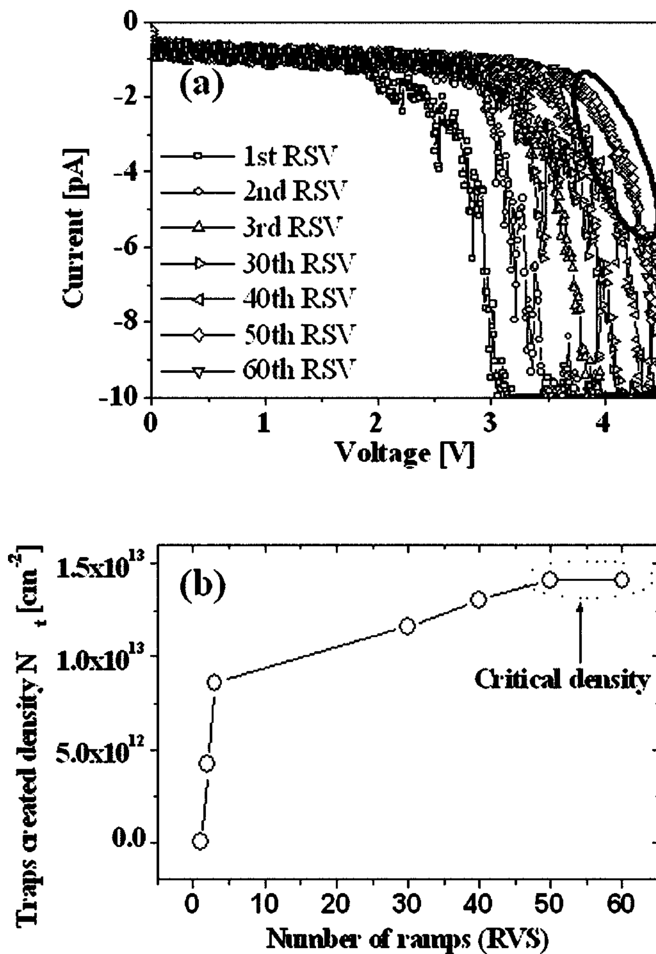


FIG. 3. (a) *I-V* characteristics after several voltage ramps. Between the 1st and the 60th there is a shift of about 1 V. In the circle the 50th and the 60th ramps are depicted. (b) Trend of the trap generation rate vs the number of ramps from 0 to 4 V.

lated to be $N_t = 1.3 \times 10^{13}$ cm$^{-2}$. It is important to emphasize that to obtain the $N_t$ value it is not necessary to know the contact area of the tip, while it is only important that the dimensions are not changing during the measurements. This condition is confirmed because these observations of sequential *I-V*'s are reproducible using the same tip at different locations. As already described, after several ramps the dimension of the stressed region stops its lateral growth and the threshold voltage does not shift anymore. Figure 3(b) shows the density of the traps created versus the number of ramps (from 0 to 4 V). The saturation density, or the critical density, has been found. This result points out that the maximum density of traps created during the stress is close to the critical defect density to trigger a BD event. In fact, BD events are triggered when, according to the percolative theory, a critical trap density is reached.[19] It is possible to suppose that changing the trap creation rate, for example, using harder stress conditions, BD events should be triggered. This means that longer stress times or higher stress voltages will induce BD phenomena.

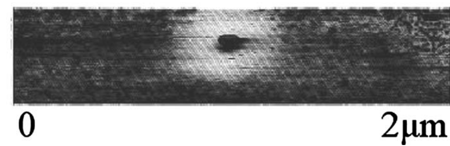


FIG. 4. Current map performed at 4 V on a 2 nm thick $SiO_2$ layer after ten RVS from 0 to 5 V.

Figure 4 shows a typical current map after harder stress conductions, ten ramps from 0 to 5 V. The higher voltage of RVS induced the breakdown after few ramps. The breakdown spot is surrounded by a charged ring. The diameter of this ring is still about 350 nm, this confirms that the degradation propagation reaches a lateral limit and that the next step in the degradation of the dielectric is BD.[10]

In conclusion, in this work the CAFM has been found to be a powerful tool to study the trap creation effect and in general the degradation of ultrathin $SiO_2$ layers. Local stress (CVS and RVS) was applied to the dielectric and stressed regions in the current maps and threshold voltage shifts in the *I-V* curves were observed. These phenomena originated from trap creation effects during the stress. Other works pointed out at nanometer scale charge trapping phenomena related to the dielectric degradation.[12,13] This work is a step forward for the understanding of the trap creation kinetics and its saturation mechanism. The saturation of the lateral propagation of the damaging has been correlated to the critical defects density and with the occurrence of BD phenomena. The critical defects density for an ultrathin $SiO_2$ layer at nanometer scale has been found.


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