Study on Modeling Techniques for CMOS Gate Delay Calculation in VLSI Timing Analysis

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In VLSI designs, designers have to do the timing analysis in order to estimate the ability of a VLSI circuit to operate at the specified frequency. Although this kind of work can theoretically be implemented using a circuit simulation, such an approach to simulate all timing conditions of a design with several million gates is too slow. In contrast, static timing analysis (STA) is a fast and exhaustive verification of all timing checks of a design. In STA, a crucial work is to calculate the gate delay time. Since the CMOS gate is composed of non-linear components, it is difficult to obtain a precise and efficient gate delay model. Thus, this dissertation is mainly focused on the issues of improving the accuracy and efficiency of gate delay calculation.

In the conventional methods for gate delay time, input signal of each gate is always simply assumed as a linear ramp. However, the actual signal will become more and more nonlinear after transferring through many gates and interconnects. As a result, computation has a significant error when the non-ramp input is assumed as the ramp waveform. Therefore, the input waveform effect should be considered in the gate delay calculation. In cell level delay calculation, an equivalent gate model called Thevenin model that considers each gate as a combination of a linear resistor and a step voltage source is widely used. Most of the conventional methods for gate delay are based on the condition that charges flowing into pure capacitance load and interconnect load are equal. With the actual gate model, this condition is accurate. However, with the Thevenin model, there is charge difference between capacitance load and interconnect load, which has a large influence on gate delay calculation. In order to improving the accuracy, a new condition with the Thevenin model is required. Besides, in the previous works, most of them use iterative algorithms to ensure the accuracy. The iterative methods are too slow for gate delay calculation of modern VLSI designs. Meanwhile, the existing non-iterative methods have the disadvantages of low accuracy and using over-simple gate model.
To overcome above drawbacks, three new models that focus on different issues have been proposed in this dissertation, respectively. First, an advanced gate delay model is proposed with adding the effect of non-ramp input waveform. Second, a simple and accurate method is proposed to calculate gate delay in the Thevenin model, where the effect of charge difference is considered. Last, a non-iterative method is presented, which can improve the efficiency of gate delay estimation without significant accuracy loss.

The dissertation is organized with six chapters as follows.

In Chapter 1 (Introduction), the background and some basic conceptions of this research are briefly introduced. Then the motivations and contributions of this dissertation are presented. The last section of this chapter is to describe the organization of this dissertation.

In Chapter 2 (Overview of conventional gate delay models), the development procedure of gate delay calculation and some different types of conventional methods are overviewed to discuss the issues of accuracy and efficiency in the conventional methods. Then, the purposes of this research that are to improve the accuracy and efficiency of gate delay calculation are shown.

In Chapter 3 (Effective capacitance model for gate delay considering input waveform effect), an advanced model for calculating the effective capacitance that is usually used to compute CMOS gate delay is proposed to consider both the interconnect load effects and the non-ramp input waveform effect. First, the non-ramp input effect is presented through some actual examples and the computation error caused by this problem is analyzed. Then, an analytical method for overcoming the non-ramp input problem is proposed and the detailed procedure of the proposed method is given. The nonlinear influence of the input waveform that can increase the gate delay time is modeled as one part of the effective capacitance
for calculating the gate delay. The experimental results show that the average error of proposed method is only about 3.7%, while that of conventional method is more than 15% when the input is non-ramp.

In Chapter 4 (Accurate effective capacitance model for gate delay with RC loads based on the Thevenin model), a method that focuses on the charge difference problem between the effective capacitance load and interconnect load in Thevenin model is proposed. First, the conventional methods for gate delay time based on the Thevenin model are overviewed. At the same time, the description of charge difference problem in the Thevenin model is given and the errors of conventional methods are analyzed. Then the proposed algorithm for solving the charge difference problem and the procedure for gate delay calculation are shown in detail. The proposed method is based on some simple and accurate approximations, which do not add much computation complexity. The accuracy of proposed method with a 1.3% average error is much better than the conventional method with a 7.3% average error.

In Chapter 5 (A non-iterative method for delay calculation of CMOS gates), a non-iterative method for improving the efficiency of effective capacitance calculation is presented. In the proposed method, a simple polynomial approximation is used to modify the nonlinear effective capacitance equation. The detailed error analysis of the polynomial approximation is given. Through using the proposed method, the value of effective capacitance and gate delay time can be computed without requiring any iteration. The efficiency of gate delay calculation has a significant improvement. Compared with the conventional method, the CPU time of proposed method is reduced by half. Meanwhile, the proposed method keeps a relative high accuracy with a 2.8% error.

In Chapter 6 (Conclusions), the conclusions of this dissertation are given.