Waseda University Doctoral Dissertation

Study on Pseudo-transient Analysis Methods for Solving Nonlinear DC Circuits

Zhou JIN

Graduate School of Information, Production and Systems

Waseda University

October 2015

Abstract

Nowadays, the circuit simulation is becoming an essential technique for the circuit designers to verify and check their designs of electrical and electronic circuits and systems before their deployment and fabrication. The applications of the circuit simulation are very wide, including microelectronics, integrated circuits, power electronics, electrical power distribution networks, and so on. Circuit simulation includes three technologies. The first one is to model the elements and devices of the circuits mathematically. The second one is the formulation of the circuit/network equations. The third one is the techniques to solve these formed circuit equations. This research mainly focuses on formulating and solving the circuit equations.

As the integrated circuits and semiconductor technologies developed rapidly, the nonlinear circuit simulation technology becomes more and more important. In the circuit simulation, the DC analysis for nonlinear circuits is the most fundamental and important task. The analysis of nonlinear circuits always needs to solve a system of nonlinear algebraic equations. The Newton-Raphson, NR, method is employed to obtain the DC operating point. This method is based on the idea of linear approximation with an initial guess to solve a system of nonlinear equations. However, the NR method is not globally convergent, which cannot guarantee the convergence unless the initial solution is sufficiently close to the true solution.

Since the NR method may fail to converge, many studies are done and many methods are proposed to overcome this limitation. The NR method is modified in several ways from the limiting viewpoint and error-reduction viewpoint. Besides, some continuation methods such as Gmin stepping and source stepping methods are studied to overcome the limitation of the NR method. However, the discontinuous solution curves will cause the non-convergence problem of these

methods. Meanwhile, the homotopy method, another method from the theoretical viewpoint, is not implemented in the commercial SPICE-like simulators since it depends on the device models and is hard to implement. Pseudo-transient analysis, PTA, method is another way to deal with the NR method non-convergence situation. The idea of the PTA method is to insert the certain pseudo elements to the nonlinear resistive circuit, and then a transient analysis will be done until achieves a steady state. The pseudo elements include pseudo-capacitors and pseudo-inductors. However, these inserted pseudo elements may cause the oscillation problem. The compound-element PTA, CEPTA, is studied in the Inoue lab (Hong Yu, IEICE Trans 2006, 2007), which uses the compound pseudo-elements to deal with the oscillation problem. Recently, to eliminate the oscillation from the numerical integration algorithm viewpoint, a damped PTA (DPTA) method is proposed (Xiao Wu, NOLTA 2014). The de-facto standard commercial circuit simulators also have a method named as DPTA, but the algorithms are confidential and not published anywhere. However, the non-convergence problem is still a great challenge for all these PTA methods when dealing with the practical large-scale circuits. Though the study of homotopy method from the theoretical viewpoint has developed recently, it is hard to implement. Therefore, the study on developing practical methods to obtain the DC solutions for large-scale circuits is an important task in circuit simulation, which should have excellent convergence performance and are easy to implement.

Thus, this research focuses on improving the convergence and efficiency of the PTA methods. In this dissertation, based on the CEPTA method, (1) a new implementation algorithm and (2) embedding algorithms are proposed. Moreover, based on the DPTA method, (3) a ramping algorithm and (4) a restart algorithm are proposed. The proposed algorithms are implemented on the SPICE simulator and applied to practical large-scale analog circuits. The effectiveness are verified.

The dissertation contains the following five chapters.

Chapter 1 [Introduction] This chapter presents the background of circuit simulation is given. The SPICE-like simulators, the different types of circuit analysis, and the conventional numerical analysis algorithms are introduced. The DC analysis is very fundamental and important, since it is the prior to perform the small signal analysis and transient analysis. After that, several continuation methods for the DC analysis, including Gmin stepping, source stepping, homotopy method and PTA method, are discussed. Then, the motivation of this research and the dissertation organization are shown.

Chapter 2 [Preliminaries] In this chapter, the PTA methods are introduced for later chapter discussions since it is one of the most effective methods to solve the nonlinear DC circuits. The conventional PTA methods are discussed, including the pure element PTA, compound element PTA (CEPTA), and Damped PTA (DPTA) methods. Then a SPICE3 implementation algorithm for CEPTA is reviewed. The drawbacks and the challenges of the PTA methods can be obtained by analyzing these conventional PTA methods.

Chapter 3 [Effective Implementation and Embedding Algorithms of CEPTA Method] An implementation algorithm and embedding algorithms of CEPTA are proposed. The conventional implementation algorithm applies the numerical integration method in the compound branch level for the compound pseudo elements. It has a limitation of the time-step size which influences the convergence and efficiency of the NR method. When the time-step size gets larger and the approximation error becomes extremely large, the NR method may fail to converge. To overcome this problem, the proposed implementation algorithm applies the numerical integration algorithm in individual element level by decomposing the compound branch. Therefore, the proposed algorithm is much

more efficient and the convergence performance of CEPTA can be greatly improved. The convergence of the proposed implementation algorithm is also proved in this chapter. In the proposed embedding algorithm, three embedding positions of the pseudo-elements are extended to the CEPTA method, including Diagonal, BC(GD) and BE(GS) positions. For different types of circuits or different simulation conditions, the appropriate embedding position should be carefully selected to obtain the best simulation performance. In order to verify the effectiveness, the proposed algorithms are implemented on our spice simulator WSPICE and applied to practical large-scale analog circuits. By using the proposed implementation algorithm and suitable embedding position, the convergence of CEPTA method can be greatly improved (the number of total iterations is reduced by 40%) compared with the conventional CEPTA method (Hong Yu, IEICE Trans 2007). Besides, the proposed methods can solve the large-scale analog DC circuits (the number of devices > 1000) while the conventional CEPTA and de-facto standard commercial circuit simulators fail. The embedding algorithm can be extended to other PTA algorithms, such as pure PTA methods.

Chapter 4 [Ramping Algorithm and Restart Algorithm in SPICE3 Implementation for DPTA Method] In this chapter, a ramping algorithm and a restart algorithm are proposed to improve the simulation efficiency. In the proposed ramping algorithm, the supply voltages are ramped up from zero to their final values over time according to the certain ramping function without inserting any pseudo-inductors. Two effective ramping functions, the sine type ramping function and the cosine type ramping function, are proposed and the continuity and smoothness are analyzed. The proposed ramping algorithm can eliminate the oscillation caused by the inserted inductor. Moreover, the number of non-zero elements and fill-ins in the Jacobian matrix can be greatly reduced. In the proposed restart algorithm, a recognition method is used to check whether the simulation is stuck into an infinite loop by detecting how many times the NR method fails

to converge in a certain time period and how the time-step size changes. If the infinite loop occurs, the restart algorithm will roll back to the previous step and do the simulation again with the constant time-step size. In order to verify the effectiveness, proposed ramping and restart algorithms are implemented on our spice simulator WSPICE and applied to the large-scale analog circuits. The effectiveness are confirmed by the numerical examples. Compared with conventional DPTA method (Xiao Wu, NOLTA2014), the proposed ramping algorithm reduces the number of non-zero elements of the Jacobian, and the number of fill-ins is reduced by 40%∼60%. As a result, the number of total iterations can be reduced by 8.67%∼66.5%, and the CPU time can be reduced by 28.14%∼70.2%. The proposed restart algorithm is proved to be effective to improve the convergence for the test circuits which have the infinite loop problem.

Chapter 5 [**Conclusions**] concludes the dissertation and gives the future work.

Contents

Abstract iii

Contents viii

List of Figures xi

List of Tables xiii

1 Introduction 1
- 1.1 Overview of Nonlinear Circuit Simulation . . . 4
  - 1.1.1 Circuit Analysis Modes . . . 4
    - 1.1.1.1 Direct Current Analysis . . . 4
    - 1.1.1.2 AC Small-Signal Analysis . . . 4
    - 1.1.1.3 Transient Analysis . . . 6
  - 1.1.2 Circuit Simulators . . . 7
  - 1.1.3 DC Analysis Algorithms . . . 8
    - 1.1.3.1 Newton-Raphson Algorithm . . . 9
    - 1.1.3.2 Continuation Methods . . . 11
    - 1.1.3.3 Homotopy Methods . . . 14
    - 1.1.3.4 PTA Methods . . . 15
- 1.2 Purpose of This Research . . . 18

2 Preliminaries 21
- 2.1 Pseudo-Transient Analysis Method . . . 22
  - 2.1.1 Pure Pseudo-element Algorithms . . . 22
  - 2.1.2 CEPTA Algorithm . . . 22
    - 2.1.2.1 Compound pseudo element . . . 23
    - 2.1.2.2 Conventional SPICE3 implementation method . . . 24
  - 2.1.3 Damped Pseudo-Transient Analysis Algorithm . . . 27
- 2.2 Initial Solution Method . . . 32

2.3 Modified Nodal Analysis 34

3 Effective Implementation and Embedding Algorithms of CEPTA Method 37
3.1 Introduction 38
3.2 Challenges in CEPTA Method 41
3.3 Proposed Method 42
3.3.1 Implementation Method in SPICE3 Simulator 42
3.3.1.1 Branch RVC 42
3.3.1.2 Branch GVL 46
3.3.1.3 Convergence consideration 48
3.3.1.4 Analysis 49
3.3.2 Embedding Algorithms 53
3.4 Numerical Examples and Comparisons 55
3.5 Conclusions 66

4 Ramping Algorithm and Restart Algorithm in SPICE3 Implementation for DPTA Method 67
4.1 Introduction 68
4.2 Challenges in the DPTA Method 70
4.3 Proposed Methods 71
4.3.1 Ramping Algorithm with DPTA 71
4.3.2 Restart Method 76
4.4 Numerical Examples 81
4.5 conclusions 88

5 Conclusions 89
5.1 Conclusions 90
5.2 Future Works 94

Bibliography 95

Related Paper 101

Publications 103

Acknowledgements 107

List of Figures

1.1 The flowchart of circuit simulation [2]. 5
1.2 The flowchart of DC analysis [6]. 6
1.3 A graphical illustration of the Newton's method in one dimension [1]. 10
1.4 A graphical illustration of overflow problem of the NR method [1]. . 11
1.5 A graphical illustration of cycle phenomenon of the NR method [1]. 12

2.1 Pseudo-elements in constant pure PTA method [27]. 23
2.2 Compound pseudo-elements for CEPTA method [36]. 24
2.3 Insert position of the compound pseudo-elements [36]. 24
2.4 Branch RVC/GVL in SPICE3 implementation. 25
2.5 The pseudo-elements of DPTA method and their insert positions into the circuit. (a) Pseudo-inductor inserted to the voltage source. (b) Pseudo-capacitor inserted to the independent current source. (c) Pseudo-capacitor for the BJT and MOS transistors. 28
2.6 Initial solution for BJT transistor. 33
2.7 Initial solution for MOS transistor. 33
2.8 A linear resistive circuit. 34

3.1 Companion model for RVC branch obtained from implementation algorithm. 45
3.2 Resistor value at time point t_n of different methods. 50
3.3 Embeding positions of pseudo elements. 54
3.4 15-stage MOS inverter chain circuit. 62
3.5 Node voltage waveform with HSPICE of 15-stage MOS inverter chain circuit. 62
3.6 Node voltage waveform with conventional CEPTA [1] method of 15-stage MOS inverter chain circuit. 63
3.7 Node voltage waveform with proposed algorithms (BE insert position) of 15-stage MOS inverter chain circuit. 63

4.1 The waveform of sinusoidal type ramping function. 74
4.2 The waveform of cosine type ramping function. 74

4.3 One node voltage waveform of intake system by using DPTA method when the pseudo-control parameter values are not suitable chosen. . 77
4.4 The time-step size of intake system by using DPTA method. 77
4.5 The recognition method for restart algorithm. 79
4.6 The waveform result of a node voltage in the intake system circuit by using the proposed restart method. 84
4.7 The node voltage waveform of jge circuit by using the DPTA method. (a) The waveform of searching phase. (b) The waveform of converging phase. The circuit is not converged. 86
4.8 The time-step size of jge circuit by using the proposed restart method. (a) The time-step size of searching phase. (b) The time-step size of converging phase when stuck into infinity loop. 87
4.9 The node waveform of jge circuit by using the proposed restart method at the converging phase. The circuit converged. 87

List of Tables

3.1 Simulation performance comparison of D1 circuit. 57
3.2 Simulation performance comparison of 6-stage limiting amplifier. . . 58
3.3 Simulation performance comparison of the benchmark circuit. . . . 58
3.4 Simulation performance comparison of UA741 5-stage PFB OP AMP. 59
3.5 Simulation performance comparison of 15-stage CMOS inverter chain. 61
3.6 Simulation performance comparison of analog adder. 64
3.7 Simulation performance comparison of the intake system. 64

4.1 Property comparisons of $0 \leqslant t \leqslant \tau_{ramp}$ part functions for sinusoidal and cosine type ramping factors. (τ here is τ_{ramp}) 75
4.2 Simulation performance comparison of UA741 10-stage PFB OP AMP circuit. 82
4.3 Simulation performance comparison of bias circuit. 83

Chapter 1

Introduction

The integrated circuit productions are so important and commonly used at present, since they can help us build a quality life. In 1958, the integrated circuit was firstly appeared by Jack Kilby. After that it has been developed a lot. Nowadays, the integrated circuits usually may contain several hundred millions of elements so that various functions can be provided and the performance can be highly. Due to these situations, the electronic design automation (EDA) techniques come out to help check and verify the integrated circuit (IC) designs [1].

From the very beginning, the engineers mainly design the electronic and electrical circuits by hand calculation according to the valuable flow chart, figures and design tables. Thus it mainly depends on the knowledge, understanding, experiences and intuition of the designers. Then the "breadboard stage" came out to help the design [1]. However, with the integrated circuits appeared, the scale of circuits and the number of elements are becoming larger and larger. The hand calculation for the designers turns into very complicate and difficult, which is not sufficient enough to verify and analyze the circuits. Moreover, the "breadboard stage" method is also time-consuming and less efficient since the components are discrete [2]. Thus, under such circumstances, the computer aided design software is considered as a very critical tool. In order to make the design much more automatically and highly efficient, in the middle 70s, the researchers developed a computer software to help verify and simulate the circuits [2].

In the 1950s and 1960s, computers were used to help the circuit simulation. Techniques of computer aided simulation software were developed. The first commonly used simulator was SPICE, which is spread widely. It was developed in the early 1970s at the University of California, Berkeley, by L. W. Nagel. Now, SPICE is the de facto standard circuit simulator. Our work is based on the version of SPICE3f5.

In the integrated circuit design workflow, the EDA techniques are widely used recently [2]. Thus, the integrated circuit designs rely on the computer aided software increasingly. The EDA technologies have to develop much more rapidly since the scale of the semiconductor techniques is continuously increasing. Meanwhile, with the help of developed EDA techniques, the design of integrated circuits becomes to be much smarter.

The EDA techniques contain many parts, including Behavioral synthesis, Design and architecture, Mask data preparation, Simulation, Floor planning and so on [2]. In this research, we mainly consider the circuit simulation part. Since the DC analysis is one of the most fundamental and also difficult part for the nonlinear circuit simulation, we mainly focused on the techniques for the DC solutions.

1.1 Overview of Nonlinear Circuit Simulation

Circuit simulation mainly includes three technologies, to model the circuit devices mathematically, to formulate the circuit equations and to solve these formulated equations [1]. An overall circuit simulation flow chart can be seen in Fig. 1.1. It is clear that the time discretization, element linearization and matrix equation solution are repeatedly applied [1][2].

1.1.1 Circuit Analysis Modes

Several circuit analysis modes are offered in the circuit simulators. They can help the designers to verify their circuits from many different viewpoints.

1.1.1.1 Direct Current Analysis

A direct current analysis (DC) calculates the quiescent operating points for circuit. All energy-storage elements in the circuit are ignored in a DC analysis since the capacitors are treated as open circuits and the inductors are treated as short circuits [3–5]. The DC analysis is automatically performed before the transient analysis to determine the initial conditions for the transient. It is the prior to perform the small signal analysis and transient analysis [3]. The Fig. 1.2 shows the DC analysis flowchart [4].

1.1.1.2 AC Small-Signal Analysis

The AC small-signal analysis computes the AC output variables as a function of frequency (transfer function), over a user-specified range of frequencies [3]. It is useful for the design of analog circuits which operate in small-signal modes. The

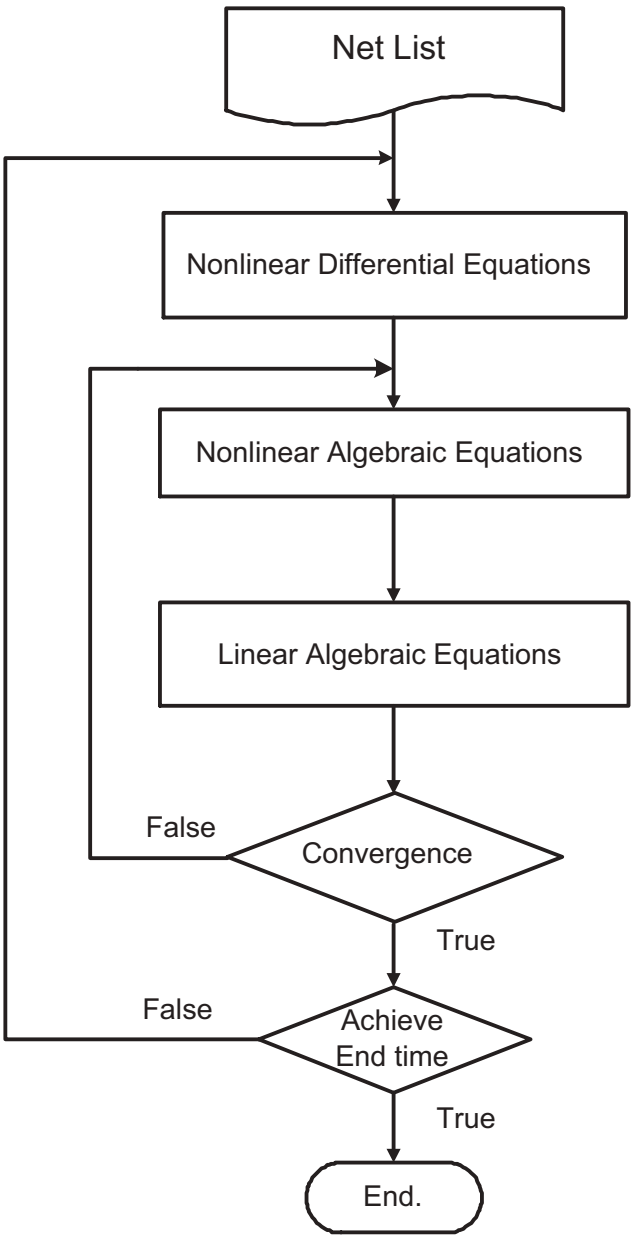

FIGURE 1.1: The flowchart of circuit simulation [2].

perturbational response of the circuit is obtained by using linearized models of the nonlinear elements. The parameters of these linearized models are determined by the DC operating point analysis.

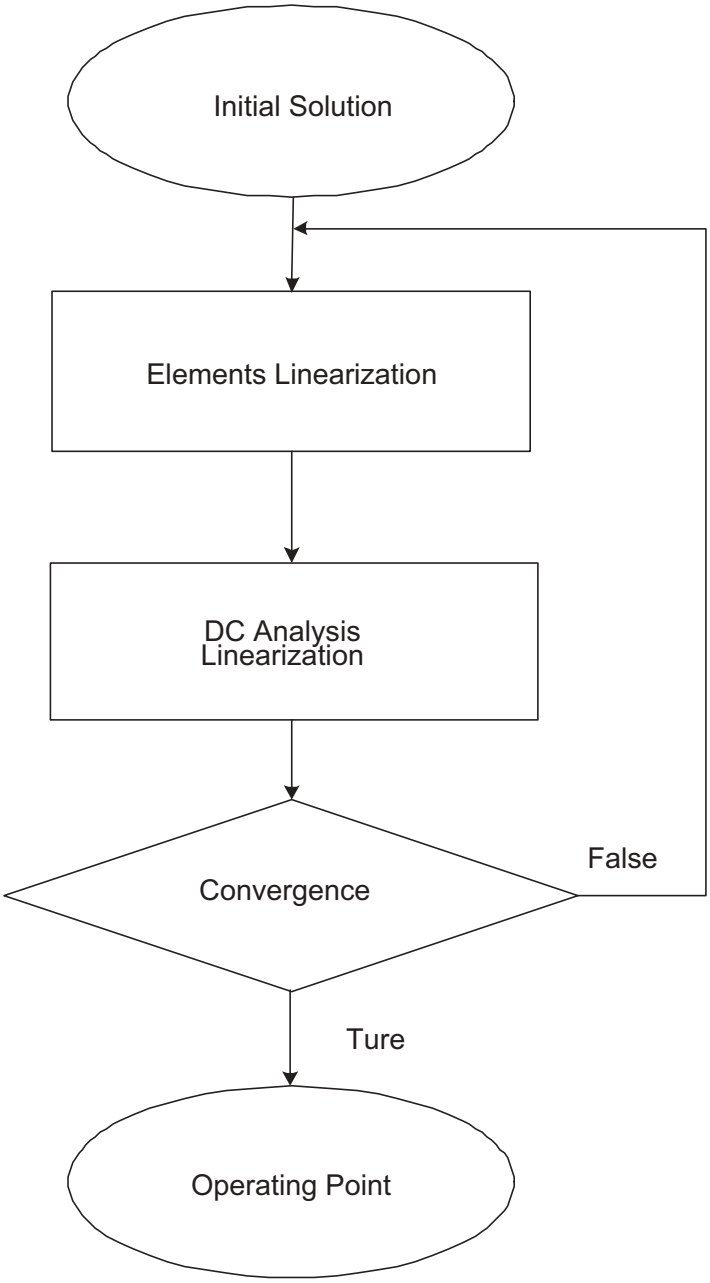

FIGURE 1.2: The flowchart of DC analysis [6].

1.1.1.3 Transient Analysis

The transient analysis finds the transient output variables, voltages and currents as functions of time over a user-specified time interval [3]. The large signal time

domain behavior of circuits can be determined by the transient analysis containing nonlinear elements. The initial timepoint arbitrarily defined as time zero, is determined by a previous DC operating point solution. The DC values are set to all the time independent sources such as power supplies. The user-specified time interval $(0, T)$ is divided into several discrete timepoints. The circuit solution at each successive timepoint is determined by the program starting from time zero. Note that, both DC and transient solutions are obtained by an iterative process which is terminated when some convergence conditions hold.

The circuit simulation is mostly used to do a DC analysis and then a transient analysis. Apart from these basic analysis modes, the simulators also offer additional capabilities, such as the Pole-Zero analysis, noise analysis, statistical analysis, switched capacitor circuit analysis, analysis at different temperatures and so on. All these circuit analysis modes are useful for the designer to evaluate their circuit from various viewpoint [4].

1.1.2 Circuit Simulators

The SPICE, "Simulator Program with Integrated Circuit Emphasis", is one of several successful circuit simulation programs that currently are available. In over 30 years of its life, SPICE has became a de-facto standard for simulating circuits. It was developed by Larry Nagel at the integrated circuits group of the Electronics Research Laboratory of the University of California, Berkeley under direction of his advisor, Prof. Donald Pederson [5–8]. Nowadays, as one of the most critical computer aided design tools, the SPICE is commonly used before the designers manufacture their circuits so that the performance can be verified in detail.

SPICE evolved from the CANCER program. The first version of SPICE essentially was finished in 1972 [5]. The SPICE simulator became to be popular and really

widely spread since 1975 with the version SPICE2 [6]. After that in 1989, Thomas Quarles developed the SPICE3 together with A. Richard Newton. The written language is C programming language, and the same netlist syntax is used [6]. Compared with SPICE2, the SPICE3 is a more advanced version, which has a much better convergence property. Today, the latest version is SPICE3f5.

As an early open source program, SPICE inspires and serves as a basis for many other circuit simulation programs in academia, in industry, and in commercial products. There are several commercial versions of SPICE simulators such as the HSPICE and PSpice simulators, which are owned by the Synopsys Cadence Design Systems now. The XSPICE is a academic version of the SPICE. It was developed at Georgia Tech, in which mixed analog/digital "code models" are added for the behavioral simulation. Another academic spinoff of SPICE is Cider, from UC Berkeley/Oregon State Univ., in which semiconductor device simulation is added [7]. Moreover, free ngspice simulator [9] is also an important improvement of SPICE3 and it is a mixed-level/mixed-signal circuit simulator. Most importantly, ngspice simulator is free for users.

1.1.3 DC Analysis Algorithms

As have been shown, the DC analysis of nonlinear circuits is an important task. The DC operating point is not only a first basic check of circuit operation, but also a precondition for further analyses, which include transient analysis, noise analysis and small-signal AC analysis. In this thesis, our work mainly focuses on the techniques of solving nonlinear DC circuits, which is to find the DC operating point for nonlinear circuits. Firstly, some conventional methods for DC analysis are shown.

Before the DC analysis for the nonlinear circuit, the most important and fundamental step is to construct the circuit nodal equations. The designed circuit structure is usually presented in the term of the netlist file [11, 12]. The circuit simulator should firstly load the netlist file into the program and formulate the circuit equations. The widely used method is the modified nodal analysis method, which formulates the set of equations by combing the equations of elements, Kirchhoff's current la ltage la [10]. The circuit will be firstly converted into the description of a netlist file even though some CAD softwares can capture the schematic.

Once the network equations have been assembled, the next thing for the simulator is to get the solution of the equations. If only the linear elements are included in a circuit, the Gaussian elimination, LU decomposition can be used to solve equations. If the circuit contains nonlinear elements, most circuit simulation programs (SPICE-like simulators) resort to the Newton-Raphson algorithm to determine the solution of algebraic equations of the nonlinear system.

1.1.3.1 Newton-Raphson Algorithm

The Newton-Raphson (NR) method shown in Fig. 1.3 is used to solve the equations in the form $f(x) = 0$. This method is based on the idea of linear approximation. An initial guess x_0 is needed to find the final root. As if the initial guess x_0 is close enough to the final solution, it is guaranteed to converge. However, it is hard to make a clear statement about how close enough since it is a highly specific problem.

To implement the NR method, we need a formula for x_{n+1} in terms of x_n. At the initial point $(x_0, f(x_0))$, the tangent line to the $y = f(x)$ is written in Eq. (1.1).

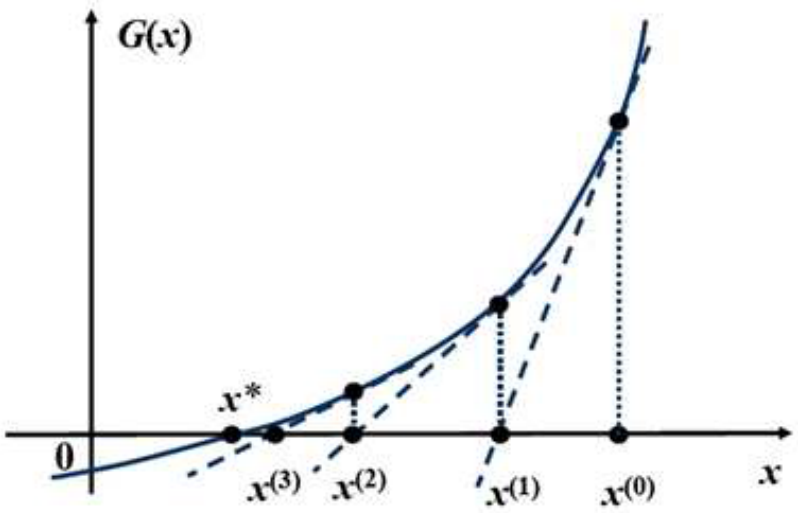

FIGURE 1.3: A graphical illustration of the Newton's method in one dimension [1].

$$y - f(x_0) = f^{'}(x_0)(x - x_0). \tag{1.1}$$

The tangent line intersects the x-axis when $y = 0$ and $x = x_1$. Therefore, $-f(x_0) = f^{'}(x_0)(x_1 - x_0)$. Solving this for x_1 gives

$$x_1 = x_0 - \frac{f(x_0)}{f^{'}(x_0)}, \tag{1.2}$$

and the general form for x_{n+1} is

$$x_{n+1} = x_n - \frac{f(x_n)}{f^{'}(x_n)}. \tag{1.3}$$

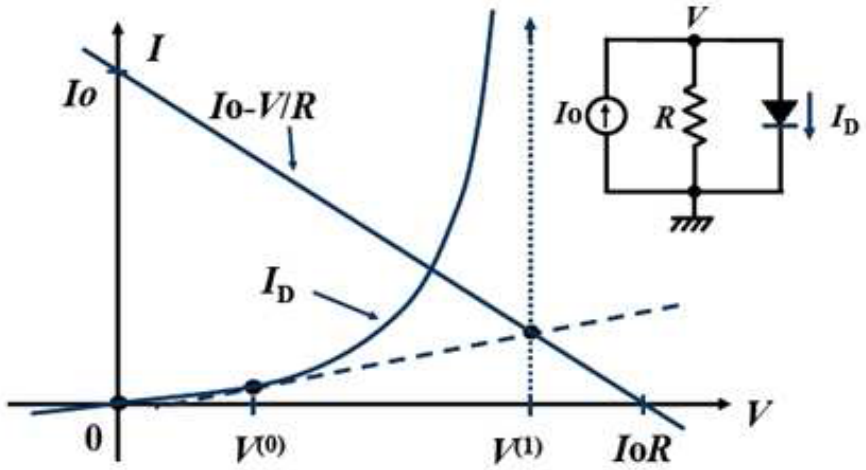

FIGURE 1.4: A graphical illustration of overflow problem of the NR method [1].

However, as we all know, the Newton-Raphson, NR, method is not globally convergent, which cannot guarantee the convergence all the time. It depends on the initial solution being close enough to the true solution [4]. There are many limitations which can make the NR method not converged. Such as shown in the Figs. 1.4 and 1.5, some special circuits' characteristics may also influence the convergence. Overflow or cycle phenomenon may occur during the Newton-Raphson iterations [14].

1.1.3.2 Continuation Methods

In order to deal with the non-convergence problem, many studies are done and many methods are proposed. From practical view, the NR method is modified in several ways from the limiting viewpoint and error-reduction viewpoint which are used in spice3 simulator and IBM's old simulator—ASTAP. Besides, some continuous methods, like Source stepping method and Gmin stepping method,

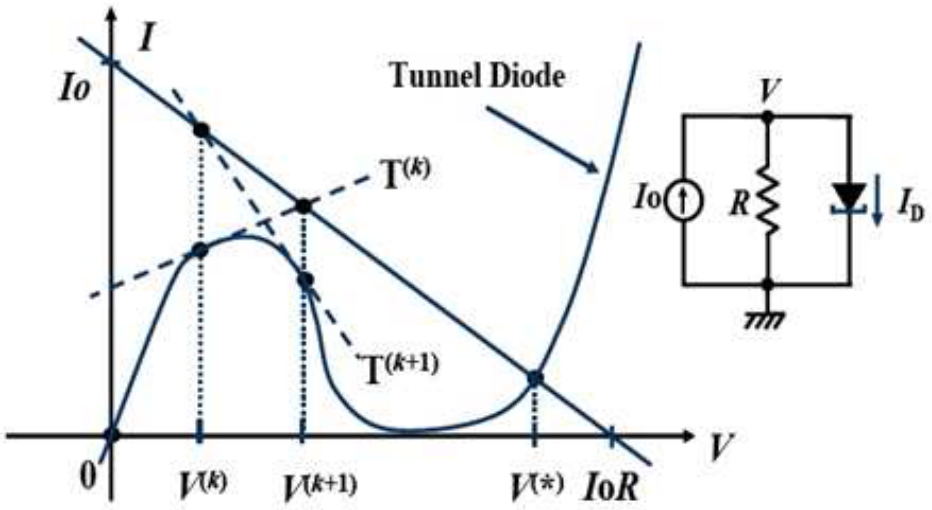

FIGURE 1.5: A graphical illustration of cycle phenomenon of the NR method [1].

are studied to deal with the limitation of the NR methods, which can improve convergence even with hundred elements.

Source Stepping Method

The source stepping is simple to implement and quite popular [19][20]. It is the fall-back approach used in SPICE when direct DC Analysis or DC sweep, using a plain Newton's method, fails to converge. Recall, the nonlinear modified nodal analysis (MNA) [13] equations are:

$$Gx + Hg(x) = s, \tag{1.4}$$

where the RHS vector s contains all (and only) the contributions from the independent sources; it is called the source vector. Most circuits have the useful property that if all independent sources are turned off, then all voltages and currents in the

circuit become zero. Thus, when $s = 0, x_0 = 0$ is a solution of the system. Note, turning off a voltage source means setting its voltage to zero, while for a current source it means setting its current to zero.

For circuits with this property, source stepping consists of first turning off all independent sources, so that $x = 0$ becomes a solution, and then ramping them up to their full values while solving the DC system at every point. Solving the DC circuit may be done using a plain Newton's method, with the solution at the previous source setting as an initial solution.

By using small enough increments (steps) in the source values, it is hoped that Newton convergence will be achieved at every point. If it fails to converge, one can retry with a smaller step size. Alternatively, one can try bringing up the different sources separately, or at different rates, etc. There are many such variations in the literature. The source stepping method works well for switching or oscillation circuits. However, it doesn't work for all cases, in particular, when the input voltage reaches the level necessary to turn on transistors in digital circuits. The solution can change sufficiently rapidly to cause converge failure.

Gmin Stepping Method

The algorithm of Gmin stepping method can be concluded as follows [13]:

1. A large conductance (called Gmin), such that, say $100\Omega = 1/G_{min}$, is connected from every node to ground. These high conductances swamp any large resistance in the elements, so that the circuit solution x_0 has every node voltage at very close to 0. This solution is easily found using a plain Newton's mehtod, starting with an initial solution of $x = 0$.

2. Then, the Gmin value is stepped down in small increments to some very small value, corresponding to a large resistance of, say $10^{12}\Omega = 1/G_{min}$. At

every step , the circuit is solved using a plain Newton's mehtod, using the solution at the previous step as a starting value.

3. The final solution is the DC solution of the original circuit.

There are other flavors of Gmin stepping, in which the conductances are connected across pn-junctions, or similar. It is a fairly simple technique to implement, similar to source stepping, and is available in most commercial simulators. As with source stepping, if it fails to converge, one can retry with a smaller step size. However, due to the increasing scale of integrated circuits, the Gmin stepping method is no more enough to succeed.

1.1.3.3 Homotopy Methods

Another important method is the homotopy methods which have been researched for many years [9–13]. It is a method from the theoretical viewpoint. Compared with all the continuation methods mentioned above, which are not necessary to guarantee global convergence, the theoretical standpoint methods are mainly focus on resolving the non-convergent problems fundamentally and strictly guarantee globally convergent. Basic concept of homotopy methods is continuous deformation of functions. In 1953, Davidenko raised predictor-corrector continuation method from mathematic viewpoint. After that, piecewise linear continuation method from the circuit simulation viewpoint, in which globally convergent is guaranteed, and simplicial algorithms are raised.

The homotopy method is a semi-analytical technique to solve nonlinear ordinary/-partial differential equations. The homotopy analysis method employs the concept of the homotopy from topology to generate a convergent series solution for nonlinear systems. This is enabled by utilizing a homotopy-Mclaurin series to deal

with the nonlinearities in the system. In the homotopy methods, the Newton homotopy method and the fixed-point (FP) homotopy method (or its variants) are well known [10–13]. These methods are proved to be globally convergent for MN equation. In particular, the FP homotopy method has an excellent property that a random choice of initial point gives a bifurcation free homotopy path with probability-one [1]. However, the homotopy method is element-dependent and hard to implement in the SPICE simulator [4]. Recently studies mainly focus on efficiency improvement [39][40]. Nowadays, the practical standpoint methods are mainly implemented in commercial circuit simulators. The homotopy method is dependent on device models so that with rapid semiconductor technology progress, it is not easy to implement in commercial simulator.

1.1.3.4 PTA Methods

Nowadays, PTA methods are considered as the very effective and promising methods [1]. Both source stepping and Gmin stepping require disabling the dynamic elements (optionally adding resistance from every node to ground). Source stepping requires modification of the independent sources, while Gmin stepping leaves the sources as they are but modifies the network. Both methods use stepping of a certain λ, as the homotopy parameter, and solve the DC circuit at every point using a plain Newton's mehtod. Pseudo-transient is another homotopy, where the homotopy parameter is time, and which has the salient features that a) the independent sources and dynamic elements are left intact and b) additional dynamic elements are added to the network [19]. The main idea of PTA method is that firstly insert certain pseudo-elements, capacitors or inductors, to the circuit, which needs to be solved. Thus a pseudo circuit will be composed. Secondly with a user-designated initial solution which can solve the pseudo circuit easily, a transient analysis will be carried out until a steady state achieved [4]. As if the steady state

can be obtained for the pseudo circuit, the solution for the original circuit is also obtained [14]. In pseudo-transient, the circuit dynamic elements help damp out the oscillations frequently encountered during the early phase of DC Analysis [14]. It can be slow, reportedly 2-19 times slower than plain Newton's method. But, it has proven to be quite successful in practice [2]. Nevertheless, the scheme can fail, for various reasons [2]:

1. At some time point, the Newton loop may not converge, even for the smallest allowable time-step.

2. We may not reach a DC steady state but, instead, an oscillatory response may be generated by the transient simulation.

3. The simulation may not reach a DC steady state during the time budget allotted to this pseudo-transient run.

There are variations on the basic pseudo-transient method [2]. One simpler possibility is to not modify the network in any way, but to ramp up the values of the independent sources over time [10]. This would be a combination of source stepping and pseudo-transient. Another variant includes adding a nonlinear capacitor from every node to ground, whose value is decreased over time [3]. During the transient simulation part of pseudo-transient, and because we only care about the final steady state solution, then [2, 3]:

1. We can take large time-steps, with little regard to numerical errors, provided us eventually converge to a DC steady state. This gives significant speed-up relative to regular Transient Analysis.

2. We can modify the dynamic elements, in an arbitrary fashion, provided we eventually converge to a DC steady state. This, crucially, is the key to establish the existence of a valid initial state.

In the commercial SPICE-like simulators, the PTA methods are also used when the source stepping fails to converge. The HSPICE has many convergence control options for the DC operating point analysis. For example, “Converge=1” uses the Damped Pseudo Transient Analysis in HSPICE [37]. Meanwhile, the LTSPICE also has ”ptranmax” option, which used the damped pseudo transient in the DC operating point analysis [41]. However, though the PTA method in HSPICE and L ICE also named as PTA, their algorithms and the source codes are confidentiality and not published in any papers or manuscript due to its commercial property.

1.2 Purpose of This Research

The technology to deal with non-convergence problem of the NR method in DC analysis shows great importance, and many methods have been researched. The compound element PTA, CEPTA, method [26][27] is researched in order to deal with the shortcomings of PTA methods. Comparing with the conventional PTA methods, oscillation problem is well eliminated with the compound element PTA method and it is more efficient for some circuits. However, from the tests, it is found that there are still some practical circuits and large-scale circuits do not have a good convergence performance due to the discontinuity problem. Besides, although delay in inverter chain circuit can be shorten by the time-varying resister so that oscillation problem can be overcome, it is obviously that oscillation problem still occurs in 15 stage MOS Invert chain circuit and BIP Invert chain circuit. Thus, the pseudo-transient algorithms need to be improved and modified. Conventional netlist method and SPICE3 implementation method of CEPTA algorithm have some limits that may influence the simulation results. Recently, to eliminate the oscillation from the numerical integration algorithm viewpoint, a damped PTA (DPTA) method [30] is proposed. However, the non-convergence problem is still a great challenge for all these methods when dealing with the practical large-scale circuits. Though the study of homotopy method from the theoretical viewpoint has developed recently, it is hard to implement. Therefore, the study on developing practical methods to obtain the DC solutions for large-scale circuits is an important task in circuit simulation, which should have excellent convergence performance and are easy to implement.

Thus, this research focuses on improving the convergence and efficiency of the PTA methods, which means better convergence performance, less cpu time and smaller number of NR iterations. In this dissertation, firstly, based on the CEPTA method, (1) a new SPICE3 implementation algorithm and (2) embedding algorithms are

proposed. In the proposed implementation algorithm, some limitations can be overcome, which may influence convergence of the NR method. The embedding algorithms provide different embedding positions of pseudo elements in the CEPTA method. The new implementation algorithm together with a suitable embedding position can extend the applicability of CEPTA method to the practical circuits and 15 stage CMOS inverter chain circuit. The convergence and efficiency of the CEPTA method can be improved.

Secondly, based on the DPTA method, (3) a ramping algorithm and (4) a restart algorithm are proposed to further improve the efficiency. In the proposed ramping algorithm, the supply voltages are ramped up from zero to their final values over time according to the certain ramping function without inserting any pseudo-inductors. Two effective ramping functions, the sine type ramping function and the cosine type ramping function, are also proposed. It can eliminate the oscillation due to the inserted inductors and improve the efficiency due to the non-zero elements in the Jacobian. Moreover, the restart algorithm can recognize whether the simulation is stuck into an infinite loop and help improve the convergence performance.

The proposed algorithms are implemented on the SPICE simulator and applied to practical large-scale analog circuits. The effectiveness are verified.

Chapter 2

Preliminaries

2.1 Pseudo-Transient Analysis Method

The pseudo-transient analysis method is firstly appeared in the advanced statistical analysis program (ASTAP), which is announced by IBM [15]. The pseudo-elements are named as reactive elements in ASTAP. By the addition of pseudo reactive elements, dc problems can be converted to transient problems [16].

2.1.1 Pure Pseudo-element Algorithms

Pure pseudo-elements are used in the pure PTA methods, which mainly include two algorithms. One of them is that insert pure constant capacitor and inductor into the circuit [1]. Another pure pseudo-element uses time-varying capacitor as the pseudo-element [17].

The PTA method with time-varying capacitor inserts small-valued capacitors between each node and ground, leading to a diagonally dominant matrix with better numerical stability. The time-step for the analysis is limited to values larger than 10^{-9}, which is usually sufficient for any network with these small capacitances included. The value of the capacitance decreases with increasing pseudo-times [17]. The efficiency of the pure PTA methods is not very satisfactory (time-consuming), and the insertion of the pure pseudo-element is easy to form an oscillator. Therefore, there are some improved PTA methods to overcome these problems.

2.1.2 CEPTA Algorithm

In [26], a CEPTA method is proposed to deal with the oscillation problem and low-efficiency problem of pure pseudo-element algorithms. The CEPTA method is

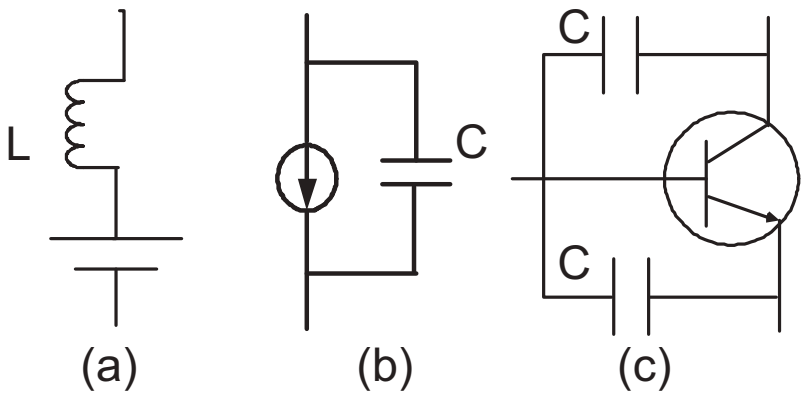

FIGURE 2.1: Pseudo-elements in constant pure PTA method [27].

demonstrated to be efficient to overcome oscillation by inserting conductance and resistors to form the compound pseudo-elements.

2.1.2.1 Compound pseudo element

Conventional PTA methods mainly use pure pseudo elements including pure constant capacitor, constant inductor as shown in Fig.2.1 or time-varying capacitor [16, 20].

In the CEPTA method, as shown in Fig.2.2, novel pseudo-elements used are compound, named as branch RVC and GVL. In the branches, the constant capacitor and inductor are used together with time-varying resistor and conductor [26].

The values of resistor and conductor increase very quickly over time with the specified initial values R_{V0} and G_{V0} as shown in Fig.2.2.(c). They can be considered as infinity so that the capacitor and inductor can be considered as open circuit or short circuit when the steady state obtained [26]. The CEPTA method has been proved to avoid oscillation problems well [26].

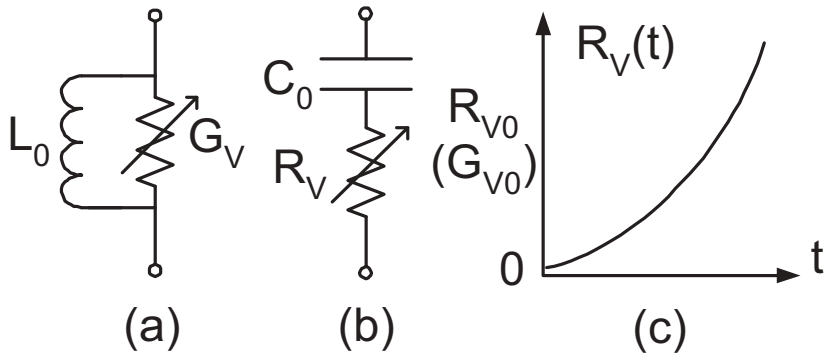

FIGURE 2.2: Compound pseudo-elements for CEPTA method [36].

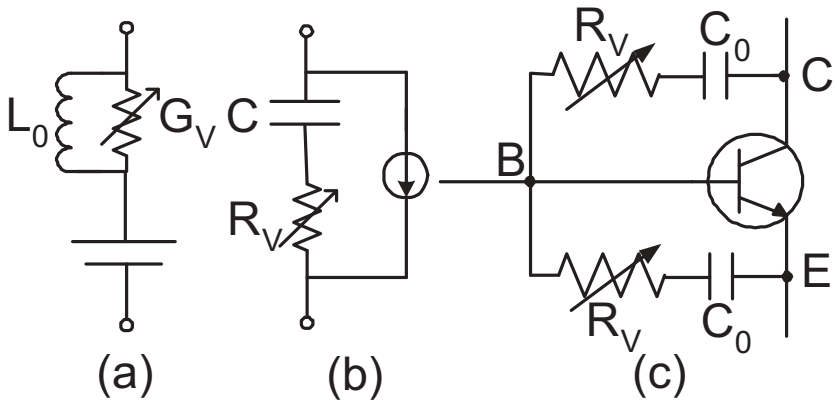

FIGURE 2.3: Insert position of the compound pseudo-elements [36].

The RVC branch is inserted into the independent voltage source as Fig.2.3.(a) shown. The branch GVL is added into the independent current source and transistors (including MOS and BJT transistors) in the circuit as Figs. 2.3.(b) and (c) shown.

2.1.2.2 Conventional SPICE3 implementation method

The CEPTA method is firstly implemented in HSPICE by modeling the pseudo elements in the netlist method [19, 26]. The G_V and R_V are modeled by using the controlled current and voltage source, GGV and ERV [26]. However, by this

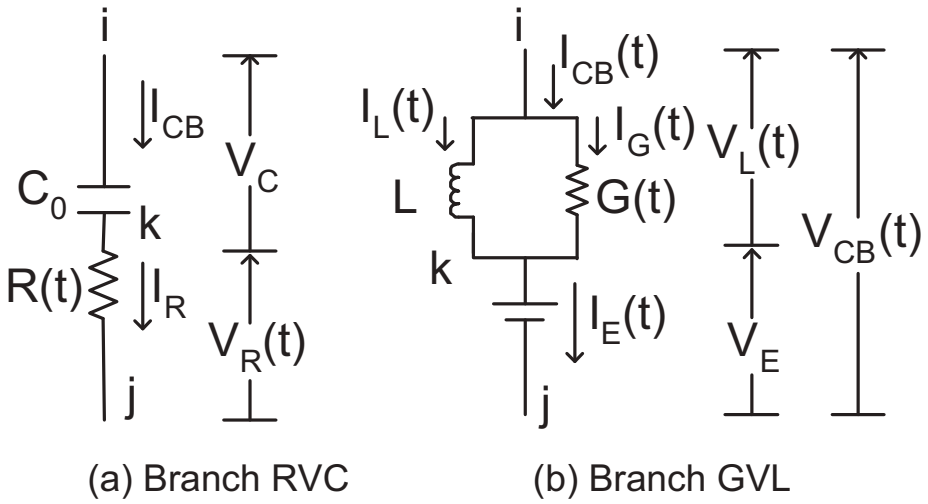

FIGURE 2.4: Branch RVC/GVL in SPICE3 implementation.

netlist method, additional nodes will be extended to the circuit, and the structure of the Jacobian matrix will be enlarged. Calculation during the simulation becomes complex especially for large-scale LSI circuits, which makes the CEPTA method is not that practical [27].

In [27], a SPICE3 implementation algorithm of the CEPTA method is reported. We call it "algorithm 1" in this paper.

The branch RVC is implemented into the circuit between node i and node j for to each independent current source in the SPICE3 as Fig.2.4.(a) shown. The current through the capacitor C_0 and resistor $R(t)$ is defined as i_{CB}. Besides, V_{CB} and V_C respectively represent the voltage of compound branch and capacitor.

The relationships between compound branch current, capacitor voltage and compound branch voltage can be expressed as following Eqs.(2.1) and (2.2). And Eq.(2.3) can be obtained.

$$I_{CB} = C_0 \frac{dV_C(t)}{dt} \ . \tag{2.1}$$

$$V_C = V_{CB} - V_R = V_{CB} - I_{CB}R(t) \ . \tag{2.2}$$

$$I_{CB} = C_0 \frac{d(V_{CB} - I_{CB}R(t))}{dt} \ . \tag{2.3}$$

According to the algorithm in [27], the numerical integration method (Backward Euler method is used here) is applied to the differential part of Eq.(2.3), at discrete time point t_{n+1}, the equation of compound branch current can be obtained as following equivalent Eq.(2.4).

$$I_{CB}^{n+1} = G_{CBeq} V_{CB}^{n+1} + C_{CBeq} \ , \tag{2.4}$$

where

$$G_{CBeq} = \left(\frac{h^{n+1}}{C_0} + R(t^{n+1}) + h^{n+1} R^{'}(t^{n+1}) \right)^{-1} \ , \tag{2.5}$$

$$C_{CBeq} = G_{CBeq} \left(I_{CB}^{n} R(t^{n+1}) - V_{CB}^{n} \right) \ . \tag{2.6}$$

The GVL branch is implemented into the circuit between node i and k for each independent voltage source. Similar as the branch RVC, by applying the numerical integration method to the differential part in Eq.(2.7), equivalent equation of branch voltage can also be obtained as Eq.(2.8).

$$V_L(t) = L\frac{d\left(I_{CB} - G(t)(V_{CB} - E)\right)}{dt} . \tag{2.7}$$

$$V_{CB}^{n+1} = R_{CBeq}I_{CB}^{n+1} + V_{CBeq} , \tag{2.8}$$

where,

$$R_{CBeq} = \left(\frac{h^{n+1}}{L} + G(t^{n+1}) + h^{n+1}G'(t^{n+1})\right)^{-1} , \tag{2.9}$$

$$V_{CBeq} = R_{CBeq}\Big(- I_{CB}^{n} + G(t^{n+1})V_{CB}^{n} + Eh^{n+1}G'(t^{n+1}) + E\frac{h^{n+1}}{L}\Big) . \tag{2.10}$$

2.1.3 Damped Pseudo-Transient Analysis Algorithm

Recently, the PTA method is developed to use artificially enlarged damping effect to eliminate the oscillation problem, which is reported in [30] and named as DPTA [1]. From the electronic circuit viewpoint, damping is an effect that reduces the amplitude of oscillations. It can be used in circuit simulation to reduce the oscillation [30]. The PTA method includes two major parts: the pseudo-elements and the numerical integration algorithms. The CEPTA method changes the pseudo-elements to overcome oscillation problem [26], while DPTA method proposes new numerical integration algorithms to get heavy damping effect [30]. In [30, 35], the consistency, convergence, and stability region of DPTA algorithm are analyzed and an implementation in SPICE3 is studied. The inserted pseudo-elements and their insert positions into the circuit are shown in Fig. 2.5, including constant pure

[1] Commercially available circuit simulator's PTA algorithms are not published and details are not known though they also named as DPTA.

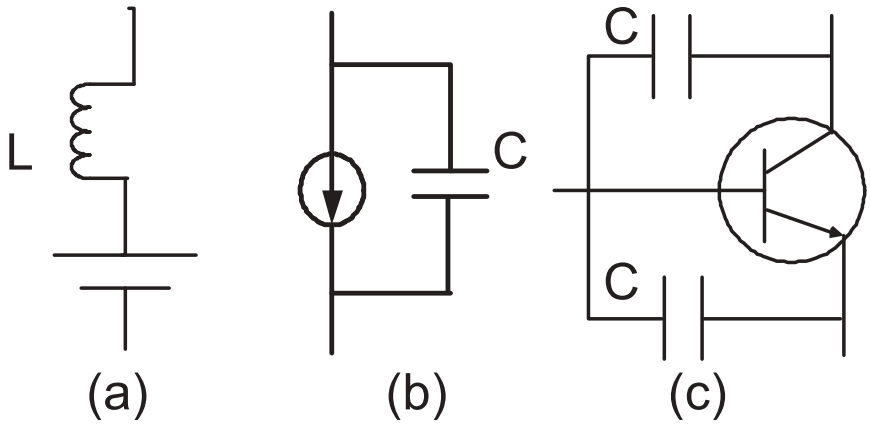

FIGURE 2.5: The pseudo-elements of DPTA method and their insert positions into the circuit. (a) Pseudo-inductor inserted to the voltage source. (b) Pseudo-capacitor inserted to the independent current source. (c) Pseudo-capacitor for the BJT and MOS transistors.

capacitors and inductors. Besides, there are also some other embedding positions also available for the DPTA method from the efficiency viewpoint [29]. Assume that the DC circuit need to be solved can be expressed as Eq. (2.11).

$$\mathbf{F}(\mathbf{x}) = \mathbf{0}, \tag{2.11}$$

where $\mathbf{x} = (\mathbf{v}, \mathbf{i})^T \in \mathbb{R}^m$, and $m = N + M$. The variable vector $\mathbf{v} \in \mathbb{R}^N$ denotes the node voltages to the datum node and the variable vector $\mathbf{i} \in \mathbb{R}^M$ denotes the branch currents of the independent voltages sources. Thus obtaining the DC operating points needs to solve this nonlinear algebraic equations. The constant, pure pseudo elements are composed of capacitors and inductors in the DPTA method. For the capacitor and inductor, the relationship between voltage and

current can be expressed as:

$$I_C(t) = C\frac{dV_C(t)}{dt}, \tag{2.12}$$

$$V_L(t) = L\frac{dI_L(t)}{dt}. \tag{2.13}$$

Therefore, after the pseudo-elements inserted, the circuit need to be solved has changed to the pseudo circuit case. Thus we can write the equations as follows [26].

$$\mathbf{D}\dot{\mathbf{x}}(t) = -\mathbf{F}(\mathbf{x}(t), t) \tag{2.14a}$$

$$\mathbf{x}(t_0) = \mathbf{x_0} \tag{2.14b}$$

$$\dot{\mathbf{x}}(t)\,\big|_{t=t_f} = \mathbf{0}, \tag{2.14c}$$

where $\dot{\mathbf{x}}(t) = (\dot{\mathbf{v}}(t), \dot{\mathbf{i}}(t))^T$ is the derivative of $\mathbf{x}$ with respect to the time t, $\mathbf{D}$ is a matrix used to represent the pseudo capacitance and inductance. The transient analysis started at the time point t_0 with the initial value of $\mathbf{x}$, $\mathbf{x_0}$. The circuit gets the solution at time point t_f finally.

After inserting the pseudo-elements into the circuit, a new pseudo circuit is formed as shown in Eq. (2.15).

$$\mathbf{F}(\mathbf{x}(t), t) + \mathbf{D}\dot{\mathbf{x}}(t) = \mathbf{0} \tag{2.15a}$$

$$\mathbf{x}(t_0) = \mathbf{x_0} \tag{2.15b}$$

$$\dot{\mathbf{x}}(t)\,\big|_{t=t_f} = \mathbf{0}. \tag{2.15c}$$

Then applying the k step damped differentiation formulas (DDF-k), with artificially damping effect described in Eq. (2.16) [30], to the differential part in Eq. (2.15) at discrete time point t_{n+1}, the Eq. (2.15a) is numerically integrated to the steady state using a variable time-step scheme that attempts to increase the time-step as $\mathbf{F}(\mathbf{x}(t), t)$ approaches $\mathbf{0}$.

$$\mathbf{x}_{n+1} \quad = \quad \mathbf{x}_{n+1-k} + \mathbf{f}(\mathbf{x}_{n+1}, t_{n+1}) \sum_{j=0}^{k-1} (h_{n+1-j}), \tag{2.16}$$

where $t \in \mathbb{R}$, $\mathbf{x} : \mathbb{R} \to \mathbb{R}^m$, and $\mathbf{f} : \mathbb{R}^m \times \mathbb{R} \to \mathbb{R}^m$.

An intuitive understanding about the difference between damped differential formula and the backward Euler method is shown in Eqs. (2.17) and (2.18) by applying to the current at discrete time point t_{n+1} as an example. The backward Euler method is shown in Eq. (2.17). Here we use the 2-step DDF method as an example, which is shown in Eq. (2.18). Different from the backward Euler method, the 2-step damped method uses the values at former discrete time point t_{n-1} instead of t_n. Thus the heavier damping effect can be obtained for the simulation. Details are shown in [30].

$$\left.\frac{di}{dt}\right|_{t_{n+1}} = \frac{I_{n+1} - I_n}{h_{n+1}}, \tag{2.17}$$

$$\left.\frac{di}{dt}\right|_{t_{n+1}} = \frac{I_{n+1} - I_{n-1}}{h_{n+1} + h_n}. \tag{2.18}$$

The DPTA method is demonstrated very efficient to overcome the oscillation because of its heavy damping effect by many test examples in [30].

2.2 Initial Solution Method

The conventional compound element pseudo-transient analysis methods run a transient analysis with zero initial value to seek the steady-state solution. In the initial solution method, appropriate non-zero initial values are set to obtain better simulation results. That the initial value is closer to the true solution during the transient analysis can reduce the number of Newton iterations and shorten of time leading to the steady-state solution once you start, and efficiency is improved [28].

As shown in Fig. 2.6, the initial voltage values of the base-collector $V_{BE}^0 = 0.7V$ and base-emitter $V_{BC}^0 = 0.0V$ are set for the bipolar transistor. For the MOS transistor, the gate-source voltage V_{GS}^0 is set to V_{th}^0, while the gate and the drain voltage V_{GD}^0 is set to $0.0V$ in Fig. 2.7. Here, the V_{th}^0 is the parameter of MOS transistor, the threshold voltage [28].

This method is implemented on our own SPICE simulator Waseda SPICE (WSPICE), and shows improvements on the simulation efficiency.

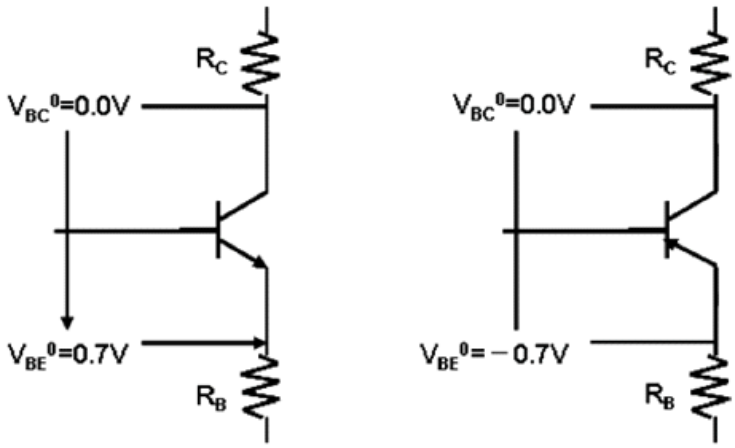

FIGURE 2.6: Initial solution for BJT transistor.

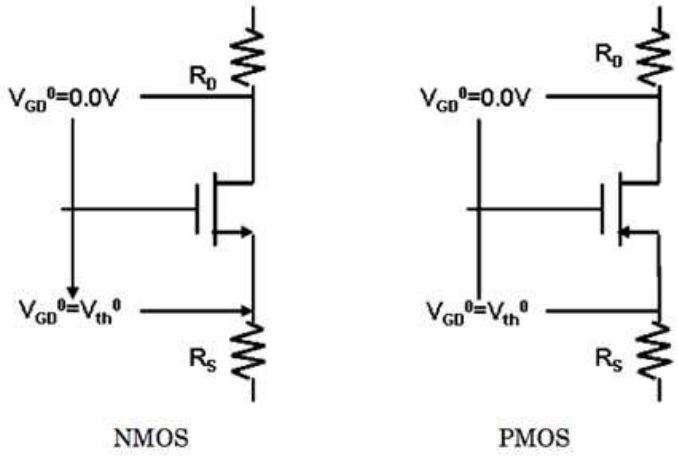

FIGURE 2.7: Initial solution for MOS transistor.

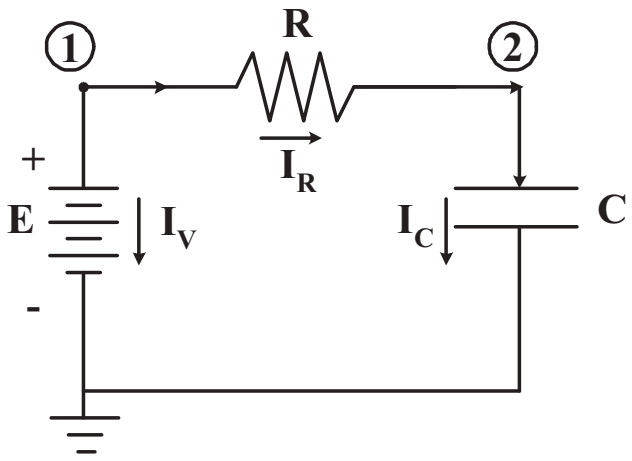

FIGURE 2.8: A linear resistive circuit.

2.3 Modified Nodal Analysis

For formulating and solving the circuit equations, a systematic and automatic approach is needed. The modified nodal analysis (MNA) is one of the popular approaches for systematic equation formulation. The MNA process mainly includes four steps according to the KCL, KVL and equations of elements. The MNA process is widely used in the current circuit simulators. Here we use a linear resistive circuit shown in the Fig. 2.8 as an example to show the MNA formulation [19]. The KCV at every node and be written as follows.

In step 1, at the node 1, we can have the KCL equations:

$$I_V + I_R = 0.$$

At the node 2, we can have equations:

$$-I_R + I_C = 0.$$

In step 2, we can observe that:

$$\begin{aligned} E &= V_1, \\ V_R &= V_1 - V_2, \\ V_C &= V_2, \end{aligned}$$

and the results are:

$$\begin{aligned} G(V_1 - V_2) + I_V &= 0, \\ C\frac{dV_2}{dt} + G(V_2 - V_1) &= 0. \end{aligned}$$

In step 3, we have the equation comes from the fact that:

$$V_1 = E.$$

In step 4, we can be obtain:

$$Dx^{'}(t) + Ax(t) = f,$$

where $x = \begin{pmatrix} V_1 & V_2 & I_V \end{pmatrix}^T$, $f = \begin{pmatrix} 0 & 0 & V \end{pmatrix}^T$, $A = \begin{pmatrix} G & -G & 1 \\ -G & G & 0 \\ 1 & 0 & 0 \end{pmatrix}$, and $D = \begin{pmatrix} 0 & 0 & 0 \\ 0 & C & 0 \\ 0 & 0 & 0 \end{pmatrix}$.

Chapter 3

Effective Implementation and Embedding Algorithms of CEPTA Method

[Related papers [A2],[B3],[C2]]

3.1 Introduction

Circuit analysis is increasingly dependent on EDA programs with the vigorous development of semiconductor technique. As one of the most widely used EDA software, SPICE or SPICE-like simulators have been studied for many years. There have been many commercial SPICE-like simulators such as HSPICE, PSPICE and so on [1, 2, 16–18, 27]. In the SPICE-like simulators, the most basic task, and sometimes the most difficult task, is to find the DC operating points for the non-linear LSI circuits. The Newton-Raphson (NR) algorithm is employed to do this due to that they share the same core SPICE 3. However, only if the initial guess is close enough to the final solution, the NR method may converge. Otherwise, the non-convergence problem occurs [1, 2, 16–18, 27].

For now, there are many techniques and improvements proposed to deal with the "fails to convergence" problem of the NR method, like source stepping method, Gmin stepping method, homotopy methods, pure PTA methods and compound element PTA (CEPTA) [1, 2, 16–18, 27]. These algorithms are now used in SPICE-like simulators [20]. HSPICE employs the PTA method. In addition, homotopy methods have been studied mainly from the theoretical viewpoint. There are many homotopy methods. However, they are device model dependent and difficult to implement in SPICE-like simulators, though it is globally convergent [21, 23–25]. Even some homotopy methods are implemented in the SPICE-like simulators, if a new model has been implemented, the codes need to be modified. The PTA method is studied from the practical viewpoint, and it does not depend on the device model. If a new device model is implemented, the codes do not need to be modified. Our standpoint in this chapter is to eliminate the limitation of NR method for the DC analysis from the practical standpoint.

Among all these continuation methods for SPICE simulators, the PTA method is regarded as the most promising one [19, 26]. The idea of PTA method is that firstly insert some certain pseudo elements to the original circuits, and then do the transient analysis with some initial values. As the circuit gets the steady state, the solution at that moment can be regarded as the solution of the original circuit. Conventional PTA methods include constant pure PTA method [23], time-varying pure PTA method [16] and CEPTA method [26].

Pure PTA methods mainly use pure pseudo elements including constant capacitor, inductor, or time-varying pseudo capacitor [16, 23, 26, 27]. Pure PTA methods have an oscillation problem due to the insert elements and time-consuming problem. In order to deal with this oscillation problem, PTA method with compound pseudo elements is proposed in [26, 27], including compound pseudo branch RVC and GVL. Compared with pure PTA methods, the CEPTA method can avoid the oscillation caused by the pseudo capacitors or inductors. Reasons are shown in [26].

As known, one of the most important advantages of PTA method is that we do not need to care about how large the step size is [26]. We can take large step size with little regard to numerical errors, which gives significant speed-up relative to regular transient analysis [19]. However, in the conventional implementation method of the CEPTA algorithm [27], large step size value may cause non-convergence problem of the Newton-Raphson method, which may make the simulation efficiency not that satisfactory. Thus, though the CEPTA method has a significant performance for some oscillation problems, there are still some practical circuits or large-scale circuits have non-convergence problems. The efficiency of simulation is still not satisfactory for nonlinear circuits. Besides, some heavy oscillation problem still can not be solved.

In this chapter, we propose a new SPICE3 implementation algorithm and embedding algorithms for the CEPTA method. In the proposed implementation algorithm, some limitations of the conventional method can be solved, which may improve convergence of the Newton-Raphson iteration. Besides, the proposed implementation method also holds the property that there is no additional node inserted in the circuit and the structure of the Jacobian matrix will not be enlarged [27]. The simulation efficiency can be confirmed. Moreover, different embedding positions of pseudo elements in the CEPTA method are also proposed. With new implementation algorithm and a suitable embedding position, it can extend the applicability of the CEPTA method to practical large-scale circuits and some heavy oscillation circuits. Simulation performance of the CEPTA method can be improved greatly. Besides, the proposed algorithms can be also extended to other PTA-like methods.

3.2 Challenges in CEPTA Method

As shown in precious, the CEPTA method cannot deal with heavy oscillation problems, such as 15-stage CMOS inverter chain circuit. Though the oscillation can be eliminated in some circuits, including the 5-stage inverter chain circuits, the oscillation problem in 15-stage CMOS inverter chain circuit still exists, and circuit cannot converge. Besides, the limitations of conventional implementation method make the CEPTA method not that practical. Non-convergence problem and low efficiency still occurs in some practical and large-scale circuits. The CEPTA method in the former publications was tested mainly for some small-scale circuits and did not consider various kinds of circuits. Thus, the simulation efficiency and convergence still need to be improved especially for large scale and practical nonlinear circuits. Therefore, we have to challenge these problems of the CEPTA method:

1. Propose a new SPICE3 implementation method, which has no limitation of the step size, to have a better convergence and efficiency performance.

2. Extend the embedding algorithm to satisfy various kinds of circuits.

3.3 Proposed Method

Two algorithms are proposed in this section. Firstly, a new SPICE3 implementation algorithm for branch RVC and GVL is presented. The convergence of this method is also analyzed and proved. Differences between the proposed implementation method and conventional algorithm [27] are also analyzed. Secondly, embedding algorithms for the CEPTA method are proposed, which can also be extended to other PTA-like algorithms.

3.3.1 Implementation Method in SPICE3 Simulator

In this section, 4 new SPICE3 implementation algorithms, which are distinguished by applying backward Euler method to different formulas, are discussed and the most efficient one is proposed. This proposed algorithm also realizes branches GVL and RVC by companion models without increasing additional nodes in the circuit. The obtained companion model for RVC branch is as shown in Fig.3.1. There is no additional node k and only insert into the circuit between nodes i and j. Thus, structure of Jacobian matrix will not be enlarged. Simulation efficiency is also guaranteed. Moreover, the proposed algorithm does not have some limitations compared with algorithm 1 by applying numerical integration method to differential parts in a different way. Thus, the convergence performance and simulation efficiency can be improved.

3.3.1.1 Branch RVC

We take the branch RVC between node i and j as a whole compound part. We can get the continuous time domain differential equations of the branch current

as shown in Eqs.(2.1) and (2.3). Besides, the voltage relationship of capacitor, resistor and compound branch can also be obtained as Eq.(3.1).

$$V_C(t) = V_{CB}(t) - V_R(t) \ . \tag{3.1}$$

For the first implementation algorithm, the BE formula is applied to the Eq. (3.1). After that, we can obtain

$$I_{CB}^{n+1} = G_{CBeq} V_{CB}^{n+1} + C_{CBeq}, \tag{3.2}$$

where

$$G_{CBeq} = (1 + G_{eq}(h^{n+1} R^{'}(t^{n+1})))^{-1} G_{eq}, \tag{3.3}$$

$$C_{CBeq} = G_{CBeq}(-V_{cb}^{n} + R(t^{n+1}) I_{CB}^{n}). \tag{3.4}$$

Different from algorithm 1, in this proposed method, we mainly consider the Eq.(2.1). Applying the numerical integration method to the Eq.(2.1) directly at discrete time point t^{n+1}. The Backward Euler method is chosen here as the numerical integration method to solve the equations. Thus, we can get

$$\left.\frac{dV_C(t)}{dt}\right|_{t=t^{n+1}} = \frac{V_C^{n+1} - V_C^{n}}{h^{n+1}} \ . \tag{3.5}$$

Then combine Eqs.(2.1) (3.1) and (3.5), through discretization, Eq.(3.6) can be got at time point t^{n+1},

$$\begin{aligned} I_{CB}^{n+1} &= C_0 \frac{V_C^{n+1} - V_C^n}{h^{n+1}} \\ &= C_0 \frac{(V_{CB}^{n+1} - V_R^{n+1}) - (V_{CB}^n - V_R^n)}{h^{n+1}} \ . \end{aligned} \tag{3.6}$$

The voltage of resistor can be expressed as Eq.(3.7) from the Fig.2.4.(a) in the circuit at discrete time point t^{n+1},

$$V_R^{n+1} = I_R^{n+1} R(t^{n+1}) = I_{CB}^{n+1} R(t^{n+1}) \ . \tag{3.7}$$

Thus,

$$I_{CB}^{n+1} = C_0 \frac{\left(V_{CB}^{n+1} - I_{CB}^{n+1} R(t^{n+1})\right) - (V_{CB}^n - I_{CB}^n R(t^n))}{h_{n+1}} \ . \tag{3.8}$$

We can obtain a new equation of compound branch current at discrete time point t^{n+1},

$$\begin{aligned} I_{CB}^{n+1} = \left(h^{n+1}/C_0 + R(t^{n+1})\right)^{-1} \left(V_{CB}^{n+1} - V_{CB}^n + \right. \\ \left. R(t^n) I_{CB}^n\right) \ , \end{aligned} \tag{3.9}$$

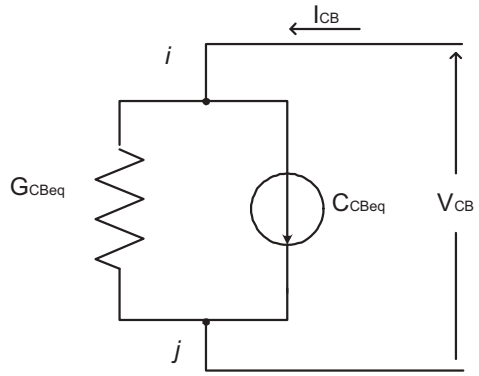

FIGURE 3.1: Companion model for RVC branch obtained from implementation algorithm.

which can be written as the following equivalent Eq.(3.10).

$$I_{CB}^{n+1} = G_{CBeq} V_{CB}^{n+1} + C_{CBeq} \ , \tag{3.10}$$

where,

$$G_{CBeq} = \left(\frac{h^{n+1}}{C_0} + R(t^{n+1}) \right)^{-1} \ , \tag{3.11}$$

$$C_{CBeq} = G_{CBeq} \left(I_{CB}^{n} R(t^n) - V_{CB}^{n} \right) \ . \tag{3.12}$$

Therefore, a new value of the G_{CBeq} and C_{CBeq} for the companion model of branch RVC can be obtained. In this obtained new equations, there is no derivative of resistor used.

3.3.1.2 Branch GVL

From Fig.2.4.(b), insert the GVL branch into the independent voltage source in the circuit. We take the GVL branch and voltage source together as a compound branch. Note that compound branch voltage is V_{CB}, and the current is I_{CB}. The inductor voltage can be expressed as Eq.(3.13). The currents can be expressed as Eqs.(3.14) and (3.15).

$$V_L(t) = L\frac{dI_L(t)}{dt} , \tag{3.13}$$

$$I_{CB}(t) = I_L(t) + I_G(t) , \tag{3.14}$$

$$I_G(t) = G(t)V_L(t) = G(t)\left(V_{CB}(t) - E\right) . \tag{3.15}$$

In the same way as branch RVC, by firstly applying the Backward Euler method to the differential part of Eq.(3.13) directly, at discrete time point t^{n+1}, we can get

$$\left.\frac{dI_L(t)}{dt}\right|_{t=t^{n+1}} = \frac{I_L^{n+1} - I_L^n}{h^{n+1}} . \tag{3.16}$$

Thus,

$$\begin{aligned} V_L^{n+1} &= V_{CB}^{n+1} - E \\ &= L\frac{di_L(t)}{dt} = L\frac{I_L^{n+1} - I_L^n}{h^{n+1}} \\ &= L\frac{I_{CB}^{n+1} - G^{n+1}(V_{CB}^{n+1} - E) - (I_{CB}^n - G^n(V_{CB}^n - E))}{h^{n+1}} \end{aligned}$$
$$. \tag{3.17}$$

The following equation can be obtained at discrete time point t^{n+1},

$$V_{CB}^{n+1} = \left(\frac{h^{n+1}}{L_0} + G^{n+1}\right)^{-1} \left(I_{CB}^{n+1} - I_{CB}^n + G^n\left(V_{CB}^n - E\right) + \left(\frac{h^{n+1}}{L_0} + G^{n+1}\right) E\right) \ , \tag{3.18}$$

which can be written as following equivalent Eq.(3.19).

$$V_{CB}^{n+1} = R_{CBeq} I_{CB}^{n+1} + V_{CBeq} \ , \tag{3.19}$$

where,

$$R_{CBeq} = \left(\frac{h^{n+1}}{L_0} + G^{n+1}\right)^{-1} \ , \tag{3.20}$$

$$V_{CBeq} = R_{CBeq}\left(-I_{CB}^n + G^n(V_{CB}^n - E)\right) + E \ . \tag{3.21}$$

Similarly, we can obtain the new equivalent resistance R_{CBeq} and voltage V_{CBeq} for the compound pseudo branch GVL. The equivalent resistance and voltage value are different from the algorithm1.

3.3.1.3 Convergence consideration

We take the branch RVC as an example to prove the convergence of the proposed SPICE3 implementation method. Assume that the solution curve is continuous.

Eq.(3.10) can be rewritten as the following Eq. (3.22),

$$I_{CB}^{n+1} = \left(\frac{h^{n+1}}{C_0} + R(t^{n+1})\right)^{-1} \left(V_{CB}^{n+1} - V_{CB}^{n}\right) + \left(\frac{h^{n+1}}{C_0} + R(t^{n+1})\right)^{-1} R(t^n) I_{CB}^{n} \ . \tag{3.22}$$

According to the time-varying function of pseudo resistor $R_v = R_{v0}e^{t/\tau}$, when $t^m \gg \tau$ [26], we can obtain

$$R(t^m) \to \infty \ ,$$
$$\left(\frac{h^{m+1}}{C_0} + R(t^{m+1})\right)^{-1} \to 0 \ .$$

Thus, we can get

$$I_{CB}^{m+1} \approx \left(\frac{h^{m+1}}{C_0} + R(t^{m+1})\right)^{-1} \left(R(t^m) I_{CB}^{m}\right) \ . \tag{3.23}$$

Then, from time step m, until time step n, $(n > m)$,

$$\frac{I_{CB}^{n}}{I_{CB}^{n-1}}\frac{I_{CB}^{n-1}}{I_{CB}^{n-2}}\cdots\frac{I_{CB}^{m+1}}{I_{CB}^{m}} \approx \frac{R(t^{n-1})}{\frac{h^n}{C_0}+R(t^n)}\frac{R(t^{n-2})}{\frac{h^{n-1}}{C_0}+R(t^{n-1})}\cdots\frac{R(t^{m})}{\frac{h^{m+1}}{C_0}+R(t^{m+1})} \ . \tag{3.24}$$

For $\forall x \in [m, n)$, we have

$$\frac{R(t^x)}{\frac{h^{x+1}}{C_0}+R(t^{x+1})} < 1 \ ,$$

thus the right side of equation (3.24) approaches to 0,

which means $I_{CB}^{n} \to 0$.

Current of capacitor branch finally becomes zero, which means capacitor and resistor branch to be open.

With similar way, it can also be proved $V_{CB}^{n} \to E$ finally in GVL branch case. Thus, the effect of pseudo-element appears and convergence of the proposed algorithm is assured.

3.3.1.4 Analysis

The conventional implementation algorithm applies the numerical integration method in the compound branch level for the compound pseudo elements, while the proposed implementation algorithm applies the numerical integration algorithm in individual element level by decomposing the compound branch. We also take the

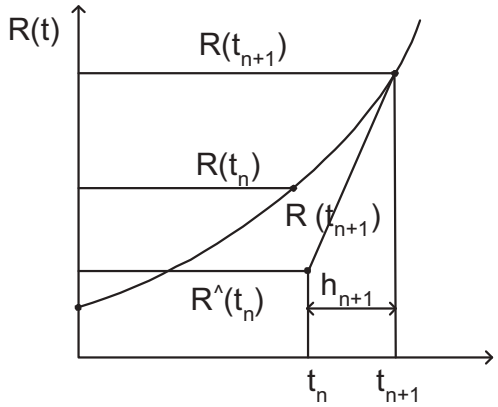

FIGURE 3.2: Resistor value at time point t_n of different methods.

RVC branch as an example here. The main difference between algorithms 1 [27] and our proposed implementation algorithm (we call it algorithm 2 in this thesis) is how to evaluate the equivalent conductance and current. From the circuit interpretation view point, the term $-G_{CBeq}^{-1}C_{CBeq}$ represents the capacitor branch voltage $V_C(t^n)$. Equation (3.25) shows how to evaluate voltage of capacitor at discrete time point n of algorithm 1, while Eq.(3.26) shows the evaluation way of algorithm 2.

$$V_C(t^n) \approx R(t^{n+1})I_{CB}^n - h^{n+1}R^{'}(t^{n+1})I_{CB}^{n+1} , \tag{3.25}$$

$$V_C(t^n) \approx R(t^n)I_{CB}^n . \tag{3.26}$$

An intuitive understanding about the differences of how to evaluate resistor value at time point t^n is shown in Fig.3.2. Algorithm 2 uses $R(t^n)$ directly. However, algorithm 1 [27] considers the information at the time point t^{n+1} only and uses $\hat{R}(t^n) = R(t^{n+1}) - h^{n+1}R^{'}(t^{n+1})$ instead. Algorithm 1 has the limitation when the time step h^{n+1} is large. If the step size h^{n+1} is large, the value of $\hat{R}(t^n)$ would be negative. Some strange phenomenon occurs in the iteration process and

iteration does not converge. So the step size can not be large in the algorithm1. While in the proposed algorithm, no such limitation. This limitation influences the convergence and simulation efficiency of the Newton-Raphson iteration method. With the proposed implementation algorithm, it does not depend on the time step size h^{n+1}. Thus, without the limitation of the step size value, simulation performance can be improved.

From this analysis, we also propose another three implementation algorithms, named as Algorithms 3-5. Five algorithms, including conventional implementation algorithm 1 and proposed algorithms 2-5, are obtained as follows:

$$
\begin{aligned}
&Algorithm1: \\
&\qquad G_{CBeq} = (1 + G_{eq}(h^{n+1}R^{'}(t^{n+1})))^{-1}G_{eq}, \\
&\qquad C_{CBeq} = G_{CBeq}(-V_{cb}^{n} + R(t^{n+1})I_{CB}^{n}). \\
&Algorithm2: \\
&\qquad G_{CBeq} = (1 + G_{eq}R(t^{n+1}))^{-1}G_{eq}, \\
&\qquad C_{CBeq} = G_{CBeq}(-V_{cb}^{n} + R(t^{n})I_{CB}^{n}). \\
&Algorithm3: \\
&\qquad G_{CBeq} = (1 + G_{eq}R(t^{n+1}))^{-1}G_{eq}, \\
&\qquad C_{CBeq} = G_{CBeq}(-V_{cb}^{n} + R(t^{n+1})I_{CB}^{n}). \\
&Algorithm4: \\
&\qquad G_{CBeq} = (1 + G_{eq}R(t^{n+1}))^{-1}G_{eq}, \\
&\qquad C_{CBeq} = G_{CBeq}(-V_{cb}^{n} + R_{V}^{0}I_{CB}^{n}). \\
&Algorithm5: \\
&\qquad G_{CBeq} = (1 + G_{eq}R(t^{n+1}))^{-1}G_{eq}, \\
&\qquad C_{CBeq} = G_{CBeq}(-V_{cb}^{n}).
\end{aligned}
\tag{3.27}
$$

3.3.2 Embedding Algorithms

The embedding algorithms provide several insert positions for pseudo capacitors. This method is applied to MOS and BJT transistors. In the compound-element pseudo transient analysis method, embedding position of pseudo element may influence the simulation results performance and efficiency a lot.

In [26, 27], the compound pseudo-capacitor is inserted between Base-Collector and Base-Emitter for BJT transistors as shown in Fig.3.3.(a). In the homotopy method, the BE-BC position is chosen for the bipolar transistors [19]. In this paper, we extend 3 positions to improve the convergence performance and simulation efficiency. We also implement them on our SPICE simulator (Waseda SPICE). These three positions for bipolar transistors in embedding algorithm are between Base-Collector, Base-Emitter and the diagonal position as shown in Figs.3.3.(b), (c) and (d). The embedding algorithm for CMOS transistor is the same as bipolar, GD, GS and diagonal positions. The diagonal position in Fig.3.3.(d) inserts capacitor between base and ground, collector and ground, emitter and ground. With the diagonal position embedding algorithm, compound pseudo elements are in the diagonal position of the Jacobian matrix.

F lation conditions, the appropriate embedding algorithm should be carefully selected to obtain the best simulation performance. From the large numbers of test results, there is no fixed embedding algorithm that can have the best performance for all circuits under all simulation conditions. The BE insert position can help the convergence of CMOS inverter chain circuits. The diagonal position is also found to be much more efficient than others for practical feedback CMOS circuits. This embedding algorithm is also suitable for other PTA-like algorithms. The constant pure PTA method [16] with the embedding algorithm can also improve the simulation efficiency.

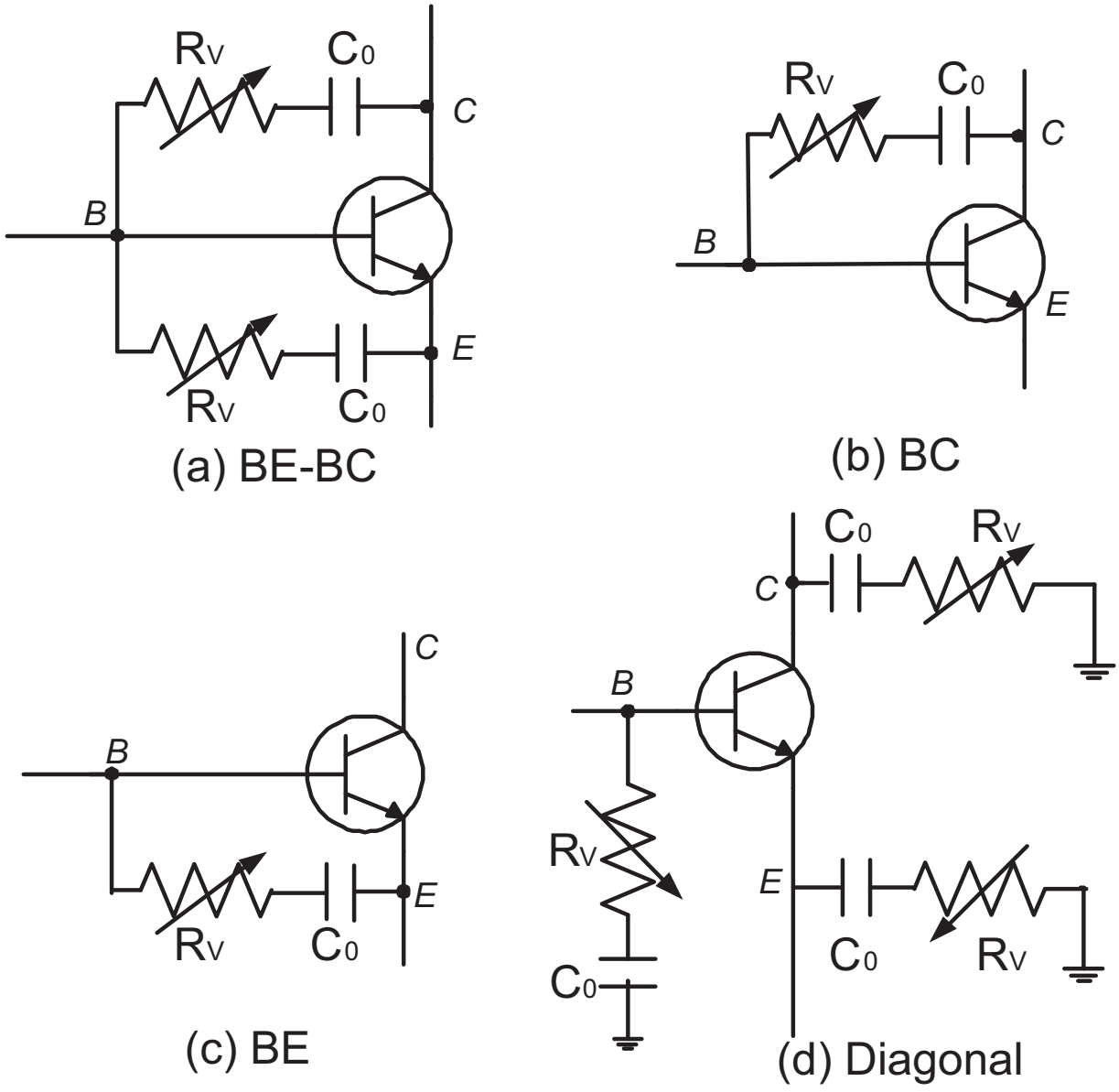

FIGURE 3.3: Embeding positions of pseudo elements.

3.4 Numerical Examples and Comparisons

The numerical examples are compared among the proposed algorithms with CEPTA method, the conventional CEPTA method in [27] (implementation algorithm 1 and the BE-BC embedding position are used), and the HSPICE to demonstrate the effectiveness in this section. Our proposed SPICE3 implementation method and the embedding algorithms for the CEPTA method are implemented on our SPICE simulator (Waseda SPICE) based on SPICE3. The source codes of the HSPICE are confidentiality and not published in any papers or manuscript due to its commercial property. Thus we cannot implement our proposed algorithms in the HSPICE with C source codes. Consider that all the commercial SPICE-like simulators, such as HSPICE, PSPICE and Spectre, share the same core SPICE3, we choose to implement our algorithms in the Waseda SPICE with C source codes based on SPICE3F5. Another way to verify the efficiency of proposed algorithm without modifying the C source codes is to modify the netlist of each circuit to add the pseudo elements as discussed in [27]. However, the netlist method is not practical particularly for large-scale circuits. It needs to modify every netlist of the test circuits, which is very inconvenient. Besides, the netlist method would enlarge the structure of Jacobian matrix, which decreased the efficiency a lot. In this paper, our researches are mainly considered from the practical viewpoint. Thus, the implementation with C source codes in the SPICE simulator is necessary. In this thesis, the conventional CEPTA method is also implemented with C source codes based on the SPICE3F5. Besides, though the HSPICE did not publish its algorithms to find the DC operating points, to compare with such practical used commercial SPICE-like simulator still shows great importance. Readers may wonder how about the performance of HSPICE, as the researches are mainly from the practical viewpoint. As a result, we prepare the comparison results of our proposed methods with the HSPICE too.

Firstly, we will verify the effectiveness of proposed implementation method. Then we will check the efficiency of proposed implementation and embedding algorithms together. We show here the comparison results for four types of analog transistor circuits. The simulation performance is compared by the convergence performance, the number of NR iterations (# of Iters) and the number of pseudo steps (# of Steps). The CPU time cannot be compared between the test results of the proposed method and the HSPICE, due to the reason that it depends on the computer performance and our computer performance is different form the server of HSPICE.

The simulator is running on Windows 7 operating system (CPU: 2.4GHz dual-core, Memory: 4GB, Compiler: Visual Studio 2008). In the pseudo transient analysis method, there are two kinds of convergence conditions. The first one is the pseudo transient convergence, which means when the condition satisfied, the transient analysis is done and the circuit is converged to the final solution. In the proposed method, we use the same convergence condition $\dot{x} = 0$ as [26]. In addition, in each transient analysis step, that is each time point, the Newton-Raphson method is used to find the solution. The convergence condition of the Newton-Raphson method at each pseudo transient step is the same as the default values of SPICE3 and HSPICE.

Firstly, a difficult circuit D1 [34] is used to verify the proposed 4 implementation algorithms. The "# of Iters" represents the number of total NR iterations while "# of Steps" means the number of pseudo steps needed for the final convergence. The simulation results are shown in Table 3.1. The conventional algorithm 1 fails to converge while the proposed algorithms 2,4,5 can easily converge. In this case, the proposed algorithm 2 shows better efficiency than others. According to a large number of tests, the proposed algorithm 2 is considered as the most efficient one, which is also recommended to be used at the first place. The other proposed

TABLE 3.1: Simulation performance comparison of D1 circuit.

Condition		**Results**		
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**	**# of Steps**
D1 circuit	Algorithm1 [1]	Not-converged	-	-
	Algorithm 2	Converged	169	39
	Algorithm 3	Not-converged	-	-
	Algorithm 4	Converged	184	43
	Algorithm 5	Converged	171	39

implementation algorithms can also be used as the fall back for various kinds of circuits. Thus, in the following tests, we consider the proposed algorithm2 as the implementation method to do the comparisons only.

Here we consider two circuits to confirm the effectiveness of the proposed implementation algorithm 2. The first circuit shown here is a six-stage limiting amplifier [24], which is a simple practical circuit . The circuit consists of six differential amplifiers directly coupled, and has a negative feedback, for biasing, with very high loop-gain. The circuit is used as an example for a typical type of practical circuits in the reference [24], including 19 bipolar and 15 resistors. Here, in order to compare the efficiency of implementation algorithms only, the conventional BE-BC embedding position of pseudo capacitors is used here.

As shown in the Table 3.2, the simulation results are presented. The number of steps (the number of NR iterations) for finding the DC operating points is 17 (39) for the proposed algorithm, and 30 (65) for the conventional algorithm, respectively. The number of NR iterations is reduced by 40% with the proposed new implementation algorithm. Thus the proposed SPICE3 implementation algorithm

TABLE 3.2: Simulation performance comparison of 6-stage limiting amplifier.

Condition		**Results**		
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**	**# of Steps**
Six-stage limiting amplifier	Algorithm1 [1]	Converged	65	30
	Algorithm2	Converged	39	17

TABLE 3.3: Simulation performance comparison of the benchmark circuit.

Condition		**Results**	
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**
Benchmark circuit	Implementation 1 [1]	Not converged	-
	Proposed algorithm 2	Converged	295

is much more efficient than the conventional one. The effectiveness of the proposed algorithm can be confirmed.

A benchmark circuit [33] is also used to verify the efficiency of our proposed SPICE3 implementation algorithm 2. As shown in Tables 3.2 and 3.3, obviously, the simulation convergence is improved and numbers of NR iterations are reduced, which means the simulation performance is improved with new implementation algorithm2. The proposed algorithm 2 can improve convergence performance and simulation efficiency compared with the algorithm 1.

TABLE 3.4: Simulation performance comparison of UA741 5-stage PFB OP AMP.

Condition		**Results**		
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**	**# of Steps**
UA 741 5-stage PFB OP AMP	Conventional CEPTA [1]	Not converged	-	-
	HSPICE	Not converged	-	-
	proposed algorithms(BC)	Converged	2007	366
	proposed algorithms(BE-BC)	Converged	1478	274
	proposed algorithms(diagonal)	Converged	1429	271

Secondly, consider a UA 741 5-stage PFB OP AMP circuit. The UA 741 operational amplifier with a positive feedback is 5-stage connected in cascade configuration in this circuit. The total number of elements is 188 including 115 BJT's, and the total number of nodes is 234. The open-loop gain of the circuit is very high. Due to the 5-stage connected, the circuit has multiple solutions. Part of this circuit is presented as difficult example in [1, 19]. Due to the positive feedback, the high loop gain and multiple solutions, the circuit is very difficult that the SPICE3 and even the HSPICE simulators can not easily converge to the solution.

Table 3.4 shows the simulation efficiency results of the conventional CEPTA method [26], the HSPICE and the proposed algorithms with different embedding positions. From the test results, we can see that the proposed algorithms with embedding positions of BC, BE-BC and the diagonal can find the DC operating point of the circuit, which can not be solved by the HSPICE simulator and the conventional CEPTA method. The HSPICE invokes different methods for solving non-convergence problems including the GMINDC ramping method, the source

stepping method, and the damped pseudo transient algorithm [37]. However, all these methods can not find the DC operating point for this circuit. Furthermore, by switching the embedding positions, we can achieve higher simulation efficiency for finding DC operating points. In this case, we found that the diagonal embedding position shows better efficiency than other positions. When we use the diagonal embedding position the number of steps is 271, the BE-BC position 274, and the BC position 366, respectively. Thus, the simulation performance of the proposed algorithms is much better than the conventional CEPTA method. And in this case, it is even much more effective than the HSPICE. Moreover, the effectiveness of the embedding algorithm is also confirmed.

Thirdly, we consider a 15-stage CMOS inverter-chain. The inverter chain circuits belong to a typical class of oscillation circuits, which are hard to converge with conventional PTA methods. However, in the practical LSI circuits design, this kind of circuits is often used as sub-circuit for some large-scale circuits. Therefore, to make this kind of inverter chain circuits converge with the PTA method shows great importance. The circuit is shown in the Fig.3.4. In [26] and [27], the 5-stage inverter chain circuits are considered as oscillation examples. The conventional pure PTA methods may fail to converge due to the oscillation problem caused by the insertion of pseudo elements, while the CEPTA can eliminate the oscillation well and make the 5-stage inverter chain converge. However, it is still easy to oscillate even with CEPTA method for the 15-stage CMOS inverter chain. Due to the 15-stage negative feedback, the loop gain of the circuit is very large. The Newton-Raphson method can not solve this circuit easily and the HSPICE simulator can only converge for 9-stage CMOS inverter chain.

The test results are shown in Table 3.5. Figs. 3.5-3.7 are the node voltage V_{out} waveforms of HSPICE, the conventional CEPTA method, and the proposed algorithm for the CMOS inverter chain circuit. Figure 3.6 shows the waveform of the

TABLE 3.5: Simulation performance comparison of 15-stage CMOS inverter chain.

Condition		**Results**		
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**	**# of Steps**
15-stage CMOS inverter chain	HSPICE	Not converged	-	-
	CEPTA [1]	Not converged	-	-
	proposed(BE)	Converged	50	17

node voltage by the conventional CEPTA method. The circuit can not converge with the conventional CEPTA method. We also compare the simulation results with the damped PTA method in the HSPICE. The solution curve with HSPICE is shown in Fig. 3.5. Even with the HSPICE, it oscillates and can not converge.

With the proposed algorithms, where the Base-Emitter position is used, the 15-CMOS inverter chain circuit can easily converge. The waveform of node voltage is shown in Fig. 3.7. It is obviously that, with the proposed new implementation algorithm and the Base-Emitter embedding position, the convergence performance for inverter chain circuits can be significantly improved compared with the conventional CEPTA method. Moreover, simulation performance is much better than the pseudo method in the HSPICE. In this inverter chain case, we found that the BE embedding position is much more effective than other positions.

Fourthly, two practical analog CMOS circuits in [36] are presented. One is an adder circuit, and another one is the intake system circuit with 1096 nodes, 1909 elements and 1516 MOSFETs. As we know, with different embedding positions, the simulation efficiency and convergence performance can be totally different. From our experience in applying our proposed algorithms to many other circuits,

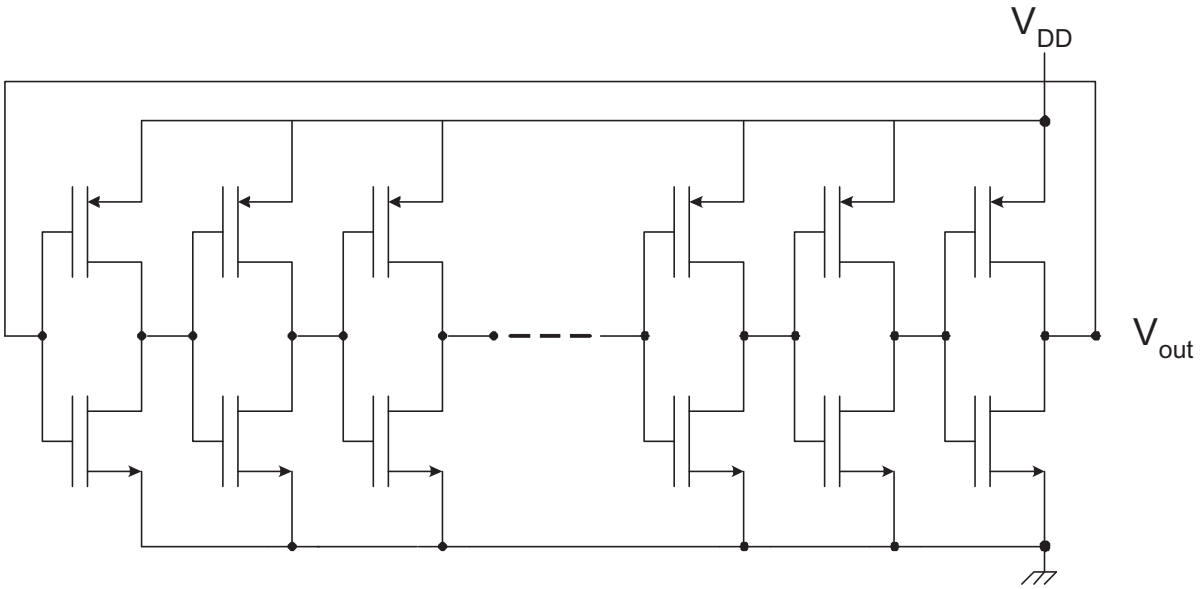

FIGURE 3.4: 15-stage MOS inverter chain circuit.

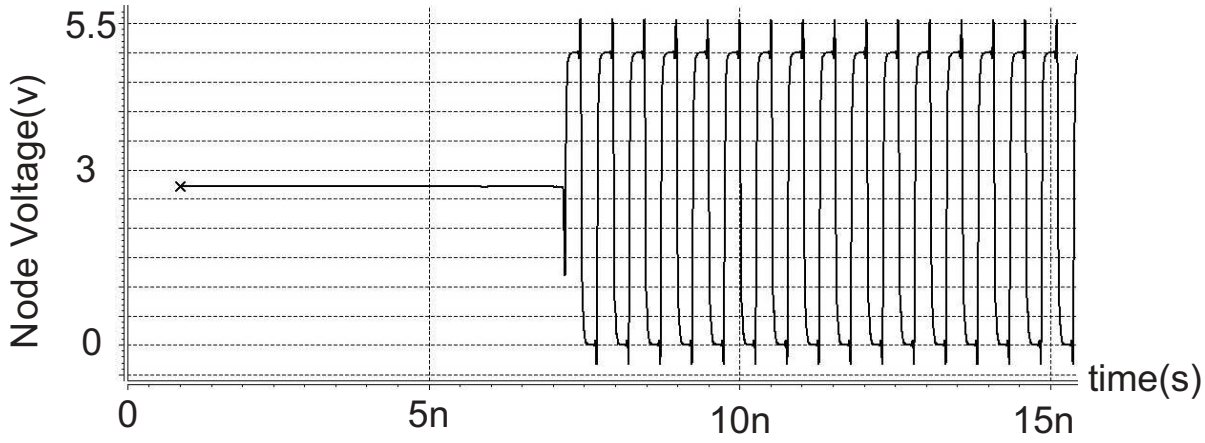

FIGURE 3.5: Node voltage waveform with HSPICE of 15-stage MOS inverter chain circuit.

we found that the diagonal embedding position is more effective than the other positions for CMOS circuits. Tables 3.6 and 3.7 show the simulation performance of conventional CEPTA and CEPTA with proposed algorithms, where the diagonal embedding position is used. From the test results, it is obviously that the

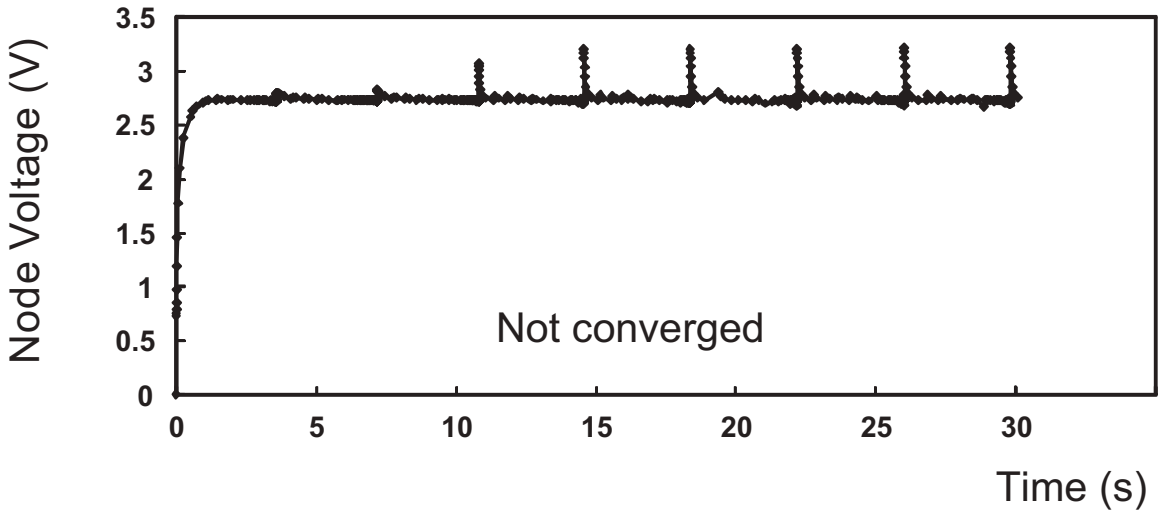

FIGURE 3.6: Node voltage waveform with conventional CEPTA [1] method of 15-stage MOS inverter chain circuit.

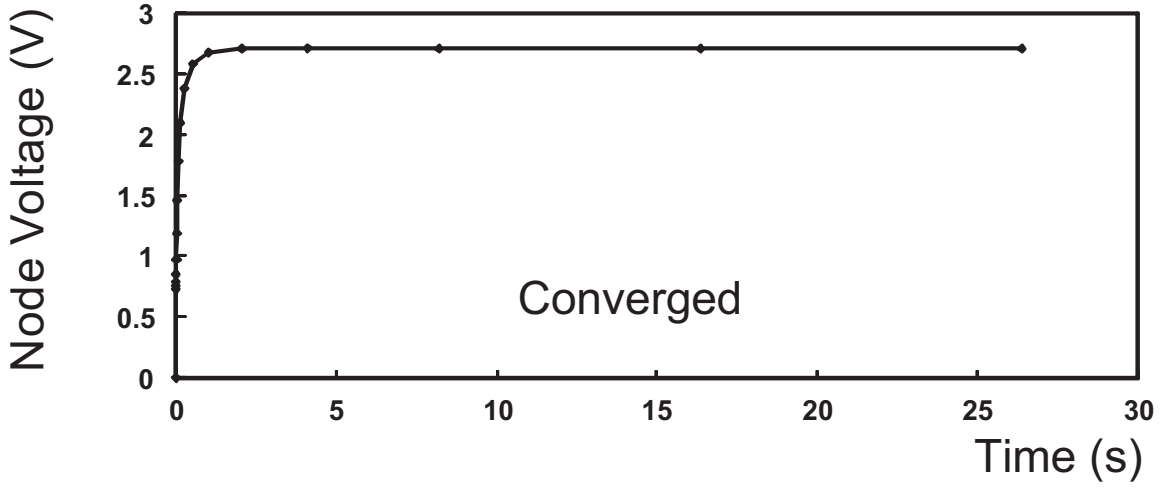

FIGURE 3.7: Node voltage waveform with proposed algorithms (BE insert position) of 15-stage MOS inverter chain circuit.

convergence performance is improved with the proposed algorithms. The CEPTA method with proposed algorithms can find the DC operating point for some large-scale circuits (MOSFETs $>$ 1000), which even can not be dealt by HSPICE

TABLE 3.6: Simulation performance comparison of analog adder.

Condition		**Results**	
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**
Analog adder	Conventional CEPTA [1]	Not converged	-
	CEPTA with the proposed algorithms (diagonal position)	Converged	242

TABLE 3.7: Simulation performance comparison of the intake system.

Condition		**Results**		
Circuit	**Algorithm**	**Convergence Performance**	**# of Iters**	**# of Steps**
Intake system	HSPICE	Not converged	-	-
	CEPTA [1]	Not converged	-	-
	proposed(BE)	Converged	6984	1226

simulators. As shown in Tables 3.6 and 3.7, the diagonal embedding position shows much better simulation results than the BE-BC position for such CMOS practical circuits. The conventional BE-BC position can't help the circuit converge, while the diagonal position can make the circuit easily converged with small iteration numbers. Thus, the proposed algorithms with the CEPTA method are much more efficient than the conventional CEPTA method.

Therefore, the simulation performance improvement of the proposed implementation and embedding algorithm with the CEPTA method are verified with the

presented circuits. In some cases, the simulation performance is even much better than the HSPICE.

3.5 Conclusions

In this work, an effective SPICE3 implementation algorithm and embedding algorithms for the CEPTA method are proposed. The proposed implementation method obtains the companion model by a different way, which has no limitation of step size. The convergence performance and simulation efficiency can be greatly improved with the proposed implementation algorithm (the number of total iterations is reduced by 40%) compared with the conventional CEPTA implementation method. The embedding algorithms provide 3 insert positions for the pseudo-capacitors to the transistors to improve the simulation efficiency for different types circuits. The Base-Emitter embedding position and diagonal position are found to be more efficient for the test circuits shown in this chapter. Combining the proposed implementation and embedding algorithms together can further improve the applicability of CEPTA method, especially for some large-scale circuits (the number of devices > 1000). And in some cases, the simulation performance is even much better than the HSPICE simulators. The embedding algorithm can be extended to other PTA-like algorithms such as the constant pure PTA method. Numerical examples demonstrate the efficiency of the proposed algorithms.

Chapter 4

Ramping Algorithm and Restart Algorithm in SPICE3 Implementation for DPTA Method

[Related papers [A1],[B1],[B2],[C1]]

4.1 Introduction

In modern commercial SPICE-like simulators, the Newton-Raphson (NR) method is employed to solve the DC operating points for the nonlinear circuits in the DC analysis, which may fail to converge unless the initial guess is close enough to the solution [1, 3]. As running DC analysis is one of the most basic and sometimes the most difficult tasks during the circuit simulation, techniques to deal with the NR not-converged problem show great importance [1, 3, 16]. Therefore, some continuation methods are studied for many years like Gmin stepping, source stepping, homotopy method and PTA methods and so on [1, 3, 16–20, 22, 26, 27, 29, 30]. In some commercial SPICE-like simulators such as HSPICE, the PTA method is the fall-back approach when direct DC analysis or DC sweep, using the source stepping and Gmin stepping methods, fail to converge [1, 3, 19]. Among all these methods, the PTA method is considered as one of the most "heavy duty" methods, whose idea is that firstly modify the network by inserting some certain pseudo elements, and then carry out a transient analysis with specified initial values until a DC steady state is reached [16, 26].

The former researches of the PTA method could be classified through insertion pseudo elements, including the constant pure element PTA, time-varying pure element PTA and the compound elements PTA method (CEPTA) [16–18, 26]. Though the CEPTA method is effective to overcome oscillation occurred in the pure element PTA methods, it may have the problem of waveform discontinuous and fails to converge. After that, a k-step damped PTA (DPTA) method, in which the damping effect is artificially increased, is researched from the numerical integration algorithm viewpoint [30]. Compared with CEPTA, the DPTA uses pure capacitor and inductor as pseudo-elements, which has no risk on that the pseudo circuit is discontinuous [30]. Besides, due to the artificially enlarged damping effect from the damped differential formula, oscillation circuits can be solved with

high efficiency. However, for both CEPTA and DPTA methods, the insertion of pseudo-capacitors and inductors may lead to time-consuming problem especially for some very large-scale circuits, since a large number of non-zero elements are inserted into the circuit Jacobian matrix. Moreover, many experiment tests demonstrate that the PTA techniques may get stuck in an infinite loop and fail to converge due to the unsuitable pseudo-control parameter values.

In this work, we propose a ramping algorithm with two ramping functions, which can avoid the oscillation problem caused by the inductors and make the circuit converge to the solution faster. It holds the property that no additional matrix elements are created at the voltage source diagonal position in the Jacobian matrix, thus time-consuming problem in large-scale circuits can be improved. Combing the ramping algorithm and DPTA together, simulation efficiency can be improved while the oscillation is well eliminated. Moreover, a restart algorithm is also proposed in the SPICE3 implementation to help the convergence when the circuit stuck in an infinite loop and is difficult to converge.

4.2 Challenges in the DPTA Method

Though the DPTA method has been proved to be efficient to deal with oscillation circuits by the artificially enlarged damping effect in the numeral integration algorithm and avoid "time step too small" problems, the simulation efficiency is still need to be improved, especially the time-consuming problem. The pseudo-elements in the damped PTA method are composed of pure pseudo-capacitors and inductors. The new formed pseudo-circuit may oscillate during the analysis due to the inserted pseudo elements [27], which may decrease the efficiency of the DPTA method. Moreover, during the SPICE3 implementation, the inserted pseudo-elements are added in the circuit Jacobian matrix so that the number of non-zero elements in the circuit Jacobian matrix are increased [1]. The non-zero elements may cause a serious fill-in problem, which destroys the sparsity of the Jacobian and may leads to a time-consuming problem especially for very large-scale circuits. Besides, many experiment tests demonstrate that the PTA techniques may stuck in an infinite loop and fail to converge due to the unsuitable pseudo-control parameter values. We will show the details in the following section.

Therefore, we have to challenge these problems of the DPTA method:

1. Improve the time-consuming problem and simulation efficiency, which means smaller number of NR iterations, less CPU time and better convergence performance.

2. Avoid the oscillation caused by insertion of pure capacitors and inductors together.

3. Recognize and deal with the infinite loop situation during the simulation. Improve the convergence in the SPICE3 implementation.

4.3 Proposed Methods

In this section, a ramping algorithm is proposed for the pseudo-transient analysis method. The ramping techniques are widely used in commercial simulators [3, 18]. In this work, a ramping technique is introduced for independent voltage source and combined with the damped pseudo transient analysis method together. Two ramping functions are proposed and compared. Moreover, a restart algorithm is also proposed in the SPICE3 implementation to help the convergence when the circuit gets stuck in an infinite loop and is difficult to converge.

4.3.1 Ramping Algorithm with DPTA

In this chapter, we combine the ramping algorithm, which is introduced for independent voltage source, and damped pseudo-transient analysis method together to achieve high efficiency including small CPU time and avoid the oscillation problem. F l PTA methods, the fixed value pseudo-inductors are used to get the ramping waveforms for the independent voltage sources. However, these waveforms depend on the circuits too. The ramping waveform is determined by the inductor value and circuit parameters together. In many cases, we cannot get the ideal ramping waveforms for all independent voltage sources. And for some complex circuits, it is not easy to choose a suitable value for the pseudo-inductors. Therefore, in this work, we use the effect of ramped voltage to replace the effect of pseudo-inductor. In the proposed method, independent of circuit parameters, the ramping time and the ramping waveform are always constant. Thus we can easily get the ideal ramping waveforms for all independent voltage waveforms. Moreover, the ramping time is much easier to be adapted. The PTA method mainly includes two major parts: the pseudo-elements inserted into the circuit and the numerical

integration method used during the transient analysis. In this combination algorithm, pure pseudo-elements are used. Only capacitors are inserted to the circuit as the pseudo-elements. The task of finding the DC solutions is to solve a set of the equations described from the circuit. The proposed combination pseudo algorithm can be described as the following manners.

1. Insert the pure constant pseudo-capacitors in parallel with the independent current sources. Insert the pure pseudo-capacitors into the bipolar and MOS transistors in the diagonal position, which means insert the capacitors to the transistors between each node and ground.

2. Meanwhile, ramp up the supply voltage from zero to their real value over time according to the certain ramping function shown in Eq. (4.1) without inserting any pseudo-inductors. Two ramping functions are proposed in this chapter and will be shown later.

3. After the pseudo-elements insertion, a new pseudo circuit is formed and a new mathematical expression can be described as shown in Eq. (2.15), where **D** is a matrix used to represent the pseudo capacitors. Applying the damped numerical integration algorithm shown in Eq. (2.16) to the differential part in the Eq. (2.15) to solve the system of the nonlinear algebraic equations. The circuit finally achieves the steady state.

For the conventional PTA methods, the fixed value pseudo-inductors are used to get the ramping waveforms for the independent voltage sources. In this proposed method, we use the effect of ramped voltage to replace the effect of pseudo-inductor so that the ramping time and the ramping waveform are always constant and independent of circuit parameters. No pseudo-inductors are inserted to independent voltage sources in the ramping algorithm. As a result, no pseudo-inductors are

inserted in the pseudo-transient when the ramping algorithm works, thus the oscillation that caused by inductors can be avoided. The independent voltage source remains kept its original pure voltage source branch. Also no additional element is created at the voltage source diagonal position in the circuit Jacobian matrix [1], thus the fill-in phenomenon in large-scale circuit caused by additional matrix elements can be reduced. Therefore, the time-consuming problem can be greatly improved in our proposed algorithm. Besides, by combing the ramping algorithm and DPTA algorithm together, the time-consuming problem and oscillation problem can be eliminated at the same time compared with the conventional DPTA. Moreover, compared with the CEPTA case, the combination algorithm uses pure pseudo-elements, which doesn't limits to the assumption that the waveform is continuous.

The source value of the independent voltage is ramped according to the ramping function, which can be described as Eq. (4.1).

$$V(t) = f(t) \cdot V_{src}, \tag{4.1}$$

where $V(t)$ is the ramping source value, $f(t)$ is the ramping factor, V_{src} is the original source value of independent voltage, and t is the pseudo-time. As shown in the ramping functions waveform in Figs. 4.1 and 4.2, the ramping function continuously ramped from zero to its original source value before some certain pseudo time τ_{ramp}, and after reach τ_{ramp}, the ramping source value gets the original source value and keeps it. From the simulation efficiency viewpoint, we propose two different functions as the ramping factor $f(t)$, named as $f_s(t)$ and $f_c(t)$, respectively. The first one is the sinusoidal (sine) type function described in Eq. (4.2) and shown in Fig. 4.1.

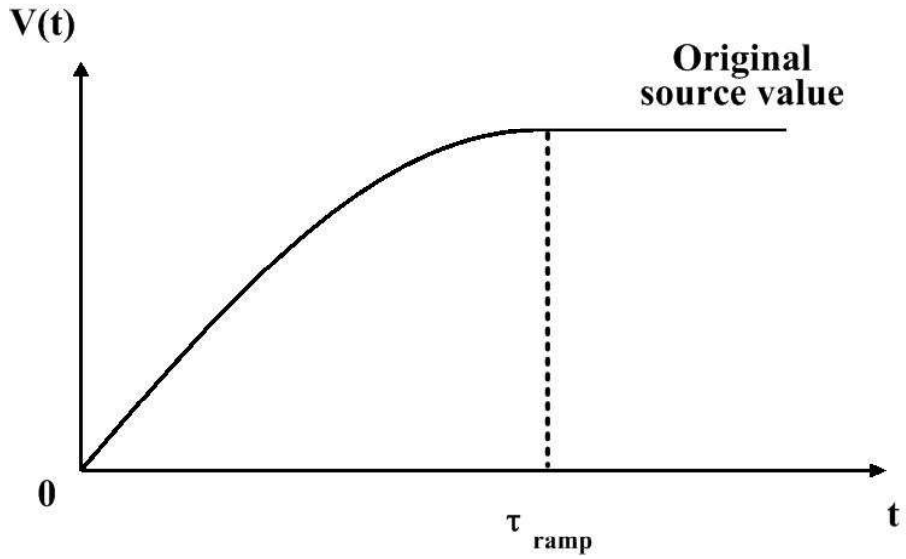

FIGURE 4.1: The waveform of sinusoidal type ramping function.

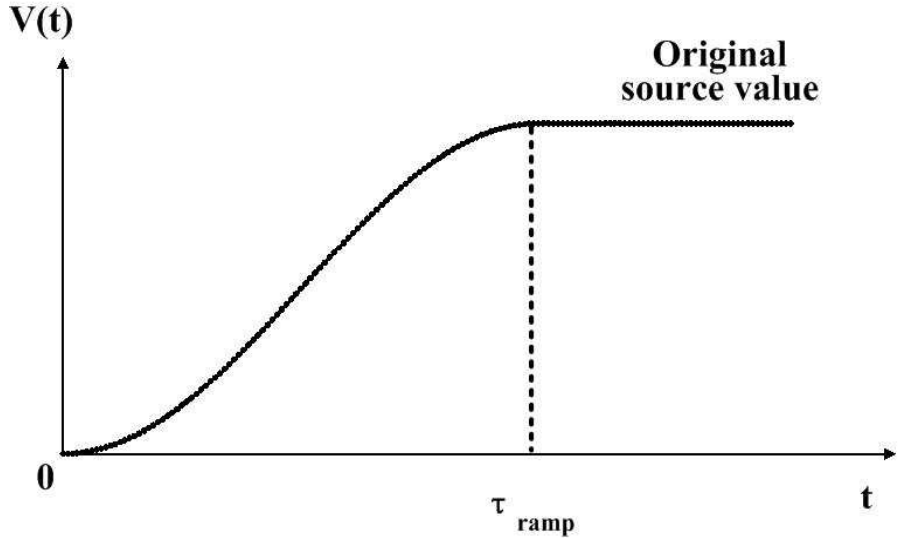

FIGURE 4.2: The waveform of cosine type ramping function.

$$f_s(t) = \begin{cases} \sin(\frac{\pi \cdot t}{2\tau_{ramp}}) & : \quad 0 \leqslant t \leqslant \tau_{ramp} \\ 1 & : \quad \tau_{ramp} < t \end{cases} , \tag{4.2}$$

TABLE 4.1: Property comparisons of $0 \leqslant t \leqslant \tau_{ramp}$ part functions for sinusoidal and cosine type ramping factors. (τ here is τ_{ramp})

$f(t)$	$f'(t)$	$f(0)$	$f(\tau_{ramp})$	$f'(0)$	$f'(\tau_{ramp})$	f'_{max}
$f_s(t)$	$\frac{\pi}{2\tau} cos \frac{\pi \cdot t}{2\tau}$	0	1	$\frac{\pi}{2\tau}$	0	$\frac{\pi}{2\tau}$
$f_c(t)$	$\frac{\pi}{2\tau} sin \frac{\pi \cdot t}{\tau}$	0	1	0	0	$\frac{\pi}{2\tau}$

where τ_{ramp} is the user specified ramping time. The second one is cosine (cos) type function as shown in Fig. 4.2, which can be described as following Eq. (4.3),

$$f_c(t) = \begin{cases} 0.5 * (1 - \cos(\frac{\pi \cdot t}{\tau_{ramp}})) & : \quad 0 \leqslant t \leqslant \tau_{ramp} \\ 1 & : \quad \tau_{ramp} < t \end{cases} . \tag{4.3}$$

Both of the ramping factor functions continuously ramped up from the initial value zero to 1 before the pseudo time τ_{ramp}, and after that, the value keeps 1. Both two functions are piecewise functions. Consider the properties of two functions at $0 \leqslant t \leqslant \tau_{ramp}$ part. Comparisons are shown in the Table 4.1. From the Table 4.1, we can see clearly that both two ramping factor functions satisfy the requirement needed for the ramping, $f(0) = 0.0$ and $f(\tau_{ramp}) = 1.0$. Moreover, the two functions have zero derivative value at $t = \tau_{ramp}$, which is preferable for smooth ramping. The maximum derivative values of the two functions are the same.

The difference between two functions are as follows:

(1) The sine type ramping factor function has non-zero derivative value and the derivative is maximum at $t = 0$.

(2) The derivative of the cos type ramping factor function is zero at both $t = 0$ and $t = \tau_{ramp}$. The maximum value of the derivative is at $t = \tau_{ramp}/2$.

From this comparison, the cos type ramping function is smoother than the sine type function and supposed to be more effective for some kinds of circuits. The source values of voltage increase gradually to the original value and are not influenced by the circuit operation. The voltage waveform can be smooth. Different ramping functions show different effectiveness. The proposed two ramping functions can help improve the simulation efficiency greatly.

4.3.2 Restart Method

From a large number of tests, we found that for some complex circuits, the demand of pseudo-control parameter values is very strict for their convergence, such as the intake system circuit from [36]. Though the conventional DPTA method can help the intake system circuit converge and have a good efficiency, this circuit is very sensitive to the pseudo-control parameter values during the pseudo-transient analysis. Only if the pseudo-capacitor value and the maximum step size value are carefully chosen, the circuit can find the DC operating point easily. Otherwise, the circuit may fail to converge and oscillate as shown in Fig. 4.3. When the pseudo-control parameters are not suitable, such phenomenon also happens with some multiple solution circuits and some circuits whose waveform is discontinuous during their simulation. Such oscillation occurs along with the rapidly cyclical change of time step size as shown in Fig. 4.4.

In this section, we propose a restart method in SPICE3 implementation for the DPTA method to help converge when such oscillation and non-convergence occurs. The proposed algorithm includes two parts: recognition part and restart part. The

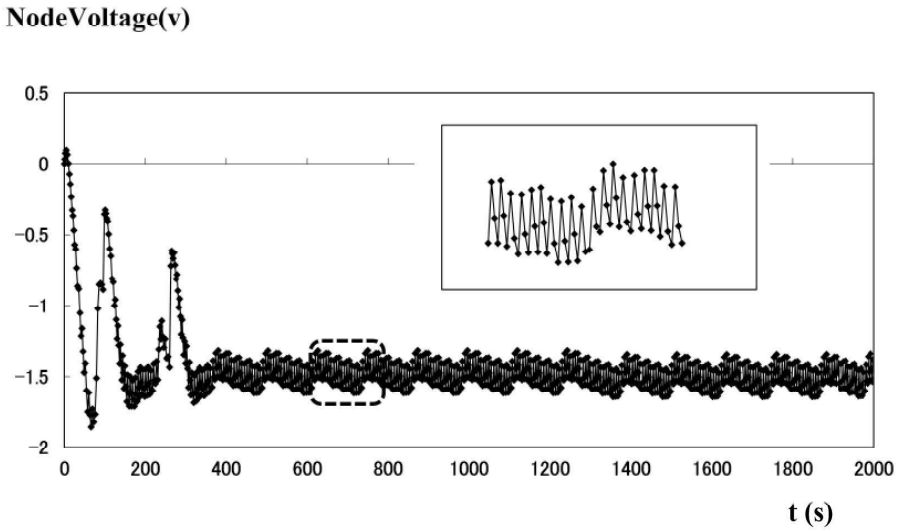

FIGURE 4.3: One node voltage waveform of intake system by using DPTA method when the pseudo-control parameter values are not suitable chosen.

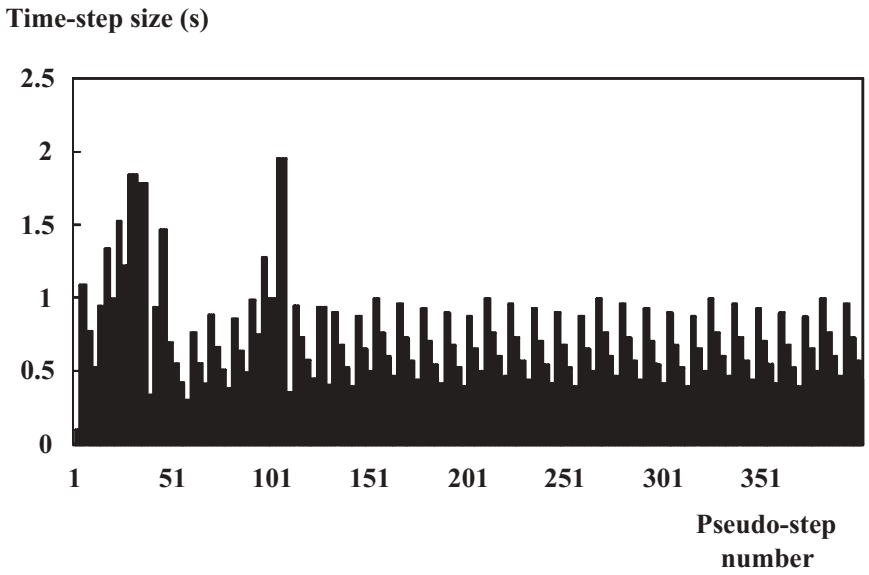

FIGURE 4.4: The time-step size of intake system by using DPTA method.

recognition part determines when to restart, while the restart part determines how to restart. The procedure of the proposed method can be concluded as following:

Step 1: once the NR method fails to converge, we begin to count the number of NR non-convergence in the next M pseudo-steps as shown in Fig. 4.5 ;

Step 2: if the proportion of non-convergence, defined as frequency in Eq. (4.4), is more than $a\%$ during the fixed pseudo-steps M and it is consecutive b times as Fig. 4.5 shown, we go to Step 3. Otherwise, we go back to Step 1;

Step 3: calculate the kurtosis defined by Eq. (4.5) with the set
$\mathbf{H} = (h_n, h_{n+1}, h_{n+2}, ..., h_{n+bM-1})$,
which is the deviation of step size h from the mean value. The set **H** is the time-step values decided by the Step 1 and Step 2;

Step 4: if the kurtosis is positive, then the restart function is active and go to Restart 1. If the kurtosis is negative, go to Step 1;

Restart 1: rollback to the step $n-1$;

Restart 2: restart the simulation with the constant time-step size, h_{n-1};

Restart 3: after c pseudo-steps, the variable time-step size is used again.

During the simulation, in each transient analysis step, that is each time point, the Newton-Raphson method is used to find the solution. The frequency of non-convergence means how many times does the NR fail to converge during a fixed number of pseudo-steps M as shown in Eq. (4.4). In the SPICE3 implementation, if the number of NR iterations is larger than 11 at that time point, we judge that the NR fails to converge. In the SPICE3 implementation, we set a counter to record how many times the NR fails to converge. If the NR method fails to converge, we make the counter plus 1.

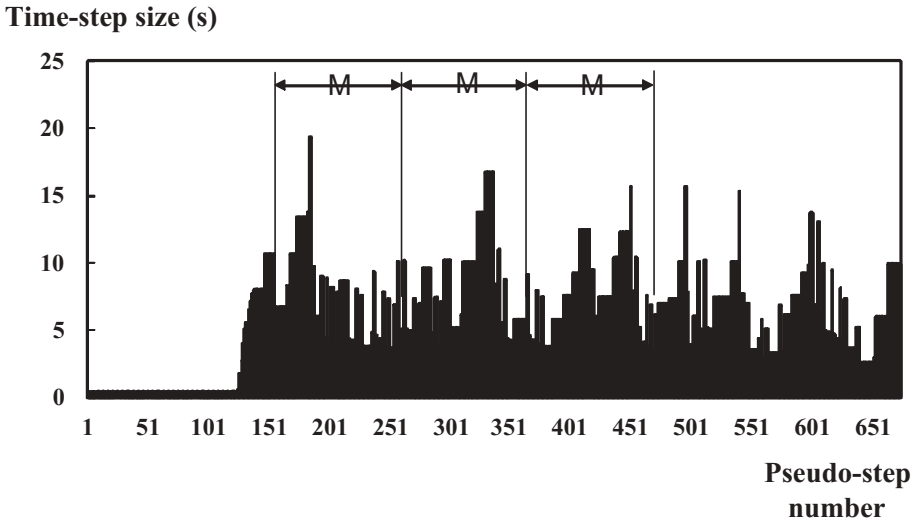

FIGURE 4.5: The recognition method for restart algorithm.

$$Frequency = \frac{\#\ of\ NR\ nonconvergence}{\#\ of\ total\ pseudo\ steps}. \tag{4.4}$$

$$kurtosis = \frac{bM(bM+1)}{(bM-1)(bM-2)(bM-3)s^4} \sum_{i=n}^{n+bM-1} (h_i - \bar{h})^4 - \frac{3(bM-1)^2}{(bM-2)(bM-3)}. \tag{4.5}$$

The kurtosis is any measure of the "peakedness" of the probability distribution of a real-valued random variable [31, 32]. Here, kurtosis is measured of time step data set **H** to verify whether the data are peaked or flat relative to a normal distribution. In the Eq. (4.5), s is the standard deviation, h_i is the i^{th} value, and $\bar{h}$ is the sample mean [32]. For the Eq. (4.5), the standard normal distribution has a kurtosis of zero, while positive kurtosis indicates a "peaked" distribution and

negative kurtosis indicates a "flat" distribution [32]. In the Eq. (4.5), $kurtosis > 0$ means that there are many data in the bM pseudo-steps far away from average value.

The proposed restart method uses a very simple recognition method to analyze the periodical change of time-step size rather than uses some complex pattern recognition algorithms to analyze all solution curves. From many experiments, the values of parameters M, a, b and c are empirically determined as 100, 20, 3 and 10. The empirically determined parameters did not depend on the target circuit in our simulation test examples. The same parameter values were applied to all the test circuits in this thesis. The restart method is proposed to recognize and overcome the phenomenon shown in Fig. 4.5. Such phenomenon may happen with some multiple DC solution circuits and occurs along with the rapidly cyclical change of time-step size. Thus the parameter values in the restart method are determined to recognize and overcome the cyclical change of time-step size and such phenomenon. The parameter values are empirically determined by the experiment of many test circuits so that such phenomenon can be efficiently recognized. By the experiment of many test circuits, we can always see this similar pattern when such phenomenon occurred. The pattern didn't change very much. With the same empirically determined parameter values, not only the target circuit shown in the thesis, but also other circuits can be efficiently recognized. We did not mean that these empirically determined parameters are the best choices for all circuits. Even if in some cases, these parameters values lead to the misjudgment of such phenomenon, the only loss is to use a constant step size value in several steps or get the recognition after several steps, which does not influence the convergence performance. It is unnecessary to recognize such phenomenon when it firstly appears. For some target circuits, such phenomenon may repeat many times until the restart method works. From many test results, considering the tradeoff between efficiency and effectiveness of recognition, the empirically determined parameters

have a good performance to efficiently recognize and overcome such phenomenon. In the restart function, a constant step size h_{n-1} is used, which brings about a stable damping effect to help the convergence.

4.4 Numerical Examples

In this section, several numerical examples are shown to demonstrate the effectiveness of the proposed algorithms. In order to verify the effectiveness, the proposed algorithms are implemented on the WASEDA SPICE (WSPICE) based on SPICE3F5, running on Windows 7 operating system (CPU: 2.4GHz dual-core, Memory: 4GB, Compiler: Visual Studio 2008) and applied to practical large-scale circuits.

Firstly, two circuits are shown to verify the efficiency of the proposed ramping algorithm. In this thesis, we also implement a linear ramping function as a conventional method based on SPICE3F5, where the voltage ramps up to the original value with linear ramping factor function $f_{con}(t) = t/\tau_{ramp}$ before time point τ_{ramp} and gets the original source value after time point τ_{ramp}. The linear function method is considered as a conventional method [19]. However, there is no publication about the test results of linear ramping function method. The problem of the linear ramping function is that it is not differential continuous at time points 0 and τ_{ramp}.

The comparisons are among the conventional DPTA method, linear ramping DPTA method and the proposed ramping DPTA methods with two ramping functions. For all these algorithms, the pseudo elements are inserted to the transistors between each node and ground, which means the diagonal embedding position [29]. The 3-step damped algorithm is used as the numerical integration method [30]. We consider the following indexes to verify the efficiency: convergence, CPU

TABLE 4.2: Simulation performance comparison of UA741 10-stage PFB OP AMP circuit.

Condition	**Results**				
Algorithm	**# of Elements**	**# of Fill-ins**	**# of Iters**	**# of Steps**	**CPU time (s)**
Conventional[30]	3468	696	4301	1317	3.713
Linear	3187	418	4302	1292	3.323
Sine	3187	418	3933	1216	2.716
Cosine	3187	418	3928	1214	2.668

time, number of the NR iterations (# of iters), number of non-zero elements in the Jacobian matrix (# of elements) and number of fill-ins (# of fill-ins).

The first circuit in this group is the UA741 10-stage PFB OP AMP circuit. Test results are shown in Table 4.2. The UA 741 operating amplifier with a positive feedback is 10-stage connected in cascade configuration in this circuit. Due to the positive feedback, the high loop gain and multiple solutions, the circuit is very difficult that the SPICE3 can't easily converge to the solution. Though the total number of NR iterations of linear ramping DPTA algorithm is almost similar with conventional DPTA algorithm, the number of steps and CPU time are decreased since the number of non-zero elements and fill-ins are decreased. Compared with the conventional DPTA and linear ramping DPTA methods, the two proposed ramping DPTA methods have smaller number of NR iterations and less CPU time since the number of steps are decreased. Compared with the conventional DPTA method [30], the number of fill-ins is reduced by 40%. The number of total iterations is reduced by 8.56% for sine function and 8.67% for cosine function, and the CPU time is reduced by 26.85% and 28.14%.

TABLE 4.3: Simulation performance comparison of bias circuit.

Condition	**Results**				
Algorithm	**# of Elements**	**# of Fill-ins**	**# of Iters**	**# of Steps**	**CPU time (s)**
Conventional [30]	337	94	755	147	0.141
Linear	275	36	301	58	0.089
Sine	275	36	253	52	0.046
Cosine	275	36	271	54	0.062

The bias circuit is also tested in this group, which is a benchmark circuit in [33]. It is a simple circuit with 4 voltage sources. The test results are shown in Table 4.3. From the simulation results of these two test example circuits shown in Tables 4.2 and 4.3, it is clear that the proposed ramping PTA method is more efficient than the conventional DPTA method from [30]. Besides, we can see that the number of fill-ins and non-zero elements of ramping algorithms are greatly decreased compared with the conventional DPTA method, due to that no pseudo-inductors are inserted to the independent voltage sources in the proposed algorithms. The CPU time efficiency is also much improved by the proposed ramping methods. The test results of the linear ramping PTA method is also shown in the table. The efficiency of proposed ramping functions is better than the linear one. In the bias circuit case, the number of fill-ins for proposed method is reduced by 61.7% compared with the conventional DPTA method, so that the number of total iterations can be reduced by 66.49% for sine function and 64.10% for cosine function, and the CPU time can be reduced by 70.2% and 56.03%. The effectiveness of the proposed ramping DPTA algorithm is confirmed.

Secondly, we verify the effectiveness of the proposed restart method. First test circuit for this group is the automobile intake system in [36] which has 1096 nodes,

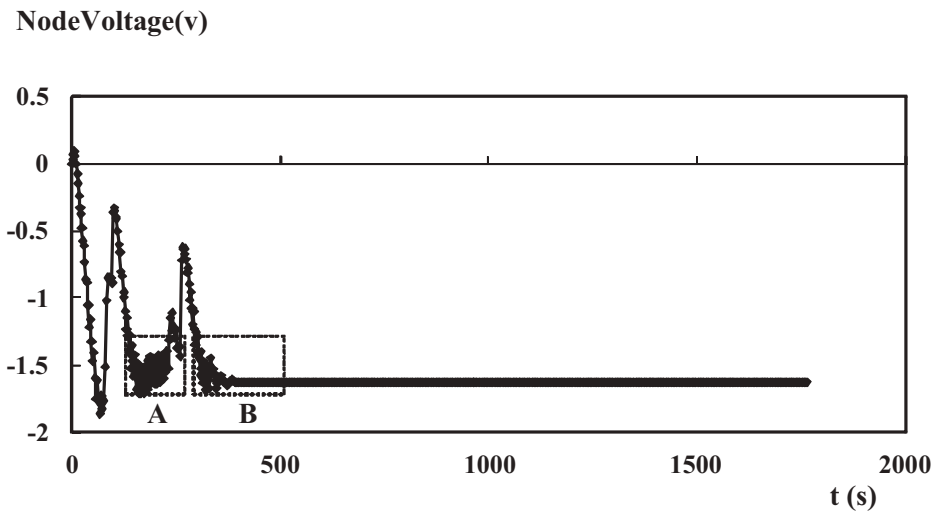

FIGURE 4.6: The waveform result of a node voltage in the intake system circuit by using the proposed restart method.

1909 elements and 1516 MOSFETs. As mentioned before, when the pseudo-control parameters are not suitable, this circuit may difficult to converge as shown in Fig. 4.3. Therefore, we use this circuit as an example to demonstrate that the proposed restart method can recognize and solve such problem. The node voltage waveform solved by the proposed restart method is shown in Fig. 4.6. In Fig. 4.6, we can see that the restart method is active in region B and the simulation is out of the infinity loop. Also note that in region A, the restart method is not active since the recognition criteria is not satisfied. With the proposed restart method, the circuit finally gets the steady state.

The second circuit for this group is a jge circuit in [33], including 348 CMOS transistors. When the DPTA method is used to solve the circuit, the circuit fails to converge. The node voltage waveform is shown in Fig. 4.7, while the (a) is waveform in the searching phase and (b) is the waveform in the converging phase. In the converging phase, the numerical solution feels the attraction of the steady state and the step size becomes very large to improve the convergence rate. However, the oscillation with periodic change of step size occurred and finally

fails to converge. The step size are shown in the Fig. 4.8. With the proposed restart method, the periodic change of step size in the converging phase as Fig. 4.8 (b) shown is recognized with the non-convergence frequency larger than 20% and positive kurtosis value. And with the restart method, the circuit is out of the infinity loop and finally converged as Fig. 4.9 shown. Also note that in searching phase, the restart method is not active since the recognition criteria is not satisfied as shown in Fig. 4.8 (a).

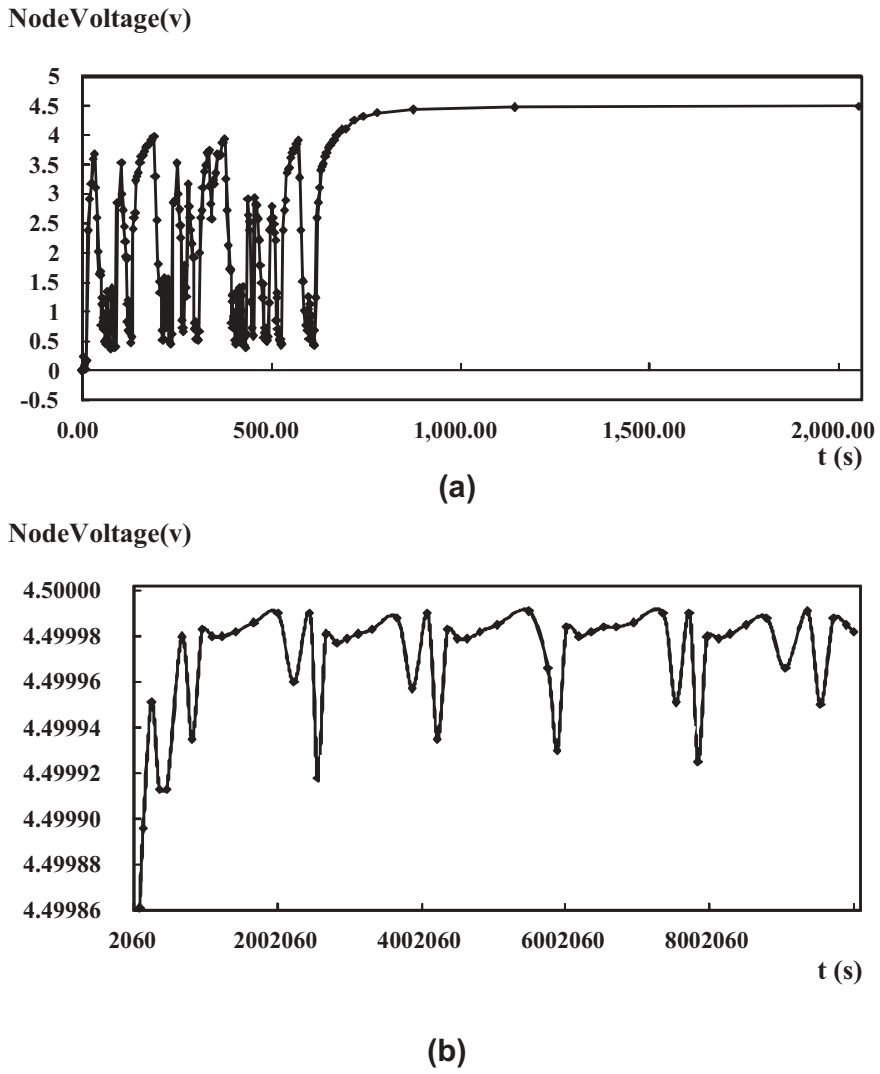

FIGURE 4.7: The node voltage waveform of jge circuit by using the DPTA method. (a) The waveform of searching phase. (b) The waveform of converging phase. The circuit is not converged.

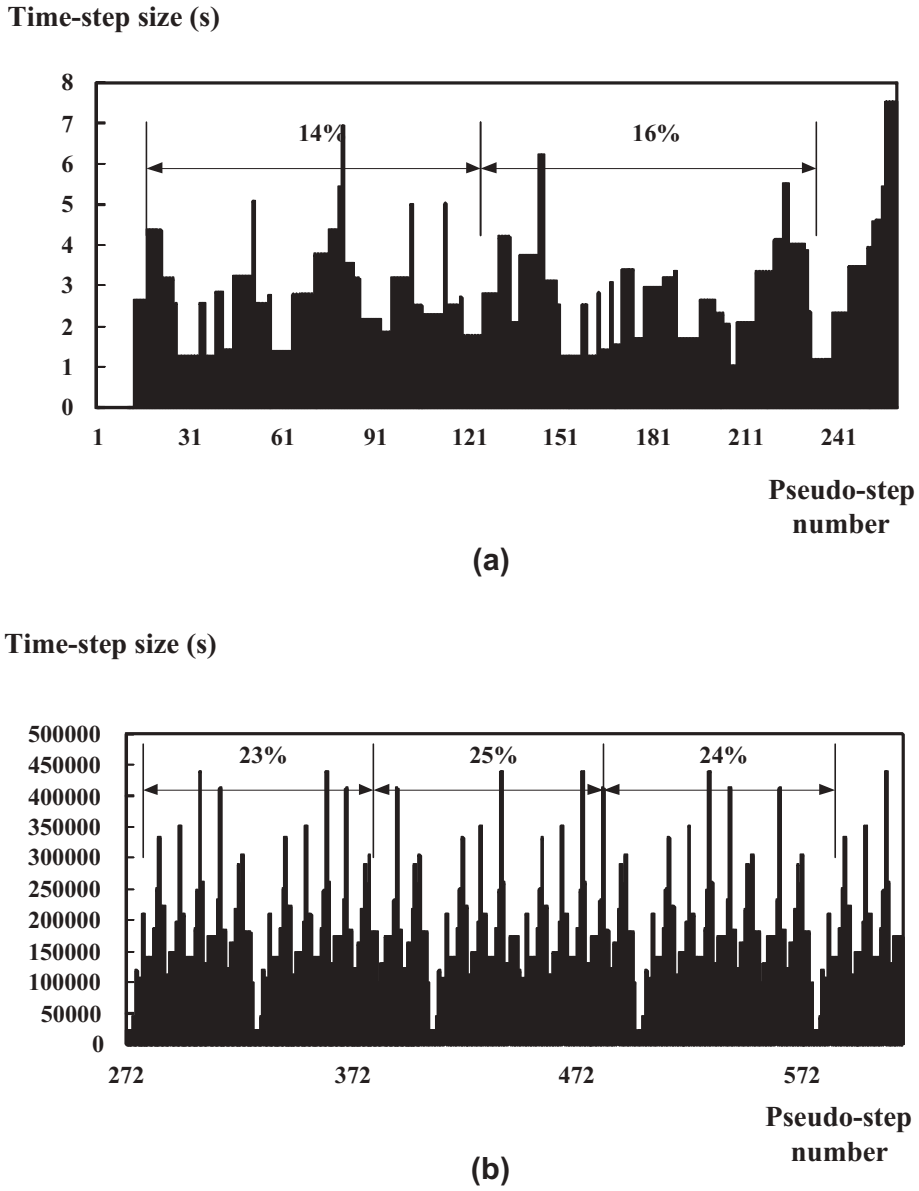

FIGURE 4.8: The time-step size of jge circuit by using the proposed restart method. (a) The time-step size of searching phase. (b) The time-step size of converging phase when stuck into infinity loop.

FIGURE 4.9: The node waveform of jge circuit by using the proposed restart method at the converging phase. The circuit converged.

4.5 conclusions

In this work, a ramping pseudo transient analysis method is proposed with two ramping functions. The value of independent voltage sources ramped up over time while the pseudo capacitors are inserted into the independent current source and transistors. The properties of the proposed ramping functions are analyzed. The proposed method holds the property that does not increase the number of non-zero elements in the diagonal positions of the Jacobian matrix, by not inserting the pseudo inductor into the circuit. Computing time decreasing and simulation efficiency improvement can be obtained compared with conventional DPTA methods. The proposed ramping algorithm reduces the number of non-zero elements of the Jacobian, and the number of fill-ins is reduced by 40%∼60%. So that the number of total iterations can be reduced by 8.67%∼66.5%, and the CPU time can be reduced by 28.14%∼70.2%. Besides, some oscillation problem caused by pseudo-inductor can also be avoided. Moreover, we combine the ramping algorithm with the damped pseudo-transient analysis method together to eliminate the oscillation and time-consuming problem at the same time. Thus the applicability of PTA method can further expended. Besides, a restart algorithm in the SPICE3 implementation is also proposed to help the circuit converge when the simulation stuck into an infinity loop. Numerical examples demonstrate the effectiveness of the proposed algorithms. Simulation efficiency can be greatly improved, and the algorithm can be applied even for some large-scale circuits.

Chapter 5

Conclusions

5.1 Conclusions

The studies on circuit simulation include three part. The first one is to model the circuit elements mathematically. The second one is the formulation of the circuit/network equations. The third one is the technologies to solve these equations. This work is mainly focus on formulating and solving the system equations. As compared to other continuation method like Gmin stepping and source stepping, PTA methods are regarded as a much more effective and practical option to solve the nonlinear circuit equations.

In this work, an effective SPICE3 implementation algorithm and an embedding algorithm for the CEPTA method are proposed. The proposed implementation method obtains the companion model by a different way, which has no limitation of step size. The convergence performance and simulation efficiency can be greatly improved with the proposed algorithms even for some large-scale practical circuits, compared with the conventional CEPTA method. And in some cases, the simulation performance is even much better than the HSPICE simulators. Combining the proposed implementation and embedding algorithms together can further improve the applicability of CEPTA method, especially for some large-scale circuits. The Base-Emitter embedding position and diagonal position are found to be more efficient for the test circuits shown in this paper. The embedding algorithm can be extended to other PTA-like algorithms such as the constant pure PTA method. Numerical examples demonstrate the efficiency of the proposed algorithms.

In this work, a ramping pseudo transient analysis method is proposed with two ramping functions. The value of independent voltage sources ramped up over time while the pseudo capacitors are inserted into the independent current source and transistors. The properties of the proposed ramping functions are analyzed. The

proposed method holds the property that does not increase the number of non-zero elements in the diagonal positions of the Jacobian matrix, by not inserting the pseudo inductor into the circuit. Computing time decreasing and simulation efficiency improvement can be obtained compared with conventional DPTA methods. Besides, some oscillation problem caused by pseudo-inductor can also be avoided. Moreover, we combine the ramping algorithm with the damped pseudo-transient analysis method together to eliminate the oscillation and time-consuming problem at the same time. Thus the applicability of PTA method can further expended. Besides, a restart algorithm in the SPICE3 implementation is also proposed to help the circuit converge when the simulation stuck into an infinity loop. Numerical examples demonstrate the effectiveness of the proposed algorithms. Simulation efficiency can be greatly improved, and the algorithm can be applied even for some large-scale circuits.

The dissertation is organized with five chapters as follows:

In Chapter 1, the background of circuit simulation is given. The SPICE-like simulators, the different types of circuit analysis, and the conventional numerical analysis algorithms are introduced. The DC analysis is very fundamental and important, since it is the prior to perform the small signal analysis and transient analysis. After that, several continuation methods for the DC analysis, including Gmin stepping, source stepping, homotopy method and PTA method, are discussed. Then, the motivation of this research and the dissertation organization are shown.

In Chapter 2, the PTA methods are introduced since it is one of the most effective methods to solve the nonlinear DC circuits. The conventional PTA methods are discussed, including the pure element PTA, compound element PTA (CEPTA), and Damped PTA (DPTA) methods. Then a SPICE3 implementation algorithm

for CEPTA is reviewed. The drawbacks and the challenges of the PTA methods can be obtained by analyzing these conventional PTA methods.

In Chapter 3, an implementation algorithm and embedding algorithms of CEPTA are proposed. The section 3.1 and 3.2 present the introduction and challenges of PTA methods. The conventional implementation algorithm applies the numerical integration method in the compound branch level for the compound pseudo elements. It has a limitation of the time-step size which influences the convergence and efficiency of the NR method. When the time-step size gets larger and the approximation error becomes extremely large, the NR method may fail to converge. To overcome this problem, the proposed implementation algorithm applies the numerical integration algorithm in individual element level by decomposing the compound branch. Therefore, the proposed algorithm is much more efficient and the convergence performance of CEPTA can be greatly improved. The convergence of the proposed implementation algorithm is also proved in section 3.3. In the proposed embedding algorithm, three embedding positions of the pseudo-elements are extended to the CEPTA method, including Diagonal, BC(GD) and BE(GS) positions. For different types of circuits or different simulation conditions, the appropriate embedding position should be carefully selected to obtain the best simulation performance. In order to verify the effectiveness, the proposed algorithms are implemented on our spice simulator WSPICE and applied to practical large-scale analog circuits. Section 3.4 shows the numerical examples and comparisons. By using the proposed implementation algorithm and suitable embedding position, the convergence of CEPTA method can be greatly improved (the number of total iterations is reduced by 40%) compared with the conventional CEPTA method (Hong Yu, IEICE Trans 2007). Besides, the proposed methods can solve the large-scale analog DC circuits (the number of devices > 1000) while the conventional CEPTA and de-facto standard commercial circuit simulators fail. The embedding algorithm can be extended to other PTA algorithms.

In Chapter 4, a ramping algorithm and a restart algorithm are proposed to improve the simulation efficiency. In the proposed ramping algorithm, the supply voltages are ramped up from zero to their final values over time according to the certain ramping function without inserting any pseudo-inductors. Two effective ramping functions, the sine type ramping function and the cosine type ramping function, are proposed and the continuity and smoothness are analyzed in section 4.3. The proposed ramping algorithm can eliminate the oscillation caused by the inserted inductor. Moreover, the number of non-zero elements and fill-ins in the Jacobian matrix can be greatly reduced. In the proposed restart algorithm, a recognition method is used to check whether the simulation is stuck into an infinite loop by detecting how many times the NR method fails to converge in a certain time period and how the time-step size changes. If the infinite loop occurs, the restart algorithm will roll back to the previous step and do the simulation again with the constant time-step size. In order to verify the effectiveness, proposed ramping and restart algorithms are implemented on our spice simulator WSPICE and applied to the large-scale analog circuits. The effectiveness are confirmed by the numerical examples in section 4.4. Compared with conventional DPTA method (Xiao Wu, NOLTA2014), the proposed ramping algorithm reduces the number of non-zero elements of the Jacobian, and the number of fill-ins is reduced by 40%∼60%. As a result, the number of total iterations can be reduced by 8.67%∼66.5%, and the CPU time can be reduced by 28.14%∼70.2%. The proposed restart algorithm is proved to be effective to improve the convergence for the test circuits which have the infinite loop problem.

The conclusions of this dissertation are given in Chapter 5.

5.2 Future Works

Until now, all the proposed methods are implemented in the WSPICE simulator. And our methods are verified by a large number of test circuits. These test circuits include many commonly used benchmark circuits and many really difficult circuits created by ourself. Although the proposed methods are proved to be very effective to solve these complex and large-scale circuits, there is still a big problem need to be solved in the future works.

This big problem is the parameter optimization. As we know that for the different kinds of circuits, the situation is totally different. The simulation process is greatly affected by the value of parameters. In the majority of cases, we can only choose the value of parameters by our experience which can not always guarantee the high efficiency and convergence. Therefore, we need much more correction mechanism, like the restart method proposed in Chapter 4, to adapt the value of parameters automatically. And we also have to improve the robustness of our methods.

Bibliography

[1] L.W. Nagel, "Spice2: A computer program to simulate semiconductor circuits," University of California, Berkeley, ERL-M520, May 1975.

[2] T. L. Quarles, "Analysis of performance and convergence issues for circuit simulation," Univ. of California, Berkeley, CA, ERL-M89/42, April 1989.

[3] R.M. Kielkowski, Inside SPICE, second ed., McGraw-Hill, 1998.

[4] D.O. Pederson, "A historical review of circuit simulation," Circuits and Systems, IEEE Transactions, vol.31, Issue 1, pp. 103 - 111 Jan 1984.

[5] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The modified nodal approach to network analysis," IEEE Trans. Circuits Syst., vol, CAS-22, no. 6, pp.504-509, Jun. 1975.

[6] Leon O. Chua and Pen-Min Lin, Computer-aided analysis of electronic circuits: algorithms and computational techniques, New Jersey, Prentice-Hall, Inc., 1975.

[7] G. Massobrio and P. Antognetti, Semiconductor device modeling with SPICE (Second edition), McGraw-Hill, Inc., US, 1993.

[8] R. J. Baker, H. W. Li and D. E. Boyce, CMOS circuit design, layout and simulation, IEEE press series on microelectronic systems, 1997.

[9] M. Tadeusiewicz, "Modeling and stability in MOS transistor circuits," 1998 IEEE Int. Conf. Electoronics, Circuits and Systems, Lisboa, Portugal, vol.1, pp71-74, Oct. 1998.

[10] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and design of analog integrated circuits, John Wiley & Sons, Inc., 2001.

[11] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," IEEE J. Solid-State, SC-3, 1968.

[12] F. S. Jenkins, E.R. Lane, W. W. Lattin, and W. S. Richardson, "MOS-Device Modeling for Computer Implementation," IEEE Trans. on Circuit Theory, vol. CT-20, pp. 649-658, Nov. 1973.

[13] C.W. Ho, A.E. Ruehli, and P.A. Brennan, "The modified nodal approach to network analysis," IEEE Trans. Circuits Syst., vol. CAS-22, no. 6, pp.504-509, Jun. 1975.

[14] A. Ushida and M. Tanaka, Electronic Circuit Simulation, Corona Publ., 2002.

[15] ASTAP general Information Manual (GH20-1271-0), IBM Corp., Mechanicsburg, Pa.

[16] W. Weeks, A. Jimenez, G. Mahoney, D. Mehta, H. Qassemzadeh, and T. Scott, "Algorithms for ASTAP-A network-analysis program," IEEE Trans. Circuits Syst., vol.20, no.6, pp.628-634, Nov. 1973.

[17] R. Wilton, "Supplementary algorithms for DC convergence," IEE Colloquium, SPICE: Surviving Problems in Circuit Evaluation, pp.3/1-3/19, June 1993.

[18] L. Goldgeisser, E. Christen, M. Vlach, and J. Langenwalter, "Open ended dynamic ramping simulation of multi-discipline systems," Proc. ISCAS, vol.5, pp.307-310, May 2001.

[19] FN. Najm, Circuit simulation, Proc. IEEE. A John Wiley & Sons, INC., 2010.

[20] E. Yilmaz and Michael M. Green, "Some standard SPICE DC algorithms revisited: Why does SPICE still not converged Circuits and Systems," Proc. ISCAS '99, Orlando, FL, vol.6, pp286-289, 30 May 1999-02 Jun 1999.

[21] C.B. Garcia and W.I. Zangwill, Pathways to Solutions, Fixed Points, and Equilibria, Prentice-Hall, 1981.

[22] D. Niu, K. Sako, G. Hu and Y. Inoue. "A Globally Convergent Nonlinear Homotopy Method for MOS Transistor Circuits," IEICE Trans. Fundamentals, vol.E95-A, no.2, pp.2251-2260, Dec. 2012.

[23] Y. Inoue, Y. Imai, and K. Yamamura, "A homotopy method using a nonlinear auxiliary function for solving transistor circuits," IEICE Trans. Inf. & Syst., vol.E88-D, no.7, pp.1401-1408, July 2005.

[24] Y. Inoue, S. Kusanobu, and K. Yamamura, "A practical approach for the fixed-point homotopy method using a solution-tracing circuit," IEICE Trans. Fundamentals, vol.E85-A, no.1, pp.222-233, Jan. 2002.

[25] Y. Inoue, S. Kusanobu, K. Yamamura, and M. Ando, "An initial solution algorithm for globally convergent homotopy methods," IEICE Trans. Fundamentals, vol.E87-A, no.4, pp.780-786, April 2004.

[26] H. Yu, Y. Inoue, Y. Matsuya, and Z. Huang, "An effective pseudo transient algorithm for finding DC operating points of nonlinear circuits," IEICE Trans. Fundamentals, vol.E89-A, no.10, pp.2724-2731, Oct. 2006.

[27] H. Yu, Y. Inoue, Y. Matsuya, and Z. Huang, "An Effective SPICE3 Implementation of the Compound Element Pseudo-Transient Algorithm", IEICE Trans. Fundamentals, vol.E90-A, no.10, pp.2124-2131, Oct. 2007.

[28] S. Du, and Y. Inoue, "Initial Solution Method for Efficient Pseudo-Transient Analysis", Master Thesis, Waseda University, 2009.

[29] Z. Jin, X. Wu, D. Niu, Y. Inoue, "Effective Implementation and Embedding Algorithms of CEPTA Method for Finding DC Operating Points," IEICE Trans. Fundamentals, vol.E96-A, no.12, pp.2524-2533, Dec. 2013.

[30] X. Wu, Z. Jin, D. Niu and Y. Inoue, "A PTA Method Using Numerical Integration Algorithms with Artificial Damping for Solving Nonlinear DC Circuits," IEICE trans. NOLTA, Vol.E5-N, No.4, pp.512-522, Oct, 2014.

[31] Y. Dodge, The Oxford Dictionary of Statistical Terms, 2003.

[32] D. N Joanes, C. A. Gill, "Comparing measures of sample skewness and kurtosis", Journal of the Royal Statistical Society, Series D, The Statistician 47 (1),pp.183-189, 1998.

[33] J. A. Barby and R. Guindi, "CircuitSim93: A circuit simulator benchmarking methodology case study," ASIC Sixth Annual IEEE International Conference and Exhibit, pp.531-535, Sep. 27-Oct. 1st, 1993.

[34] J. Wang, and Y. Inoue, "Efficient Pseudo-transient Method for Nonlinear Circuit Analysis", Master Thesis, Waseda University, 2009.

[35] X. Wu, Z. Jin, X. Lian, D. Niu and Y. Inoue, "An Effective Switching Algorithm for the Damped Pseudo-Transient Analysis," ITC-CSCC2013, Yeosu, Korea, pp.922-925, July 2013.

[36] Z. Huang, Y. Inoue, H. Yu, J. Pan, Y. Yang, Q. Zhang, S. Fang, "Behavioral Circuit Macro modeling and Analog LSI Implementation for Automobile Engine Intake System," IEICE Trans. Fundamentals, vol.E90-A, no.4, pp.732-740, April 2007.

[37] Star-Hspice Manual, pp.6(24)-6(25), Release 1998.2, July 1998.

[38] Z. Jin, X. Wu, D. Niu, X. Guan and Y. Inoue, "Effective Ramping Algorithm and Restart Algorithm in the SPICE3 Implementation for DPTA Method," Nonlinear Theory and Its Applications, IEICE (NOLTA), Vol.E6-N, No.4, pp.499-511, Oct. 2015.

[39] D. Niu, K. Sako, G. Hu and Y. Inoue, "A globally convergent nonlinear homotopy method for MOS transistor circuits," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, vol. E95-A, no.12, pp.2251-2260, Dec. 2012.

[40] D. Niu, X. Wu, Z. Jin and Y. Inoue, "An effective and globally convergent Newton fixed-point homotopy method for MOS transistor circuits," IEICE Transactions Fundamentals of Electronics, Communications and Computer Sciences, vol.E96-A, no.9, pp.1848-1856, Sep. 2013.

[41] LTspice IV User Manual, Linear Technology, Oct 2011.

Related Paper

Related Paper

1. Zhou Jin, Xiao Wu, Dan Niu, Xiaoli Guan and Yasuaki Inoue, "Effective Ramping Algorithm and Restart Algorithm in the SPICE3 Implementation for DPTA Method," Nonlinear Theory and Its Applications, IEICE (NOLTA), Vol.E6-N, No.4, pp.499-511, Oct. 2015.

2. Zhou Jin, Xiao Wu, Dan Niu, and Yasuaki Inoue, "Effective Implementation and Embedding Algorithms of CEPTA Method for Finding DC Operating Points," IEICE Transactions Fundamentals of Electronics, Communications and Computer Sciences, vol.E96-A, no.12, pp.2524-2533, Dec. 2013.

3. Zhou Jin, Xiao Wu, Dan Niu and Yasuaki Inoue, "A ramping method combined with the damped PTA algorithm to find the DC operating points for nonlinear circuits," IEEE, the 14th International Symposium on Integrated Circuits (ISIC), Singapore, pp.576-579, Dec.10-12, 2014.

4. Zhou Jin, Xiao Wu, Xiaoli Guan, Dan Niu and Yasuaki Inoue, "An Effective Ramping PTA Method for the DC Analysis of Nonlinear Circuits," IEICE, the 28th International Technical Conference on Circuits/Systems, Computers and Communications, Yeosu Korea (ITC-CSCC2013), pp.317-320, June 30-July 3, 2013.

5. Zhou Jin, Xiao Wu and Yasuaki Inoue, "An Effective Implementation and Embedding Algorithm of PTA Method for Finding DC Operating Points," IEEE International Conference on Communications, Circuits and Systems (ICCCAS2012), pp.417-420, Taichung, Aug.20-22 2012.

Publications

Journal Papers

[A1] Zhou Jin, Xiao Wu, Dan Niu, Xiaoli Guan and Yasuaki Inoue, "Effective Ramping Algorithm and Restart Algorithm in the SPICE3 Implementation for DPTA Method," Nonlinear Theory and Its Applications, IEICE (NOLTA), Vol.E6-N, No.4, pp.499-511, Oct. 2015.

[A2] Zhou Jin, Xiao Wu, Dan Niu, and Yasuaki Inoue, "Effective Implementation and Embedding Algorithms of CEPTA Method for Finding DC Operating Points," IEICE Transactions Fundamentals of Electronics, Communications and Computer Sciences, vol.E96-A, no.12, pp.2524-2533, Dec. 2013.

[A3] Xiao Wu, Zhou Jin, Dan Niu and Yasuaki Inoue, "An Effective Time-step Control Method in Damped Pseudo-transient Analysis for Solving Nonlinear DC Circuit Equations," IEICE Transactions Fundamentals of Electronics, Communications and Computer Sciences, Vol.E98-A, No.11, 9 pages, to appear, Nov. 2015.

[A4] Xiao Wu, Zhou Jin, Dan Niu and Yasuaki Inoue, "PTA Method Using Numerical Integration Algorithms with Artificial Damping for Solving Nonlinear DC Circuits," Nonlinear Theory and Its Applications, IEICE (NOLTA), Vol.E5-N, No.4, pp.512-522, Oct, 2014.

[A5] Dan Niu, Xiao Wu, Zhou Jin and Yasuaki Inoue, "An effective and globally convergent Newton fixed-point homotopy method for MOS transistor circuits," IEICE Transactions Fundamentals of Electronics, Communications and Computer Sciences, vol.E96-A, no.9, pp.1848-1856, Sep. 2013.

International Conference

[B1] Zhou Jin, Xiao Wu, Dan Niu and Yasuaki Inoue, "A ramping method combined with the damped PTA algorithm to find the DC operating points for nonlinear circuits," IEEE, the 14th International Symposium on Integrated Circuits (ISIC), Singapore, pp.576-579, Dec.10-12, 2014.

[B2] Zhou Jin, Xiao Wu, Xiaoli Guan, Dan Niu and Yasuaki Inoue, "An Effective Ramping PTA Method for the DC Analysis of Nonlinear Circuits," IEICE, the 28th International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC2013), Yeosu Korea, pp.317-320, June 30-July 3, 2013.

[B3] Zhou Jin, Xiao Wu and Yasuaki Inoue, "An Effective Implementation and Embedding Algorithm of PTA Method for Finding DC Operating Points," IEEE International Conference on Communications, Circuits and Systems (ICCCAS2012), pp.417-420, Taichung, Aug.20-22 2012.

[B4] Dan Niu, Yasuaki Inoue, Zhou Jin and Xiao Wu, "A Netlist Implementation of the Newton Fixed-point Homotopy Method for MOS Transistor Circuits," IEEE International Midwest Symposium on Circuits and Systems, Colorado, USA, August 2-5, 2015 (Accepted).

[B5] Xiao Wu, Zhou Jin, and Yasuaki Inoue, "Numerical integration algorithms with artificial damping for the PTA method applied to DC analysis of

nonlinear circuits," IEEE, the 14th International Symposium on Integrated Circuits (ISIC), Singapore, pp.421-424, Dec.10-12, 2014.

[B6] Xiao Wu, Zhou Jin, Xiuming Lian, Dan Niu and Yasuaki Inoue, "An Effective Switching Algorithm for the Damped Pseudo-Transient Analysis," IEICE, the 28th International Technical Conference on Circuits/Systems, Computers and Communications, Yeosu Korea (ITC-CSCC2013), pp.922-925, June 30-July 3, 2013.

[B7] Dan Niu, Zhou Jin, Xiao Wu, Yasuaki Inoue, "A Globally Convergent and Highly Efficient Homotopy Method for MOS Transistor Circuits," IEEE 7th International Conference on Computing and Convergence Technology (ICCCT2012), pp.1349-1352, Seoul, Dec. 2012.

[B8] Xiao Wu, Zhou Jin and Yasuaki Inoue, "Numerical Integration Algorithms with Artificial Damping for the PTA Method Applied to DC Analysis of Nonlinear Circuits," IEEE International Conference on Communications, Circuits and Systems (ICCCAS2012), pp. 421-424, Taichung, Aug.20-22 2012.

Others

[C1] Zhou Jin, Xiao Wu, Dan Niu and Yasuaki Inoue, "An Effective Ramping PTA Method for the DC Analysis of Nonlinear Circuits," IPS-ICS2013, Kitakyushu, Nov. 2013.

[C2] Zhou Jin, Xiao Wu, Dan Niu and Yasuaki Inoue, "Effective Implementation and Embedding Algorithms of CEPTA Method for Finding DC Operating Points," The Institute of Electrical Engineers of Japan, IEEJ, Technical Committee on Electronic Circuit, kumamoto university, vol. ECT-12-77, pp.81-91, Oct. 2012.

[C3] Zhou Jin, Xiao Wu, and Yasuaki Inoue, "A norm step size control algorithm for the PTA method to find DC operating points," the 8th International collaboration Symposium on Information, Production and Systems (ISIPS 2014), Kitakyushu, Nov. 2014.

[C4] Xiao Wu, Zhou Jin and Yasuaki Inoue, "The Limitation for the Growth of Step of DPTA Method," the 8th International collaboration Symposium on Information, Production and Systems (ISIPS 2014), Kitakyushu, Nov. 2014.

[C5] Dan Niu, Zhou Jin, Xiao Wu, Ziming Zhao and Yasuaki Inoue, "An Effective and Globally Convergent Homotopy Method for MOS Transistor Circuits, " the 6th IPS International Collaboration Symposium (IPS-ICS2012), Kitakyushu, Nov. 2012.

Acknowledgements

At the point of finishing this paper, I would like to express my sincere thanks to my supervisor, Professor Yasuaki INOUE of Waseda University, for his technical mentoring, advices, and direction during past 5 years. He helped me a lot not only from the research lives but also the daily lives at the Waseda University. I appreciate so much for his kindness. I would also like to thank Professor Takahiro Watanabe and Professor Shinji Kimura of Waseda University, for their technical review and support.

I extend my thanks to the fellow members of the INOUE Laboratory for their valuable suggestions and help during the past five years, Xiao WU, Zhangcai HUANG, Li DING, Dan NIU, Qiang LI, etc.. I also thank very much for the accompanies of other members from the INOUE Laboratory, Jing WANG, Wenqin XU, Junjie HUANG, Qian GUO, Chang GAO, Yufeng SUN, Zhao CHEN, Hao WU. I thank all of my friendes in IPS, and I appreciate the many happy hours that I spent with them.

The "Teijin scholarship" and "Global-COE program" are very generous in granting me financial assistance. These supports are very important to my study.

Finally, I would like to thank my husband Xiao WU and my parents, Yaping JIN and Deqin ZHOU, for their kind support over these years. The support from the family gives me a lot of courage and faith to the life.