Adaptive Power Amplifiers for Modern Communication Systems with Diverse Operating Conditions

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

In this thesis, novel designs for adaptive power amplifiers, capable of maintaining excellent performance at dissimilar signal parameters, are presented. These designs result in electronically reconfigurable, single-ended and Doherty power amplifiers (DPA) that efficiently sustain functionality at different driving signal levels, highly varying time domain characteristics and wide-spread frequency bands. The foregoing three contexts represent those dictated by the diverse standards of modern communication systems.

Firstly, two prototypes for a harmonically-tuned reconfigurable matching network using discrete radio frequency (RF) microelectromechanical systems (MEMS) switches and semiconductor varactors will be introduced. Following that is an explanation of how the varactor-based matching network was used to develop a high performance reconfigurable Class F^{-1} power amplifier.

Afterwards, a systematic design procedure for realizing an electronically reconfigurable DPA capable of operating at arbitrary centre frequencies, average power levels and back-off efficiency enhancement power ranges is presented. Complete sets of closed-form equations are outlined which were used to build tunable matching networks that compensate for the deviation of the Doherty distributed elements under the desired deployment scenarios. Off-the-shelf RF MEMS switches are used to realize the reconfigurability of the adaptive Doherty amplifiers.

Finally, based on the derived closed-form equations, a tri-band, monolithically integrated DPA was realized using the Canadian Photonics Fabrication Centre (CPFC®) GaN500 monolithic microwave integrated circuit (MMIC) process. Successful integration of high power, high performance RF MEMS switches within the MMIC process paved the way for the realization of the frequency-agile, integrated version of the adaptive Doherty amplifier.

Acknowledgements

I would like to recognize all my colleagues in the EmRG and CIRFE research groups who have been constantly providing me with help and support during my research. A special acknowledgement should be remembering our great CIRFE lab manager; Bill Jolley for all his valuable efforts during every stage in my work. Last but not least, I would like to express my deep gratitude to my supervisors who gave me the support and the strength to face challenges in research; Prof. Slim Boumaiza, and Prof. Raafat Mansour.

Dedication

I would like to dedicate this dissertation to my parents, my lovely wife and my awesome sister who are always supportive to me and believe in me in reaching my dreams. Also, my work is dedicated to all my friends who present the model of true friendship and are always helpful to me.

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Chapter 1
Motivation and Introduction

1.1 Introduction

Recent developments in wireless communications have brought numerous challenges which are considerably increasing the complexity of wireless networks infrastructure design. One of the considerable consequences of these developments is the introduction of a broad spectrum of communication standards. Mobile systems such as the global system for mobile communications (GSM) and wideband code division multiple access (WCDMA), as well as wireless local area networks such as WiFi and WiMAX, are expected to co-exist and, hence, dynamic management of wireless networks is becoming an essential requirement.

Consequently, a shift from dedicated single operating condition radios to versatile and adaptive systems, capable of maintaining efficient operation over diverse deployment scenarios, is unavoidable. These scenarios include wide spread of carrier frequencies with different operating bandwidths as well as dissimilar signal characteristics which result in diverse peak to average ratios in the corresponding signals of values up to 6 or even 12 dB, depending on the standard and the modulation scheme. In addition, the continuously changing characteristics (e.g., average power) of the communication signals engendered by the dynamic networks' loads are posing additional performance challenges.

The diverse requirements of modern communication systems create numerous challenges in the design of infrastructure for radio systems and the corresponding RF frontend circuitry. The latter is expected to maintain competitive performance when fed with dissimilar signal characteristics such as centre frequencies, bandwidths, time domain statistics and modulation schemes. In summary, intelligent radio systems have to maintain their high efficiency and quality of signal (i.e., minimal distortion), when processing multi-mode and multi-standard communication standards.

1.2 Power Amplifiers in Modern Communication Systems

Like any communication system, radio systems are composed of numerous building blocks (BBs). These BBs can be either passive or active. Examples of passive BBs are switches, filters, couplers, power dividers, and antennas. These BBs are responsible for signal shaping and filtering. Active BBs consist of, among others, amplifiers; power amplifiers (PAs) in transmitters

and low noise amplifiers (LNAs) in receivers. They are responsible for boosting the transmitted and receiving signals' power. Other active blocks are mixers and oscillators essential for signal synthesis and frequency conversion of the signals (Figure 1-1).
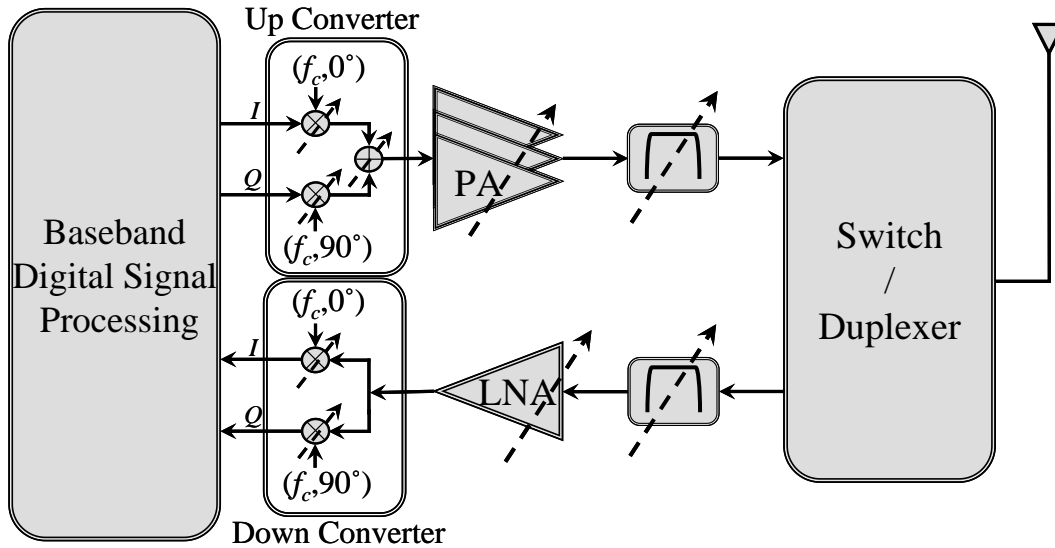
Figure 1-1, Modern Radio Systems Block Diagram

For adaptive radio systems, the different BBs have to maintain their expected performance parameters at various standards and for different applications. Among others, the radio front-end module (FEM), used in base stations and handsets, is required to meet various performance criteria, such us linearity and power efficiency, under different operation conditions (i.e., carrier frequency, modulation techniques, access technologies, and power levels).

The efficiency and linearity of the FEM are mainly dominated by that of PAs. The PA converts the direct current (DC) power into output radio frequency (RF) power which is provided to the transmitted signal. Hence, the design of the PA is extremely challenging as it is required to maintain high efficiency and minimize nonlinearities during multi-frequency and multi-mode operation.

1.3 High Efficiency Multi-mode Multi-frequency Power Amplifiers

PAs are generally designed to maximize efficiency at a given operating condition (i.e., peak power level and centre frequency) by presenting optimal source and load terminations at this arrangement. Hence, PAs only maintain high efficiency at a single frequency and peak input power level. Consequently, techniques must be developed to enhance the PA efficiency by

targeting the PA's optimum performance parameters, in other words source and load optimal terminations, at various back-off power levels and wide spread centre frequencies (Figure 1-2).

Γ_s (*f*, P_{in}) Γ_L (*f*, P_{in})

| Input Matching Network *(IMN)* | Active Device | Output Matching Network *(OMN)* |
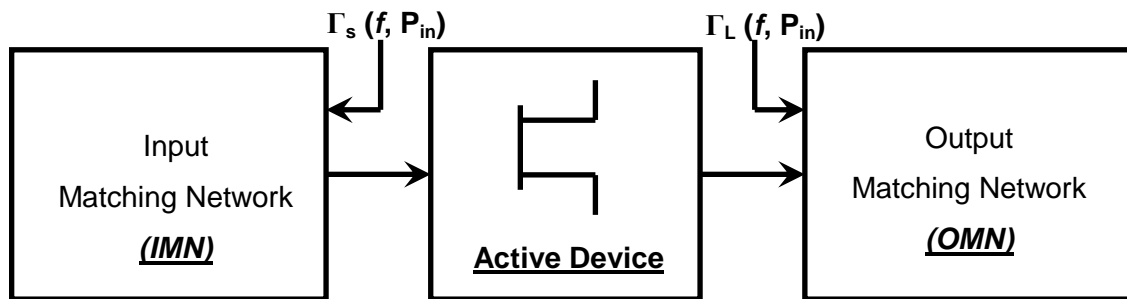
Figure 1-2, Block Diagram for a High Performance Power Amplifier

One of the potential techniques for PA efficiency enhancement is the reconfigurable PA. The design of electronically tunable matching networks at the source and load of the transistor, providing optimum impedances at back-off power levels as well as at the peak power level, becomes of great interest. These tunable source and load terminations enable PA reconfigurability versus power levels, however, handling dissimilar centre frequencies is still challenging. In order to fulfill the multi-standard operation of PAs, the matching networks have also to be multi-band, broadband or frequency agile.

Multi-band and broadband PAs are among the alternative solutions for PA efficiency enhancement for a preset group of operating frequencies. Multi-band PAs rely on the design of matching networks capable of simultaneous realization of optimal terminations at two or more frequencies. On the other hand, broadband PA designs achieve optimal terminations for a wide range of frequencies instead. These techniques improve PA operation versus the operating frequency. Maintaining competitive performance at reduced input signal levels, however, is still a challenge. One of the possible solutions is to extend the operating band of a pre-established efficiency enhancement technique, for example Doherty or Envelope Tracking. These techniques were originally designed to enhance the PA efficiency at back-off power levels.

1.4 Thesis Objectives

From the previous discussion it can be seen that the main limitation of RF PAs in modern radio systems is their optimized performance at a single operating scenario with dedicated single carrier frequency when the input signal operates at peak power level. Several efficiency enhancement

techniques, discussed in detail in Chapter 2, are available to maintain the PA optimized performance at reduced input power levels and efficiently handle signals with predetermined statistics. In this thesis, we focus on the complete design and development of PAs capable of maintaining their competitive performance under different operating scenarios including dissimilar signals statistics and centre frequencies. PAs with variable operating conditions (e.g., peak-to-average power ratios (PAPR), centre frequencies and variable peak driving signal levels) are addressed throughout the presented work. Towards realizing the targeted adaptive PAs for modern radio systems, specific objectives were set for this research;

- Development and implementation of reconfigurable impedance matching networks using discrete tunable elements capable of synthesizing diverse impedances at widely spaced centre frequencies while controlling the corresponding harmonic impedances. The reconfigurable networks will be applied to implement a reconfigurable Class F^{-1} PA with harmonic tuning for efficiency enhancement at different power levels and diverse center frequencies.

- Development of a reconfigurable Doherty PA (DPA) for efficient amplification of multi-frequency, multi-standard radio signals.

- Development of a reconfigurable DPA for efficient handling and amplification of signals with variable average power levels.

- Development and implementation of GaN-based, high power RF microelectromechanical systems (MEMS) switches using the available NRC-CPFC$^{®}$ GaN500 monolithic microwave integrated circuit (MMIC) process.

- Development and implementation of an electronically tunable, integrated DPA, for multi-band radio systems operation, using the GaN500-compatible designed RF MEMS switches to achieve the required reconfigurability.

1.5 Thesis Outline

In Chapter 2, a brief review will be conducted of PA classes of operation. These classes are optimized to efficiently operate around a predetermined frequency and at a peak input power level. In addition, efficiency enhancement techniques targeting reduced input power level operation will be presented. Afterwards, a comparative study is presented of different approaches and techniques devised to maintain the PA's competitive performance over different frequency bands, dissimilar signals' time domain characteristics and back-off input power levels. Special attention is given to the DPA as an astute approach to back-off PA efficiency enhancement. DPAs

achieve this enhancement by actively modulating the load impedances for a predetermined PAPR value. Practical and theoretical limitations of DPAs under wideband operation and dissimilar signal PAPR values are examined. In addition, the features of AlGaN/GaN technology will be discussed as a candidate technology for realizing reconfigurable PAs.

Chapter 3 presents different solutions for extending the single-ended PA's high performance to simultaneous handling of wireless signals with different time domain characteristics, in other words PAPR, which are centered around widely spread operating frequencies. Complete design, fabrication and measurement results for two prototypes of harmonically-tuned reconfigurable Class F^{-1} PAs will be presented.

Afterwards, in Chapter 4, the design of electronically tunable multi-frequency multi-standard Doherty amplifier is presented. Systematic closed form equations are developed in order to achieve this. The design methodology is applied to design three Doherty prototypes; multi-frequency single PAPR, single frequency multi-PAPR and multi-frequency multi-mode DPAs. Fabrication and measurement results will be presented and discussed in details.

In Chapter 5, a similar design approach is conducted to develop closed form equations for designing a reconfigurable DPA that maintains high efficiency when driven by communication signals with highly varying average power levels for dynamic loads networks. The design procedure is then applied to realize a 10 W DPA that operates efficiently at average output power levels of 35, 30 and 25 dBm.

Chapter 6 discusses the GaN MMIC process available for realizing the integrated version of the reconfigurable Doherty PA. Challenges associated with implementing the tunable RF MEMS switch using the GaN MMIC process are highlighted in details. The design, fabrication and measurements of an integrated frequency-agile DPA, based on the analysis conducted in Chapter 4, is presented and discussed in this chapter.

Finally, we conclude what has been achieved through this research and the possible future developments for completing a fully integrated power amplifier for all possible operating conditions of modern wireless radio systems.

Chapter 2

Overview of Power Amplifier Efficiency Enhancement Techniques for Modern Radio Systems

2.1 Power Amplifier Classes of Operation

Power amplifiers (PAs) are used to convert the supply direct current (DC) power into radio frequency (RF) power which results in an enlarged version of the input signal at the output. Different design characteristics are considered when dealing with PAs including gain, output power delivered, bandwidth, and drain efficiency. The design of a PA is challenging as it is required to amplify the input RF signal with a minimum of distortion; this contradicts the nonlinear nature of the PA (Figure 2-1). As a result, a trade-off between efficiency and linearity must be carefully considered in the design of a PA. Different PA classes of operation were introduced to target the efficiency-linearity trade-off [1]. Conventional classes range from linear, low efficient class A to highly nonlinear, highly efficient class C. Other classes of high efficiency PAs (HEPAs) exploit harmonic impedance terminations to engineer the voltage and current waveforms, consequently maximizing the efficiency.
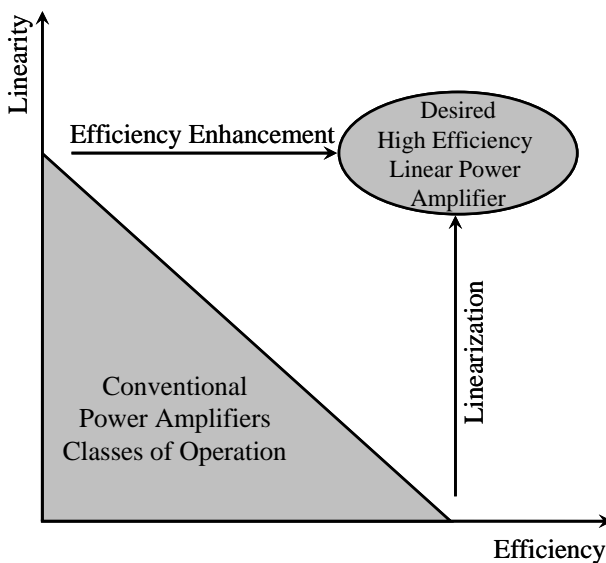
Figure 2-1, Trade-off between Linearity and Efficiency of Power Amplifiers

Figure 2-2 depicts various classes of operation of PAs. The conventional classes of operation, A, AB, B and C, consider the active device as a current source. Efficiency is increased from class

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A all the way to class C, at the expense of linearity [2], [3], by reducing the current conduction angle, 2θ (Figure 2-3). High efficiency classes of operation were introduced so that the efficiency can ideally be equal to one. For instance, class F/F^{-1} is biased like conventional PA classes yet requires appropriate tuning of harmonic impedances as well as fundamental ones. Switched mode PAs such as class D and E, where the active device operates as a switch, introduce a new generation of PAs that can deal directly with incoming digital signals. All of the high efficiency classes require tuning of harmonic impedances to achieve the theoretical highest efficiency. The more the harmonics are appropriately tuned, the more the efficiency approaches unity.
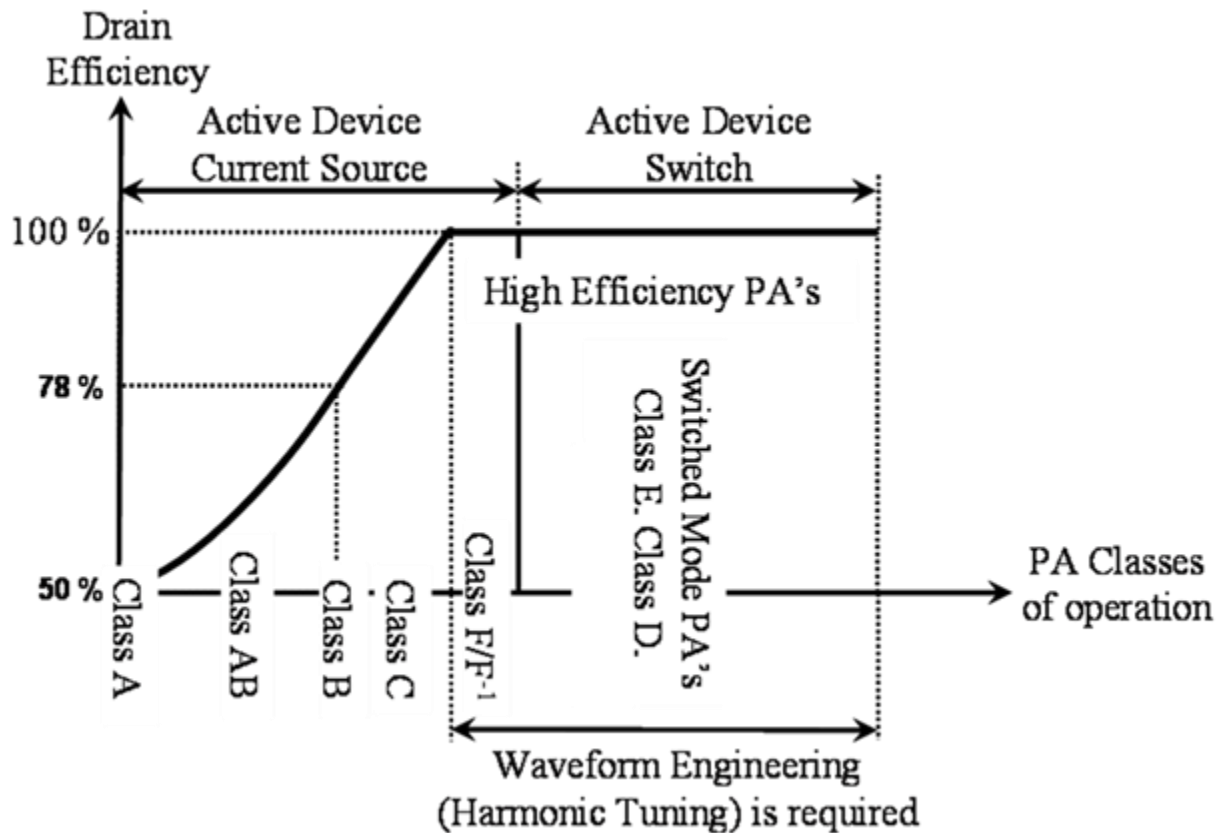
Figure 2-2, Different Classes of Operation for Power Amplifiers
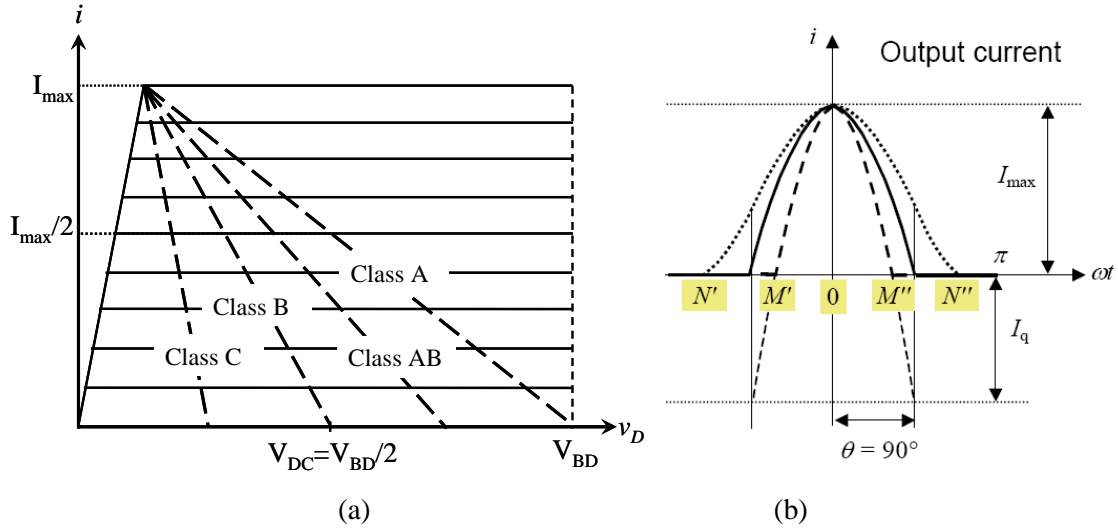
Figure 2-3, (a) Load/line Characteristics for Different Classes, (b) Output Current Waveforms for Class AB (dotted), Class B (solid), and Class C (dashed) [2]

2.2 Power Amplifier Efficiency Enhancement

Conventional PA circuits are generally designed to operate at single predetermined centre frequency and, at the same time, are optimally matched at a single input power level which is normally the peak power. However, recent evolutions in wireless communications have resulted in a broad spectrum of standards which involve highly varying envelope signals with different average power levels and which are centered around widely spaced frequency bands. As a result, adaptive PAs that maintain their competitive performances under diverse conditions are needed.

2.2.1 Single-Ended High Efficiency Multi-frequency Power Amplifiers

Development of efficiency enhancement techniques has been the objective of numerous research initiatives aimed at efficiently amplifying signals at back-off power levels and different operating frequencies. As previously mentioned, PAs require the precise introduction of optimal source and load terminations for the operating condition in order to efficiently amplify the incoming RF signal. In order to accommodate dissimilar deployment scenarios, like those dictated by modern radio systems, the PA matching networks should create the terminations of the preset operating conditions. Several techniques, including reconfigurable multi-band and broadband matching networks, may be utilized to acquire the desired PA designs for modern communication systems.

2.2.1.1 Reconfigurable Power Amplifiers
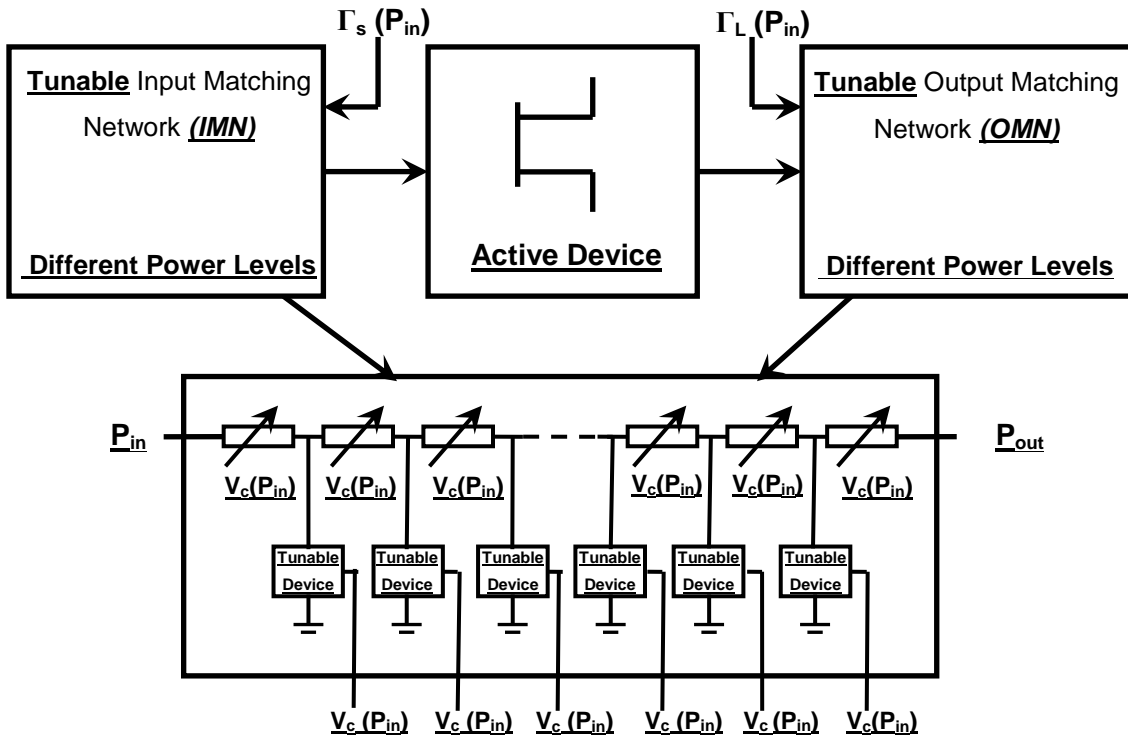
Figure 2-4, Schematic diagram for a Reconfigurable Power Amplifier

The load and source impedances of the active device can be passively modulated in order to introduce the transistor optimal impedances at different power levels, thus, realizing a reconfigurable PA (Figure 2-4). Passive load modulation implies the introduction of discrete, distributed, or integrated tunable devices in the matching networks circuitry. Optimal impedances at back-off power levels are introduced to improve the PA efficiency; tunable matching devices such as semiconductor varactors and switches, microelectromechanical systems (MEMS) based tunable devices, and tunable dielectrics are utilized to realize reconfigurable matching networks [4], [5], [6], [7].

In [4], a reconfigurable PA was fabricated using GaAs semiconductor varactors. The enhancement was only targeted at 1.75 GHz versus different power levels. Figure 2-5 shows the PA circuit schematic and the efficiency enhancement achieved.
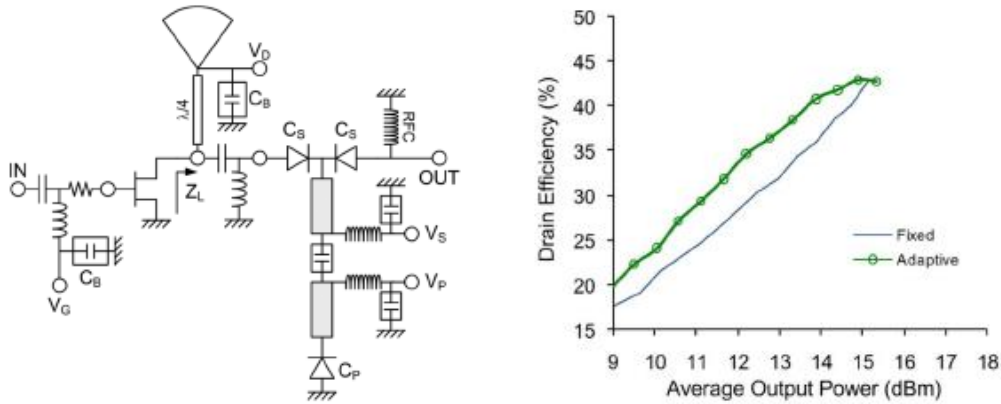
Figure 2-5, Schematic and Efficiency Enhancement Results for a Power Amplifier [4]

Another passively load modulated laterally-diffused metal oxide semiconductor (LDMOS) class E 7 W PA with enhanced efficiency at 10 dB output back-off power levels is presented in [5]. Tunability was achieved with 2x2 SiC Schottky diode stacked varactors to improve the tuning range and increase the breakdown voltage. The fabricated amplifier was centered around three different frequencies: 1 GHz which achieved more than 60% power-added efficiency (PAE) at peak output power, 7 W which achieved 30% PAE, and 0.7 W which achieved more than 10% enhancement (Figure 2-6).
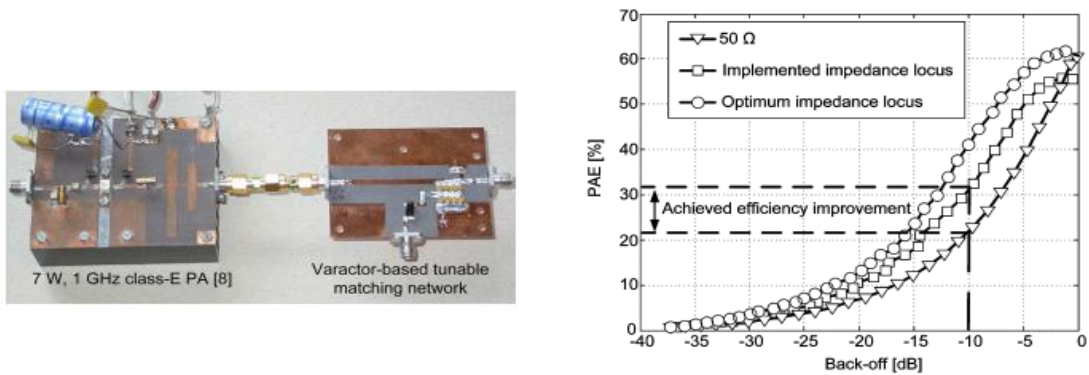
Figure 2-6, Circuit Demonstrator and Resulting Efficiency Enhancement Values [5]

The frequency-agile operation required for an adaptive PA is still challenging for reconfigurable PA prototypes. Moreover, the nonlinearity of the available tunable device technologies affects the linearity of the overall PA design. MEMS technology which on the

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contrary is highly linear, suffers from slow switching speeds. This limitation makes it challenging for variable envelope and wideband signals.

2.2.1.2 Multi-Band and Broadband Power Amplifiers

With a view to tackling the limited band of operation of conventional PAs, various approaches have been investigated to design broadband and multi-band amplifiers capable of handling multiple standards [8], [9], [10], [11], [12], [13], [14], [15]. These approaches have employed the class J design space [16], [17], [18], [19], [20] and dynamic passive load modulation. As an example, a novel methodology for dual-band PA design is achieved by transferring between Class F and Class F^{-1} operations [12] (Figure 2-7a). This design presents a three stage transmission lines-based low pass matching network for a Cree 10 W packaged device. Complete analysis was conducted to ensure the dual-band nature of the matching networks and subsequently, the demonstrator was fabricated as shown in Figure 2-7b. The dual-band PA achieved gain of higher than 10 dB and drain efficiency of about 80% for centre frequencies ranging between 1.8 and 2.8 GHz (Figure 2-7c). The approach, presented in this paper, is valid only when two frequencies have a specific relationship ($\dfrac{f_2}{f_1} = 1.5$).

A broadband design for a linearized class F PA is designed and presented in [13]. The PA design reduces the device sensitivity to harmonic terminations by using the device nonlinear capacitance for voltage and current wave-shaping. A complete analysis of the nonlinear device capacitance CDS was conducted to determine the high efficiency reactance values region in the design plane. Figure 2-8a shows the merged output power and peak efficiency optimal fundamental impedance contours at the appropriate output reactance termination. The fabricated prototype (Figure 2-8b) used a packaged 10 W Cree active device and achieved drain efficiency of more than 70% in the 1.45-2.45 GHz band (Figure 2-8c).
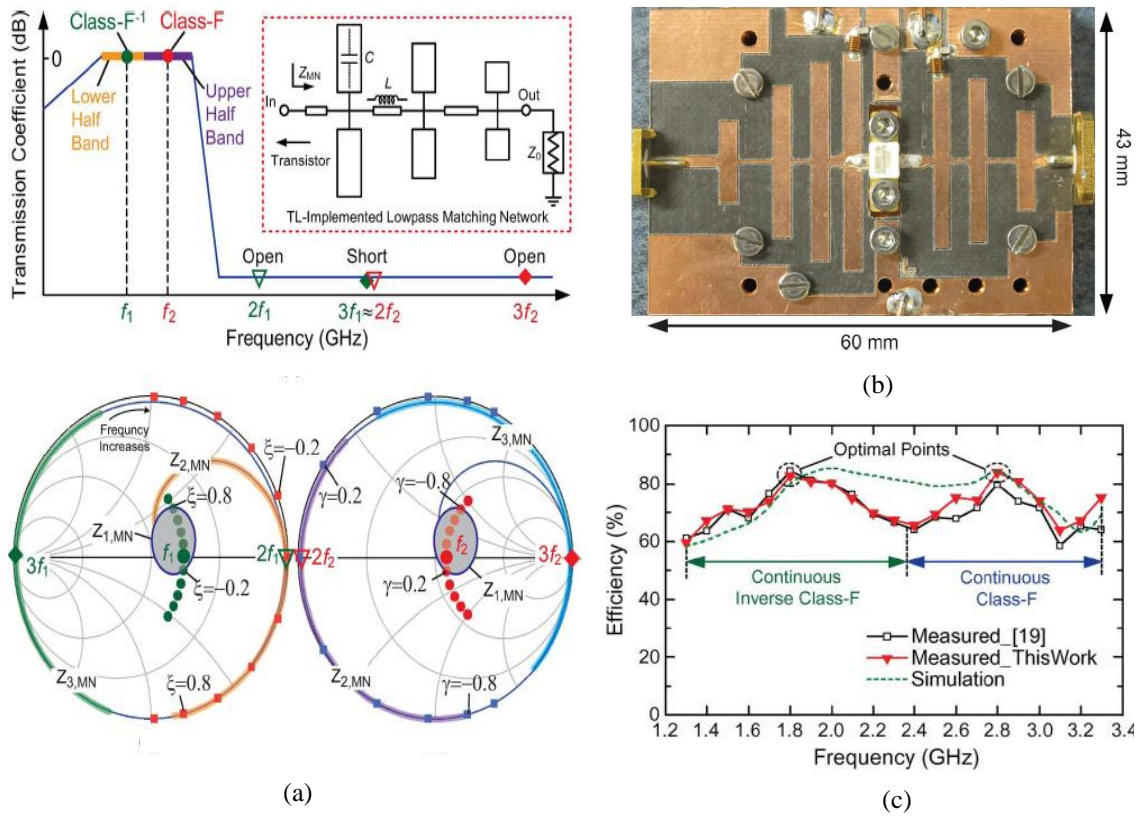
Figure 2-7, (a) Dual-band Dual Operating Frequency Matching Network Design, (b) Fabricated Power Amplifier, (c) Drain Efficiency Results for the Broadband Power Amplifier [12]

(a)

(b)
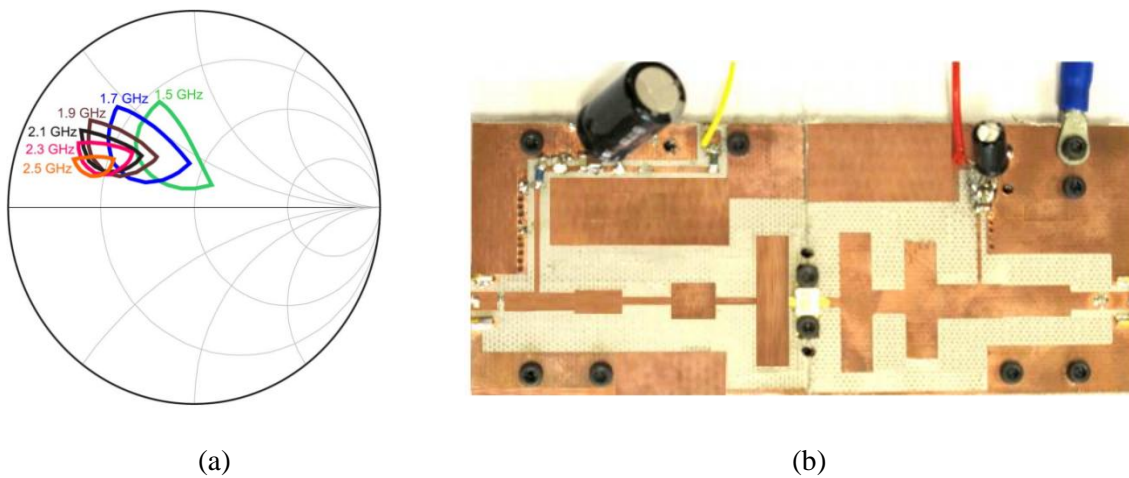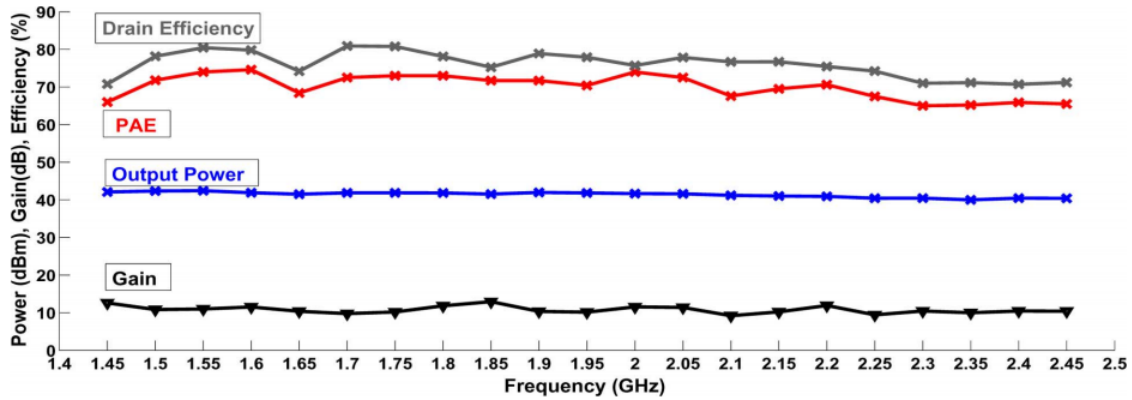
(c)

Figure 2-8, (a) Peak Output Power and Efficiency Contours of the Power Amplifier, (b) Circuit Demonstrator, (c) Measurement Results for the Broadband Class F Power Amplifier [13]

2.2.2 Envelope Tracking

Unlike passive load modulation of the PA optimal loads which uses reconfigurable matching networks, Envelope Tracking (ET) [21], [22], [23], [24], [25], [26], [27] achieves PA efficiency enhancement at back-off power levels by modulating the active device drain supply as a function of the input signal strength. Figure 2-9 shows the ET architecture with analog control where an envelope detector is used at the input to detect the signal envelope. A DC-DC converter (envelope amplifier) is used to provide the dynamically controlled supply voltage to a linear PA. ET architecture needs a delay line to compensate for the phase misalignment between the envelope and the RF signal due to the envelope feedback path. The ET system suffers from linearity issues to a greater extent than does the PA with fixed supply voltage.
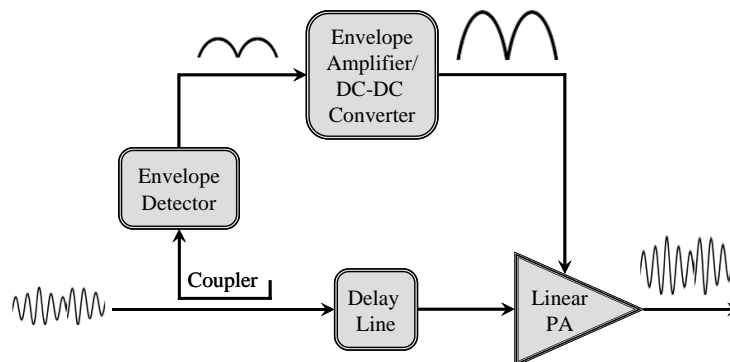
Figure 2-9, Envelope Tracking Architecture Block Diagram [2]

Thus, ET achieves PA efficiency enhancement versus reduced input power levels, however, the frequency agility remains unsolved. This challenge is addressed in [27]. The ET saturated amplifier's broadband matching networks are capable of covering the band from 1.3 to 2.7 GHz, achieving peak drain efficiency higher than 55% over the operating bandwidth (Figure 2-10a, b). The switching amplifier has a hybrid configuration, a schematic of which is shown in Figure 2-10c. The continuous wave (CW) measurements of the ET system's overall gain and efficiency at three selected frequencies are depicted in Figure 2-10d.

(a)

(b)

(c)

(d)
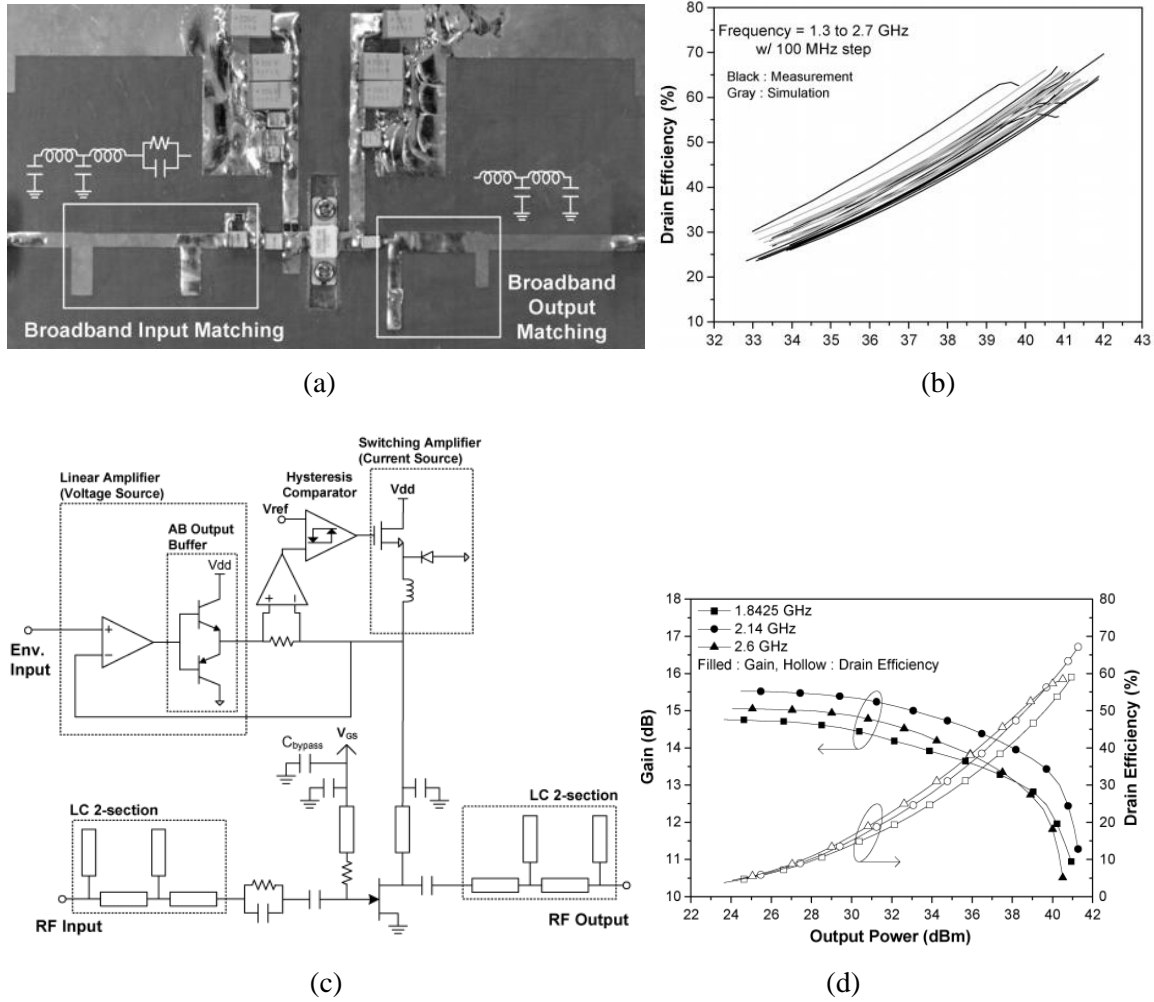
Figure 2-10, Broadband Saturated Amplifier (a) Demonstrator and (b) Continuous Wave Measurements; ET System (c) Circuit Schematic and (d) Continuous Wave Measurements [27]

ET technique is an attractive candidate for realizing multi-frequency multi-mode PAs, however, the limited speed of the DC-DC converter presents challenges for wideband and highly

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varying signal operation. The Doherty technique, however, achieves high efficiency over reduced power levels for rapidly varying envelope signals.

2.2.3 The Doherty Power Amplifier

2.2.3.1 Doherty Power Amplifier Operation Overview

The Doherty technique is an astute approach that has achieved a considerable shift in back-off power drain efficiency levels by actively modulating the load impedance of the PA; referred to as the main. The Doherty technique was first introduced in 1936 [28]. It actively modulates the load seen by the main transistor to improve its efficiency in the back-off via a judiciously configured auxiliary transistor [29], [30], [31]. This auxiliary transistor starts conduction at a desired power threshold value which is determined based on the efficiency enhancement power range calculated from the input signal peak-to-average power ratio (PAPR). The relatively challenging realization of the Doherty technique in practice, with real devices, delayed its successful implementation to the late 1990s and its commercial adoption to recent years. In the following paragraphs, a brief analysis of the Doherty technique will be given to demonstrate the limitations of the technique for efficient handling of modern wireless signals under multiple operating conditions.

Figure 2-11 depicts a generic Doherty amplifier block diagram that includes peaking and main transistors, input and output matching networks (IMN and OMN respectively), and two impedance inverters. The main amplifier is class AB biased and matched to ensure peak efficiency at a predetermined power level, denoted here as ρ-dB which corresponds to a reduced input voltage level of $\dfrac{V_{in,\max}}{p}$ where $\rho(dB) = 20\log p$. The auxiliary device is biased at class C and is required to start conducting at the given reduced input voltage. In order to maintain the maximum efficiency at the widely separated values of the desired back-off power levels, the output impedance seen by the main amplifier needs to follow (2-1) for given values of p, while at the same time, the auxiliary amplifier should be capable of supplying the required current values for proper load modulation (2-2).

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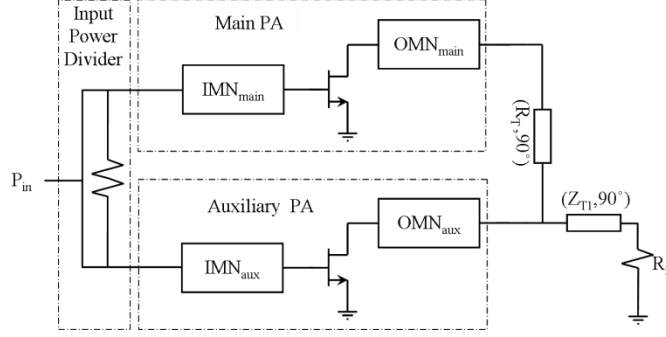
Figure 2-11, Conventional Doherty Amplifier Block Diagram

$$Z_{main} = \begin{cases} pR_L & 0 \le v_{in} \le \dfrac{1}{p}V_{in,max} \\ pR_L(1 - \dfrac{\alpha(p-1)}{1+(p-1)\alpha}) & \dfrac{1}{p}V_{in,max} \le v_{in} \le V_{in,max} \end{cases} \tag{2-1}$$

$$I_{aux} = I_{main}\frac{p\alpha(p-1)}{1+\alpha(p-1)} \tag{2-2}$$

2.2.3.2 Multi-frequency Multi-mode Doherty Power Amplifier Design Challenges

In this section, we explore the challenges that accompany the extension of Doherty PA (DPA) design to signals with different centre frequencies and extended PAPR levels. From the previous discussion, it can be seen that the dependence of the Doherty generic network design on the operating frequency and the preset PAPR value is non-negligible. Figure 2-12 illustrates the necessary variation of the desired main amplifier output load impedances and the corresponding auxiliary current profiles at PAPR values between 6 and 12 dB to achieve the proper load modulation. The resulting ideal drain efficiency profiles vs. input power for different back-off levels were obtained and are plotted in Figure 2-13.

In equations 2-1 and 2-2, $\alpha = \dfrac{pv_{in} - V_{in,max}}{V_{in,max}}$. Z_{T1}, R_T and R_L represent the two inverters' characteristic impedances and the Doherty load resistance, respectively. For proper Doherty operation, the characteristic impedance and the load resistance are equal to

$$R_L = R_{opt}, \quad R_T = R_L = R_{opt}, \quad Z_{T1} = \frac{R_{opt}}{\sqrt{p}} = \frac{R_L}{\sqrt{p}} \tag{2-3}$$

where R_{opt} denotes the optimum load impedance for the Doherty amplifier at peak input power.

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The plots in Figure 2-12 and Figure 2-13 were obtained at an operation frequency for which the length of the impedance inverters in Figure 2-11 were equal to quarter-wavelength. However, as the frequency varied, the load modulation in the DPA was affected directly by the varying of the impedance inverters' electrical lengths with frequency. The inclusion of the frequency dependency of the impedance inverters in (2-1) leads to the following expression of the impedance seen by the main transistor:
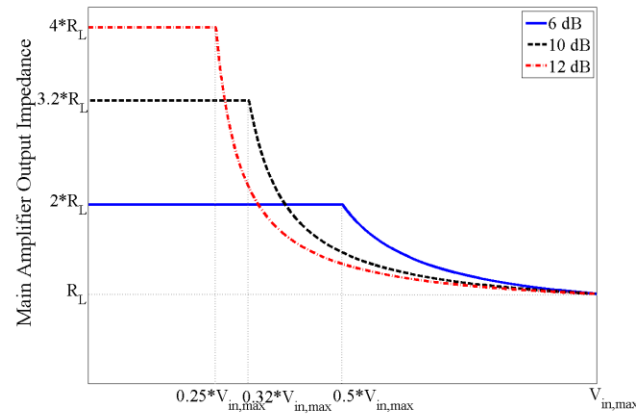
(a)
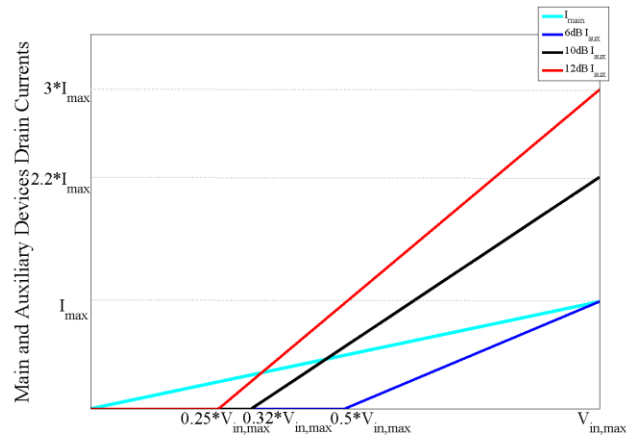
(b)

Figure 2-12, Ideal Profiles for (a) Main Amplifier Output Impedance and (b) Auxiliary Transistor Drain Current at Variable Peak to Average Power Ratio Values

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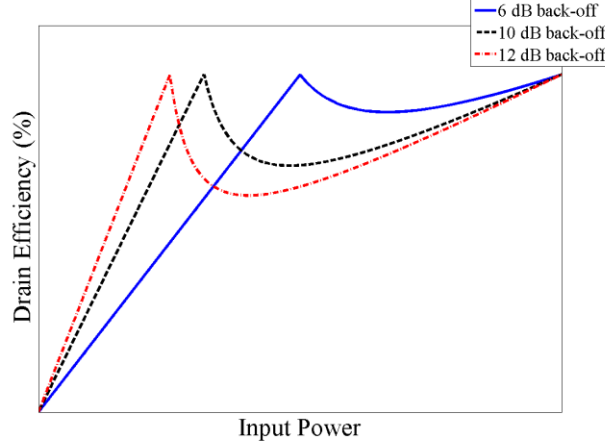
Figure 2-13, Ideal Drain Efficiency Profiles at Different Peak to Average Power Ratio Values

$$Z_{main} = \begin{cases} R_L \dfrac{(\sqrt{p}\cos^2\theta - p\sin^2\theta) + j(1+\sqrt{p})\sin\theta\cos\theta}{(\sqrt{p}\cos^2\theta - \sin^2\theta) + j(p+\sqrt{p})\sin\theta\cos\theta} \\[4pt] \qquad 0 \le V_{in} \le \dfrac{V_{in,\max}}{p} \\[6pt] R_L \dfrac{(\sqrt{p}\beta\cos^2\theta - p\sin^2\theta) + j(\beta+\sqrt{p})\sin\theta\cos\theta}{(\sqrt{p}\cos^2\theta - \beta\sin^2\theta) + j(p+\sqrt{p}\beta)\sin\theta\cos\theta} \\[4pt] \qquad \dfrac{V_{in,\max}}{p} \le V_{in} \le V_{in,\max} \end{cases} \qquad (2\text{-}4)$$

where $\beta = 1 + \dfrac{I_{aux}}{I_{main}} = 1 + \dfrac{p(p-1)\alpha}{1+(p-1)\alpha}$, p refers to the desired back-off level and θ denotes the new

electrical length of the impedance inverters at a given frequency. The real impedance seen by the

main transistor, $R_L = 50\Omega$, deviates from the ideal as presented in Figure 2-14. The improper

load modulation resulting from the frequency variation accentuates the efficiency degradation

versus frequency as the value of p increases. Figure 2-15 shows the efficiency deterioration due to

the strong sensitivity to frequency deviation of the Doherty amplifier impedance inverters. It is

worth mentioning, that both the main and auxiliary transistors exhibit additional parasitics and,

therefore, require output impedance matching networks. These parasitics contribute to the

frequency dependence of the DPA circuitry and cause additional challenges when attempting to

satisfy the conditions of proper load modulation over widely separated frequencies.

2.2.3.3 Multi-band and Broadband Doherty Power Amplifiers

Several attempts have targeted the development of broadband and multi-band DPAs [32], [33],

[34], [35], [36], [37] and yielded, thus far, relatively reduced efficiency compared to their

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narrowband counterparts especially in the back-off regions. In [34], a complete circuit analysis was presented to design a broadband DPA which would achieve the optimal load impedances for the main and auxiliary transistors over the targeted bandwidth. The design used packaged Cree devices to assemble symmetrical broadband DPA matching networks using 2.6 GHz centre frequency which covered a bandwidth of 2.2-3 GHz of operation. Figure 2-16 shows the maximum available flat drain efficiency, over 40% at 6 dB output back-off, over the desired frequency band.
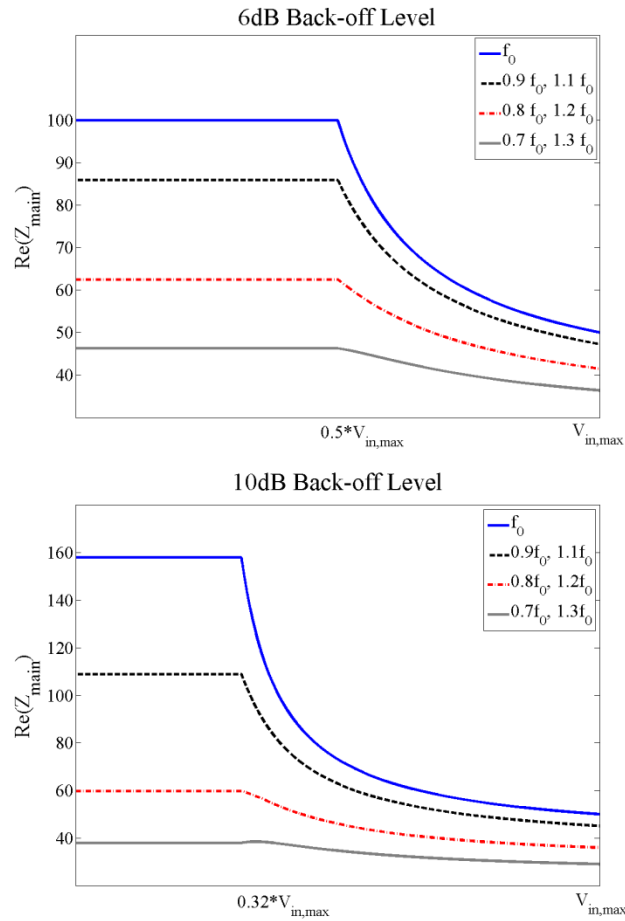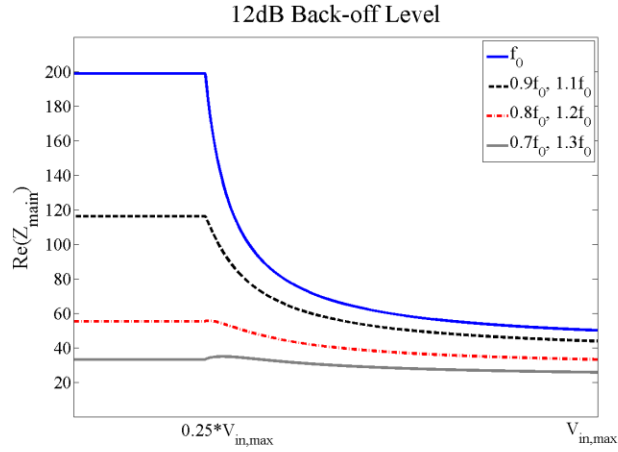
Figure 2-14, Main Transistor Output Impedance vs. Frequency for Different Doherty Power
Amplifier Configurations at Variable Peak to Average Power Ratio Values
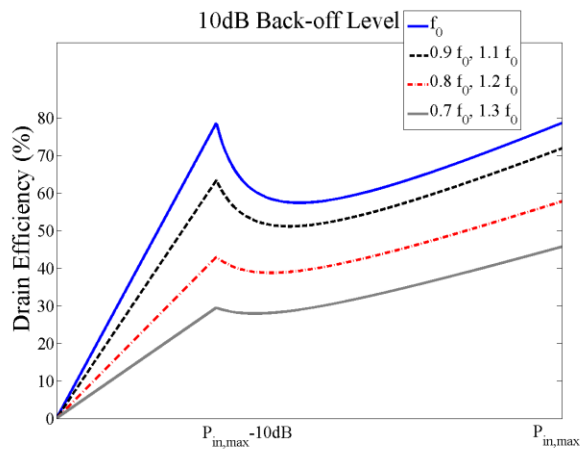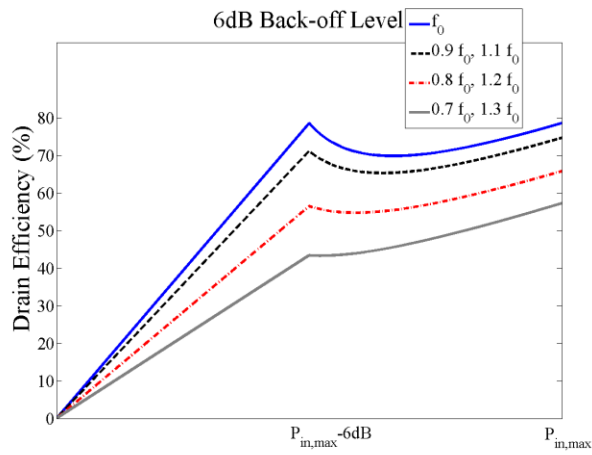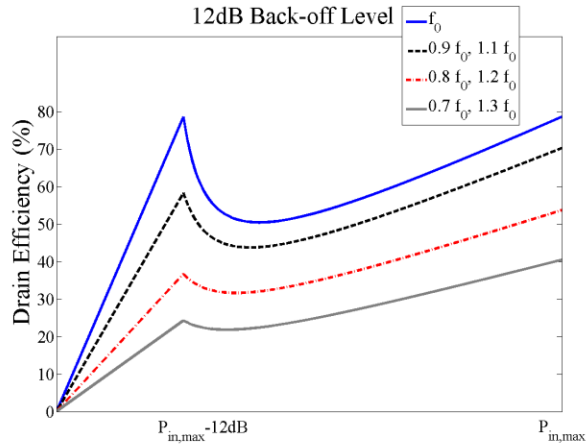
Figure 2-15, Main Transistor Drain Efficiency Deterioration vs. Frequency for Different Doherty Power Amplifier Configurations at Variable Peak to Average Power Ratio Values
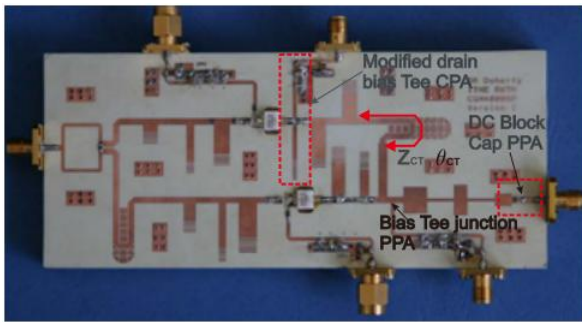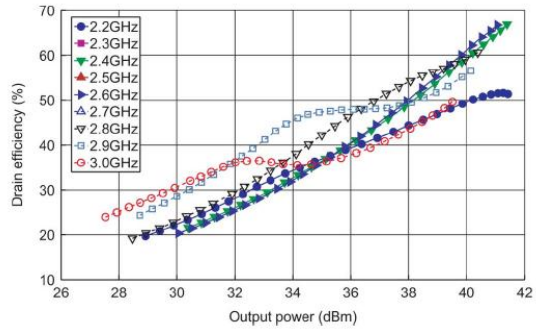
(a)   (b)

Figure 2-16, (a) Circuit Photograph and (b) Measured Drain Efficiency Results for the Broadband Doherty Power Amplifier [34]

A dual-band DPA operating at 0.88 and 1.96 GHz was designed and presented in [35] using careful design of dual-band T-shaped passive network components. The proposed design and the equivalent circuits for the dual-band building components are depicted in Figure 2-17. The paper presented two fabricated DPA prototypes with balanced and unbalanced input power division for enhancing the drain efficiency at back-off power levels.
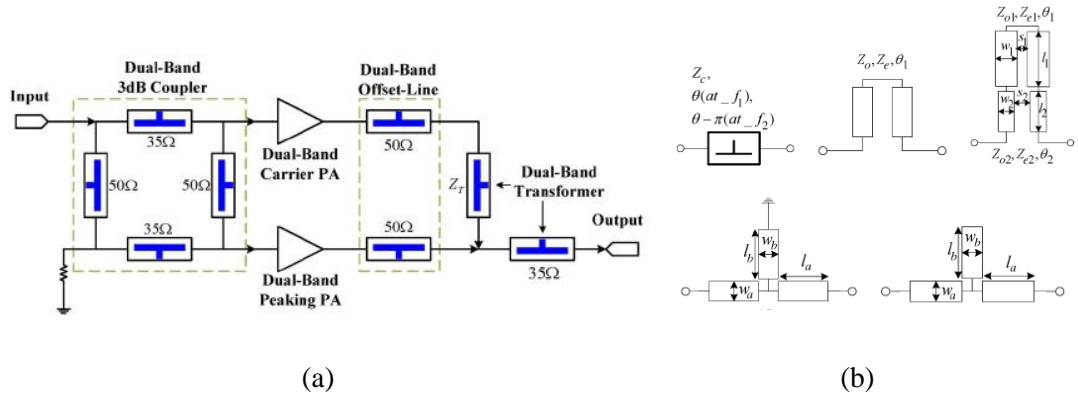
Figure 2-17, (a) Dual-band Doherty Power Amplifier Schematic and (b) Equivalent Circuit for the Dual-band Distributed Element [35]

2.2.3.4 Extended Peak to Average Power Ratio Doherty Power Amplifiers

For extended PAPR Doherty values, the efficiency profile in the back-off region drops. Several variations of the DPA main circuit design have been introduced for amplifying signals with extended PAPR values. Tailoring the efficiency curve requires N-way DPA [38], [39], [40] with N-1 auxiliary devices. However, as in [39], the size of the auxiliary transistors is directly proportional to the desired PAPR values. Hence, relatively large auxiliary amplifiers are required to shift the efficiency profile up in the back-off region. Recently, authors have proposed an interesting approach to reconfigure a Doherty amplifier, using die transistors, as a function of the input signal [41]. The PA was designed to operate at centre frequencies between 1.5 and 2.5 GHz. The reconfigurability was achieved by varying the drain supply voltage of the main transistor. Despite excellent drain efficiency achieved at PAPR as high as 10 dB (Figure 2-18) the overall gain was relatively low and the linearizability of the DPA was not presented. Moreover, the effect of reducing the main transistor drain bias on the power utilization factor was not discussed.
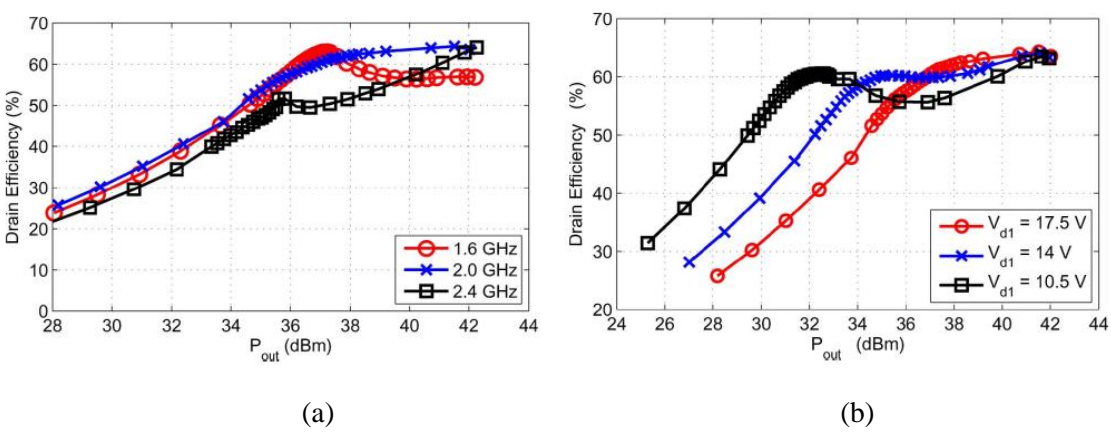
Figure 2-18, (a) 6-dB PAPR Efficiency Enhancement at Different Frequency Bands and (b) Multi-PAPR Efficiency Enhancement Results at 2 GHz [41]

In order to solve the problem of linearizability of the extended PAPR DPA, a modified design which deviated from the basic DPA circuit was presented in [42]. New auxiliary current profiles, and main amplifier drain bias values, optimized for every targeted PAPR value were derived. These findings are depicted in Figure 2-19a. The output matching network absorbed the parasitic capacitances of the main and auxiliary devices for wide band operation (Figure 2-19b). The amplifier achieved efficiency of greater than 50% (Figure 2-19c) and a small signal gain of more than 15 dB for output back-off up to 10 dB at 790, 870 and 960 MHz.

(a)

(b)

(c)
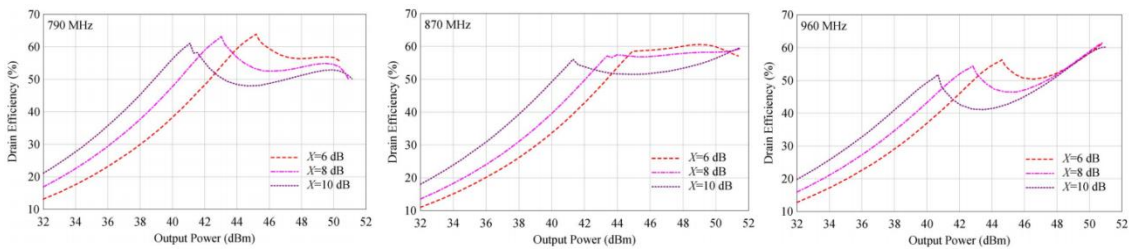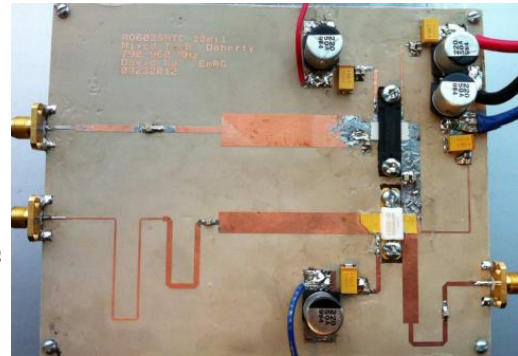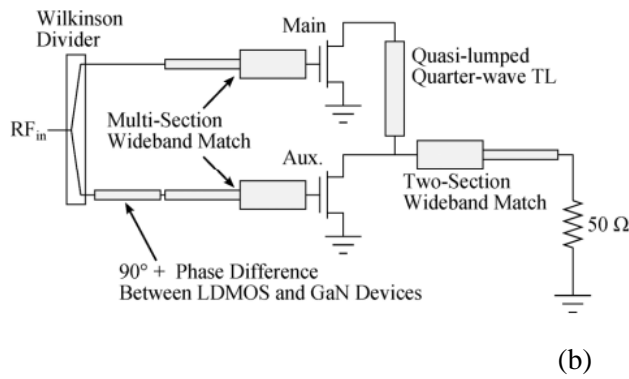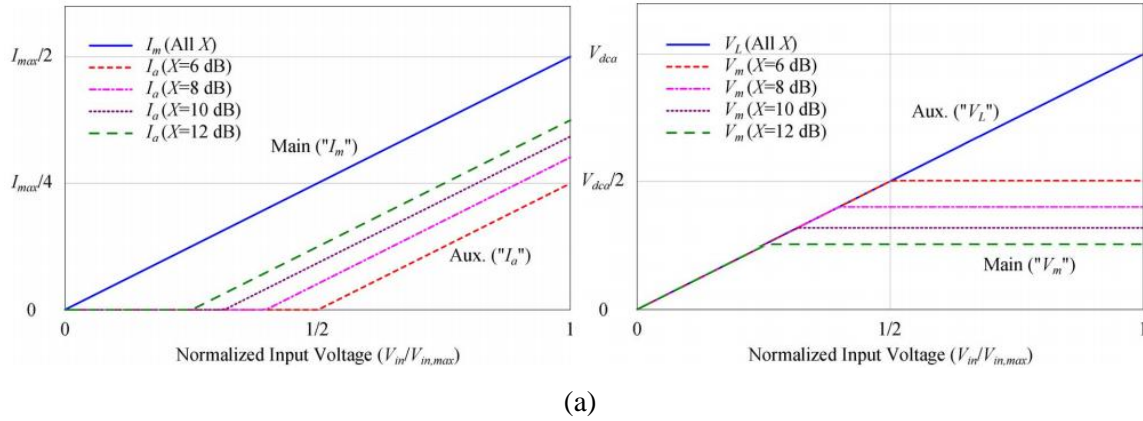
Figure 2-19, (a) Optimal Auxiliary Drain Current and Main Drain Bias Values for Different PAPR Values, (b) Circuit Schematic and Demonstrator, and (c) Efficiency Enhancement Measurement Results [42]

2.3 Transistor Technology

As the market for cellular, personal communications services, and broadband access is expanding, and fourth-generation (4G) standards are becoming closer to reality, high power RF PAs are beginning to be the focus of attention. A variety of PA technologies are in the market now, such as, bipolar devices, GaAs metal-semiconductor field-effect transistors (MESFETs) [43], [44], GaAs heterojunction bipolar transistors (HBTs) [45], [46], [47], SiC MESFETs [48], [49] LDMOS technology [50], [51], [52], [53], [54], [55], [56], [57], [58], and GaN high-electron mobility transistors (HEMTs). The latter technology [59] is an attractive candidate for high power handling applications. The high power at high frequency capacity is the biggest advantage of GaN HEMT over LDMOS technology. Excellent high frequency (f_t =110 GHz for a 0.15 μm gate length [60]) and high power density (30 W/mm at 10 GHz [61]) have been demonstrated. The wide bandgap feature allows high breakdown voltage (typically > 100 V) and the higher amount of charge provides high current (1-1.4 A/mm for GaN HEMT compared to 150 mA/mm for LDMOS).

The competitive advantages of GaN devices and amplifiers for commercial products are described in Table 2-1. In every single category, GaN devices excel over conventional technology. The last column summarizes the resulting performance advantages at the system level for the customer. The high power per unit width translates into smaller devices that are not only easier to fabricate, but offer much higher impedance as well. This makes the GaN-based devices much easier to match to the system. The task of matching is often a complex one with conventional devices (e.g., GaAs and LDMOS devices have three to five times lower optimum impedances than those of GaN devices).

Table 2-1, Competitive Advantages of GaN Devices

Need from a new Technology	Enabling feature of GaN Technology	Performance Advantage
High Power Handling/ unit width	Wide band gap (3.4 eV), High breakdown field	Compact, therefore; easier for matching

High Voltage Operation	High breakdown field	Reducing need for high current
High Frequency	High electron velocity	Fast operation speed
High Efficiency	High operating voltage	Reducing cooling due to low current
Low SNR	High power gain	High dynamic range
Thermal Management	SiC substrates	Reducing cooling needs

Research attempts have targeted integrated high efficiency broadband and multi-mode PAs, among them DPAs, for wireless communications using the existing GaN monolithic microwave integrated circuit (MMIC) technology [62], [63], [64], [65], [66], [67], [68]. As an example, a monolithically integrated class J PA was fabricated [65] using the Canadian Photonic Fabrication Centre® (CPFC) GaN800, 0.8um gate length MMIC process offered by the National Research Council (NRC) of Canada. Complete load/source-pull simulations for the selected device and the required fundamental and second harmonic terminations were conducted to obtain the required terminations over frequency band 2.25-3.05 GHz. The targeted output power was 0.5 W, and the transistor was biased at 15 V. Figure 2-20a shows a photograph of the fabricated MMIC PA. The amplifier achieved more than 50% drain efficiency and 23 dBm over the whole band (Figure 2-20b).
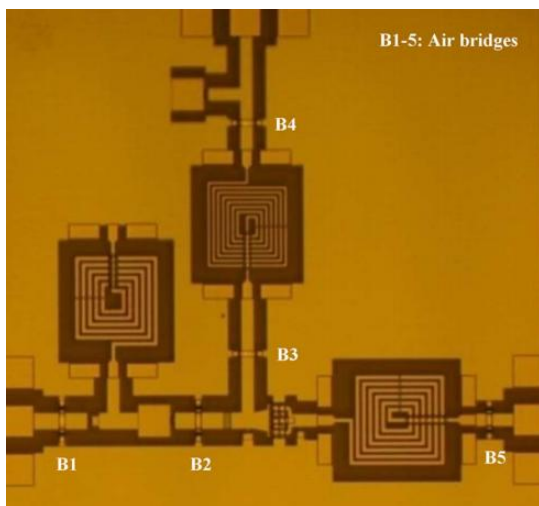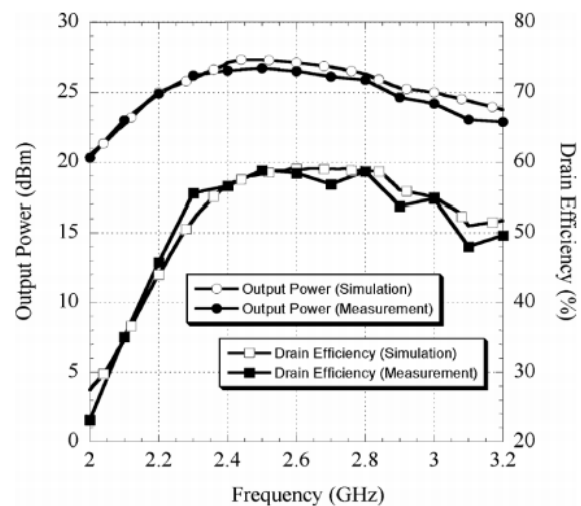
(a)   (b)

Figure 2-20, CPFC® GaN MMIC Fabricated Class J PA (a) Photo, (b) CW Measured Output Power and Efficiency [65]

2.4 Discussion

In the previous literature survey, research initiatives targeting the efficiency enhancement of PAs for different operating conditions, including wide spread centre frequencies and extended peak-to-average power ratios were presented. Broadband and multi-band as well as reconfigurable matching networks were aimed at introducing optimal device terminations under different deployment scenarios. However, both solutions only solve the performance preservation versus either the power level or frequency. Moreover, the optimization nature of broadband/multi-band designs result in performance figures that cannot compete with their single frequency counterparts.

Doherty technique, using active load modulation, is used for PA efficiency enhancement at reduced power levels but, at the same time, suffers from narrow band limitation. Intensive efforts were exercised in the design of broadband and multi-band DPAs which extended the power back-off efficiency enhancement range. Reconfigurable, in other words frequency agile, DPAs are interesting candidates to manage all the variations in operating situations. As previously presented from the literature, tuning the drain bias for the main transistor can target multiple centre frequencies and PAPRs. However, this approach is not able to handle wideband signals due to the slow speed of the DC-DC converter. In our work we focus on designing electronically tunable matching networks for DPAs which maintain competitive performance at different frequencies, different PAPR values and different peak power levels.

In Chapter 4, a complete, systematic design approach to the design of high efficiency DPAs capable of efficiently amplifying signals with dissimilar PAPR centered around wide spread operating frequencies, using electronically tunable matching networks, is introduced. The design approach is then modified, in Chapter 5, to realize a DPA capable of handling incoming signals with variable peak and average power levels depending on dynamic networks loads. Knowing the attributes of candidate realizations of electronically tunable devices, MEMS devices [69], [70], [71], [72], [73] are considered to modulate the load seen by the transistor as a function of the incoming signal centre frequency and PAPR.

In Chapter 6, we present a detailed design and fabrication of high power RF MEMS switches on the CPFC® GaN500 0.5 um gate length MMIC process as a first step towards the design of a fully integrated, electronically tunable DPA for multi-standard operation. Afterwards, the strengths of the GaN transistor and the flexibility of MEMS devices are combined to build a high efficiency frequency agile, monolithically integrated DPA.

Chapter 3

Electronically Tunable Inverse Class F Power Amplifier for Multi-Frequency Multi-Mode Base Stations

3.1 Introduction

Evolution of wireless communications has resulted in a broad spectrum of standards. These multiple standards are expected to co-exist, and dynamic management of wireless networks becomes an essential attribute. This calls for an important shift from dedicated, single operating condition wireless systems to adaptive systems capable of handling dissimilar signal requirements (e.g., centre frequency, signal peak average power ratio (PAPR), bandwidth, and modulation scheme).

In the following sections we propose a novel harmonically tuned reconfigurable class F^{-1} power amplifier (PA) which achieves high efficiency enhancement at input power levels and widely spread centre frequencies. This is accomplished by using a reconfigurable matching network (MN) that utilizes the optimal fundamental terminations at the given power level and frequency settings, as well as tuning the impedances of the second and third harmonic frequencies for appropriate operation of high efficiency PAs (HEPAs).

3.2 Harmonically-Tuned Reconfigurable Class F^{-1} Power Amplifier

3.2.1 Theory and Design of Tunable Matching Network

The design of HEPAs requires proper fundamental and harmonic terminations in order to obtain appropriate current and voltage waveforms. This design targets the design of a reconfigurable MN that should enable fundamental and harmonic tuning as well as maximizing the tuning range (Figure 3-1).

The proposed fundamental/harmonically tunable MN is composed of two main blocks, second and third harmonic tuning, and fundamental matching blocks. First, the desired values for harmonic impedances are set by adjusting the capacitance value. Then, the fundamental impedance is matched in two steps to maximize the tuning range. The load impedance is first set to a certain predetermined impedance region in the Smith Chart using a pi-matching pre-matching network with two variable capacitors and a transmission line (TL). Then, a TL loaded with four variable capacitors is used to obtain the final value of desired impedance.
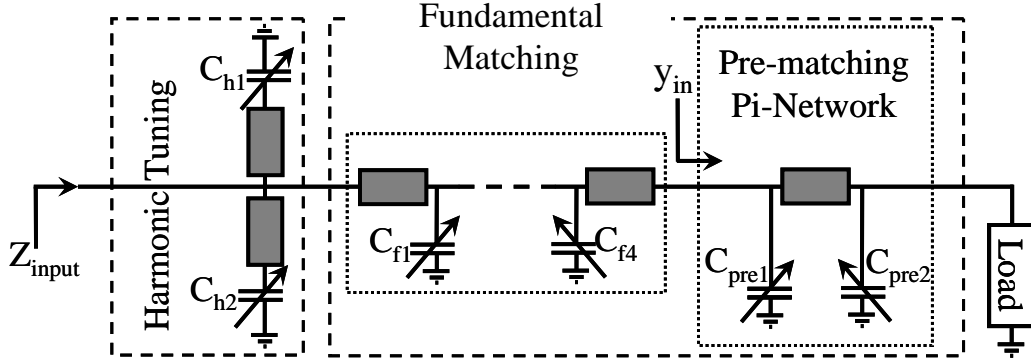
Figure 3-1, Proposed Design For the Harmonically-Tuned Matching Network

3.2.1.1 Harmonic Impedance Tuning

HEPAs require optimum harmonic impedance to be either open or short circuited. This fact leads to the design of two-state matching which makes the impedance short or open. Practically speaking, packaging the transistor can change the overall phase of the required impedances. Consequently, the complete harmonic MN should reflect the harmonic impedance and have a unity reflection coefficient with tunable phase shift.

The basic idea is to achieve tunable pure imaginary input impedance in a shunt TL terminated with a variable capacitor. Choosing the appropriate characteristic impedance Z_0, and the electrical length θ, for the shunt TL should achieve the desired tuning in the input impedance for a given varactor tuning range. For a 2.5 GHz design, two parallel stubs were used to achieve an extra degree of freedom in the design for wider tuning range at the edge of the Smith Chart. The susceptance of the parallel connection is as follows:

$$B_{in} = \frac{Z_{01} + X_{ch1}\alpha_1}{Z_{01}X_{ch1} + Z_{01}^2\alpha_1} + \frac{Z_{02} + X_{ch2}\alpha_2}{Z_{02}X_{ch2} + Z_{02}^2\alpha_2} \tag{3-1}$$

where $\alpha_n = tan\ (2\theta_n)$ is the second harmonic and $\alpha_n = tan\ (3\theta_n)$ is the third harmonic.

In this design, the varactor value was chosen arbitrarily to vary from 0.5 pF to 1.5 pF. Thus, the impedance spans for X_{ch1} and X_{ch2} are from 21 to 63 Ω at 5 GHz and from 14 to 42 Ω at 7.5 GHz. In order to maximize the coverage of the Smith Chart outer circle, the variance of B_{in} given by (3-1) needed to be maximized at both the second and third harmonic frequencies simultaneously. The optimum values obtained for this objective were 20 and 25 Ω for Z_{01} and Z_{02}, while the electrical lengths of the two stubs were set to 10 and 105° respectively.

To extend the harmonic tuning to the point of being frequency agile, three parallel stubs were used instead. The corresponding optimum values of Z_{01}, Z_{02}, and Z_{03}, were set to be 55, 30 and 25 Ω and the electrical length of the three stubs was set to 15, 125 and 20° respectively at 1.9 GHz.

The first estimate of the TL's optimal parameters was obtained by a MATLAB[®] code which maximized the variance of B_{in}, while the exact values were finalized using the tuning feature in Agilent ADS[®].

3.2.1.2 Fundamental Impedance Matching

In order to extend the fundamental impedance tuning range inside Smith Chart coverage, the pre-matching concept was used. A C-L-C pi-network was selected for this purpose. Low Q-factor inductors were avoided by replacing them with an equivalent TL. In (3-2) and (3-3) b_{pre1}, b_{pre2} and x designate the susceptance of the capacitance and the reactance of the inductor. The equations to design the circuit to achieve the desired input admittance, y_{in}, in Figure 4-1, are given by

$$\sqrt{\frac{1+b_{h1}{}^2 - g_{in}}{g_{in}}} = xb_{h1}{}^2 - b_{h1} + x \tag{3-2}$$

$$b_{h2} = b_{in} + \frac{(1+b_{h1}{}^2)(xb_{h1}{}^2 - b_{h1} + x)}{1 + (xb_{h1}{}^2 - b_{h1} + x)} \tag{3-3}$$

The value of x was chosen to be 0.5. Six different sets of (b_{pre1}, b_{pre2}), called 'states', were chosen to divide the Smith Chart into 6 pre-determined regions (Figure 3-2). The values of (b_{pre1}, b_{pre2}) of the 6 states depend on the targeted frequency. Table 3-1 presents the calculated values for the pre-matching capacitors and the corresponding average reflection coefficient for each state for the 2.5 GHz design.

For the frequency agile design, the impedance values were calculated at 1.9 GHz. The only modification was found to be varying the value of C_{pre2} for 'State 1' only to select the operating frequency and covering 'State 1' for every frequency. For 1.8, 1.9, and 2.1 GHz, the optimal C_{pre2} was 7.5, 6.5, and 4.5 pF respectively, whereas for 2.4, and 2.7 GHz, C_{pre2} is 3.5 pF.

Table 3-1, 2.5 GHz Design Pre-matching Capacitor Values for Different States

	C_{pre2} (pF)	C_{pre1} (pF)	Reflection Coefficient (Γ)
State 1	6.5	3.5	(0.5,10°)
State 2	1.75	1.25	(0.5,190°)
State 3	4	0.5	(0.8,10°)
State 4	10	3	(0.8,190°)
State 5	16	4	(0.95,-60°)
State 6	16	2	(0.95,120°)
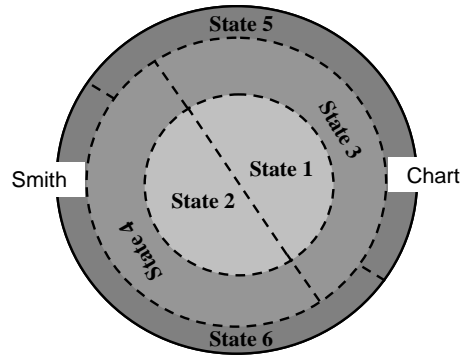
Figure 3-2, Smith Chart Regions Covered by Each State

For the remaining part of the fundamental MN, we used a capacitively loaded TL with a total of four varactors that varied from 0.5 to 1.5 pF. The lengths of the TL sections between the shunt varactors were optimized using tuning in Agilent ADS®.

It is worth mentioning here that we avoided any tunable devices in the main signal line so as to not limit the power handling capabilities of networks to those of tunable devices. This assumption was strengthened by running a harmonic balance simulation for the final fundamental MN design in Agilent ADS® with an input power level of 40 dBm. The maximum power level at any shunt tunable element was found not to exceed 1.6 W which is within the safe power handling capabilities for the discrete matching components used. Consequently, the condition of the power handling capabilities for tunable devices has been highly relaxed and at the same time the total power handling of the whole network is no longer sensitive to that of the tunable devices.

3.2.2 Fabrication and Measurement Results

Both MN prototypes were fabricated using a microwave integrated circuit (MIC) process fabricated at the University of Waterloo in the Centre for Integrated RF Engineering (CIRFE) lab with via-holes [74]. The substrate used was alumina substrate with 25 mils thickness, relative permittivity of 9.8, and loss tangent of 0.001 at 1 MHz. The conductor layer was a 4 μm electroplated Au layer on top of a 50nm/0.1 μm evaporated Cr/Au seed layer. The sputtered gold was found to be sufficient to plate the via-holes with Au. Figure 3-3 presents the complete fabricated circuits using both Radant MEMS® SP4T switches and Skyworks® semiconductor varactors.
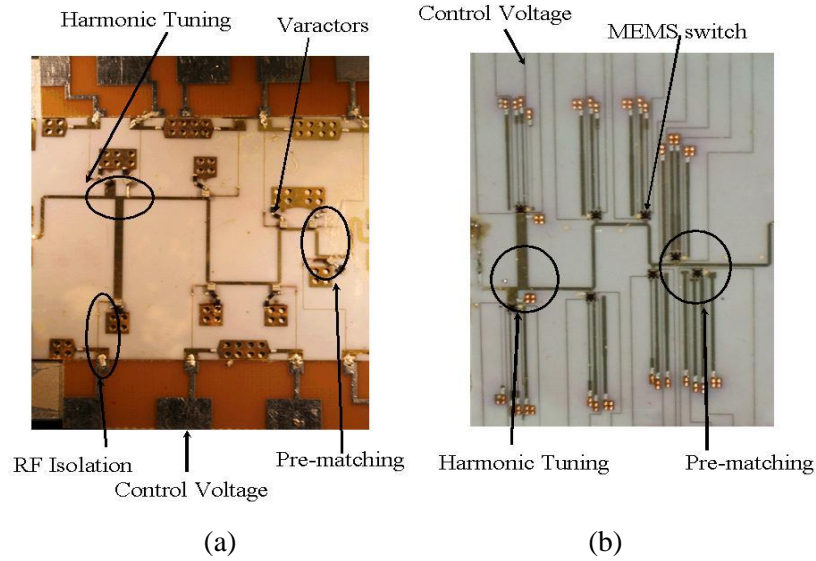
Figure 3-3, Fabricated (a) Varactor-Based Frequency Agile, (b) MEMS-based 2.5 GHz Matching Network

For the MEMS-based design, excellent impedance coverage was achieved at the fundamental frequency (Figure 3-4). It allowed for a maximum |Γ| of 0.834 with corresponding insertion loss of less than 1.213 dB (Figure 3-5). Moreover, almost all the rim of the Smith Chart was covered at the second and third harmonics (Figure 3-6) except for the impedance near the open circuit where fundamental matching part affected the performance. Similar results were obtained for the varactor- based design (Figure 3-6, and Figure 3-7) with satisfactory coverage for all targeted frequencies except 2.7 GHz as it was far away from the design frequency, 1.9 GHz. The maximum covered reflection coefficient was higher than 0.85 except at 2.7 GHz. The measured insertion loss did not exceed 1.4 dB at the highest covered |Γ| (Figure 3-8).
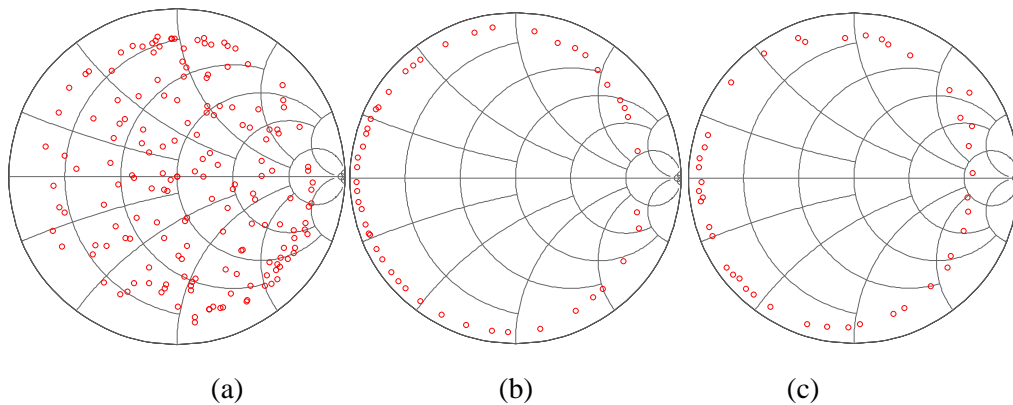
Figure 3-4, Selected Measured Impedance States to Prove Coverage for 2.5 GHz Design; (a) Fundamental 2.5 GHz, (b) Second Harmonic 5 GHz, (c) Third Harmonic 7.5 GHz

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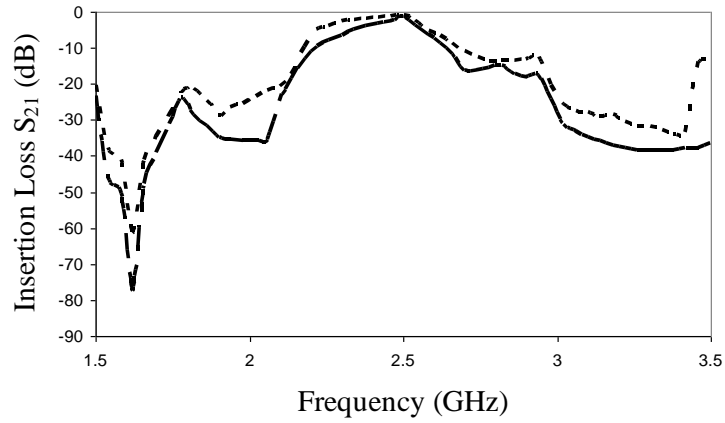
Figure 3-5, Measured IL =-1.213 dB for 2.5 GHz Design at Maximum |Γ| of 0.834

(a)   (b)   (c)

(d)   (e)
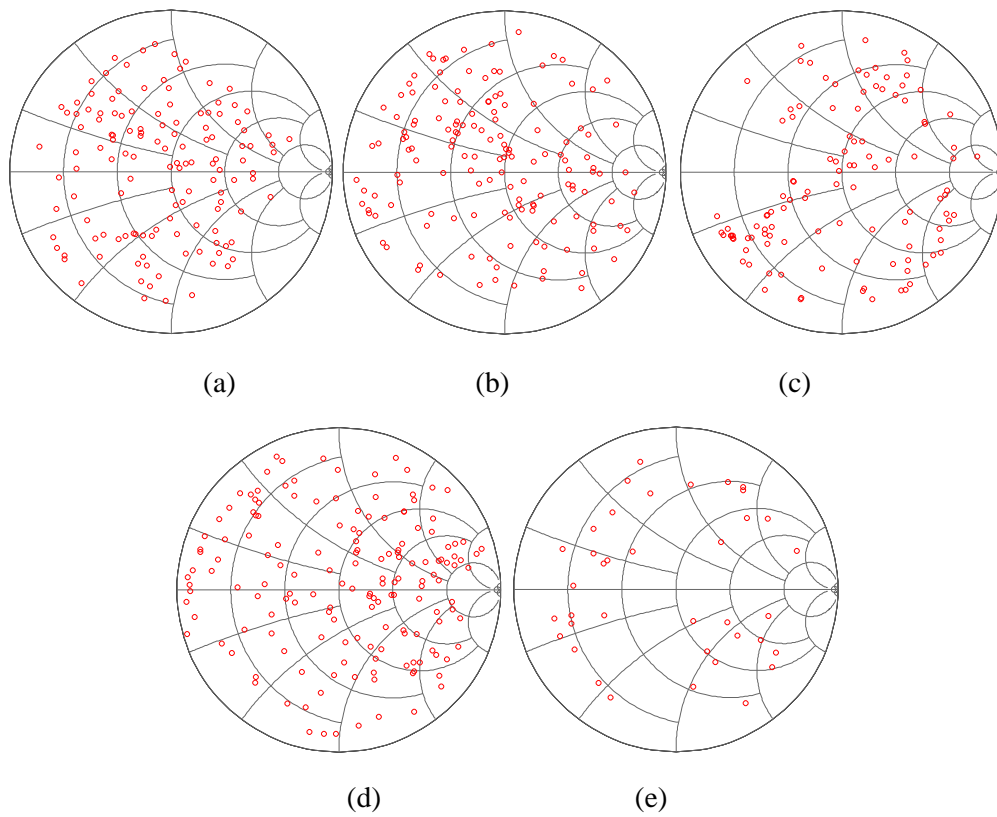
Figure 3-6, Selected Measured Impedance States to Prove Fundamental Impedance Coverage for Frequency Agile Design; (a) 1.8 GHz, (b) 1.9 GHz, (c) 2.1 GHz, (d) 2.4 GHz, and (e) 2.7 GHz

(a)   (b)   (c)
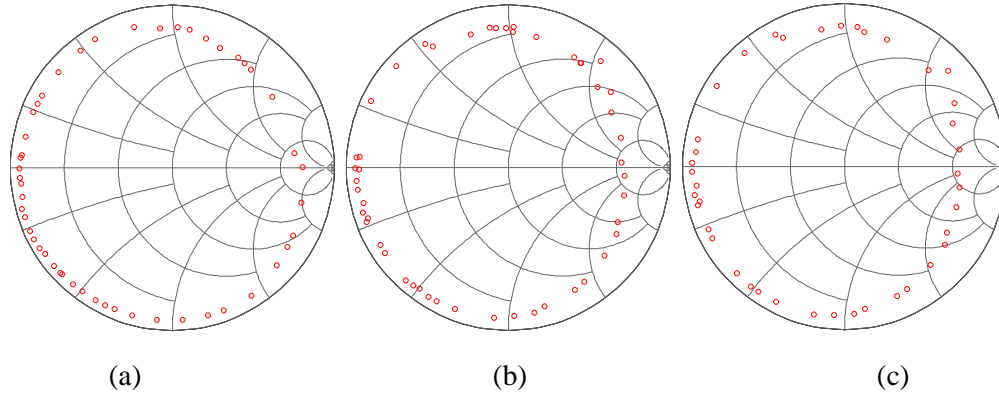
Figure 3-7, Examples for Measured Harmonic Tuning for Frequency Agile Design; (a) 3.8 GHz, (b) 4.8 GHz, and (c) 5.4 GHz

(a)   (b)

(c)   (d)
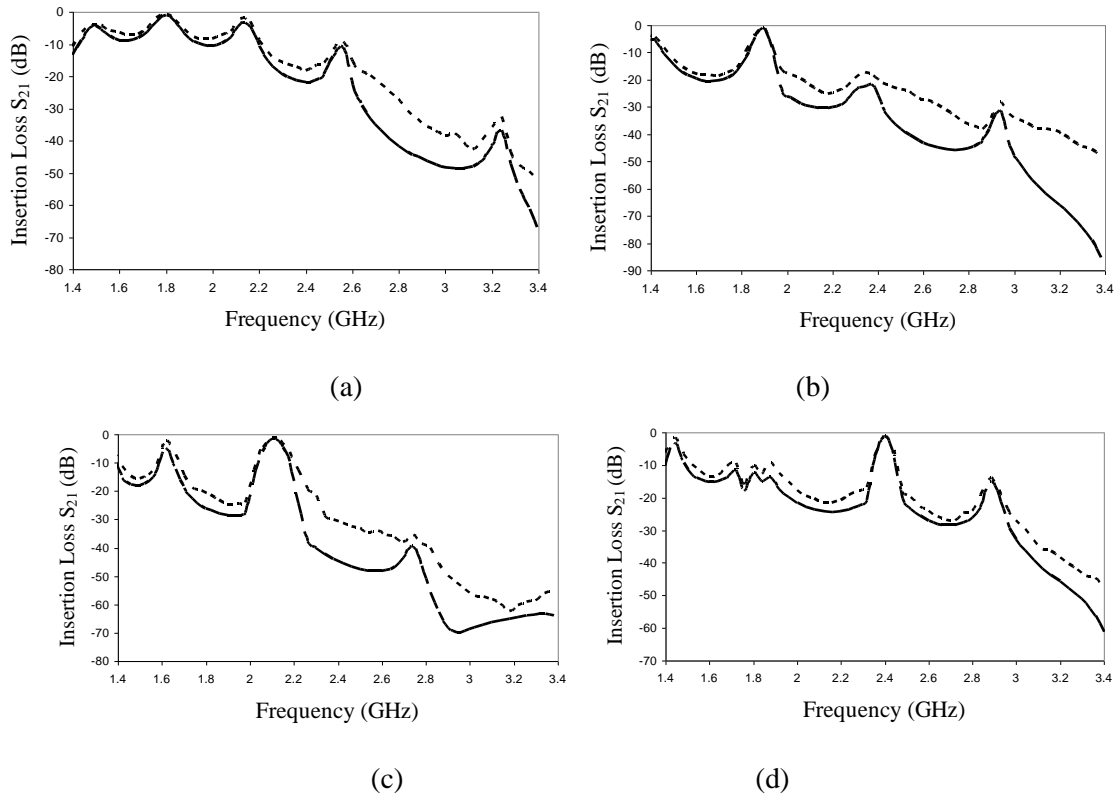
Figure 3-8, Measured Insertion Loss of (a) -1.121 dB at $|\Gamma|$ of 0.862 for 1.8 GHz, (b) -1.313 dB at $|\Gamma|$ of 0.868 for 1.9 GHz, (c) -1.38 dB at $|\Gamma|$ of 0.853 for 2.1 GHz, and (d) -1.328 dB at $|\Gamma|$ of 0.876 for 2.4 GHz

3.2.3 Load Modulated Varactor-Based Frequency Agile Class F^{-1} HEPA

The first step towards a harmonically-tuned tunable PA was using the fabricated varactor-based MN as an output MN for the PA with a fixed input MN operating at 2.4 GHz, for proof of concept purposes. For the fabricated PA, at 6 dB back-off, the drain efficiency was improved by

18% compared with what was obtained using a static MN optimized only at the peak input power level. The varactor-based frequency agile MN is subsequently used for the source and load modulation of a class F^{-1} HEPA. Two tunable MN were fabricated for source and load impedance tuning. The active device used was the 10 W GaN device from Cree®, CGH40010F. Figure 3-9 shows a photo of the fabricated reconfigurable class F^{-1} PA for efficiency enhancement. The PA was measured by manual tuning of the fundamental and harmonic impedances of the MN simultaneously at every input power level at the operating frequencies.

Table 3-2 summarizes the obtained drain efficiency, and the efficiency enhancement at various frequencies. Moreover, Figure 3-10 shows efficiency curves vs. input power levels.
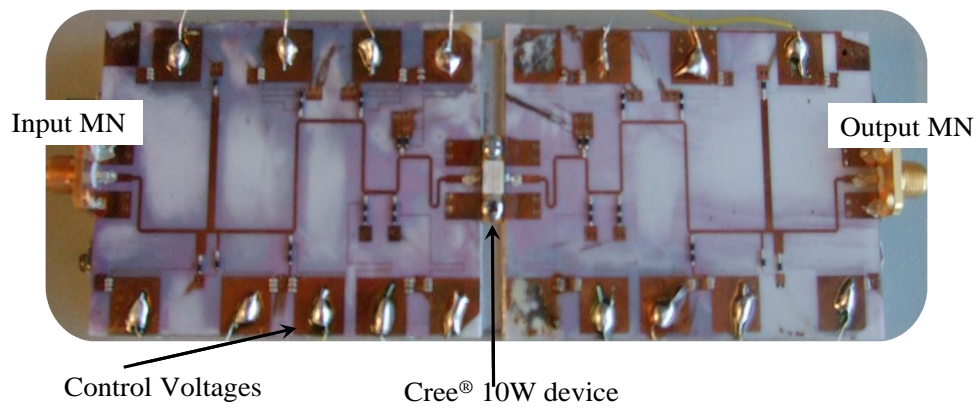
Figure 3-9, Fabricated Harmonically-Tuned Reconfigurable Power Amplifier

Table 3-2, Peak Efficiency and Efficiency Enhancement for the Harmonically-Tuned Reconfigurable Power Amplifier at Different Frequencies

Frequency of Operation	Drain Efficiency at Peak Input Power (%)	Efficiency Enhancement at 6 dB back-off (%)	Efficiency Enhancement at 10 dB back-off (%)
1.8 GHz	70.55	12.73	6.1
1.9 GHz	68.72	12.29	7.71
2.1 GHz	65.21	10.23	5.145
2.4 GHz	72.05	14.97	10.18
2.7 GHz	63.54	8.03	4

(a)

(b)

(b)

(d)

(e)
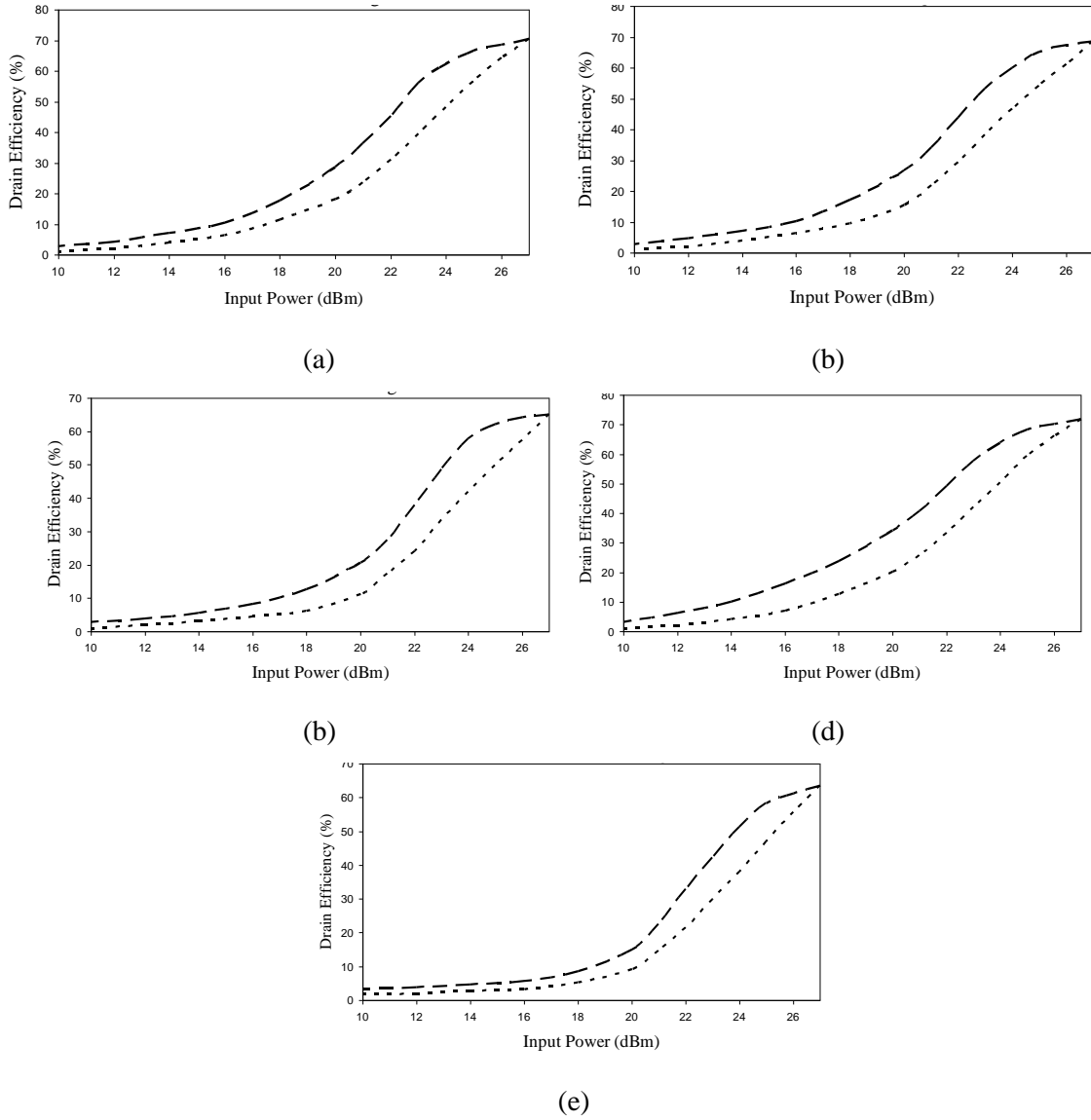
Figure 3-10, Efficiency vs. Input Power at (a) 1.8 GHz with 12.73% Enhancement at 6 dB Back-off, (b) 1.9 GHz with 12.29% Enhancement at 6 dB Back-off, (c) 2.1 GHz with 10.23% Enhancement at 6 dB Back-off, (d) 2.4 GHz with 14.97% Enhancement at 6 dB Back-off, and (e) 2.7 GHz with 8.3% Enhancement at 6 dB Back-off

Chapter 4

Reconfigurable Doherty Power Amplifiers for Multi-Band Multi-Mode Base Stations

4.1 Introduction

In this chapter, a complete systematic procedure for the design of high efficiency Doherty power amplifiers (DPAs), able to efficiently amplify signals with different peak to average power ratios (PAPR) centered around diverse operating frequencies, is outlined. This procedure was applied to design three different demonstrators that operated under different conditions: three different frequency bands and a single PAPR value, three PAPR values centered around the same frequency, and three simultaneous centre frequencies and three PAPR values.

4.2 Novel Reconfigurable Multi-Standard Multi-Frequency Reconfigurable Doherty Power Amplifier

Following the analysis for the DPA in Chapter 2, eq. 2-4 shows the deviation of the main impedance profile, compulsory for proper load modulation, while changing the frequency (θ) and peak to average power ratio (PAPR; p). To mitigate the effects of the frequency and PAPR variation in a conventional Doherty amplifier, a new reconfigurable Doherty architecture is proposed. This new architecture includes two reconfigurable output compensation networks (OCN) that are added in the main and auxiliary paths of the Doherty architecture in addition to the reconfigurable input and output matching networks (IMN, OMN). The reconfigurable OCNs are carefully designed to:

- Eliminate the deviation of the impedance profiles from the ideal profiles implied by the frequency variation as shown before (Figure 2-11) and
- Adjust the impedance profiles as the value of *p* varies.

The reconfigurable IMN and OMN are designed to:

- Attain the optimal source and load impedances needed to be seen by the transistors at different drive levels and operating frequencies and
- Compensate for the transistors' parasitics at different operating conditions.

The design of the two compensation networks was conducted using the following procedure where a set closed form equations serves to make it systematic. These equations allow the determination of the ABCD parameters of the compensation networks given the values of the frequency (represented by θ), and the input signal PAPR (represented by *p*). It is worth

mentioning that the impedance inverters are kept unchanged vs. frequency and *p*.

4.2.1 Multi-Standard Multi-Frequency Doherty Power Amplifier Synthesis

Figure 4-1 portrays the proposed reconfigurable multi-standard multi-frequency DPA where the tunability is achieved by variable capacitors shunt loading from the matching network distributed elements. The synthesis of the reconfigurable Doherty amplifier is carried out in two steps. First the ABCD parameters of the OCN in the main path are determined by analyzing the resulting circuit at low power levels (auxiliary amplifier is OFF). Then, the knowledge of the OCN$_{main}$ is exploited to determine the ABCD parameters of the auxiliary path's OCN. In both cases we used the ideal ABCD parameters needed to satisfy the conditions for proper load modulation as goals.
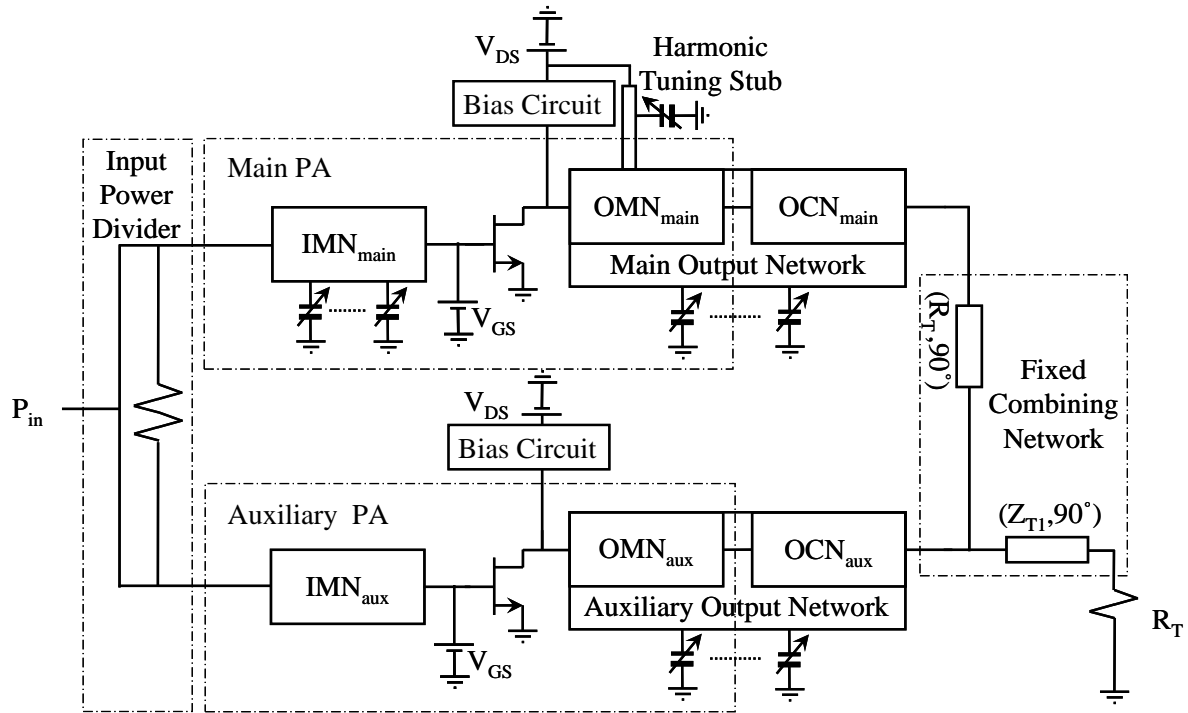
Figure 4-1, Generalized Multi-Standard Multi-Frequency Doherty Block Diagram

4.2.1.1 Low Power Compensation
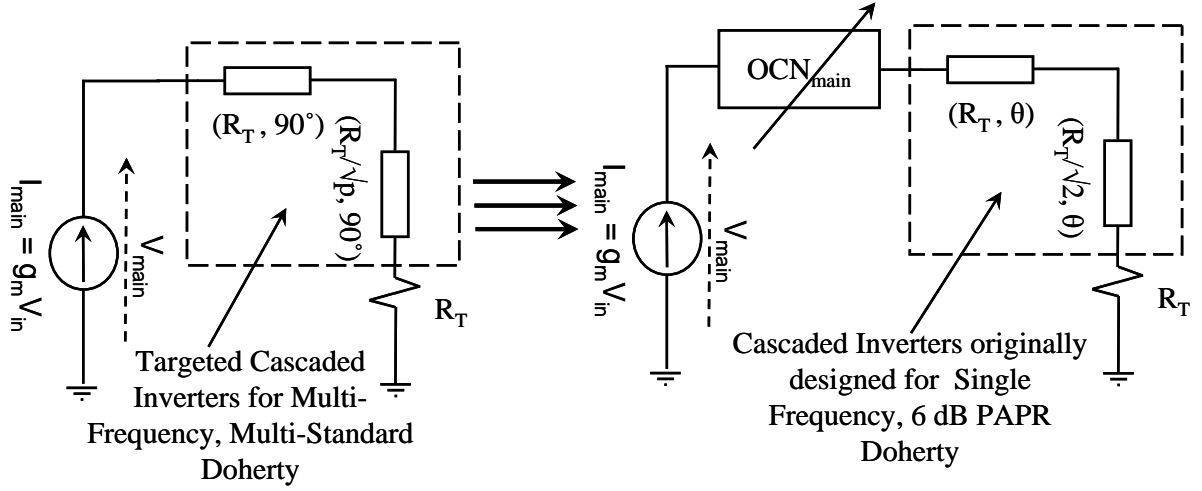
Figure 4-2, Equivalent Circuits of the Conventional and Proposed Doherty Amplifiers at Low Power Levels Compensation

Based on Figure 4-2, a number of expressions were derived to deduce the ABCD parameters of the required OCNs.

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Frequency Dependent Cascaded Inverters} = \begin{bmatrix} \cos\theta & jR_T\sin\theta \\ \dfrac{-1}{jR_T}\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} \cos\theta & jZ_{T1}\sin\theta \\ \dfrac{-1}{jZ_{T1}}\sin\theta & \cos\theta \end{bmatrix}
$$

$$
= \begin{bmatrix} \cos^2\theta - \dfrac{R_T}{Z_{T1}}\sin^2\theta & j(R_T+Z_{T1})\sin\theta\cos\theta \\ j(\dfrac{1}{R_T}+\dfrac{1}{Z_{T1}})\sin\theta\cos\theta & \cos^2\theta - \dfrac{Z_{T1}}{R_T}\sin^2\theta \end{bmatrix}
$$

(4-1)

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Targeted\ Cascaded\ Inverters} = \begin{bmatrix} -\dfrac{R_T}{Z_{T1}} & 0 \\ 0 & -\dfrac{Z_{T1}}{R_T} \end{bmatrix} = \begin{bmatrix} -\sqrt{p} & 0 \\ 0 & -\dfrac{1}{\sqrt{p}} \end{bmatrix}\begin{bmatrix} -\dfrac{R_T}{\sqrt{p}Z_{T1}} & 0 \\ 0 & -\dfrac{\sqrt{p}Z_{T1}}{R_T} \end{bmatrix}
$$

(4-2)

To maintain proper load modulation, the ABCD matrix of the cascade composed on the impedance inverters should be kept equal to the ideal inverters' ABCD matrix.

$$
\begin{bmatrix} -\sqrt{p} & 0 \\ 0 & -\dfrac{1}{\sqrt{p}} \end{bmatrix}\begin{bmatrix} -\dfrac{R_T}{\sqrt{p}Z_{T1}} & 0 \\ 0 & -\dfrac{\sqrt{p}Z_{T1}}{R_T} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{main}}\begin{bmatrix} \cos^2\theta - \dfrac{R_T}{Z_{T1}}\sin^2\theta & j(R_T+Z_{T1})\sin\theta\cos\theta \\ j(\dfrac{1}{R_T}+\dfrac{1}{Z_{T1}})\sin\theta\cos\theta & \cos^2\theta - \dfrac{Z_{T1}}{R_T}\sin^2\theta \end{bmatrix}
$$

(4-3)

$$\begin{bmatrix} -\sqrt{p} & 0 \\ 0 & -\dfrac{1}{\sqrt{p}} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{main}} \begin{bmatrix} \cos^2\theta - \dfrac{R_T}{Z_{T1}}\sin^2\theta & j(R_T + Z_{T1})\sin\theta\cos\theta \\ j(\dfrac{1}{R_T} + \dfrac{1}{Z_{T1}})\sin\theta\cos\theta & \cos^2\theta - \dfrac{Z_{T1}}{R_T}\sin^2\theta \end{bmatrix} \begin{bmatrix} -\dfrac{\sqrt{p}Z_{T1}}{R_T} & 0 \\ 0 & -\dfrac{R_T}{\sqrt{p}Z_{T1}} \end{bmatrix} \quad (4\text{-}4)$$

$$\begin{bmatrix} -\sqrt{p} & 0 \\ 0 & -\dfrac{1}{\sqrt{p}} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{main}} \begin{bmatrix} \cos^2\theta - \sqrt{2}\sin^2\theta & jR_T(1+\dfrac{1}{\sqrt{2}})\sin\theta\cos\theta \\ j\dfrac{1}{R_T}(1+\sqrt{2})\sin\theta\cos\theta & \cos^2\theta - \dfrac{1}{\sqrt{2}}\sin^2\theta \end{bmatrix} \begin{bmatrix} -\sqrt{\dfrac{p}{2}} & 0 \\ 0 & -\sqrt{\dfrac{2}{p}} \end{bmatrix} \quad (4\text{-}5)$$

Equation 4-5 is later used to determine the ABCD parameters of the OCN_{main}, given the target frequency and signal PAPR, which serve as the basis for the realization of the corresponding circuit.

4.2.1.2 High Power Compensation
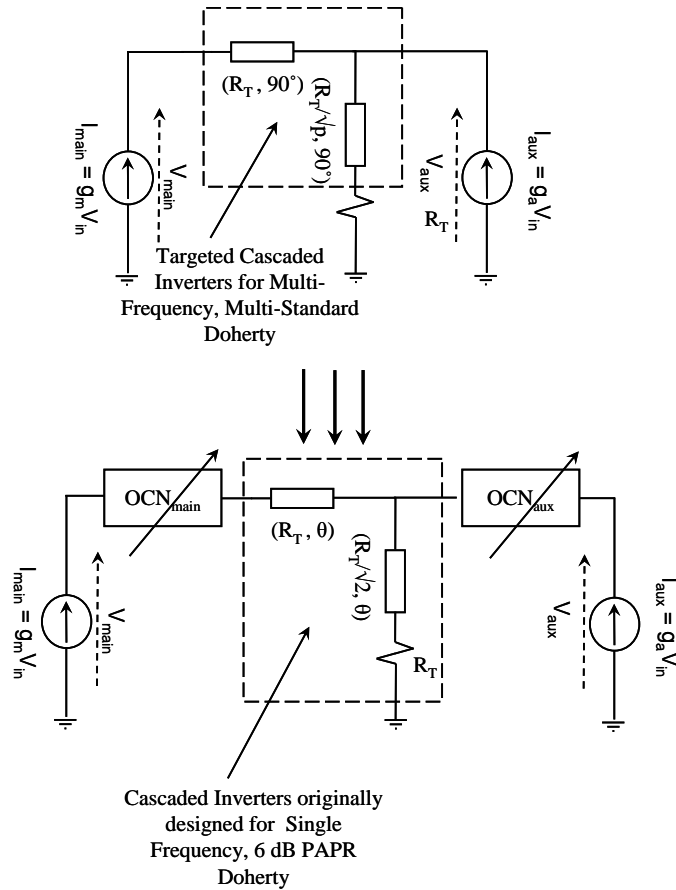
Figure 4-3, Equivalent Circuits of the Conventional and Proposed Doherty Amplifiers at High Power Levels Compensation

Figure 4-3 shows the equivalent circuit of the proposed Doherty amplifier that was used to extract the ABCD parameters of the OCN_{aux}. The following two equations provided the expressions of the ABCD parameters of the inverters as function of the frequency and PAPR as well as those for ideal inverters.

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Frequency\ Dependent\ Combining\ Network} = \begin{bmatrix} \cos\theta & jR_T \sin\theta \\ \dfrac{-1}{jR_T}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{1}{Z_{T1}}\dfrac{Z_{T1}\cos\theta + jR_T\sin\theta}{R_T\cos\theta + jZ_{T1}\sin\theta} & 1 \end{bmatrix}
$$

$$
= \begin{bmatrix} \dfrac{\cos^2\theta - \dfrac{R_T}{Z_{T1}}\sin^2\theta + j(1+\dfrac{Z_{T1}}{R_T})\sin\theta\cos\theta}{\cos\theta + j\dfrac{Z_{T1}}{R_T}\sin\theta} & jR_T\sin\theta \\ \dfrac{1}{R_T}\dfrac{\cos^2\theta - \dfrac{Z_{T1}}{R_T}\sin^2\theta + j(1+\dfrac{R_T}{Z_{T1}})\sin\theta\cos\theta}{\cos\theta + j\dfrac{Z_{T1}}{R_T}\sin\theta} & \cos\theta \end{bmatrix}
\tag{4-6}
$$

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Targeted\ Combining\ Network} = \begin{bmatrix} j(\dfrac{R_T}{Z_{T1}})^2 & jR_T \\ \dfrac{j}{R_T} & 0 \end{bmatrix}
\tag{4-7}
$$

Rewriting Equation 4-6 yields the following expression

$$
\begin{bmatrix} j(\dfrac{R_T}{Z_{T1}})^2 & jR_T \\ \dfrac{j}{R_T} & 0 \end{bmatrix} = \begin{bmatrix} jp & jR_T \\ \dfrac{j}{R_T} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{R_T}{Z_{T1}^2} - \dfrac{p}{R_T} & 1 \end{bmatrix}
\tag{4-8}
$$

Equating Equations 4-6 and 4-8 yields the following expression that must be satisfied for different carrier frequencies and signals' PAPR to maintain high efficiency.

$$
\begin{bmatrix} jp & jR_T \\ \dfrac{j}{R_T} & 0 \end{bmatrix} =
$$

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{main}} \begin{bmatrix} \dfrac{\cos^2\theta - \dfrac{R_T}{Z_{T1}}\sin^2\theta + j(1+\dfrac{Z_{T1}}{R_T})\sin\theta\cos\theta}{\cos\theta + j\dfrac{Z_{T1}}{R_T}\sin\theta} & jR_T\sin\theta \\ \dfrac{1}{R_T}\dfrac{\cos^2\theta - \dfrac{Z_{T1}}{R_T}\sin^2\theta + j(1+\dfrac{R_T}{Z_{T1}})\sin\theta\cos\theta}{\cos\theta + j\dfrac{Z_{T1}}{R_T}\sin\theta} & \cos\theta \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{aux}} \begin{bmatrix} 1 & 0 \\ \dfrac{p}{R_T} - \dfrac{R_T}{Z_{T1}^2} & 1 \end{bmatrix}
\tag{4-9}
$$

where $\begin{bmatrix} 1 & 0 \\ \dfrac{R_T}{Z_{T1}{}^2} - \dfrac{p}{R_T} & 1 \end{bmatrix}^{-1} = \begin{bmatrix} 1 & 0 \\ \dfrac{p}{R_T} - \dfrac{R_T}{Z_{T1}{}^2} & 1 \end{bmatrix}$

Equation 4-9 can be rewritten as follows and allows for the determination of the ABCD parameters of the OCN_{aux} given the frequency, the value of p and the ABCD parameters of the OCN_{main}.

$$\begin{bmatrix} jp & jR_T \\ \dfrac{j}{R_T} & 0 \end{bmatrix} = $$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{main}} \begin{bmatrix} \dfrac{\cos^2\theta - \sqrt{2}\sin^2\theta + j(1+\dfrac{1}{\sqrt{2}})\sin\theta\cos\theta}{\cos\theta + j\dfrac{1}{\sqrt{2}}\sin\theta} & jR_T\sin\theta \\ \dfrac{1}{R_T}\dfrac{\cos^2\theta - \dfrac{1}{\sqrt{2}}\sin^2\theta + j(1+\sqrt{2})\sin\theta\cos\theta}{\cos\theta + j\dfrac{1}{\sqrt{2}}\sin\theta} & \cos\theta \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{OCN_{aux}} \begin{bmatrix} 1 & 0 \\ \dfrac{p-2}{R_T} & 1 \end{bmatrix}$$

(4-10)

In conclusion, Equations 4-5 and 4-10 are closed form equations for designing the compensation network parameters of both OCNs which maintain proper load modulation given the operating frequencies (θ) and the desired PAPR value (p) to ensure effective multi-standard and multi-frequency DPA operation.

The circuit realization for the reconfigurable matching networks starts with choosing the cascaded transmission line sections topology to reduce the matching network frequency sensitivity. The transmission lines initial sections were designed at the highest targeted centre frequency that corresponds to the shortest section electrical length or the lowest peak-to-average power ratio (PAPR) desired. Afterwards, a sensitivity analysis was conducted to determine the most sensitive section whose tunability will maximize the tuning range and achieve the targeted circuit parameters at the other operating conditions. The selected sections are then loaded with single-pole double through (SPDT) with three switching states; both poles are OFF and each pole is ON at a time. The OFF state for the switch was selected for the operating condition for the initial design. A fixed capacitor with a series transmission line section is connected in parallel with the switch to compensate the OFF state non-idealities. Afterwards, each pole of the switch is connected to a capacitor with a series transmission line section in order to modify the transmission line section length to achieve the desired network parameters for the other operating condition. Each tunable transmission line is designed separately and the achievement of its desired electrical length to realize of the new transmission line circuit parameters was confirmed.

Three different design scenarios are presented hereafter to serve as validation of the proposed

reconfigurable Doherty amplifier, namely

- Single Standard Multi-Frequency DPA: high efficiency is maintained over multiple frequencies when driven with constant PAPR signals
- Multi-Standard Single Frequency DPA: high average efficiency can be maintained when the amplifier is operated at a single frequency but driven with signals with varying PAPR
- Multi-Standard Multiple Frequency DPA : high average efficiency can be maintained when the amplifier is operated at multiple frequencies and driven with signals with varying PAPR

4.2.2 Multi-Frequency Single Standard Doherty Power Amplifier Prototype

In order to validate the feasibility of the reconfigurable Doherty amplifiers, and based on the previously established design equations, a tri-band Doherty amplifier prototype was designed and fabricated. The prototype [75] (Figure 4-4) was designed to operate at 1.9, 2.14, and 2.6 GHz for $p = 2$ (PAPR= 6 dB). The main OMN achieved optimal second harmonic termination in addition to the fundamental termination for efficiency enhancement purposes. The simulations demonstrated the need for five tunable elements; two for the main IMN, one for the main OCN, one for the main OMN for second harmonic impedance adjustment, and one for the auxiliary OCN. The main and auxiliary transistors are generally biased in class AB and class C respectively. This was done to compensate for the difference between the input-voltage to output-current relationships in a class AB and class C. To achieve the current profiles shown in Figure 2a, a 25 W Cree® GaN high electron mobility transistor (HEMT) (CGH40025F) was used for the auxiliary amplifier that was 2.5 times larger than the main one (Cree® 10 W GaN HEMT CGH40010F). The packaged RMSW221 microelectromechanical systems (MEMS) single pole, double throw (SPDT) from RadantMEMS® was selected to ensure the electronic tunability of the reconfigurable Doherty prototype. The chosen MEMS switch has an actuation voltage of about 110 V. This ensures proper operation of the MEMS switches as the voltage swing in the DPA is lower than the actuation voltage. In addition, switches were placed in shunt to the direct signal path in order to reduce the power handling requirements and the corresponding loss.
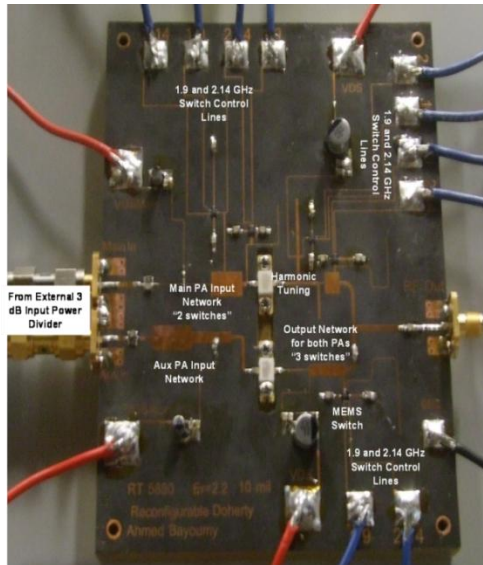
Figure 4-4, Frequency-Agile Doherty Amplifier Prototype [75]

The experimental validation of the proposed design methodology involved building a 2.14 GHz single frequency Doherty amplifier designed to quantify the differential performance between the multi-frequency Doherty amplifier and the single frequency amplifier. Figure 4-5 shows the comparison between the measured drain efficiencies obtained at 2.14GHz using the single frequency and the reconfigurable Doherty amplifier prototypes. According to Figure 4-5, the flexibility achieved by the reconfigurable Doherty amplifier was accompanied by a minimal drain efficiency reduction of about 4%. This drain efficiency reduction was attributed to the losses associated with the non-idealities of the MEMS switch and the wire bonding used for its assembly on the printed circuit board.
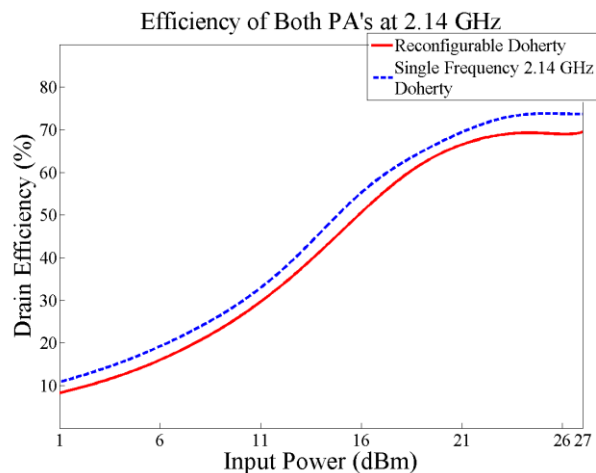
Figure 4-5, Efficiency of Single Frequency and Frequency-Agile Amplifiers at 2.14 GHz

The measurement results of the drain efficiency for the reconfigurable Doherty amplifier prototype when driven with a continuous wave input signal are shown in Figure 4-6. According to this figure, the reconfigurable DPA achieved a drain efficiency of 71, 68.5, and 70.8%, and PAE of 67.2, 65.1, and 67.8% at peak input power levels for the operating frequencies, 2.6, 2.14, and 1.9 GHz, respectively. In addition, excellent drain efficiencies of 67.6%, 65%, and 66.2% were maintained at 6 dB input back-off over the three frequencies. This confirms the proper Doherty technique realization at the three frequencies. The peak output power levels achieved were about 41 dBm, 40.5 dBm, and 42.1 dBm for the operating frequencies, 2.6, 2.14, and 1.9 GHz, respectively.
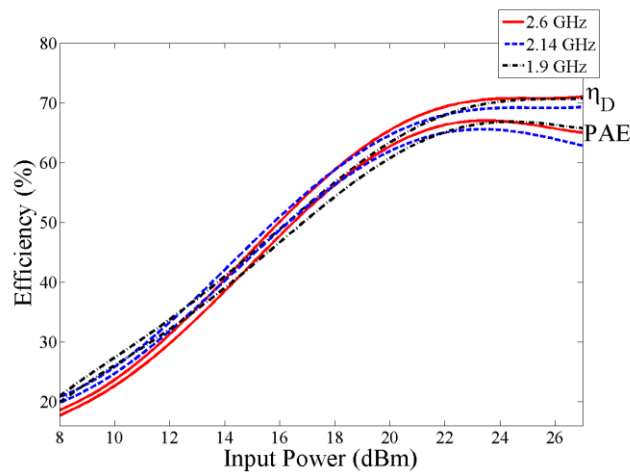
(a)
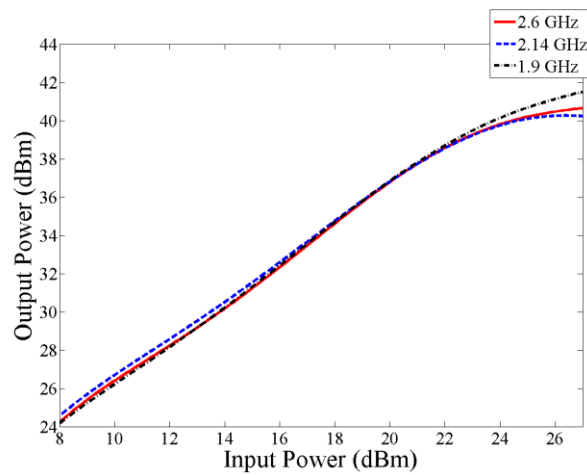
(b)

Figure 4-6, Multi-frequency Doherty PA (a) Efficiencies and (b) Output Power Enhancement Results

44

According to Figure 4-7, which depicts the measured AM/AM characteristics of the reconfigurable DPA, a small signal gain of about 13 dB was obtained at each of the three targeted frequencies. In addition, a similar nonlinearity trend was recorded for the three frequencies. Furthermore, measurements were conducted to assess the matching of the reconfigurable Doherty amplifier for the three different tuning settings. As shown in Figure 4-8, acceptable matching at input and output was maintained for the different configurations of the Doherty amplifier. The assessment of the linearizability of the reconfigurable Doherty amplifier prototype was conducted by synthesizing a pruned Volterra [76] based predistorter and applying it to the mitigation of both static nonlinearity and memory effects exhibited when driven with typical wideband signals. In order to accomplish this, a 20 MHz LTE signal with PAPR of 9.6 was generated around 2.6 GHz and 1.9 GHz and used as a first test signal. In addition, a 4C WCDMA signal with a PAPR of 8.6dB was generated around 2.14 GHz to serve as a second test signal. Figure 4-9 shows the output power spectrum density of the reconfigurable DPA before and after linearization, when driven with the two test signals. According to Figure 4-9, the pruned Volterra series based predistorter reduced the out of band emissions by about 17 dBc, at the three frequencies, for both test signals. Hence, one can conclude that the reconfigurability did not compromise the Doherty amplifier linearizability.
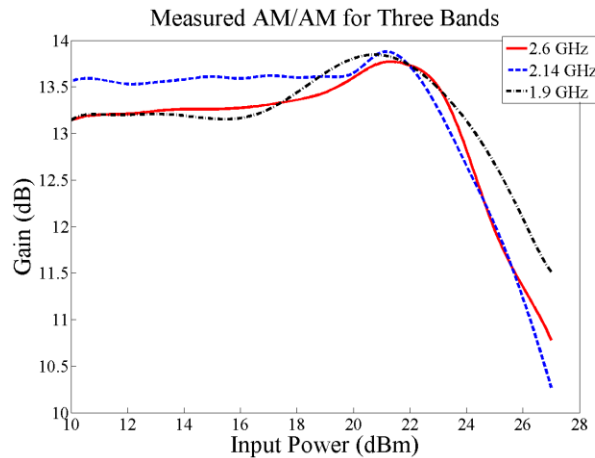
Figure 4-7, AM/AM Characteristics of the Frequency-Agile Doherty amplifier
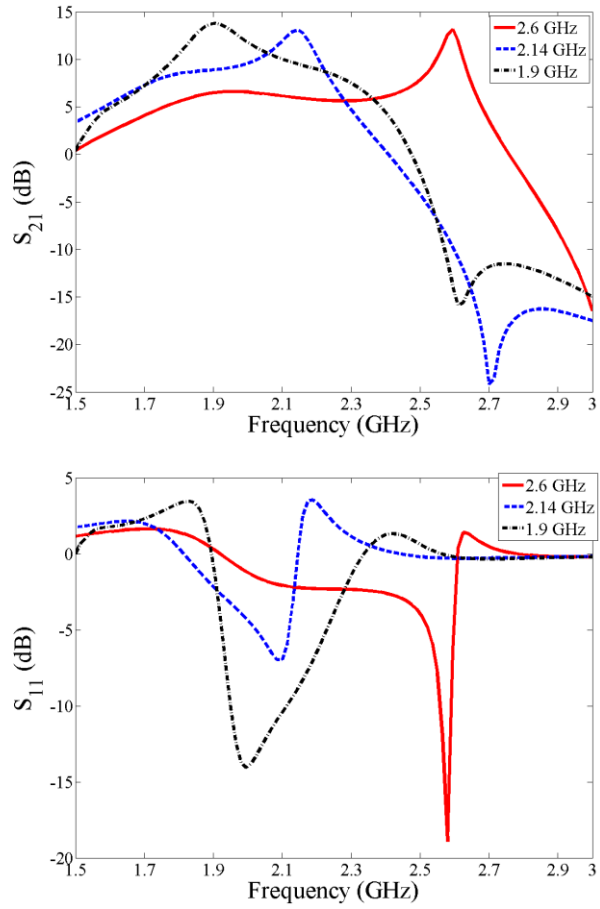
Figure 4-8, Measured Doherty S-parameters at Different Switching States
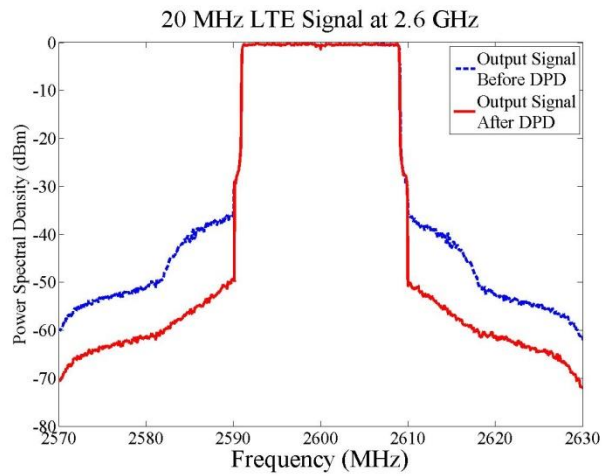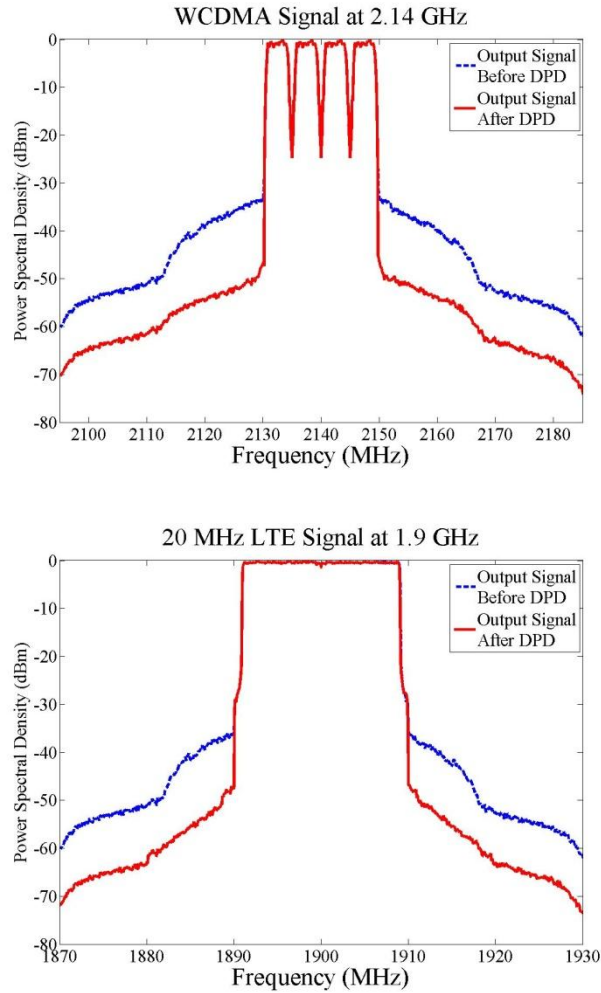
Figure 4-9, Output Spectrum of the Linearized and Non-linearized Frequency-agile Doherty

4.2.3 Multi-Standard Single Frequency Doherty Power Amplifier Prototype

The first prototype successfully validated the closed form design equations for multi-frequency operation and showed excellent agreement between simulation and experimental results. The second demonstrator [77] (Figure 4-10) targeted multi-PAPR operation (variable value of p) and fixed frequency (constant value for θ). The designed prototype operated at a centre frequency of 2.6 GHz and targeted handling of 6, 9, and 12 dB back-off levels. The simulation showed the need for four tunable elements for circuit realization; one in the main OCN, one in the main OMN for second harmonic tuning, one in the auxiliary OCN, and one in the main IMN. Similar transistor sizes for the main and auxiliary amplifiers, as well as tunable MEMS switches, were used to realize this prototype.
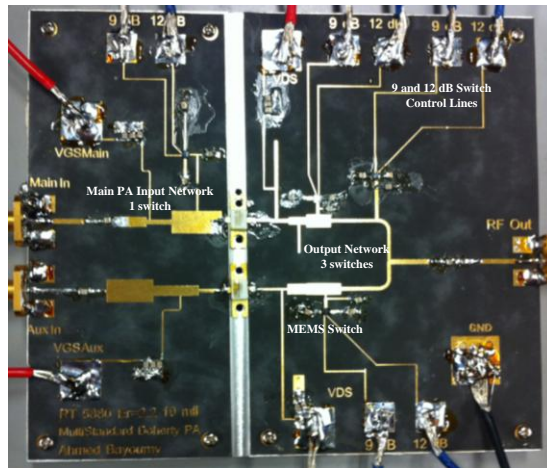
Figure 4-10, Reconfigurable DPA Demonstrator for Variable PAPR Signals [77]

Measurement of the reconfigurable DPA under continuous wave stimulus revealed drain efficiencies of more than 68.3, 67.8, and 64.1% for the three PAPR settings (6, 9 and 12 dB), as shown in Figure 4-11. In addition, excellent drain efficiencies of 65.1, 64.3, and 60.2% were maintained at the 6, 9 and 12 dB output back-off levels. Figure 4-12 depicts a small signal gain of 13.5 dB at each of the three targeted PAPR settings with a similar nonlinearity trend. Figure 4-13 shows the output power spectral density of the Doherty amplifier using an input 4C WCDMA signal with PAPR of 7.2 and 11.6 dB using a pruned Volterra predistorter [79]. The predistorter reduced the out of band emissions by about 16 dBc at the PAPR settings.
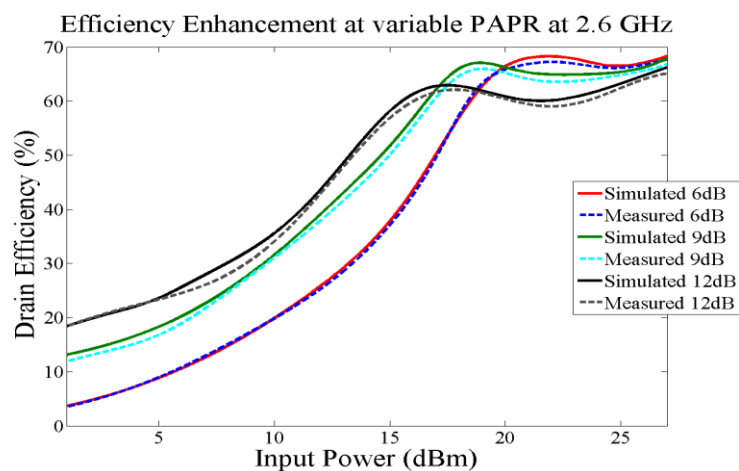
Figure 4-11, Simulated and Measured Results for the Reconfigurable DPA at 6, 9 and 12 dB Back-off Levels at 2.6 GHz
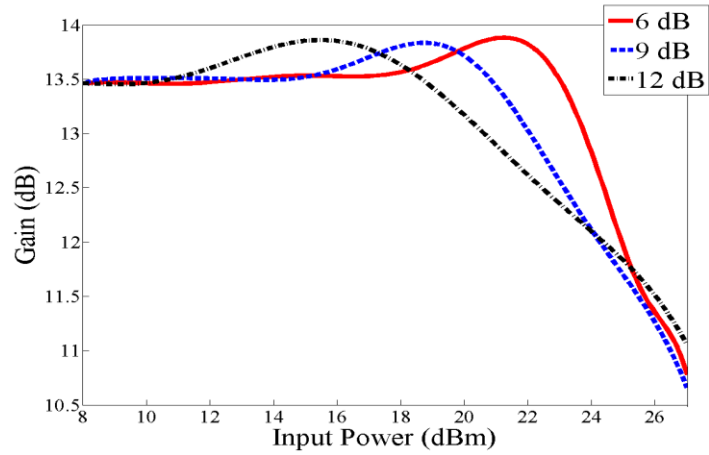
Figure 4-12, AM/AM Characteristics of the Multi-standard DPA
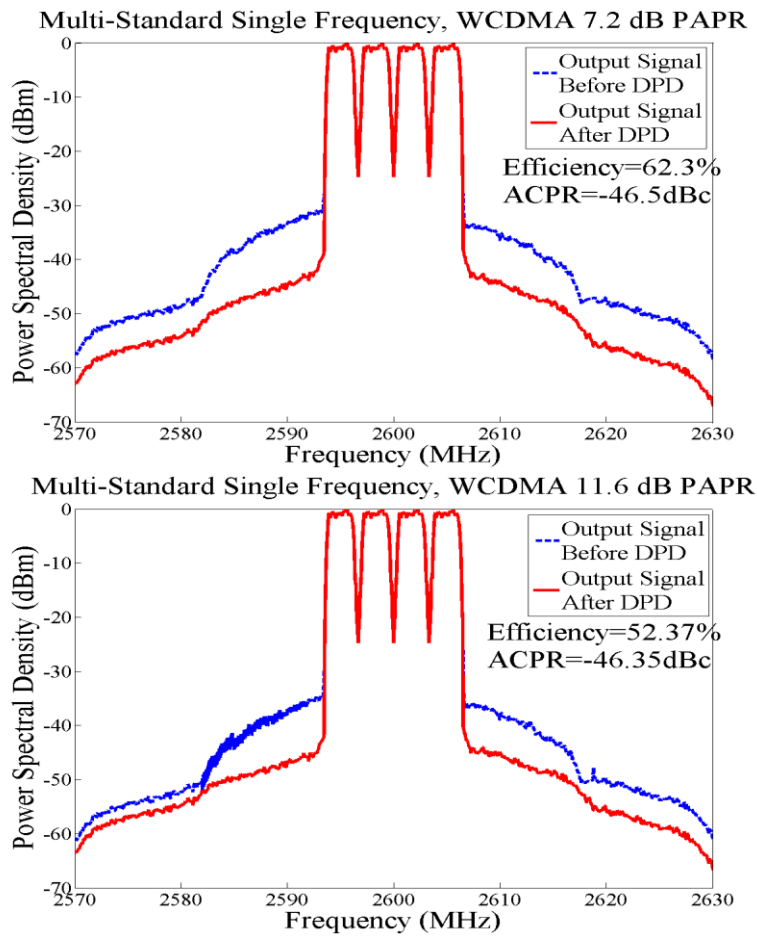
Figure 4-13, Output Spectrum of the Linearized Multi-standard DPA

4.2.4 Multi-Standard Multi-Frequency Doherty PA Prototype

To combine the two previous design dimensions into a single prototype, a multi-standard multi-frequency (MSMF) reconfigurable Doherty was designed using variable θ and p values [78]. The prototype (Figure 4-14) was designed to handle signals with a PAPR of 6, 9, and 12 dB and to operate at centre frequencies of 1.9, 2.14, and 2.6 GHz. Eight tunable elements were needed for the circuit realization; three in the main OCN, one in the main OMN for the second harmonic tuning, two in the auxiliary OCN, and two in the main IMN.
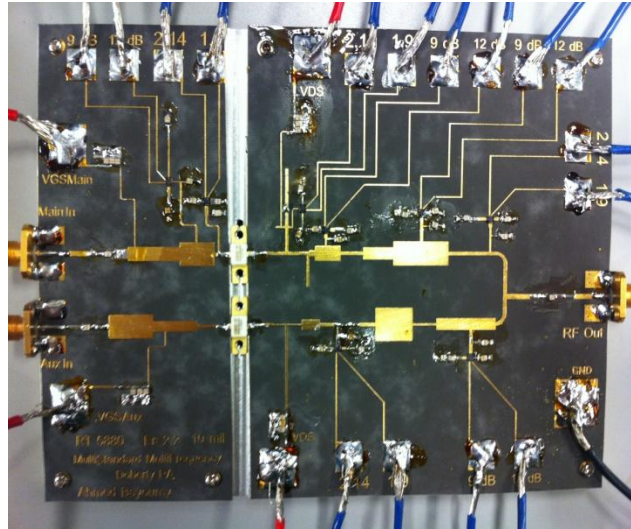
Figure 4-14, The Proposed Multi-standard Multi-frequency DPA Prototype [78]

Continuous wave measurements of the drain efficiency of the MSMF DPA prototype are shown in Figure 4-15 and Figure 4-16. According to Figure 4-15, there was excellent agreement between the simulated and measured efficiency profiles. The MSMF reconfigurable DPA achieved drain efficiency, at 2.6 GHz, of 67% at peak power output level and 65, 64, and 59% respectively at input back-off power level values of 6, 9 and 12 dB. When using a 2.14 GHz centre frequency, the peak power level efficiency was 66% while the input back-off efficiencies were 67, 66, and 61%. Similar efficiency enhancement results were achieved at the third operating frequency; 1.9 GHz. This confirmed the proper Doherty technique realization at the three frequencies and the three back-off power levels. As can be seen in Figure 4-16, the peak output power levels achieved were about 41.8 dBm, 40.8 dBm, and 41.5 dBm at the three back-off levels' circuit arrangements for the operating frequencies, 2.6, 2.14, and 1.9 GHz, respectively.
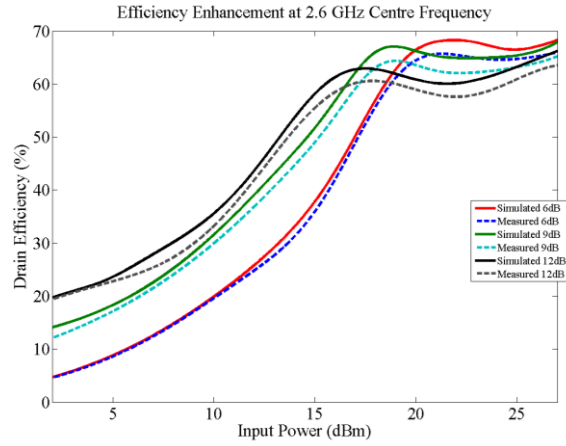
(a)
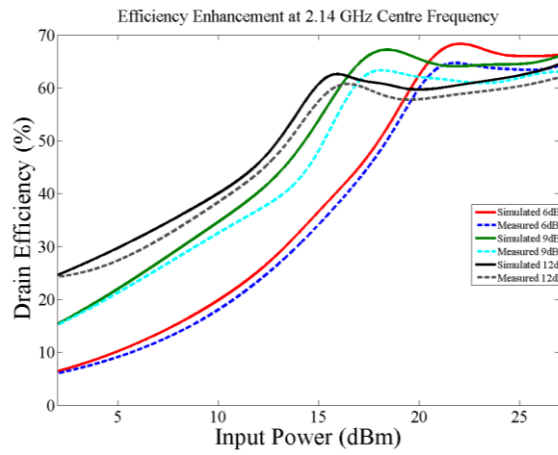
(b)
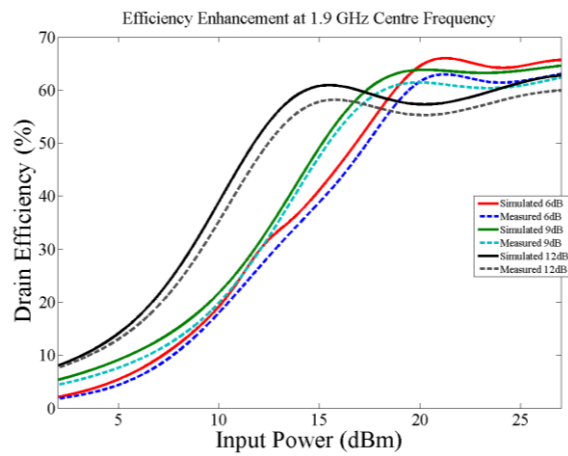
(c)

Figure 4-15, Multi-standard Multi-frequency DPA Efficiency Enhancement Results
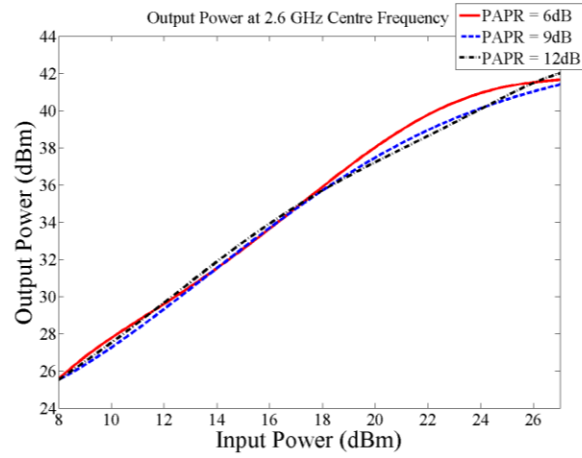
(a)
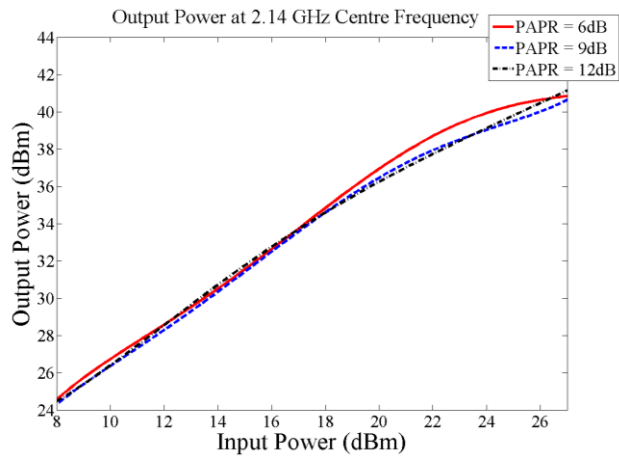
(b)
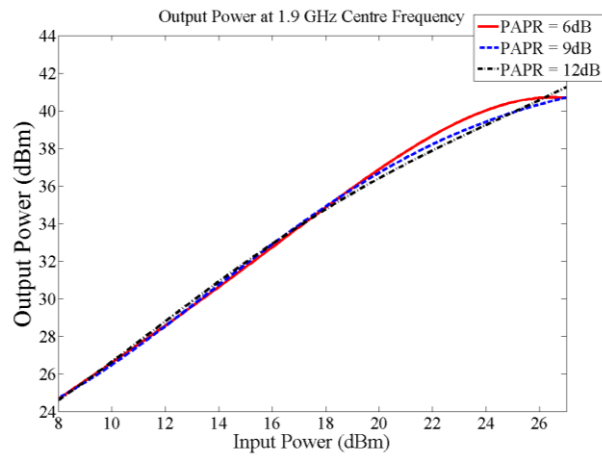
(c)

Figure 4-16, Multi-standard Multi-frequency DPA Measured Output Power
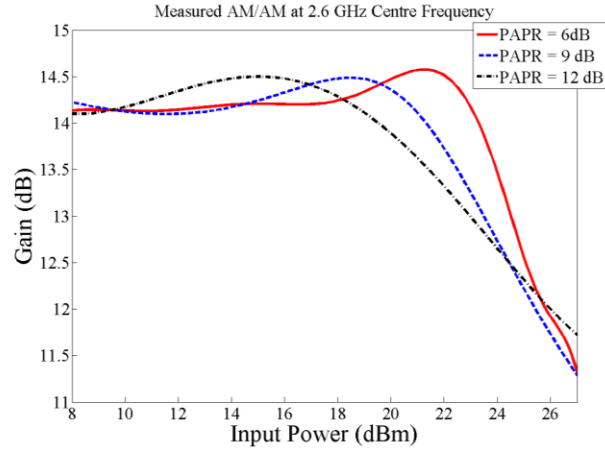
(a)
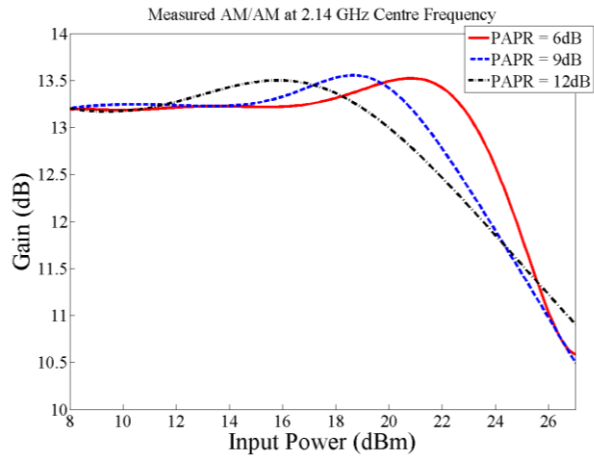
(b)
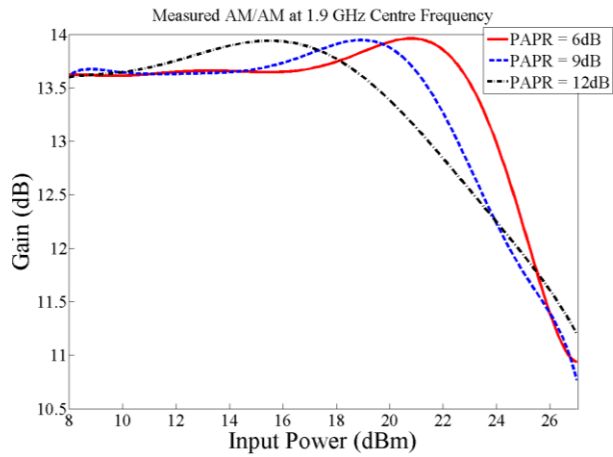
(c)

Figure 4-17, AM/AM Characteristics of the Multi-standard Multi-frequency DPA

According to Figure 4-17, which depicts the measured AM/AM characteristics of the MSMF

Doherty, small signal gains of about 14.0, 13.3, and 13.6 dB were obtained at 2.6, 2.14 and 1.9 GHz targeted operating frequencies respectively. Figure 4-17 also reveals the expected nonlinearity trends for the three operating frequencies where the auxiliary transistor begins conducting at the desired predetermined back-off power level.

A pruned Volterra [76] based predistorter was used for the linearizability assessment of the DPA prototype and was synthesized and applied to compensate for both static nonlinearity and memory effects exhibited when driven with typical wideband signals. A 20 MHz LTE signal with a PAPR of 11.5 dB was generated around 2.6 GHz and used as the first test signal. In addition, two 4C WCDMA signals with PAPR of 11.6 dB and 7.2 dB, generated around 2.14 and 1.9 GHz respectively, served as the test signals for the other two operating frequencies. The linearity test signals were selected to cover all of the centre frequencies and the different targeted PAPR values for different communication standards.

Figure 4-18 demonstrates the output power spectrum density of the proposed MSMF Doherty amplifier, before and after the digital predistorter (DPD) linearization, when driven with the prepared test signals. The pruned Volterra series based predistorter reduced the out of band emissions by more than 12 dBc at the three frequencies and for different PAPR values achieved an adjacent channel power ratio (ACPR) of higher than 45 dBc. Hence, one can conclude that the reconfigurability did not compromise the amplifier's linearizability.
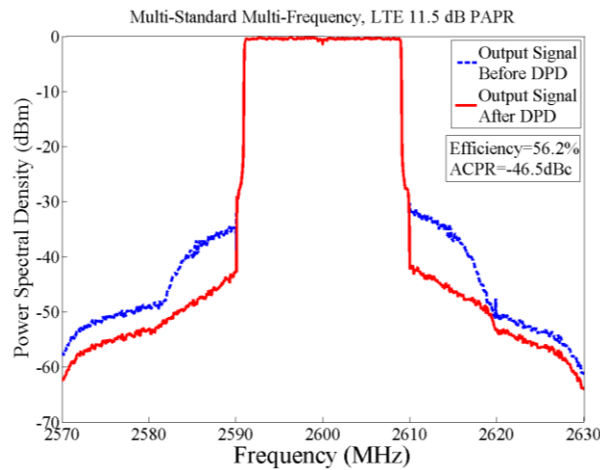
(a)
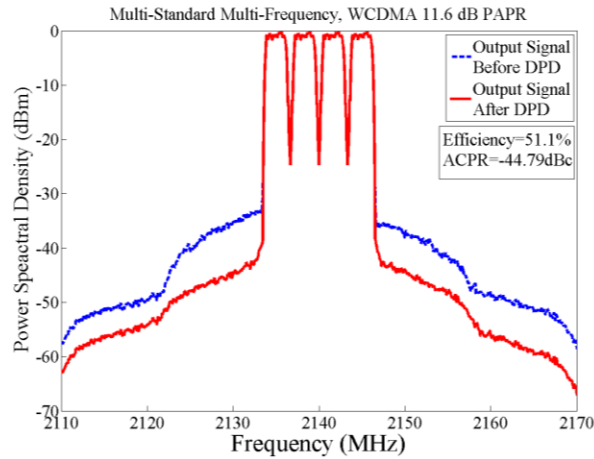
(b)
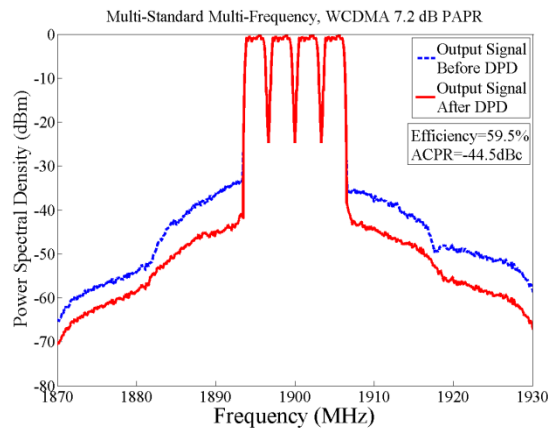
(c)

Figure 4-18, Output Spectrum of the Linearized and Non-linearized Reconfigurable DPA

4.3 Conclusion

This chapter expounded the design of electronically reconfigurable Doherty amplifiers capable of maintaining high efficiency when driven by highly varying wideband signals with variable time domain characteristics and wide spread centre frequencies. In order to achieve this objective, systematic closed-form design equations were developed. The design procedure involved compensating for the deviation of Doherty distributed elements with the operating frequency and targeted back-off power levels. This design methodology was applied to realize three reconfigurable Doherty prototypes. The first prototype was a tri-band 25 W DPA, operating at 1.9 GHz, 2.14 GHz and 2.6 GHz, capable of maintaining high efficiency at a back-off power level of 6 dB. It used five tunable RF MEMS SPDT switches to achieve the reconfigurability. The second prototype was a 2.6 GHz variable PAPR Doherty amplifier capable of enhancing the back-off power levels of 6, 9 and 12 dB using four tunable elements. The final, and most general

prototype, used eight MEMS switches to realize a tri-band 25 W DPA, operating at 1.9 GHz, 2.14 GHz and 2.6 GHz, capable of maintaining high efficiency at back-off power levels of 6, 9 and 12 dB. The measurement results of the MSMF Doherty amplifier prototype confirmed the proper load modulation over the three targeted frequencies and three PAPR levels. Excellent drain efficiencies of about 67% at peak power levels and 60% at 12 dB back-off were found. The MSMF reconfigurable Doherty amplifier was also linearized using a pruned Volterra series predistorter which allowed for an ACPR of about 47 dBc when driven with 4C-WCDMA and 20 MHz LTE signals located at the targeted frequencies, while PAPR varied from 7 to 11 dB.

In the next chapter a similar design approach was applied to the generic DPA in order to develop closed form equations for designing a reconfigurable DPA capable of efficiently amplifying input RF signals with variable peak and average power levels for dynamic network loads. The newly developed design equation were applied to fabricate a reconfigurable DPA demonstrator which was tested and driven by input signals with average power levels of 21, 16 and 11 dBm.

Chapter 5

Reconfigurable Doherty Power Amplifiers with Enhanced Efficiency at Extended Operating Average Power Levels

5.1 Introduction

Doherty technique has been widely adopted to enhance the efficiency of radio frequency (RF) power amplifiers (PAs) used in communication equipment that processes signals with highly variable envelopes. Doherty technique was devised to maintain high efficiency in the high power region of RF transistors, typically 6 dB away from their peak power. However, the continuously changeable characteristics (average power) of the communication signals, resulting from the dynamic networks' loads, are posing additional efficiency challenges. Indeed, while designed to enhance efficiency in the power region close to their peak power, Doherty power amplifiers (DPAs) operate most of the time in a much lower power region. This low power region yields very low power efficiency since the load modulation suggested by the Doherty technique does not hold in this region. In order to maintain high average efficiency for variable average power levels, the load modulation mechanism must be maintained over a large power range.

In this chapter, a systematic design approach is proposed to enhance the average efficiency of a Doherty amplifier as the average power changes. This approach consists of adjusting the gate supply voltage of the auxiliary transistor, reconfiguring the input/output matching networks (IMN, OMN) of the main transistor, and adjusting the OMN of the auxiliary transistor as the input signal average power varies. Microelectromechanical systems (MEMS) switches were employed to electronically tune the matching networks so that the proper load modulation was maintained over a large range of average input power levels.

5.2 Conventional Doherty Power Amplifier Efficiency vs. Average Power

Figure 2-11 depicts a generic Doherty amplifier block diagram that includes a peaking and a main transistor, an IMN and an OMN, and two impedance inverters. In the following analysis, $R_L = R_T$. The main transistor is class AB biased and matched to ensure peak efficiency at a predetermined "ρ dB back-off" that corresponds to the peak to average power ratio (PAPR) of the input signal (input voltage $V_{in} = \dfrac{V_{in,\max}}{p}$ where $\rho(dB) = 20\log p$). The auxiliary PA is class C biased and begins conducting at $V_{in} = \dfrac{V_{in,\max}}{p}$.

The DPA, which will be referred to as a reference DPA, is required to maintain high efficiency for input power levels between the peak power $P_{in,max}$ and a reference back-off power level $P_{in,avg}^{ref} = \dfrac{P_{in,max}}{p^2}$ and has the following circuit parameters:

$$R_T^{ref} = R_{opt}^{ref}, Z_{T1}^{ref} = \frac{R_{opt}^{ref}}{\sqrt{p}} \tag{5-1}$$

where $R_{opt}^{ref} = \dfrac{V_{DS,max}}{I_{1,max}}$ is selected to achieve the maximum efficiency at $P_{in,avg}^{ref} = \dfrac{P_{in,max}}{p^2}$, and where $V_{DS,max}$ and $I_{1,max}$ represent the maximum main transistor drain voltage and current respectively.

Maintaining a high efficiency at extended back-off power levels requires load modulation of the main transistor impedance as a function of the input that follows the expression below:

$$Z_{main}^{ref} = \begin{cases} 2R_T^{ref} & 0 \le V_{in} \le \dfrac{V_{in,max}}{p} \\[4mm] R_T^{ref}(2 - \dfrac{1}{1+\sigma}) & \dfrac{V_{in,max}}{p} \le V_{in} \le V_{in,max} \end{cases} \tag{5-2}$$

where $\sigma = \dfrac{V_{in}}{V_{in,max}}$

If the average power of the input signal decreases, the reference DPA will yield low average efficiency since the load modulation is only maintained in the last reference power range (ρ dB). This efficiency degradation is shown in the first trace of Figure 5-1. Improving the average efficiency, when the average input power is less than $P_{in,avg}^{ref}$, requires maintenance of the proper load modulation over different power ranges. Extending the power level at which the second efficiency peak occurs. by increasing the value of ρ to $\rho + 2\gamma$, can address this problem (see the extended DPA trace of Figure 5-1). However, this will engender low average efficiency for average power higher than $P_{in,avg}^{ref}$. Alternatively, a more effective solution for maintaining high efficiency at different average power levels is proposed. This solution consists of a Doherty amplifier with adaptable parameters, R_T and Z_{T1}, which vary as functions of the input signal's average power, shown by the solid curve of Figure 5-1. In this case, we start with a reference

DPA. The values of R_T^{ref} and Z_{T1}^{ref} are designed to maximize the average power efficiency at a given $P_{in,avg}^{ref}$, while the electronic tuning of the matching networks and the adjustment of the auxiliary transistor gate supply voltage are used to maintain high efficiency at an average power which is backed off $n\gamma$ dB from the $P_{in,avg}^{ref}$ (n is an integer that sets the average power decrement based on the reference one), resulting in $P_{in,avg}^{n} = (P_{in,avg}^{ref} - n\gamma)dB$. Hence, high drain efficiency can be maintained over a wide range of back-off power (as illustrated in Figure 5-1). The average power reduction γ corresponds to a reduction of the input signal V_{in} by ratio α, where $\gamma(dB) = -20\log\alpha$.
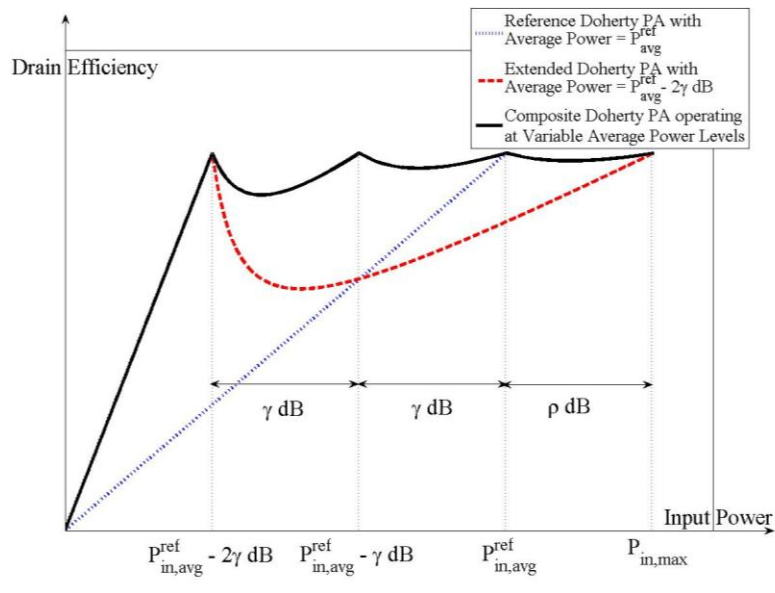
Figure 5-1, Variable Operating Average Power DPA Efficiency Enhancement

Assuming a main transistor with linear trans-conductance, the main amplifier drain current follows the input voltage according to the equation:

$$I_1 = g_m V_{in} \tag{5-3}$$

At reduced average power $P_{in,avg}^{1} = (P_{in,avg}^{ref} - \gamma)dB$, the main amplifier drain current will be decreased by a factor of α, hence $I_1 = \alpha I_{1,max}$. Furthermore, the auxiliary amplifier will be required to begin conducting at a new threshold that is directly related to the new reduced average power. Figure 5-2 demonstrates the required current profiles for proper load modulation at variable operating average power levels. In order to obtain a maximum efficiency at $P_{in,avg}^{1}$, the

value of the optimal load impedance must be adjusted from its reference value R_{opt}^{ref} to

$R_{opt} = \dfrac{R_{opt}^{ref}}{\alpha}$. The change of the optimum impedance with the average power calls for the

adjustment of the combining network parameters (Equation 5-1) in order to maintain the proper

Z_{main} profile modulation in the required power range. Figure 5-3 shows the main transistor load

impedance profile needed to obtain the desired efficiency enhancement at variable average power
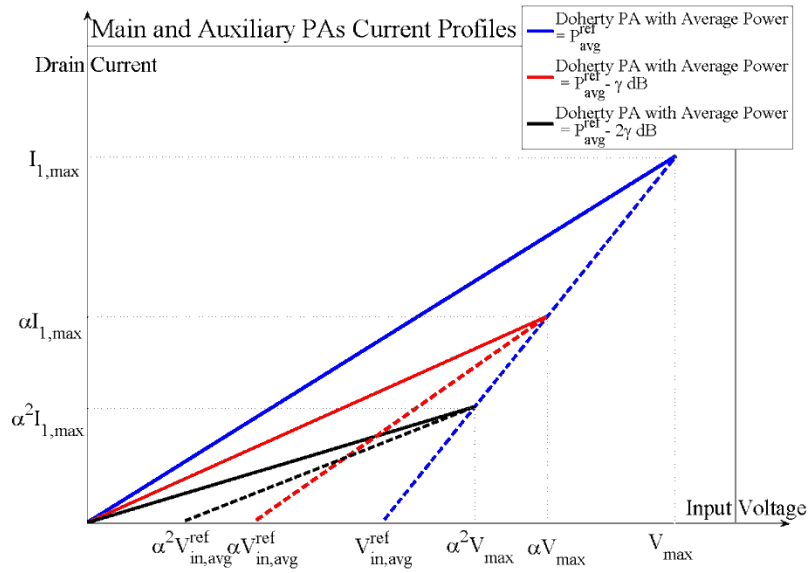
levels.

Figure 5-2, Ideal Main and Auxiliary PAs Current Profiles for Variable Operating Average
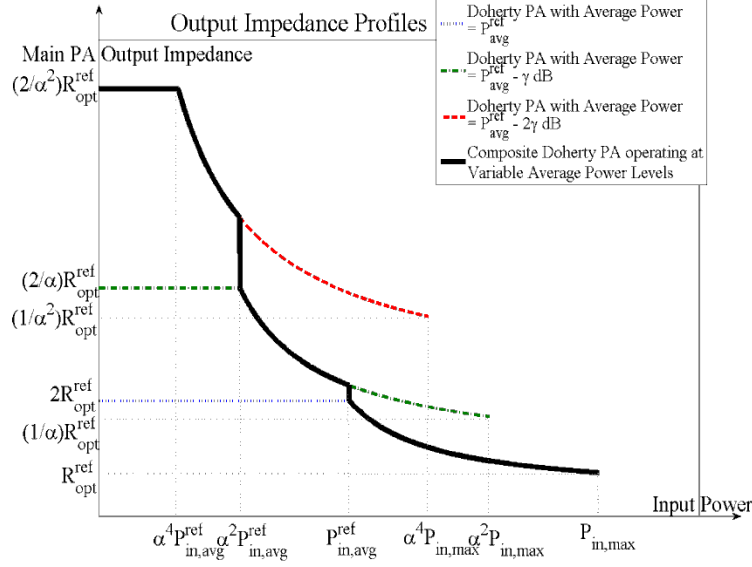
Power Levels

Figure 5-3, Main Transistor Output Impedance Profiles at Each Average Power Level as well as the Targeted Profile for Variable Operating Power Levels in a Doherty Amplifier

In conclusion, for a given average power level, $P_{in,avg}$, which is γ dB away from the reference average power, $P_{in,avg}^{ref}$, the proper Z_{main} profile can be achieved if R_T and Z_{T1} vary to reflect the change of the R_{opt} value (shown in Equation 5-4).

$$R_T = R_{opt}, Z_{T1} = \frac{R_{opt}}{\sqrt{p}} \tag{5-4}$$

Achieving proper load modulation requires changing the gate biasing voltage of the auxiliary transistor so that it turns on at the right input power level for a given average power.

5.3 Design of Doherty Amplifier with Enhanced Efficiency at Variable Average Power

In order to alleviate the effects of average power variation on the conventional Doherty amplifier's efficiency, a new Doherty amplifier with enhanced efficiency at variable operating average power is proposed. The new Doherty includes two reconfigurable OMN added in the main and auxiliary paths of the Doherty. These matching networks are carefully designed to cope with the variation in the value of the optimal load impedance R_{opt} and consequent changes in R_T and Z_{T1} values when $P_{in,avg}$ differs from $P_{in,avg}^{ref}$. This ensures the proper main transistor

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impedance and current profiles are maintained and consequently, the correct load modulation (Figs. 5-2 and 5-3). The design of the two matching networks was conducted using the following systematic procedure. A set of closed form equations allowed the determination of the ABCD parameters of the matching networks, given the reference value of the average input power (represented by p), and the desired power reduction ratio α that, in turn, determined the set of values of the optimal load impedance R_{opt} with respect to its reference value R_{opt}^{ref} .

It is worth mentioning that the impedance inverters were kept unchanged when the average power varied and the required circuit adjustments were implemented using the reconfigurable matching networks. The non-reconfigurable combining networks improve the DPA proposed prototype power handling capabilities by revoking the need for tunable MEMS switches in the high power network part. Moreover, this feature allows for the future design of a GaN monolithic microwave integrated circuit (MMIC) integrated DPA version where the non-reconfigurable bulky inverters can be fabricated off-chip reducing the fabrication cost.

In this analysis, the set of R_{opt} values that correspond to different levels of $P_{in,avg}$ are described in terms of R_{opt}^{ref} following the equation

$$R_{opt}^i = \frac{1}{\alpha^{i-1}} R_{opt}^{ref} \qquad (5\text{-}5)$$

where i is an integer greater than zero. It represents the index used to set the power decrement, $\frac{1}{\alpha^{i-1}}$, of the actual realized average power relative to the reference average power.

In the following analysis, closed form equations have been derived to support the design of the tunable OMN in the main and auxiliary Doherty paths. This analysis was conducted in two steps which are detailed below.

5.3.1 Low Power Compensation

Based on Figure 5-4, a number of expressions were derived to deduce the ABCD parameters of the OMN in the main amplifier path. At low power levels, the desired ABCD parameters of the reconfigurable DPA fixed combining network (targeting an average power $P_{in,avg}$) are expressed in terms of power decrement index i , as follows:
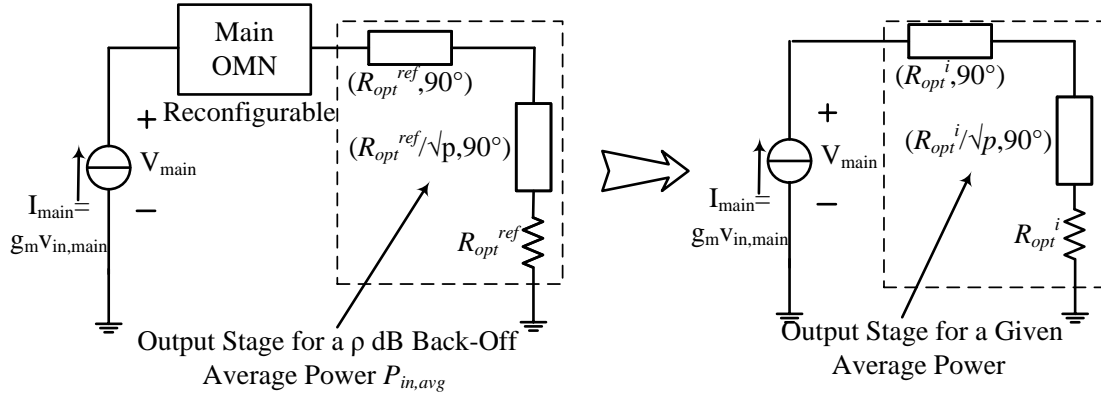
Figure 5-4, Equivalent Low Power Levels Circuits of the Conventional and the Proposed Doherty, Capable of Operation at Any Given Average Power Level

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Low\ Power\ Combining\ Stage\ P_{in,avg}}
$$

$$
= \begin{bmatrix} 0 & jR_{opt}^i \\ \dfrac{-1}{jR_{opt}^i} & 0 \end{bmatrix} \begin{bmatrix} 0 & j\dfrac{R_{opt}^i}{\sqrt{p}} \\ \dfrac{-\sqrt{p}}{jR_{opt}^i} & 0 \end{bmatrix} \begin{bmatrix} 1 & R_{opt}^i \\ 0 & 1 \end{bmatrix} \tag{5-6}
$$

$$
= \begin{bmatrix} -\sqrt{p} & 0 \\ 0 & -\dfrac{1}{\sqrt{p}} \end{bmatrix} \begin{bmatrix} 1 & R_{opt}^i \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^i \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix}
$$

To maintain proper load modulation, the ABCD matrix of the cascade output stage, shown in Figure 5-4, composed of the reconfigurable OMN and the reference output combining stage, should be kept equal to Equation 5-6.

$$
\begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^i \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix}
$$

$$
= \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main\ OMN} \begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^{ref} \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix} \tag{5-7}
$$

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main\ OMN}
$$

$$
= \begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^{i} \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix} \begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^{ref} \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix}^{-1}
$$

$$
= \begin{bmatrix} -\sqrt{p} & -\sqrt{p}R_{opt}^{i} \\ 0 & \dfrac{-1}{\sqrt{p}} \end{bmatrix} \begin{bmatrix} \dfrac{-1}{\sqrt{p}} & \sqrt{p}R_{opt}^{ref} \\ 0 & -\sqrt{p} \end{bmatrix}
$$

(5-8)

Hence, one can deduce the main transistor's reconfigurable OMN circuit parameters using the following equation:

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main\ OMN}
$$

$$
= \begin{bmatrix} 1 & p[R_{opt}^{i} - R_{opt}^{ref}] \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & pR_{opt}^{ref}[\dfrac{1}{\alpha^{i-1}} - 1] \\ 0 & 1 \end{bmatrix}
$$

(5-9)

Equation 5-9 is used to determine the ABCD parameters of the main IMN given the average power decrement index, i, and served as the basis for the realization of the corresponding circuit.

5.3.2 High Power Compensation
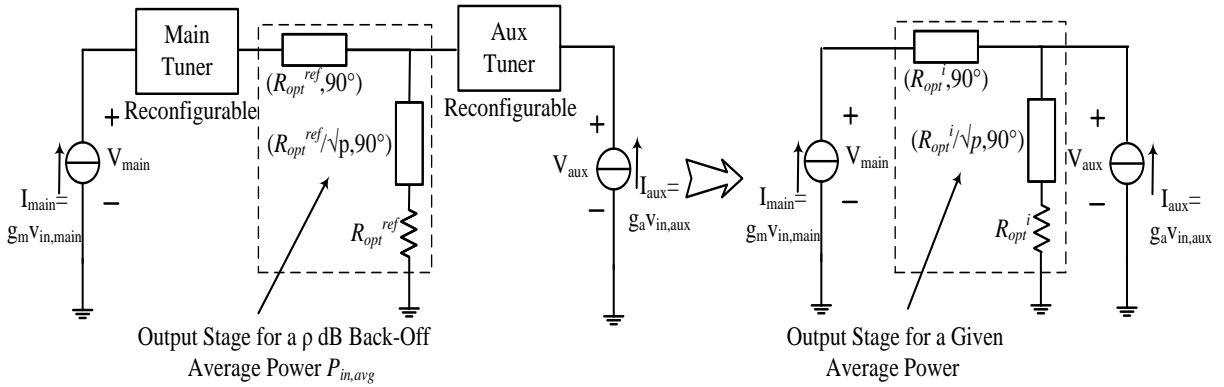
Figure 5-5, Equivalent High Power Levels Circuits of the Conventional and the Proposed Doherty, Capable of Operation at Any Given Average Power Level

Figure 5-5 shows the equivalent circuit of the proposed combining network of the Doherty amplifier which was used to deduce the ABCD parameters of the reconfigurable OMN in the

auxiliary amplifier path. At high power levels, the desired ABCD parameters of the combining network (targeting an average power $P_{in,avg}$), in terms of the power decrement index, i, are given by the following equation:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{High\ Power\ Combining\ Stage\ P_{in,avg}}$$

$$= \begin{bmatrix} 0 & jR_{opt}^{i} \\ \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \dfrac{p}{R_{opt}^{i}} & 1 \end{bmatrix} \tag{5-10}$$

$$= \begin{bmatrix} jp & jR_{opt}^{i} \\ \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix}$$

To maintain proper load modulation, the ABCD matrix of the cascade output stage, composed of the reconfigurable OMN and the reference output combining stage (Figure 5-5), should be kept equal to those presented in Equation 5-11.

$$\begin{bmatrix} jp & jR_{opt}^{i} \\ \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Main\ OMN}$$

$$\begin{bmatrix} jp & jR_{opt}^{ref} \\ \dfrac{-1}{jR_{opt}^{ref}} & 0 \end{bmatrix}\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Aux\ OMN} \tag{5-11}$$

$$\begin{bmatrix} jp & jR_{opt}^{i} \\ \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix} = \begin{bmatrix} 1 & p[R_{opt}^{i} - R_{opt}^{ref}] \\ 0 & 1 \end{bmatrix}$$

$$\begin{bmatrix} jp & jR_{opt}^{ref} \\ \dfrac{-1}{jR_{opt}^{ref}} & 0 \end{bmatrix}\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Aux\ OMN} \tag{5-12}$$

$$= \begin{bmatrix} jp(\dfrac{R_{opt}^{i}}{R_{opt}^{ref}}) & jR_{opt}^{ref} \\ \dfrac{-1}{jR_{opt}^{ref}} & 0 \end{bmatrix}\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Aux\ OMN}$$

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{Aux OMN}}
$$

$$
= \begin{bmatrix} jp(\dfrac{R_{opt}^{i}}{R_{opt}^{ref}}) & jR_{opt}^{ref} \\[2ex] \dfrac{-1}{jR_{opt}^{ref}} & 0 \end{bmatrix}^{-1} \begin{bmatrix} jp & jR_{opt}^{i} \\[2ex] \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix}
$$

$$
= \begin{bmatrix} 0 & -jR_{opt}^{ref} \\[2ex] \dfrac{1}{jR_{opt}^{ref}} & jp(\dfrac{R_{opt}^{i}}{R_{opt}^{ref}}) \end{bmatrix} \begin{bmatrix} jp & jR_{opt}^{i} \\[2ex] \dfrac{-1}{jR_{opt}^{i}} & 0 \end{bmatrix}
$$

(5-13)

Similarly, the auxiliary transistor's reconfigurable OMN circuit parameters can be represented by the following equation:

$$
\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{Aux OMN}}
$$

$$
= \begin{bmatrix} \dfrac{R_{opt}^{ref}}{R_{opt}^{i}} & 0 \\[3ex] \dfrac{p}{R_{opt}^{ref}} - \dfrac{p}{R_{opt}^{i}} & \dfrac{R_{opt}^{i}}{R_{opt}^{ref}} \end{bmatrix}
$$

$$
= \begin{bmatrix} \alpha^{i\text{-}1} & 0 \\[3ex] \dfrac{p}{R_{opt}^{ref}}[1-\alpha^{i\text{-}1}] & \dfrac{1}{\alpha^{i\text{-}1}} \end{bmatrix}
$$

(5-14)

Equations 5-9 and 5-14 are closed form equations used to obtain the network parameters for both reconfigurable OMNs while maintaining proper load modulation for every desired operating average power level represented by the power decrement index $\dfrac{1}{\alpha^{i-1}}$.

The proposed Doherty amplifier uses a variable gate biasing voltage, so that the auxiliary transistor turns ON at the proper input power level for each targeted $P_{in,avg}$. The main amplifier includes a reconfigurable IMN to adjust the phase balance between the two Doherty branches. Figure 5-6 presents the complete design procedure for the variable average power reconfigurable Doherty amplifier. The design also capitalizes on the accuracy of the main transistor optimal second harmonic termination to improve the overall efficiency.

V_{DS}^{Main}

Bias Circuit

Harmonic Tuning Stub

Input Power Divider

Reconfigurable Main Input Matching Network

V_{GS}^{Main}

Reconfigurable Main Output Matching Network

$(R_T, 90°)$

Fixed Combining Network

P_{in}

V_{DS}^{Aux}

Bias Circuit

$(Z_{T1}, 90°)$

Auxiliary Input Matching Network

V_{GS}^{Aux}

Reconfigurable Auxiliary Output Matching Network

R_T
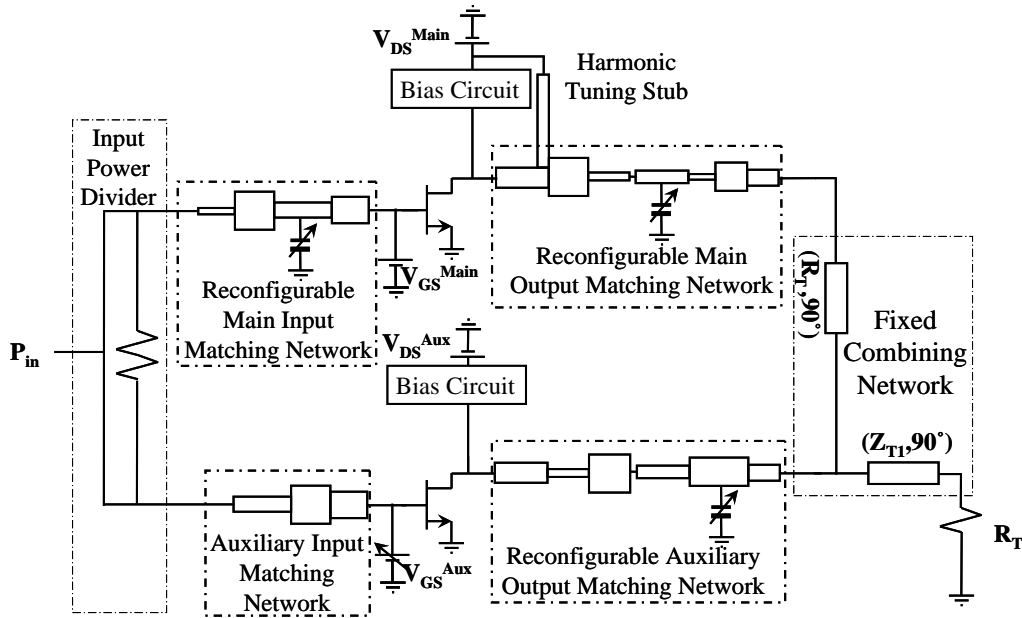
Figure 5-6, Block Diagram of the DPA with Enhanced Efficiency for Variable Average Input Power (11, 16 and 21 dBm)

As described earlier, the required reconfigurability of the DPA was achieved using electronically tunable devices (RF MEMS switches) characterized by low insertion loss and high linearity. Minimizing the number of switches needed to produce proper load modulation at the targeted average power levels was achieved by using a sensitivity analysis. This analysis examined the multi-step transmission line based matching network to identify the most effective segment of line to maximize the tuning range.

As a proof of concept, a Doherty amplifier with 6 dB back-off power, operated at 2.6 GHz was designed. Its purpose was to maintain the load modulation and, hence; high efficiency for average input power ranging from 21 dBm down to 11 dBm. In the design, three ranges of load modulation were targeted. For each 5 dB γ power decrement, the corresponding voltage reduction ratio was $\alpha = \dfrac{9}{16}$. The design parameters' values are presented in the Table 5-1. In this realization, three electronically tunable devices were employed to achieve the proper load modulation in each of the three targeted average power levels: one in the main OMN, one in the auxiliary OMN, and one in the main IMN (with a variable gate bias for the auxiliary transistor). The electromagnetic simulation demonstrated an efficiency of higher than 66% for the 16 dB back-off power region. The simulation results show that the proposed DPA enhanced the

efficiency compared to the reference Doherty by 24% at 16 dB and by 39% at 11 dB average power levels, $P_{in,avg}$.

Table 5-1, Variable Average Power Doherty Design Parameters

P_{avg} (dBm)	$V_{GS,aux}$(V)	R_{opt}(Ω)
21($P_{in,avg}^{ref}$)	-6.7	50 (R_{opt}^{ref})
16	-5.0	87
11	-4.1	155

5.4 Experimental Validation

A 10 W GaN High-Electron-Mobility Transistor (HEMT) (CGH40010F from Cree), and a 25 W GaN HEMT (CGH40025F from Cree), were used as the main and auxiliary transistors respectively. The difference in transistor sizes was used to compensate for the difference between the input-voltage to output-current relationships in class AB and class C modes of operation. They were biased in class AB and class C to provide the current profiles shown in Figure 5-2.

The reconfigurability feature of the Doherty prototype under investigation was achieved using the packaged RadantMEMS® RMSW221 MEMS SPDT switch connected to a fixed capacitors tank. The chosen switch had an actuation voltage of approximately 110 V, thus ensuring no switches would suffer from self-actuation as the voltage swing in the DPA is lower than the self-actuation voltage. To reduce the requirements on the switch power handling and the impacts of the corresponding loss, the tunable devices were placed in shunt to the direct signal path.

Figure 5-7 shows the demonstrator of the reconfigurable Doherty amplifier designed to operate at 2.6 GHz and to efficiently amplify signals with average power levels of 21, 16 and 11 dBm. The validation of the proposed reconfigurable DPA began with plotting the currents of the main and auxiliary transistors vs. the magnitude of a continuous wave input signal for the three targeted average power levels. According to Figure 5-8, the measured main and auxiliary transistors' current profiles are very close to those depicted in Figure 5-2 except for the anticipated nonlinearity which was attributed to the variation of the conduction angle with input signal strength which has considerable effect when $P_{in,avg}$ is equal to 11 dBm. Figure 5-8 clearly shows the reduction of the maximum current value which confirms the change of the optimum load resistance value.
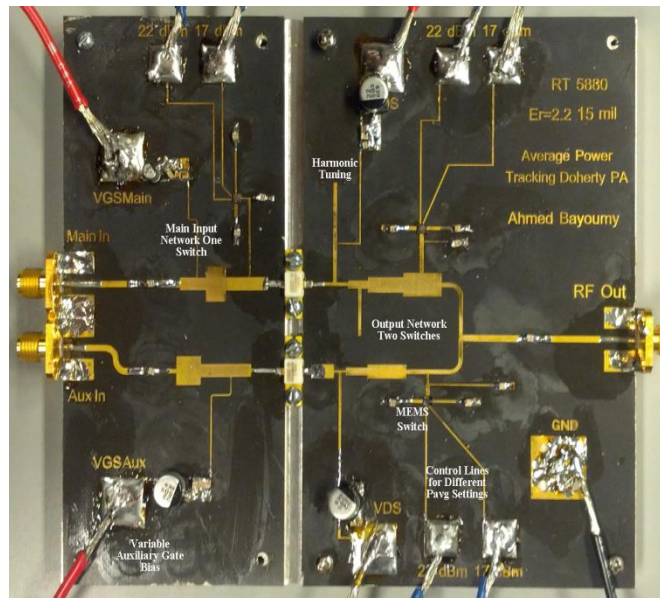
Figure 5-7, The Proposed Prototype for the Reconfigurable DPA for Three Average Power Settings at 2.6 GHz
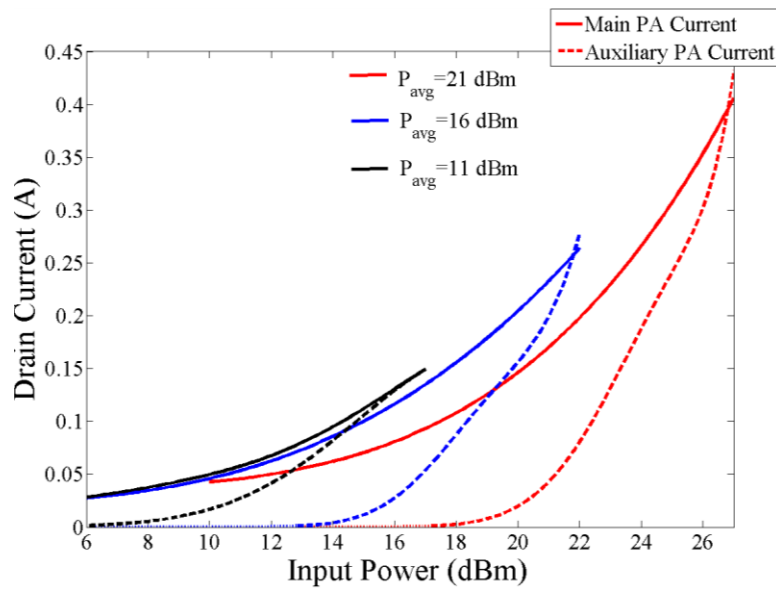
Figure 5-8, Measured Main and Auxiliary Active Devices' Drain Currents for the Reconfigurable Doherty Amplifier for Three Average Power Settings at 2.6 GHz
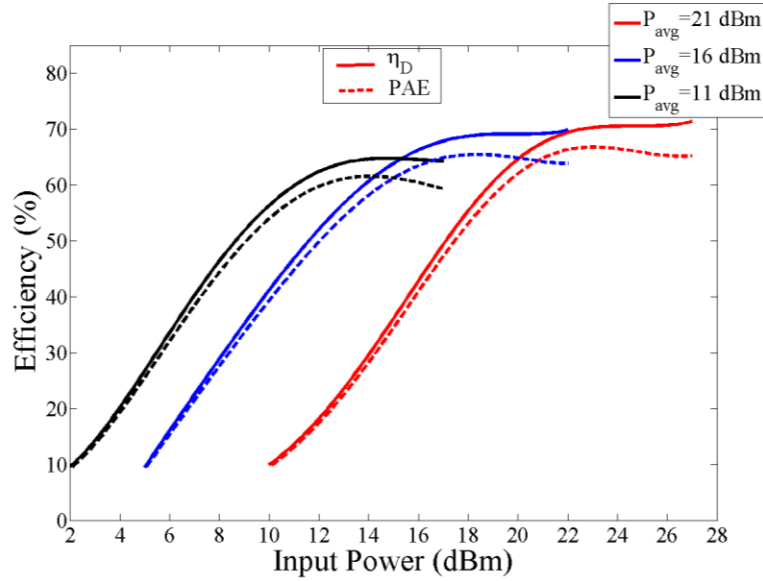
Figure 5-9, Measured Drain and Power Added Efficiencies of the Reconfigurable Doherty
Amplifier for Three Average Power Settings at 2.6 GHz
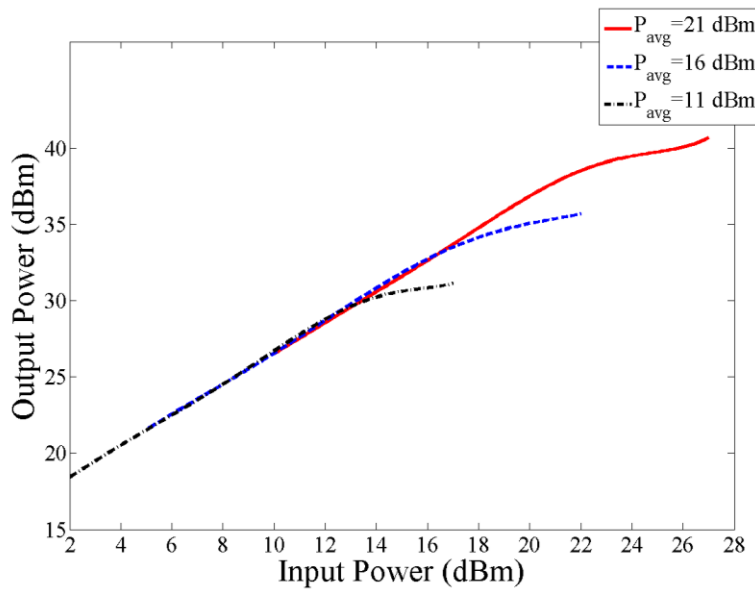
Figure 5-10, Measured Output Powers of the Reconfigurable Doherty Amplifier for Three
Average Power Settings at 2.6 GHz

Continuous wave measurements of the drain efficiency, power added efficiency (PAE) and
output power of the reconfigurable DPA prototype are shown in Figure 5-9 and Figure 5-10. The
electronically reconfigurable DPA achieved a drain efficiency, at 2.6 GHz, of 66% at average
input power levels down to 16 dBm and 62% at average input power levels down to 11 dBm.

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This confirmed the proper Doherty technique realization at the three average power levels. As per Figure 5-10, the peak output power levels achieved were about 32 dBm, 36.8 dBm, and 41.9 dBm at the three average power levels' circuit settings.

Figure 5-11 depicts the measured AM/AM characteristics of the reconfigurable Doherty; a similar small signal gain of about 13.5 dB was obtained in each of the three average power levels' operating conditions. Figure 5-12 demonstrates good matching at the input and output for the different configurations of the reconfigurable Doherty amplifier.
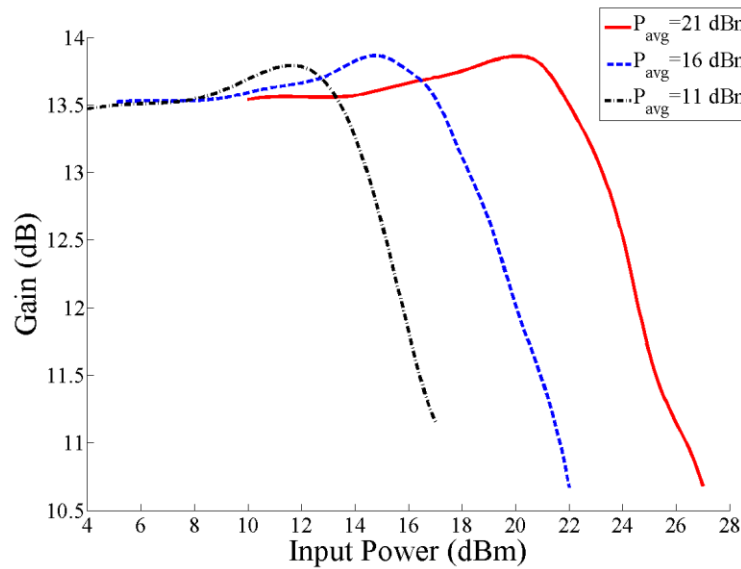
Figure 5-11, AM/AM Measurements for the Reconfigurable DPA for Three Average Power Settings at 2.6 GHz

(a)

(b)
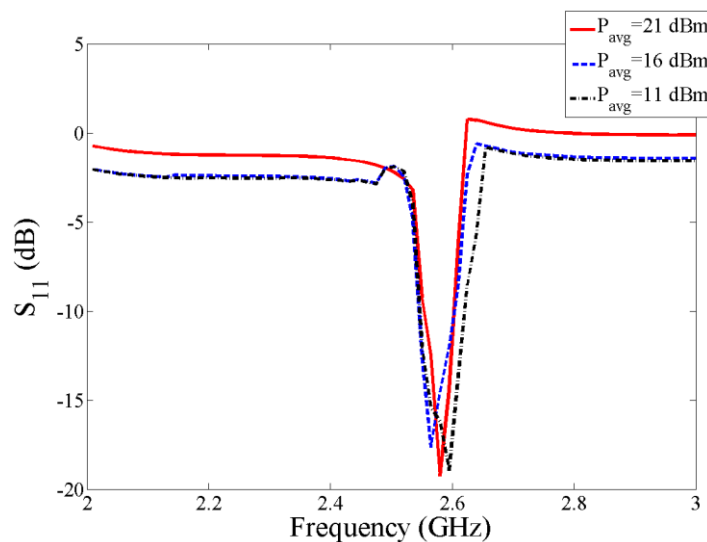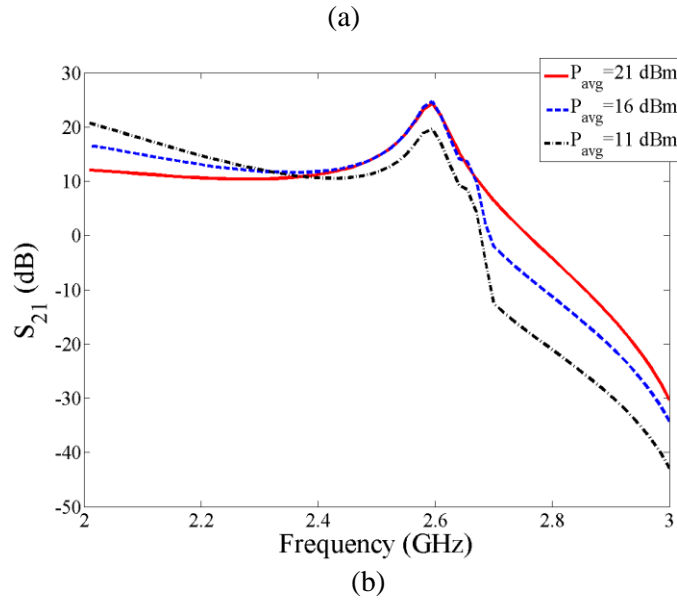
Figure 5-12, Scattering Parameters Measurements for the Reconfigurable DPA for Three Average Power Settings at 2.6 GHz

A pruned Volterra based predistorter was used for the linearizability assessment of the reconfigurable DPA prototype when driven with a 20 MHz LTE signal. It was found to have a PAPR of 7.2 dB and was centered around 2.6 GHz. The average input power, $P_{in,avg}$, values were set to 21, 16 and 11 dBm. Figure 5-13 demonstrates the power spectrum density of the proposed reconfigurable DPA output signal, before and after the digital predistorter (DPD) linearization, when driven with the aforementioned test signals. The pruned Volterra series based predistorter reduced the out of band emissions by more than 12 dB at the three operating average power levels and allowed for an adjacent channel power ratio (ACPR) of higher than 45 dBc. Hence, one can conclude that the reconfigurability did not compromise the amplifier's linearizability.
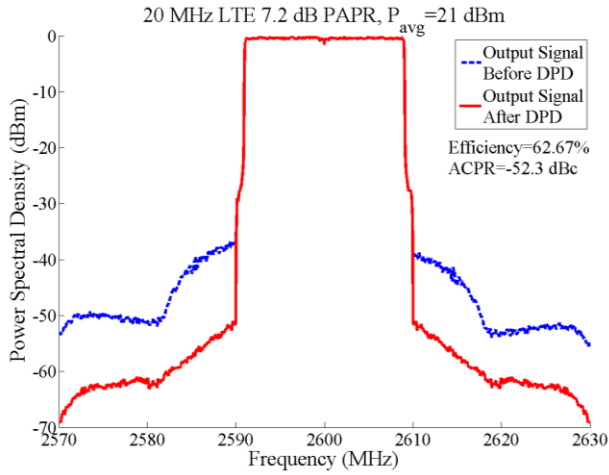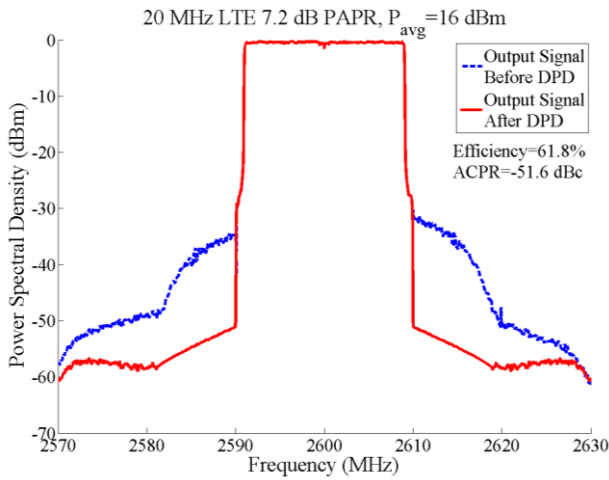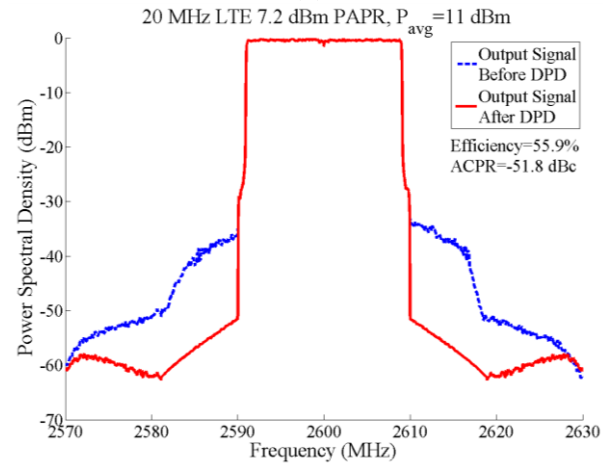
Figure 5-13, Output Spectrum of the Linearized and Non-linearized Reconfigurable DPA for Three Average Power Settings at 2.6 GHz

5.5 Conclusion

This chapter expounded the design of an electronically reconfigurable Doherty amplifier capable of maintaining high efficiency when driven by communication signals with highly varying average power levels. In order to achieve this, systematic closed-form design equations were developed. The design procedure involved adjustment of the DPA optimum load impedance value and reconfiguration of the Doherty OMN to compensate for the load impedance change. This design methodology was applied to design a 25 W DPA that operated at 2.6 GHz and was capable of maintaining high efficiency at average power levels of 21, 16 and 11 dBm. The measurement results from the Doherty amplifier prototype confirmed the proper load modulation over the three average power levels. Excellent PAE of more than 62% for the full range of input power levels from 11 to 27 dBm was achieved. The multi-average power levels reconfigurable Doherty amplifier was also linearized using a pruned Volterra series predistorter which allowed for an ACPR of about 47 dBc when driven with a 7.2 dB PAPR 20 MHz LTE signal centered at 2.6 GHz while the average power took on values of 21, 16 and 11 dBm.

Chapter 6

Frequency Agile Monolithic Integrated Reconfigurable GaN Doherty Power Amplifier using MEMS on GaN Integration

6.1 Introduction

The development of fully integrated power amplifiers (PAs) is predicated on the need for circuitry capable of achieving competitive performance in wireless mobile devices and handsets. These Monolithic Microwave Integrated Circuit (MMIC) PAs have to keep the competitive performance of the PAs that utilize discrete components over different operating conditions dictated by the advances in wireless communication standards. The design of fully integrated reconfigurable PAs, capable of efficiently handling signals with variable centre frequencies and PAPR, is limited by the challenges of the integration of tunable devices (e.g., MEMS devices, semiconductor varactors) with the existing active device technologies. In order to realize the demanded high power levels for base stations as well as handsets, GaN technology has become the most attractive candidate, thanks to its superior properties as discussed in Chapter 2. GaN technology works well at both high frequencies and high power levels simultaneously. RF MEMS technology, widely used for microwave applications, is favored for reconfigurable PAs for its ultra-linear behavior; the third order intercept point (IIP3) can easily reach 70 dBm. This linear behavior minimizes additional sources of nonlinearity.

The following design aims to combine the strengths of the GaN transistor and the flexibility of the MEMS devices to build a frequency agile, monolithically integrated Doherty PA (DPA). To begin with, we used our detailed design and fabricated a set of high power RF MEMS switches through the Canadian Photonics Fabrication Centre (CPFC) GaN500 MMIC process. Based on the switches' measurement results, a particular switch was selected to be the tunable element in the integrated GaN MMIC DPA which was capable of operating over three widely spaced frequencies with enhanced efficiency at 6dB back-off power level.

6.2 CPFC® GaN500 MMIC HFET Process

The most significant challenges when dealing with GaN HFET technology are the lack of foundry availability and the high expense for technology access. The available access through CMC to the NRC-CPFC Gallium Nitride MMIC foundry® brings the integration of our designed reconfigurable DPA closer to reality.

The first step in the manufacturing of the devices is to define the ohmic contact using the ohmic mask, and then to deposit the contacts. The contacts are then annealed at a high temperature to ensure low resistance for the contact. The next step in the process is the definition of the active area of the devices using the mesa mask, etching the area outside of it down to the buffer layer. The third step is to deposit the gate metal in the channel area using the gate mask. Afterwards, the wafers are passivated using a thin layer of dielectric. Openings are etched into the dielectric, where required, by defining openings in a resist layer using the VIA1 (dielectric1) mask. In the fifth step, a thin layer of nichrome (50 ohm/sq) is deposited where resistors are required. The first level of interconnect metal (1 μm of gold) is next deposited using the 1ME mask. The 1ME provides contacts to the ohmic metal and gate pads, as well as the nichrome layer. Next, a thin layer of dielectric is deposited and openings defined where required using the VIA2 (dielectric2) mask to define the vias. This layer of dielectric is used as the insulator in the MIM capacitors. In the eighth step, the areas where a second level of interconnect is required to bridge over other layers is defined with a temporary layer of a special resist using the bridge mask. Finally, the second layer of interconnect is defined using the 2ME mask. This layer is usually 1 μm of gold. 2ME is used to make the top layer of the MIM capacitors. Figure 6-1 shows the layers cross-section for the complete process, for a two-gate device.
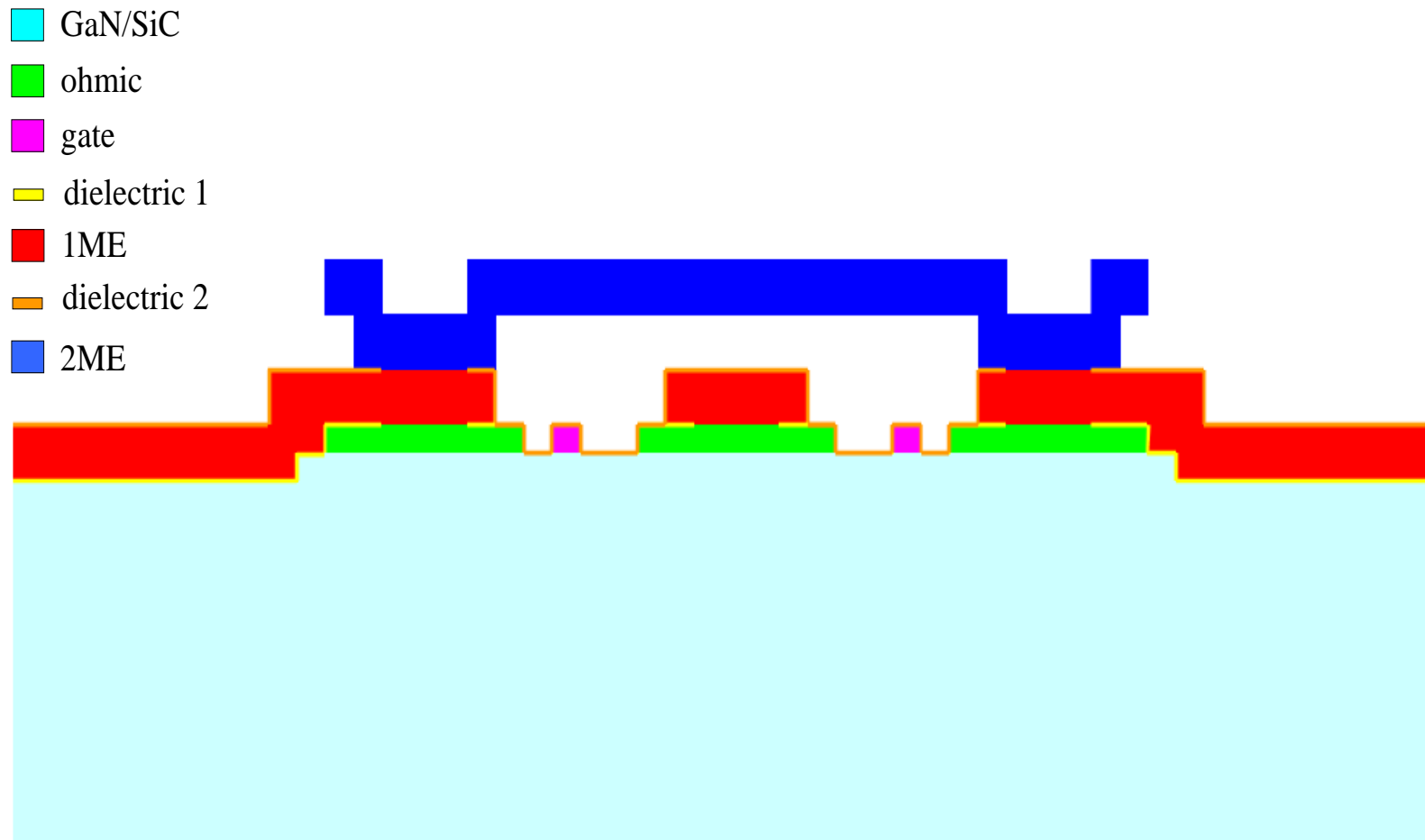
Figure 6-1, Cross-section of a 2-Gate Device with an Air Bridge Interconnection

Figure 6-2 shows an SEM photo for the GaN500 MMIC process where passive elements are fully integrated with the GaN HFET. The process therefore involves two metal layers, two dielectric layers and an Ni/Cr layer for the resistors, in addition to the layers involved in the active device fabrication. An attractive feature of the device is the available suspended air bridge, originally tailored for interconnects between 1ME metal tracks via the suspended layer 2ME. Using this air bridge, and with careful design, MEMS integration with the GaN500 process becomes viable.
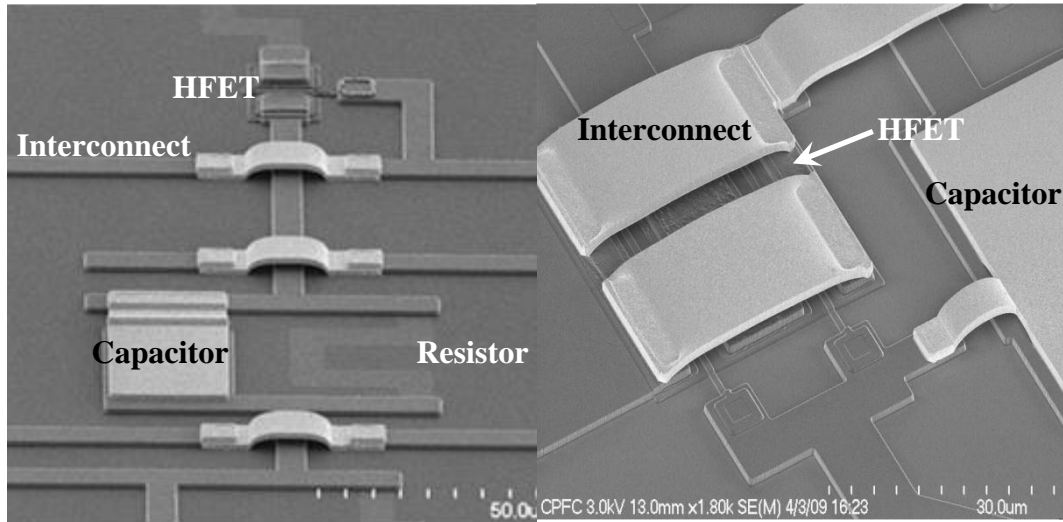
Figure 6-2, SEM Photo of CPFC® GaN500 Process Components

6.3 High Power GaN Monolithically Integrated RF MEMS Switches

The aforementioned RF MEMS technology advantages, as well as the presence of the air bridge layer in the available GaN MMIC process, motivated the selection of the RF MEMS for integration with the GaN HFET active devices. However, besides the integration challenges of MEMS devices, their relatively low switching speeds make it difficult for MEMS switches to follow envelope varying RF signals. The selected PA topology, the Doherty amplifier, achieves efficiency enhancement over the required reduced back-off power levels. As a result, the tunable devices are not asked to follow the fast changes of the incoming signals' envelopes. The reconfigurability is only required when the carrier frequency changes, which is not often, and does not require fast switching. Therefore, the lower switching speed and reliability of the MEMS switches are not serious challenges in this case.

The GaN MMIC process, which has been optimized for HFET active device operation, introduces several challenges to MEMS device design and optimization. The suspended structure's length and

width are limited to 100 and 20 um. Moreover, the measurement results of the first patch of the designed switches, portrayed in Figure 6-3, show that the air gap's actual height varies from 2 to 3 um. Beyond this, the thermal stresses accompanied with the fabrication process cause the plates to curl, increasing their stiffness. The first patch of switches had actuation voltages that were higher than the breakdown voltages of the dielectrics which made them impractical for integrated DPA design. Also, the dimensions of the sacrificial layer should be optimized to have full release of the second metal layer. It should be noted that the process does not allow the use of enclosed metal layers; therefore, no etch holes could be implemented.
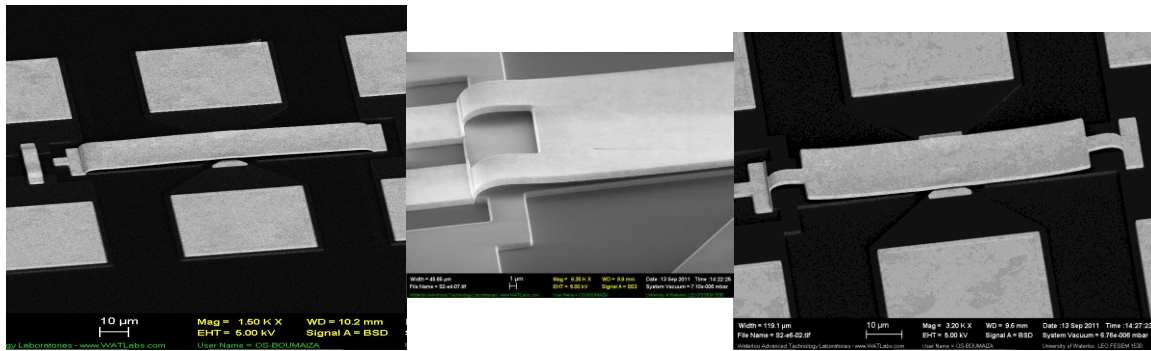
Figure 6-3, First Patch of the Fabricated RF MEMS Switches Showing the Curling in the Suspended Plates that Increases the Stiffness

As a result, the main objective in the design of the switches is to follow the process design rules but end up with switches which have actuation voltages below the breakdown limit of the process. At the same time, the switch actuation voltage has to be higher than the expected RF voltage swing for the targeted PA application (>3 times GaN active device drain bias V_{DD}, where V_{DD} of the integrated amplifier is 24V).

Addressing the design rules, three different switch designs have been proposed in Figure 6-4. These designs were optimized in order to reduce the switch stiffness following the design rules; recesses were used in the top plates. More than one design was presented in order to assess the switches' yield, as well as to compare the actuation voltages and the power handling. The yield of the designs is crucial as the switches will be part of the tunable matching networks and it is necessary to have all switches working properly. After investigating twenty fabricated switches, of each design, it was found that 95% of switches 1 and 2 survived, while switch 3 had a yield of 85%.

Switch 1
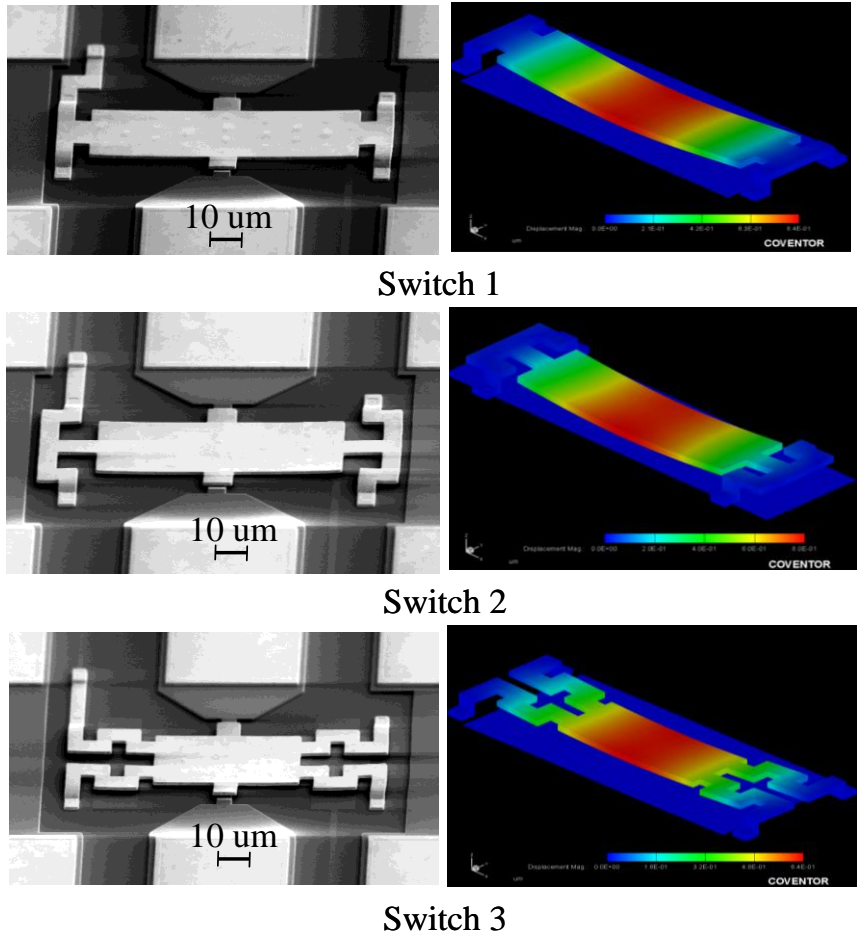
Switch 2

Switch 3

Figure 6-4, The SEM Image and the Corresponding Simulated Actuation of Each Switch Design

Figure 6-4 presents the SEM images of the fabricated switches. After extraction of the tapered line circuit models, L=0.27 nH and C_{step}=25 fF, the equivalent circuit parameters (Figure 6-5) of the switches' ON and OFF states are presented in Table 6-1. The OFF-state shunt capacitance C_g is 160 fF for all switches.
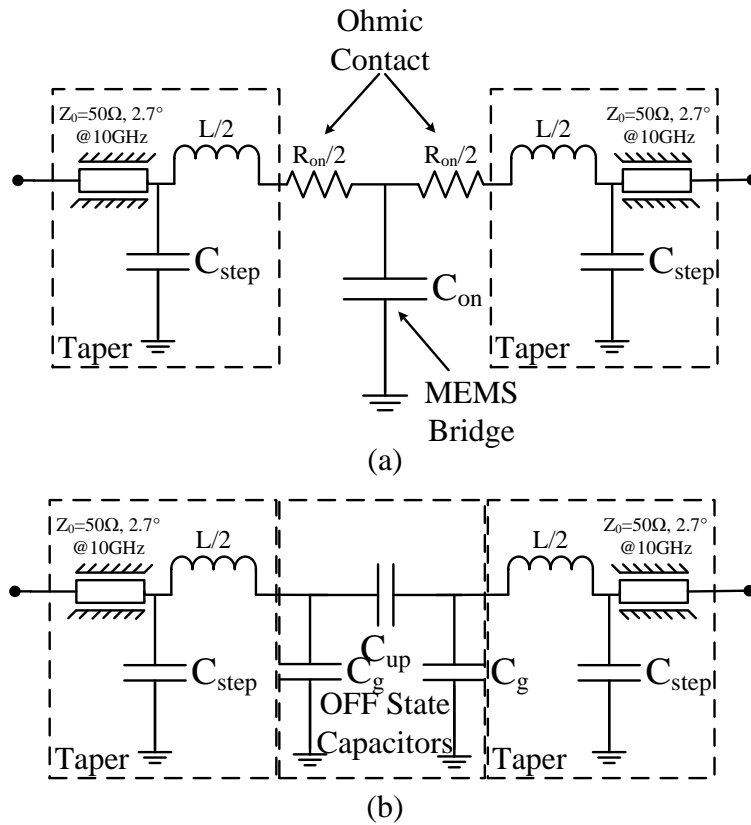
Figure 6-5, (a) ON-state and (b) OFF-state Switch Equivalent Circuit

Table 6-1, Switches Extracted Equivalent Circuit Parameters

	C_{on} (pF)	R_{on} (Ω)	C_{up} (fF)	IL at ≤ 10 GHz (dB)
Switch 1	0.308	1.35	27	0.382
Switch 2	0.3026	1.362	24.5	0.421
Switch 3	0.296	1.376	23.62	0.43

Figure 6-6 depicts good agreement between the extracted and measured S-parameters for Switch 1 [79]. The measurement of the S-parameters of the switches, in both ON and OFF states, is shown in Figure 6-7. The insertion loss of the switches did not exceed 0.45 dB, whereas, the return loss and isolation are depicted to be higher than 18 and 15 dB to 10 GHz respectively.
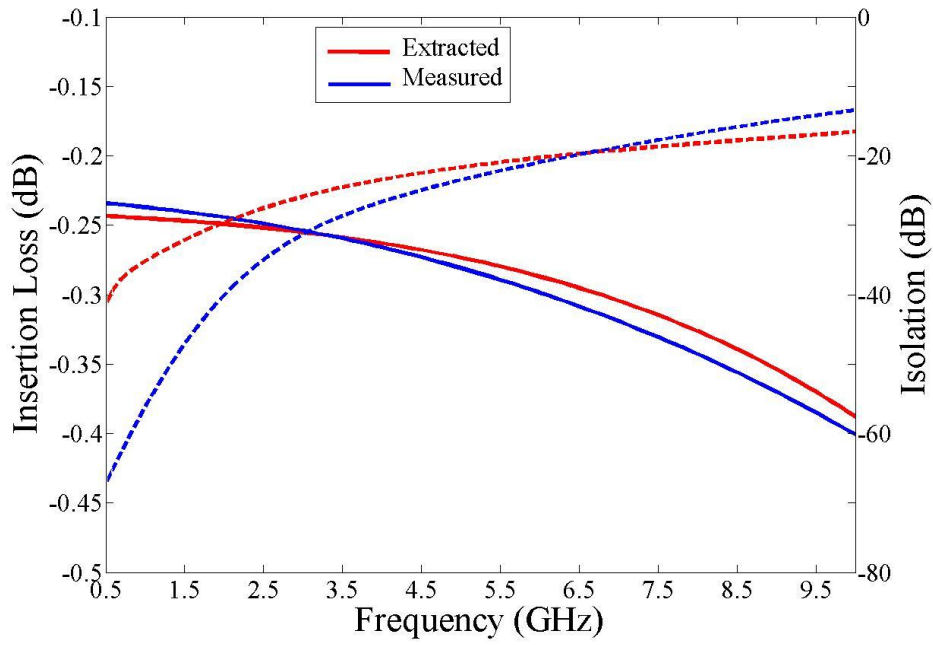
Figure 6-6, Switch 1 Extracted and Measured Insertion Loss and Isolation
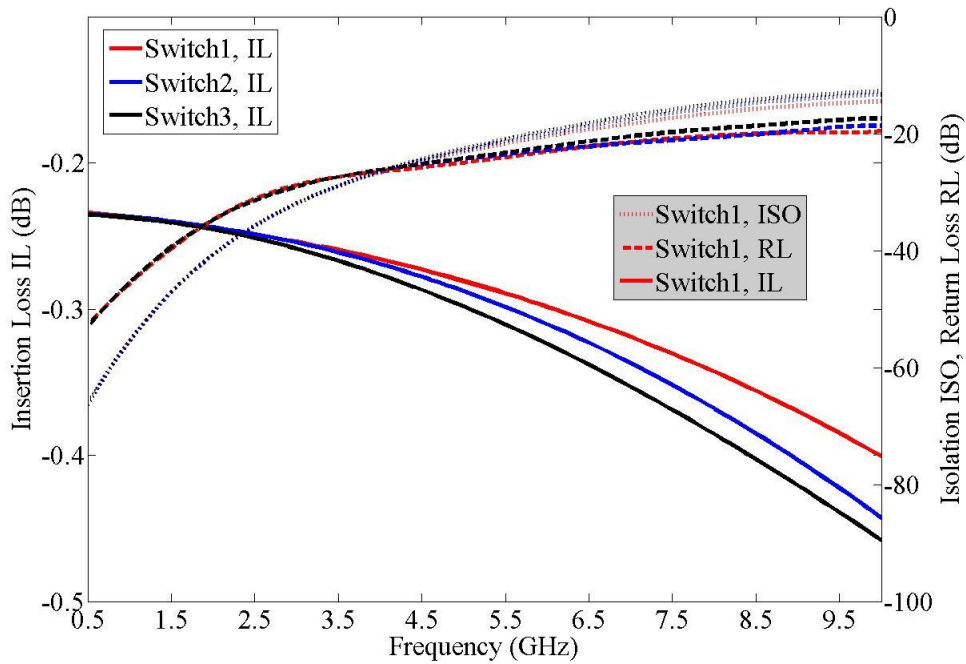
Figure 6-7, Switches Measurement Results

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Using the power handling measurement set-up, shown in Figure 6-8, and using DC actuation voltage varying from 50-80 V, switches 1, 2 and 3 managed to handle RF powers of 3.7, 3.2 and 2.9 W under hot switching conditions. Figure 6-9 demonstrates the deviation of the switches' pull-in and release voltages with the increase of the input RF power. The linearity of the three fabricated switches was assessed by measuring the third order intermodulation distortion (IMD3) using a two-tone signal with 1 MHz spacing. As illustrated in Figure 6-10, the three switches achieve IMD3 less than 45 dBc for the complete power range. Switch 1 had the most suitable measurement results in terms of yield, power handling and actuation voltage. A summary of Switch 1 measurement results is presented in Table 6-2.
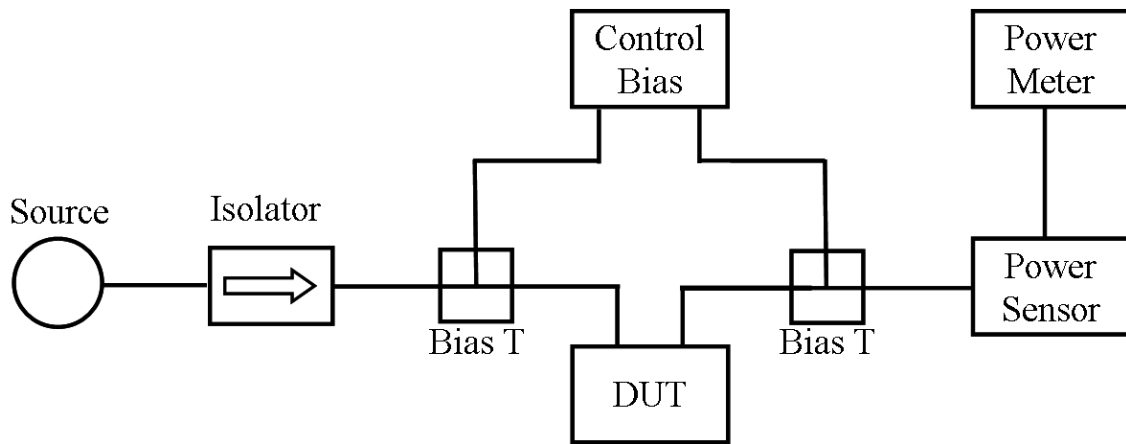
Figure 6-8, Switch Pull-in and Release Voltages Variation at Different Input RF Power Levels

Table 6-2, Switch 1 Extracted Performance Parameters

	IL at ≤ 10 GHz (dB)	RL at ≤ 10 GHz (dB)	ISO at ≤ 10 GHz (dB)	Actuation voltage (V)	Hot Switching Power Handling (W)
Switch 1	0.382	18	15	81.3	3.7
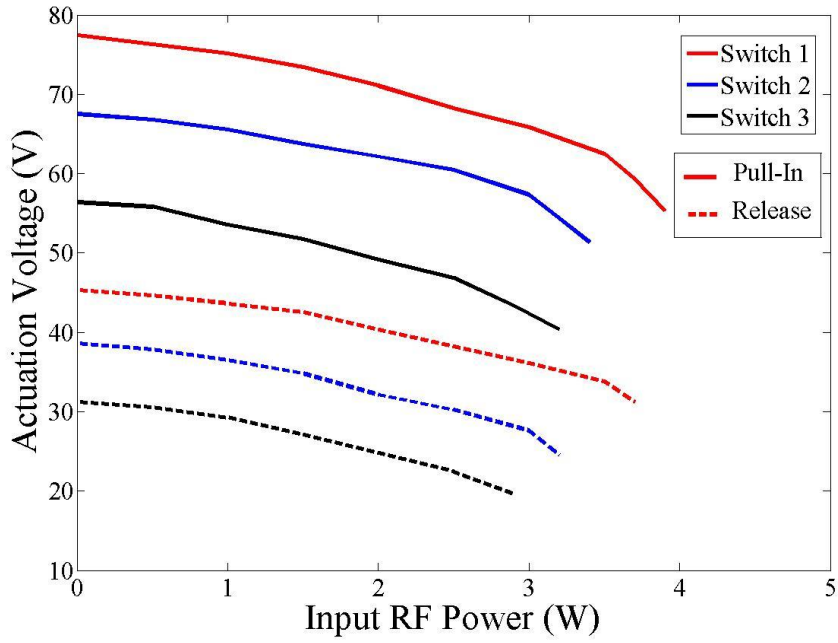
Figure 6-9, Switches Pull-in and Release Voltages Variation at Different Input RF Power Levels
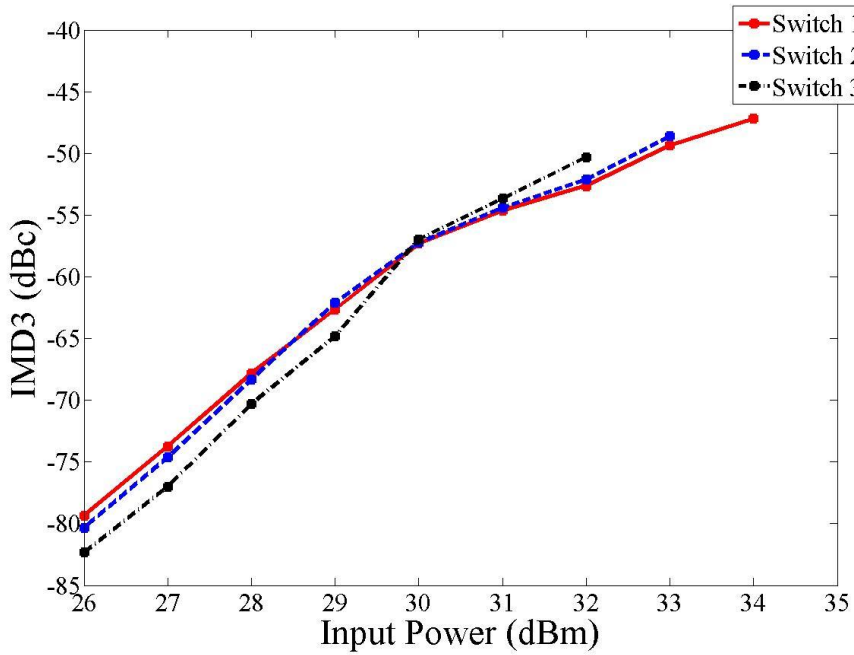
Figure 6-10, Switches Linearity Measurements

Table 6-3 shows the performance parameters of Switch 1 compared to selected state of the art switches. It is important to mention that the newly designed switches are built through a well-defined process, in a commercial foundry, using design rules to achieve very high yield. The result is that the developed switch is a good candidate to be integrated in reconfigurable amplifiers.

Table 6-3, Recent MEMS Switch Performance Summary

Ref.	Insertion Loss @ 10GHz	Return Loss @ 10GHz	Isolation@ 10GHz	Linearity Test
RMSW201HP™ [80]	< 0.45 dB	< -22 dB	> 21 dB	IIP3 > 65 dBm
RMSW101HP™ [80]	< 0.32 dB	< -21dB	> 12 dB	IIP3 > 65 dBm
[81] Oct. 2012	< 0.3 dB	< -27dB	> 28 dB	IIP3 > 70 dBm
Switch 1	< 0.4 dB	< -18dB	> 15 dB	IIP3 > 68 dBm

6.4 Multi-band Monolithically integrated GaN Reconfigurable Doherty PA

6.4.1 DPA MMIC Module Design

The successful realization of the GaN MEMS switch using the CPFC$^®$ GaN MMIC process paved the way for the implementation of the frequency agile DPA on the same process. The design of the integrated DPA [82] was carried out using the switch model extracted from the measurement data, as represented in Figure 6-7, and the large signal models of the transistors provided in the GaN process design kit. The main and auxiliary transistor sizes were selected in order to achieve a 5 W peak output power.

Based on a load pull analysis, the main and auxiliary transistors were composed of four and eight fingers each with widths of 300 um. These transistors achieved the current values necessary for the targeted output power level with the appropriate impedance terminations. The load/source pull simulations identified the optimum impedances to be presented to the input and output of both transistors at different frequencies and power levels. Those impedances were used in the synthesis of the reconfigurable input and output matching networks (IMN, OMN).

The procedure used in the frequency agile MMIC DPA design was discussed in detail in Section 4.2. Closed form design equations were developed for the OMN design using different centre frequencies and power levels. Accordingly, the MMIC DPA design underwent a similar approach to the discrete multi-frequency DPA fabricated in Section 4.3. However, the MMIC reconfigurable matching network design employed MMIC inductors, supported by the process with enhanced insertion loss, as depicted in Figure 6-11. These inductors were used in the main signal line, rather than distributed elements, in order to reduce chip size and cost. The proposed frequency agile DPA was designed to operate at 2.6, 2.14 and 1.7 GHz. The latter centre frequency was selected to be lower than the discrete PA frequency, 1.9 GHz, in order to benefit from the broader bandwidth of the integrated solution. This fact was confirmed by the load/source pull simulations that showed close values for the optimal terminations of the two centre frequencies 2.14 and 1.9 GHz.

In the IMN and OMN designs, each inductor was capacitively loaded by two shunt MEMS switches connected to fixed MIM capacitors to shift the DPA centre frequency from the initial value of 2.6 GHz to one of the other two bands: 2.14 or 1.7 GHz. A circuit schematic for the MMIC reconfigurable IMN/OMNs is shown in Figure 6-12.
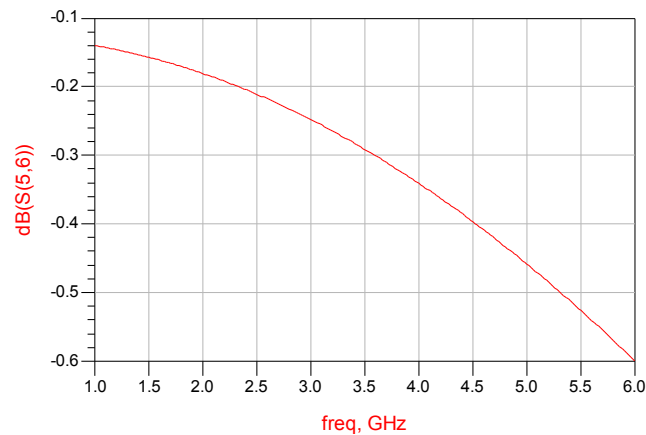
(a)
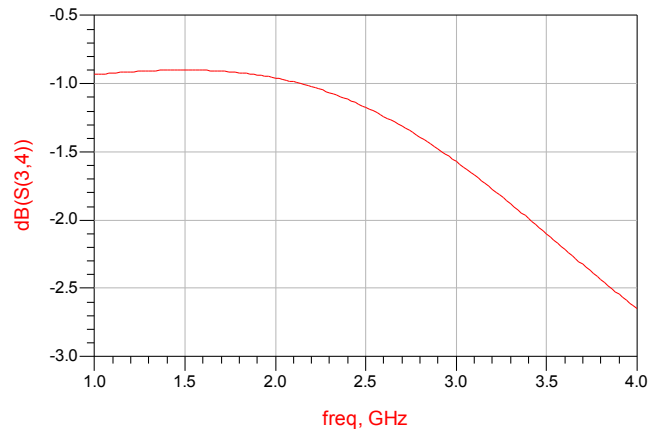
(b)

Figure 6-11, Simulated Insertion Loss for (a) 3 Turns and (b) 9 Turns MMIC Inductors with 250 um Side Length
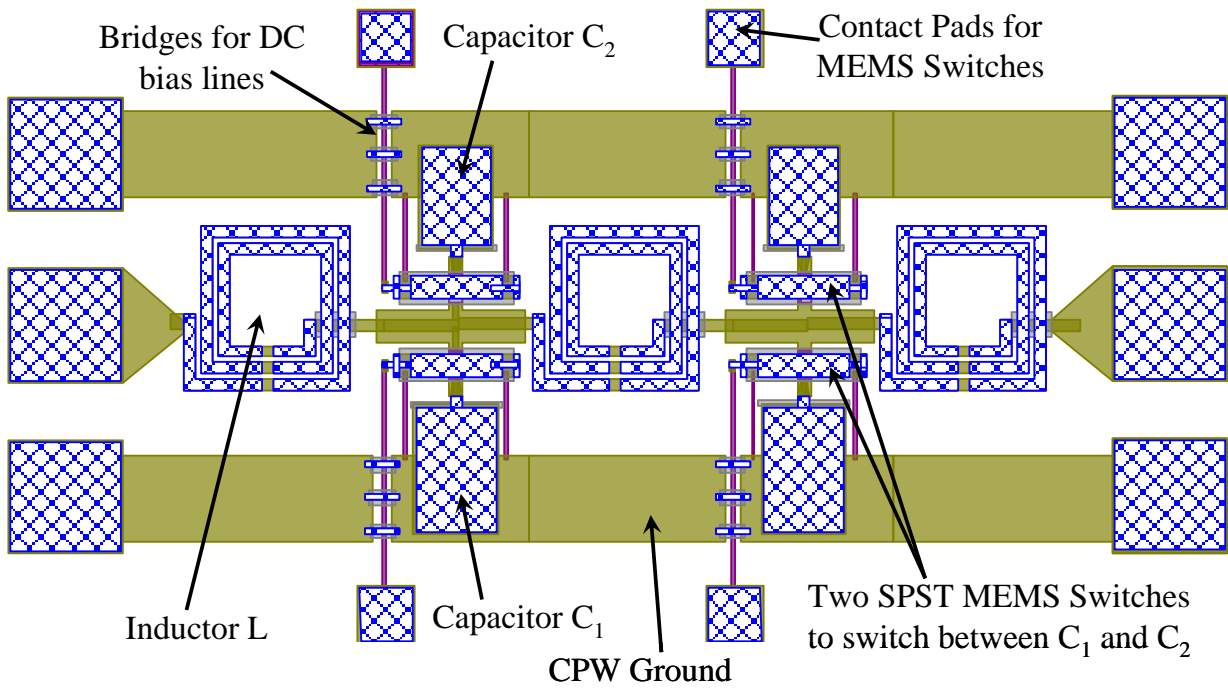
Figure 6-12, Circuit Schematic for the Matching Networks of the Integrated Reconfigurable DPA

Simulations proved that six pairs of MEMS switches, two in each OMN and two in the main transistor IMN, were needed to satisfy the conditions required for the DPA. In order to enhance the efficiency in the last 6 dB back-off, p was set to 2 in the design equations, for 1.7, 2.14 and 2.6 GHz. The advantage of having a non-reconfigurable output combining network was used efficiently by fabricating the impedance inverters off-chip reducing the area used in the expensive GaN process. Figure 6-13 shows a picture of the frequency agile demonstrator including the MMIC module attached to the off-chip fixed combining network.
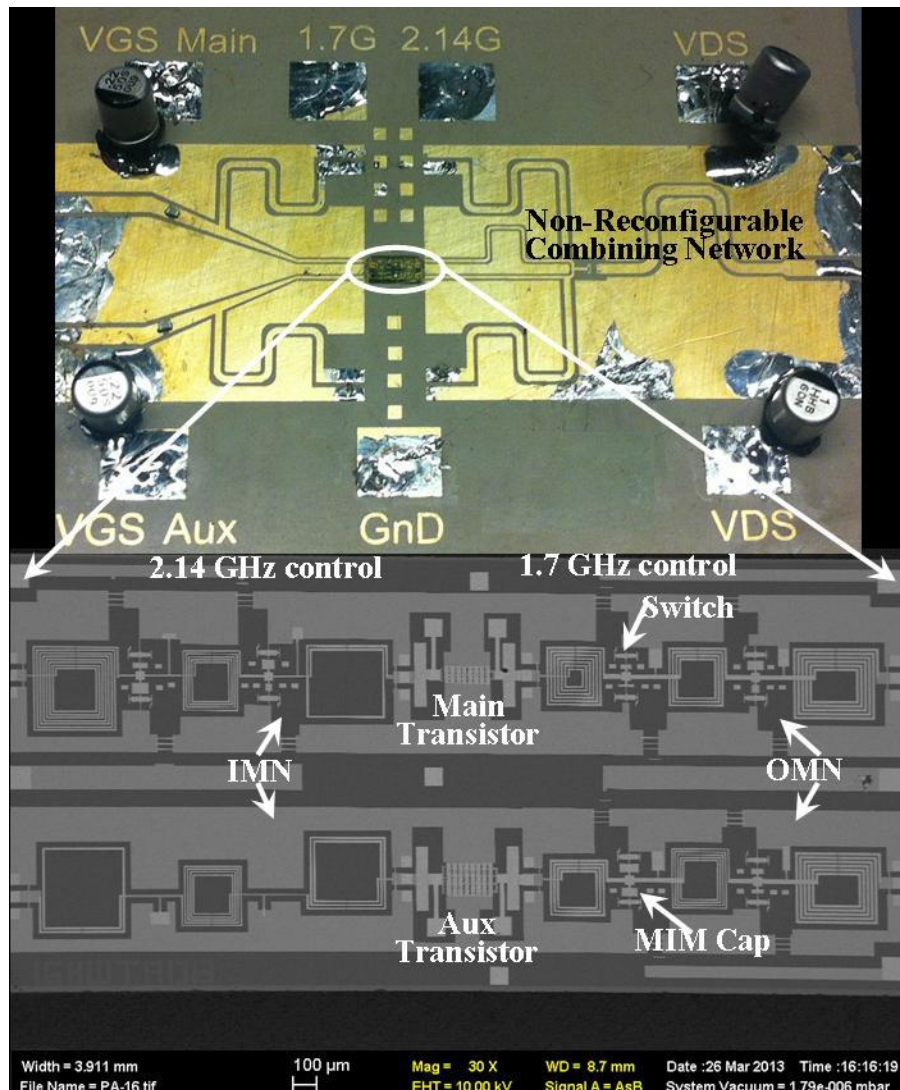
Figure 6-13, Frequency Agile Monolithic GaN DPA [82]

6.4.2 DPA MMIC Measurement Results

The measured gain and peak power output power of the DPA were higher than 9.5 dB and 36 dBm, respectively, at the three frequencies. As seen in Figure 6-14, the designed demonstrator satisfied Doherty load modulation requirements in the three operating frequencies, deduced from the significant efficiency improvement in the back-off region. Drain efficiency in excess of 50% was maintained in the last 6 dB power range for the three frequency bands. Figure 6-15 depicts a small signal gain of 9.5 dB at the three targeted frequencies with the same nonlinearity trend.
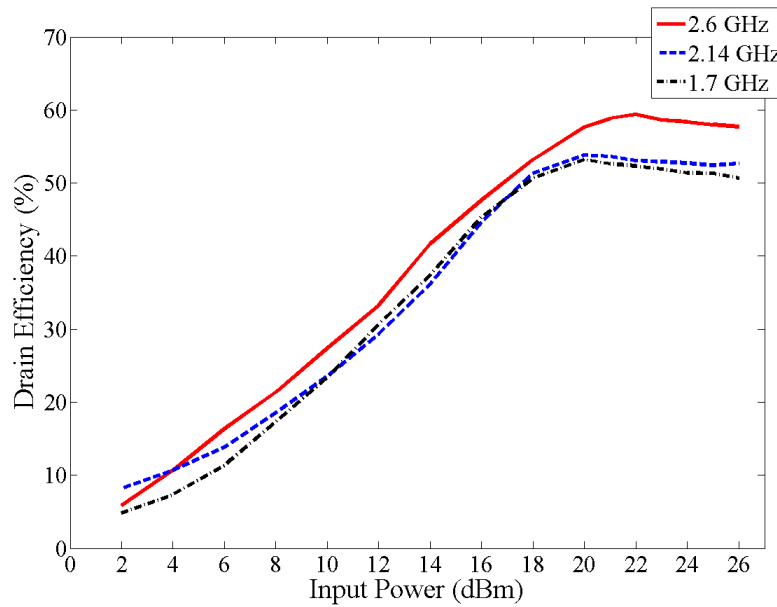
Figure 6-14, Measured Drain Efficiency at 1.7 GHz, 2.14 GHz and 2.6 GHz
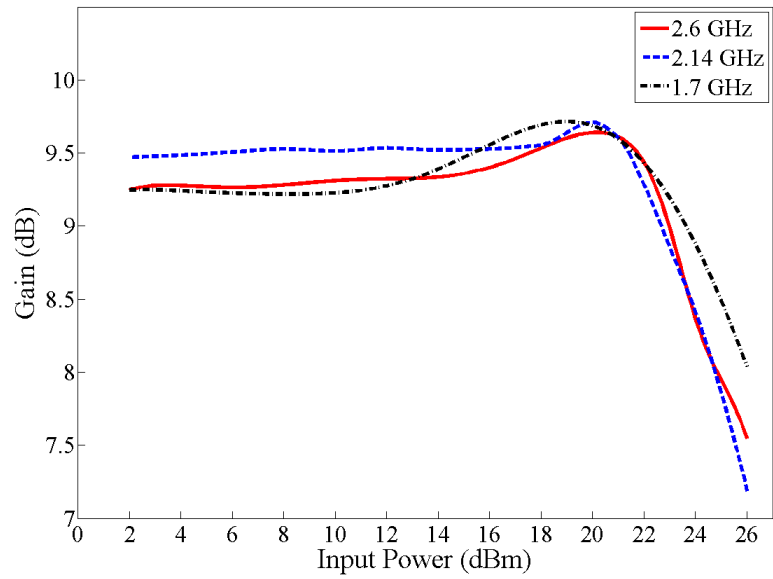
Figure 6-15, AM/AM Measurement Results at the Three Operating Frequencies

Conclusion

For modern wireless communication systems, the design of RF front ends attracts great concern thanks to the continuously increasing user requirements and system complications. Nowadays, RF circuitry has to efficiently handle signals of diverse communication standards with dissimilar power levels and time domain statistics and wide spread centre frequencies. In the RF front end, the power amplifier is the main component responsible for supplying the transmitted wireless signals with sufficient power levels without affecting linearity to minimize signal distortion. Therefore, the realization of power amplifiers capable of targeting the wide range of operating frequency bands, bandwidths, dynamic network loads and time domain signal variations is a critical attribute.

In this thesis, the main goal of the introduced work was the development of adaptive power amplifiers that can sustain excellent performance under different deployment scenarios dictated by diverse communication standards. In this work, this goal was achieved by implementing reconfigurable matching networks which included optimal input and output terminations, at various centre frequencies and power levels, in both single ended high efficiency power amplifiers and modified Doherty power amplifier (PA) circuitry, in order to maintain back-off efficiency enhancement.

The first research step presented a novel tunable matching network schema suitable for the design of reconfigurable RF front ends. The network included a harmonic tuning feature essential to the design of high efficiency power amplifiers (HEPAs). Two different types of electronically tunable devices, namely MEMS switches and semiconductors varactors, were used in the realization of the MNs. The prototypes proposed were found to have excellent coverage at multi-bands with reflection coefficient $|\Gamma| < 0.85$ and insertion loss IL<1.3 dB. The varactor-based network was used for efficiency enhancement of class F-1 PAs using load modulation technique. This network allowed for efficiency improvement of about 18% at 6 dB back-off at 2.4 GHz.

Utilizing the Doherty PA schematic, a reconfigurable frequency agile DPA design capable of maintaining high efficiency was used to amplify multi-mode wideband signals. For that a detailed and meticulous methodology was developed. This design methodology was applied to design a tri-band 10 W Doherty amplifier which operated at 1.9 GHz, 2.14 GHz and 2.6 GHz. The measurement of the DPA prototype affirmed the proper load modulation over the three targeted frequencies. This manifested in excellent drain efficiencies of about 70% at peak power levels and 60% at 6 dB back-off. The tri-band reconfigurable DPA was also linearized, demonstrated ACPR higher than 50 dBc,

could be used with a pruned Volterra series predistorter and allowed for adjacent 20 MHz 4C-WCDMA and 20 MHz LTE signals located at the three targeted frequencies.

Targeting multi-standard DPA operation, the design methodology was modified to implement a reconfigurable DPA capable of efficiently amplifying signals with variable peak-to-average power ratio (PAPR). The fabricated 40 dBm demonstrator operated at 2.6 GHz and demonstrated average power added efficiencies of 64, 63 and 59% at 6, 9 and 12 dB power back-offs, respectively. The output signal of the DPA proved to have an ACPR of higher than 46 dBc when driven with WCDMA signals with variable PAPR.

Combining previous reconfigurabilities, the design of an electronically tunable multi-frequency multi-standard DPA was expounded which maintained high efficiency when driven by highly varying wideband signals. The same design procedure was used to develop systematic closed-form design equations that involved compensating for the deviation of Doherty distributed elements with the operating frequency and targeted back-off power levels. This methodology was applied to design a tri-band 40 dBm DPA for operation at 1.9, 2.14 and 2.6 GHz, capable of maintaining high efficiency at back-off power levels of 6, 9 and 12 dB. The measurement of the Doherty PA confirmed drain efficiencies of about 67% at peak power levels and 59% at 12 dB back-off. The fabricated demonstrator proved its linearizability with ACPR of about 47 dBc when driven with 4C-WCDMA and 20 MHz LTE signals located at the targeted frequencies while PAPR varied from 7 to 11.6 dB.

Similarly, a complete set of closed form design equations was generated which targeted the achievement of DPA circuit reconfigurability for different peak and average power levels as dictated by the dynamic load nature of the communication networks. The next step in the proposed work developed an electronically reconfigurable DPA capable of maintaining excellent performance over a wide range of average power levels. The design procedure adjusted the DPA optimum load impedance value and the necessary reconfiguration required of the Doherty output matching networks to compensate for the load impedance change. The fabricated DPA demonstrator was designed to operate at 2.6 GHz and to maintain its performance at average input power levels of 21, 16 and 11 dBm. The measured power added efficiencies were higher than 62% for the full range of the targeted power levels. The demonstrator linearizability was proven as well.

The final objective of the presented work confirmed a monolithically integrated frequency-agile DPA on CPFC MMIC GaN500 process. The same methodology, used for designing the discrete frequency-agile DPA, helped with the design and optimization, size and cost of the MMIC module,

by substituting the required tunable matching network with two integrated matching networks and one off-chip fixed bulky combining network. The first step in designing such an integrated frequency-agile DPA was the integration of tunable devices on the selected MMIC process. GaN monolithically integrated MEMS switches were designed and optimized within the given process restrictions to achieve high actuation voltage and high power handling. Excellent results were obtained in terms of insertion loss (< 0.4 dB), power handling (more than 3.7 W) and linearity (IIP3 > 68 dBm). The switch paved the way for implementing the integrated tunable matching networks with minimum performance overhead. The fabricated 37 dBm DPA operated at three desired centre frequencies; 1.7, 2.14 and 2.6 GHz, and confirmed drain efficiencies at 6 dB back-off of more than 53% at all the targeted bands with a small signal gain of about 10 dB.

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