



Procedia Computer Science

Volume 41, 2014, Pages 114-119



BICA 2014. 5th Annual International Conference on Biologically
Inspired Cognitive Architectures

Memristive Operational Amplifiers

Timur Ibrayev¹, Irina Fedorova¹, Akshay Kumar Maan^{2, 3}, and Alex Pappachen James^{1*}

¹Nazarbayev University, Kazakhstan. ²Griffith University, Australia. ³Enview R&D Labs, India. apj@ieee.org

Abstract

The neuronal algorithms process the information coming from the natural environment in analog domain at sensory processing level and convert the signals to digital domain before performing cognitive processing. The weighting of the signals is an inherent way the neurons tell the brain on the importance of the inputs and digitisation using threshold logic the neurons way to make low level decisions from it. The analogue implementation of the weighted multiplication to input responses is essentially an amplification operation and so is the threshold logic comparator that can be implemented using amplifiers. In this sense, amplifiers are essential building in the development of threshold logic computing architectures. Specifically, operational amplifier would act as the best candidate for use with threshold logic circuits due to its useful properties of large gain, low output resistance and high input resistance. In this paper, a reconfigurable operational amplifier is proposed based on quantised conductance devices in combination with MOSFET devices. The designed amplifier is used to design a threshold logic cell that has the capability to work as different logic gates. The presented quantised conductance memristive operational amplifier show promising performance results in terms of power dissipation, on-chip area and THD values.

Keywords: Neuromorphic computing, Threshold Logic, Memristors, Amplifiers

1 Introduction

The need to develop operational amplifiers that can handle wide range of gains with low on-chip area is essential for developing futuristic neuron inspired computing devices [1-2]. Operational amplifiers due to their property of wide gain control, bandwidth and impedance matching satisfy the idealised requirements of an amplifier [3], [4], [5]. In cognitive computing architectures that are inspired from the neuronal models, the amplifiers find use in the amplification of signals between the hierarchical network layers arranged in a modular manner [6], [7], [8]. The signal deformation

^{*}Corresponding author

between the network layers needs to be minimised to ensure proper working of the network [9], [10], [11]. The increase in complexity requires a wider use of amplifiers in the design of analog neural networks for meeting signal stability and conditioning requirements [12], [13]. The need for amplification is different from one layer to another, and the problem become even more complex with the increase in the number of layers and number of neurons [14], [15].

The ability to program the properties of the amplifiers offer additional levels of flexibility to ensure improved signal quality between network layers [16], [17], [18]. The aim of this paper is to report the first of its kind application of quantised memristive devices in designing a programmable operational amplifer useful for neural network implementations. Through this paper, we present the possibility to configure open loop gain of the operational amplifier with improving the circuit implementation with lower on chip area and lower leakage currents than conventional MOSFET based implementations.

2 Quantised Conductance Amplifier Configurations

The need for reduced area and larger packaging densities is uncovering the limitations of scaling circuits beyond the fundamental limits. Newer devices and technologies are required to be explored to reduce the issue of leakage currents and lower area. In neuromorphic chips, memristor like devices offer useful alternative to existing CMOS based technologies [19]. In quantised conductance memristive devices, the individual switching states contain quantised conductance $G_0(=2e^2/h)$ where $G_0(=2e^2/h)$ is the charge of electron and $G_0(=2e^2/h)$ and enables the discretized control of resistor values.

In early design of amplifiers, the resistors have been used as load resistors and also a way to control the current flow to the circuit as a biasing element. However, semiconductor resistors need a large area to implement variable resistor values, in addition to having issues of leakage currents. Memristors in general only offer two resistors states, however, they have low leakage currents and are smaller in area. They are also proved to be compatible with the CMOS processes, making it a practical alternative to resistors in analog circuits. Retaining the properties of memristors, the quantized conductance can be used to achieve a different levels of resistor values useful for controlling the load currents in the amplifier.

2.1 Differential Amplifier

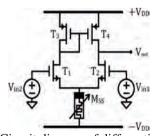


Figure 1: Circuit diagram of differential amplifier

Fig. 1 represents the differential amplifier configuration with the variable memristive element M_{SS} -Transistors T_1 and T_2 as well as the other two transistors T_3 and T_4 are in parallel. Common Mode gain A_{CM} for the differential pair is expressed as :

$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}},\tag{1}$$

where ΔV_{out} is the single-ended output parameter and $\Delta V_{in,CM}$ is the common mode input change. It could be further shown that:

$$A_{CM} \approx \frac{-\frac{1}{2g_{t3,4}} \left| \frac{m_{o3,4}}{2}}{\frac{1}{2g_{t1,2}} + M_{SS}} = \frac{-1}{1 + 2g_{t1,2}M_{SS}} \frac{g_{t1,2}}{g_{t3,4}},\tag{2}$$

Where $g_{m3,4}$ and $m_{o3,4}$ are the transconductance and output resistance of the transistors T_3 and T_4 respectively and $g_{m1,2}$ is the transconductance of the transistors T_{1} and T_{2} .

2.2 Operational Amplifier

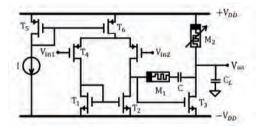


Figure 2: Circuit diagram of operational amplifier

Figure 2 shows the circuit diagram of the operational amplifier incorporating the quantised conductance memristive devices.

$$g_{m} = \sqrt{2I_{D}k'\frac{W}{L}}$$

$$A_{CL} = \frac{\Delta V_{o}/\Delta t}{\Delta V_{i}/\Delta t} = \frac{SR}{\Delta V_{i}/\Delta t}$$
(3)

(4)

where A_{CL} is a close loop voltage gain, SR is slew rate of the opamp which is dependent on the memristances in the opeamp. This operational amplifier can be use can used as a comparator in threshold logic as shown in Fig. 3.

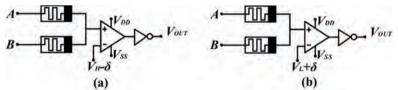


Figure 3: (a) NAND and (b) NOR configuration using memristivethreshold logic

Figure 3 shows one future application of the proposed operational amplifier. The figure shows a memristor based NAND and NOR configuration, where the cell structure is same. The functionality difference is achieved by changing the reference voltage applied to the -ve terminal of the op-amp. Hence the size and speed of the op-amp is very crucial in the total performance of the logic cell. The improved power dissipation and chip area will make the memristorthreshold logic[20]more closer in performance with corresponding CMOS logic gates.

3 Experimental Results

The quantised conductance device offers different resistor values in its working states, and we make use of this to adjust the gain of the amplifiers. The ability of the memristor like devices to be programed to different logic state enable the practical realisation of these amplifiers as tunable open loop amplifiers within integrated circuits paradigm. Our quantised conductance memristive device offer resistances of $1.72k\Omega$, $1.99k\Omega$, $2.15k\Omega$, $3.23k\Omega$, $6.45k\Omega$ and $8.60k\Omega$. The simulations were done using BSIM models and memristors SPICE model for simulating the quantized conductance devices. The parameters from the IBM process technology for different technology size were used for the BSIM models to emulate realistic implementations.

Fig. 4(a) shows frequency response of the differential gain magnitude for various memristor device values M_{SS} applied with the 0.18 technology of the transistors. The variations in the value of memristor device makes it possible to alternate the value of the differential gain for the differential amplifier. Fig. 4(b) shows the effect of technology scaling on the differential gain magnitude at the M_{SS} =1.72k Ω . Because of the similarity in gain magnitude and bandwidth, it is possible to have practical implementation of memristor devices in differential amplifiers for different purposes.

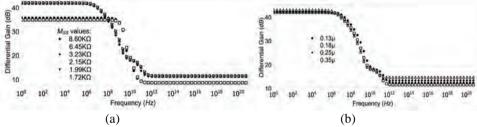


Figure 4: (a) Graph for differential amplifier showing differential gain for various values of M_{SS} . (b) Graph for differential amplifier showing differential gain for various technologies at memristor value of M_{SS} =1.72k Ω

Fig. 5(a) shows frequency response of differential gain magnitude for various memristor values M_2 used in operational amplifier design. It could be observed that for operational amplifier different gain values can be achieved by changing the values of the memristor. Fig. 10(b) shows how the change in technology affects the differential gain obtained by the operational amplifier at the values of memristor M_2 =1.72k Ω .

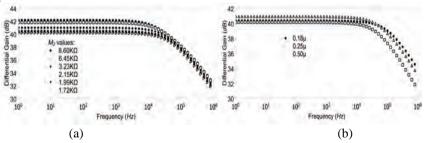


Figure 5: (a) Graph for operational amplifier showing differential gain for various values of M_2 (b) Graph for operational amplifier showing the effect of technology change at memristor value of M_2 =1.72k Ω

Fig. 6 shows the dependency of output resistance on memristance values for two different configurations. It could be observed that the results are in agreement with the corresponding equations describing behaviour of the amplifiers.

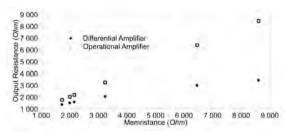


Figure 6: Graph showing output resistance versus memristance values for each of three amplifier types.

Table 1: The table indicating the performance measures for different amplifier configurations

	Quantised Conductance Memristors		
Configuration	Area $(pm^2)^a$	Power $(\mu W)^{b}$	THD (%)
Differential	32.90	1805.512	0.601°
Operational	787.54	122.6548	1.833 ^d

^a - assuming memristor dimensions to be 185nm*112nm; ^b - values are taken at M=1.72k Ω ; ^c - input is sine signal (amplitude=10 mV, frequency=1kHz); ^d - input is sine signal (amplitude=0.1mV, frequency=1kHz)

The circuit performance in terms of the area required for implementation of the circuit, power consumption and Total Harmonic Distortion (THD) for each of the three configurations are presented in the Table 1. Area for operational and differential amplifiers were calculated taking into account each transistor and memristor of the circuit. These values are lower than that uses semiconductor resistors or pseudo-resistors of MOSFETs. In addition, the simplicity in the design without the need to increase the circuit complexity makes it a useful alternative in mainstream circuit design.

4 Conclusion

This paper provides the introductory idea of using memristive based devices in operational amplifier design that can find application in wide range of circuits, and in particular support the threshold logic implementations. The results of the simulations showed the improved performance of the operational and differential amplifiers in terms of the area, power and THD when implemented using the memristor elements instead of the conventional resistors or pseudo-resistors. The programmability of the open loop properties of the opamp is one of major advantages presented in the approach, which is practically not possible with conventional operational amplifier designs. Improving the speed of operation and reducing the area requirements for sub-nanometer technology size remains an open problem, and could further enhance use of it.

References

- [1] Rajendran, Jeyavijayan, et al. "Memristor based programmable threshold logic array." *Proceedings of the 2010 IEEE/ACM International Symposium on Nanoscale Architectures.* IEEE Press, 2010.
- [2] Ng, Kian Ann, and Pak Kwong Chan. "A CMOS analog front-end IC for portable EEG/ECG monitoring applications." *Circuits and Systems I: Regular Papers, IEEE Transactions on* 52.11 (2005): 2335-2347.
- [3] Mallinson, Martin, and Paul Spitalny. "Programmable gain amplifier." U.S. Patent No. 5,233,309. 3 Aug. 1993.
- [4] Hall, Tyson S., et al. "Large-scale field-programmable analog arrays for analog signal processing." *Circuits and Systems I: Regular Papers, IEEE Transactions on* 52.11 (2005): 2298-2307.
- [5] Harrison, Reid R., et al. "A CMOS programmable analog memory-cell array using floating-gate circuits." *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on* 48.1 (2001): 4-11.
- [6] Türel, Özgür, and Konstantin Likharev. "CrossNets: Possible neuromorphic networks based on nanoscale components." *International journal of circuit theory and applications* 31.1 (2003): 37-53.
- [7] Afifi, Ahmad, Ahmad Ayatollahi, and FarshidRaissi. "STDP implementation using memristivenanodevice in CMOS-Nanoneuromorphic networks." *IEICE Electronics Express* 6.3 (2009): 148-153.
- [8] Afifi, A., A. Ayatollahi, and F. Raissi. "Implementation of biologically plausible spiking neural network models on the memristor crossbar-based CMOS/nano circuits." *Circuit Theory and Design*, 2009. ECCTD 2009. European Conference on. IEEE, 2009.
- [9] Turel, O., et al. "Nanoelectronicneuromorphic networks (crossnets): new results." *Neural Networks*, 2004.Proceedings.2004 IEEE International Joint Conference on. Vol. 1.IEEE, 2004.
- [10] Likharev, Konstantin, et al. "CrossNets: High-Performance Neuromorphic Architectures for CMOL Circuits." *Annals of the New York Academy of Sciences* 1006.1 (2003): 146-163.
- [11] Türel, Özgür, et al. "Neuromorphic architectures for nanoelectronic circuits." *International Journal of Circuit Theory and Applications* 32.5 (2004): 277-302.
- [12] Alspector, Joshua. "Neuromorphic learning networks." U.S. Patent No. 4,874,963. 17 Oct. 1989.
- [13] Indiveri, Giacomo, ElisabettaChicca, and Rodney J. Douglas. "Artificial cognitive systems: from VLSI networks of spiking neurons to neuromorphic cognition." *Cognitive Computation* 1.2 (2009): 119-127.
- [14] Widrow, Bernard, David E. Rumelhart, and Michael A. Lehr. "Neural networks: Applications in industry, business and science." *Communications of the ACM*37.3 (1994): 93-105.
- [15] Boser, Bernhard E., et al. "An analog neural network processor with programmable topology." *Solid-State Circuits, IEEE Journal of* 26.12 (1991): 2017-2025.
- [16] Xiang, Li, et al. "A method for analog circuits fault diagnosis by neural network and virtual instruments." *Intelligent Systems and Applications (ISA), 2011 3rd International Workshop on.*IEEE, 2011.
- [17] Stoica, Adrian, et al. "Evolution of analog circuits on field programmable transistor arrays." Evolvable Hardware, 2000.Proceedings.The Second NASA/DoD Workshop on.IEEE, 2000.
- [18] Giannini, Vito, et al. "Flexible baseband analog circuits for software-defined radio frontends." *Solid-State Circuits, IEEE Journal of* 42.7 (2007): 1501-1512.
- [19] Mehonic, A., et al. "Quantum Conductance in Silicon Oxide Resistive Memory Devices." *Scientific reports* 3 (2013).
- [20] James, Alex Pappachen, Linu Rose VJ Francis, and Dinesh S. Kumar. "Resistive threshold logic." *IEEE Transactions on Very Large Scale Integration(VLSI) Systems.* (2014): Vol 22. No. 1: 190-195