Energy Position of the Active Near-Interface Traps in Metal−Oxide−Semiconductor Field-Effect Transistors on 4H−SiC

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Based on the insight that the Fermi level in a metal–oxide–semiconductor field-effect transistor (MOSFET) channel is set in the conduction band, due to the quantum confinement of the channel electrons, this letter provides an experimental demonstration that the near-interface traps responsible for degradation of channel-carrier mobility in SiC MOSFETs are energetically aligned to the conduction band of SiC. The experimental demonstration is based on conductance measurements of MOS capacitors in accumulation. The accumulation conductance does not change with temperature, which demonstrates that there is channel-carrier communication with the near-interface traps by tunneling.

Favourable intrinsic properties, such as high bulk carrier mobility, high breakdown field, and high thermal conductivity, make SiC a very attractive material for use in high power semiconductor applications[1]. In recent years, SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) have become commercially available due to the rapid maturity in material processing and device technology. In light of these advances, SiC MOSFETs are poised to become the main control switch

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over pre-existing Si based devices, offering substantial advantages in applications where high power, temperature, and frequency are required.

Although commercial SiC MOSFETs are now available, their performance is still far from theoretical limits. The 4H-SiC polytype is the material of choice owing to its high bulk mobility of electrons, however the performance of n-channel 4H-SiC MOSFETs is still limited by very low mobility of the electrons in the MOSFET channel. Extensive research has attributed the low mobility to a large density of shallow acceptor-type near-interface oxide traps (NITs) that are energetically located near the bottom of the conduction band (E_C) in the 4H-SiC energy gap[2]. The exact origin of these NITs is yet unclear although it has been speculated that they are associated with electrically active carbon and other related defects formed in the oxide, near the SiC–SiO_2 interface during the thermal oxidation process[3]. Vast improvements of this interfacial region have been realised by growing or annealing gate oxides in nitric oxide (*NO*) ambients. Nitridation methods are known to significantly reduce the density of NITs [3-7]and increase channel mobility[8,9] although it is still far from the bulk mobility limit. Evidently a strong link exists between the large density of near-interface traps and the channel-electron mobility of 4H-SiC MOSFETs. Therefore, it is important to correctly characterise and determine the nature of these NITs to enable further improvements in the mobility of SiC MOSFETs. Previous research has focused on NITs that are energetically located in the SiC energy gap, based on measurements of capacitance–voltage (C–V) curves and conductance of MOS capacitors in depletion. The NITs that are aligned to the energy gap, which are active when a MOSFET is biased in the depletion mode, can impact the threshold voltage of a MOSFET. However, these NITs cannot explain the large

reduction of channel-electron mobility of MOSFETs biased in the strong-inversion region. Given that the quantum-confinement effect in the channel of a MOSFET in strong inversion sets the Fermi level inside the conduction band, it becomes important to investigate potential existence of NITs with energy levels that are aligned to the conduction band. It is possible to explain the occupancy of NITs aligned to the conduction band without surface quantization, which means using the classical approach where the Fermi level remains well below $E_{C.}$ However, this approach would be less realistic given that the quantum-confinement effects in MOS inversion layers do exist.

In this letter, we show that alternating-current (AC) conductance measurements on N-type MOS capacitors in accumulation based on the quantum-confinement effect, can be used to identify the NITs that can directly impact channel-carrier mobility in SiC MOSFETs.

Quantum confinement effects are pronounced in the channel of MOSFETs because of the very high electric fields and, consequently, very narrow energy wells confining the channel electrons. The quantum confinement of carriers to a potential well that restricts the carrier motion in two dimensions is characterized by quantized two-dimensional energy subbands inside the conduction band[10-14], as illustrated in Fig. 1. Given that the bottom of the lowest two-dimensional subband (E_0) is well above the energy that corresponds to the bottom of the three-dimensional conduction band (E_C), the channel electrons do not appear in the two-dimensional subbands before the surface energy bending is so strong that the Fermi level appears well above E_C. The location of the Fermi level well above *Ec* is consistent with the SiC inversion layer subband structures determined by Pennington *et al.*[14].

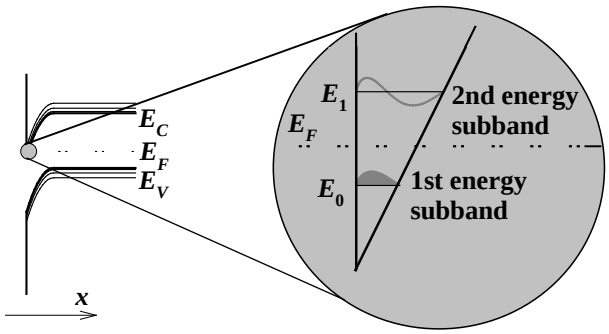

FIG. 1. Illustration of the quantum well and the formation of two-dimensional subbands in a strongly inverted semiconductor surface. The Fermi level (E_F) appears above the bottom of the first energy subband (E_0) and well above E_C (the bottom of the triangular potential well). Reproduced by permission of Oxford University Press, from *Principles of Semiconductor Devices*, Second Edition, by Sima Dimitrijev (2011), Figure 10.5 from p. 418, see Ref. 13.

Physical models and simulations to quantify quantum confinement effects on 4H-SiC MOSFET conduction-band trap occupancy, employing the density gradient formalism[15] and density functional theory[16], have been investigated. They have shown excellent comparison to experimentally measured MOSFETs with significant differences observed in trap occupancy compared to classical methods implying that quantum confinement effects should be considered while evaluating trap distributions.

Given that the quantum confinement effect sets the Fermi level in strong inversion well above E_C, the electrons from the inversion layer are able to directly communicate with near-interface traps whose levels are aligned to the conduction band by tunneling. Figure 2(a) illustrates these effects on a strongly inverted P-type substrate to form the N-type channel in a SiC MOSFET. The Fermi level is positioned above

E_C at the SiC–SiO_2 interface due to the additional band bending caused by the quantum confinement of electrons. Any NITs with energy levels below the Fermi level have a high probability of electron occupancy. These trapped electrons are therefore unavailable for channel conduction. The electrons in the channel should be highly mobile due to the high density of states in the two-dimensional subbands. Realistically this is not observed. The most likely scenario is that the density of NITs with energy levels below the Fermi level becomes comparable to the density of states in the subbands. Given the large ($\approx 10^{13} cm^{-2} eV^{-1}$) density of NITs reported near the 4H-SiC conduction-band edge[3], this scenario is very plausible. If the majority of electrons attracted to the SiC–SiO_2 surface are captured by NITs with energy levels below the Fermi level, the density of electrons remaining in the conduction subbands in the channel is significantly reduced, as illustrated in Fig. 2(a). The measured current (I_D) is usually used to calculate the average channel-carrier mobility for the total charge attracted by the gate voltage (V_G), which is $V_G C_{ox}$ (C_{ox} is the gate-oxide capacitance). This procedure averages the mobility of the trapped electrons (zero mobility) and the mobility of the electrons in the subbands, which is then referred to as the channel-mobility reduction.

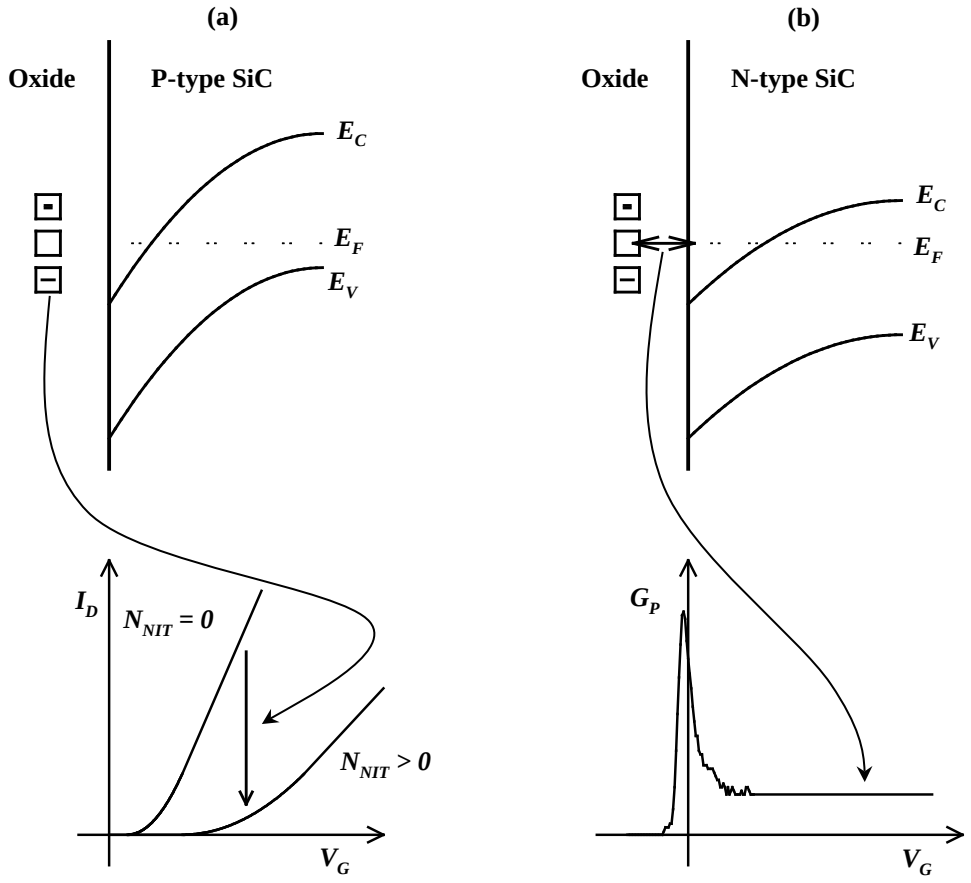

FIG. 2. The effects of near-interface traps energetically aligned to the conduction band, on (a) an N-channel SiC MOSFET and (b) an N-type MOS capacitor. The Fermi level enters the conduction band in the band diagrams due to quantum mechanical effects. The near-interface traps situated below the Fermi level are occupied with electrons whereas the near-interface traps aligned to the Fermi level are active and in direct communication with electrons. Traps located above the Fermi level are inactive and neutral.

Since it is very useful to utilize MOS capacitors rather than complete MOSFETs for characterization of the quality of SiC–SiO_2 interface, we will show that the described effect of NITs can be experimentally observed with conductance measurements on N-type MOS capacitors. Figure 2(b) shows that the surface region of an N-type MOS

capacitor biased well into accumulation is equivalent to the N-channel MOSFET in strong inversion in terms of the possible communication between the surface electrons and near-interface traps. Figure 2(b) also illustrates that this communication can be detected by conductance measurements when a direct-current (DC) gate bias sets the structure in the accumulation region. To enable the conductance measurements, a small AC signal is superimposed to the DC bias. This oscillates the energy levels of the NITs above and below the Fermi level, which results in electron capture from and release into the channel. The measured equivalent parallel conductance (G_P) in the accumulation region is a direct result of the capture and release of these electrons, which is also shown in Fig. 2(b).

To measure the effects of NITs situated above E_C, MOS capacitors were fabricated on *n*-type, silicon faced, 4H−SiC wafers with an epitaxial layer doped by nitrogen to a concentration of 10^{16} cm^{-3}. Prior to oxidation the samples were prepared using a Radio Corporation of America (RCA) cleaning procedure. The gate oxide was thermally grown using a similar nitridation "sandwich" process to improve interface qualities as proposed by Schorner *et al.*[8]. Aluminium gate contacts were sputter deposited and defined by photolithography to form 500 µm squares. Aluminium was also deposited on the back of the samples for the ohmic contact. Capacitor gate voltages were swept between 10 V to -10 V at 10 kHz and 25°C to measure the conductance between strong accumulation and deep depletion, as shown in Fig. 3(a). The samples were then biased well into accumulation (V_G = 9.5 V) and swept between 1 kHz to 100 kHz at both 25°C and 200°C to determine the frequency and temperature dependencies of the measured accumulation conductance, as illustrated in

Fig. 3(b). The gate-oxide thickness was approximately 50 nm as determined from the accumulation capacitance.

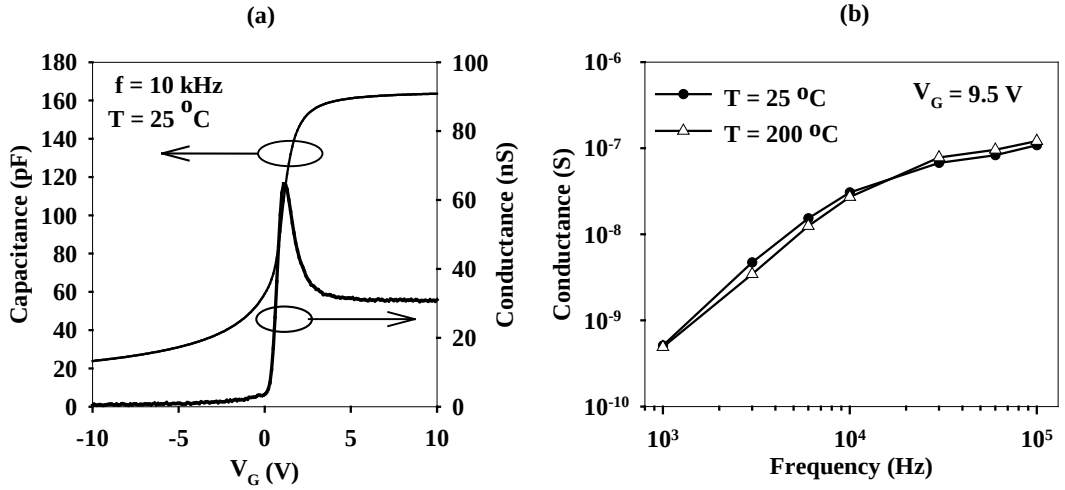

FIG. 3. Capacitance–voltage and conductance–voltage characteristics of an N-type MOS capacitor (a) and the accumulation conductance measured over different freqencies and temperatures (b).

The fact that the measured AC conductance in accumulation does not drop to zero level, as seen in Fig. 3(a), indicates the presence of the suspected conduction-band NITs. To verify this conclusion, the DC conductance was measured and found to be at low ρA values, close to measurement noise levels. This shows that the AC accumulation conductance is not due to oxide leakage. The bias independence of the accumulation conductance is largely due to the effective *pinning* of the Fermi level, whereby the influence of additional gate bias becomes quite minor once Fermi level enters the conduction band.

Clearly, the capture and the release of electrons by these NITs, as illustrated in Fig. 2(b), have to occur by tunneling as opposed to thermal emission. According to this mechanism, the accumulation conductance has to be independent of temperature. The results presented in Fig. 3(b) show that the accumulation conductance (V_G = 9.5V) exhibits no temperature dependencies that indicate the presence of thermal emission. These measurements therefore demonstrate that the accumulation conductance is due

to temperature-independent tunneling which is in full agreement with the presented model. Provided the carrier-NIT communication is due to temperature-independent tunneling, then the strong frequency dependence of the accumulation conductance, also shown in Fig. 3(b), must correspond to the carrier tunneling times and therefore directly relate to the tunneling distances. The tendency of the accumulation conductance to increase at higher frequencies indicates that the density of NITs increases closer to the SiC/SiO_2 interface, thereby having shorter tunneling distances resulting in shorter tunneling times.

In summary, the existence of NITs with energy levels aligned to the conduction band have been proposed as the main impacting factor on the channel mobility of SiC MOSFETs, as opposed to traps residing in the SiC energy gap. Because of very strong band bending and quantum confinement in the strong inversion and accumulation regions, the Fermi level enters energy levels above the bottom of the conduction band. This coincides with the concept that the electrons in the inversion and accumulation layers can directly tunnel to and from NITs with energy levels above the bottom of the conduction band. Trapping of electrons from the inversion layer by these NITs results in the effective reduction of MOSFET channel mobility. Conductance measurements of N-type MOS capacitors biased in accumulation can be used as a direct method to detect and characterise these NITs. This is possible because the surface region of the energy band diagram of an MOS capacitor in accumulation is distinctly similar to that of an N-channel MOSFET in strong inversion. Measurements carried out on 4H-SiC MOS capacitors have shown that the accumulation conductance shows no temperature dependence to suggest thermal emission, therefore confirming that direct tunnelling is the responsible mechanism for capture of channel

electrons by these NITs. The frequency dependence of the accumulation conductance indicates that the NIT density significantly increases closer to the SiC/SiO_2 interface due to shorter carrier–NIT tunneling distances and therefore shorter tunneling times, increasing the accumulation conductance at higher measuring frequencies.

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