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CNTFET-Based Design of a High-Efficient Full Adder Using XOR Logic

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This paper presents a new low power and high speed full adder based on Carbon Nano Tube Field Effect Transistor (CNTFET) technology. This proposed full adder is based on a XOR logic function using 32 nm CNTFET technology. The MOSFET-like CNTFET is applied in this paper to use CMOS (Complementary Metal Oxide Semiconductor) logic gate. The better structure of CNTFET transistors can improve the performance of full adder based on CNTFET technology [1]. The proposed full adder is simulated in different frequencies, various supply voltages, temperatures and load capacitances to prove better performance in different conditions using the Synopsys HSPICE simulator software in comparison with previous full adders in CNTFET technology.

Keywords: CNTFET, Full adder, Low power, XOR logic, PDP (Power Delay Product).

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1. INTRODUCTION

By developing mobile devices, the importance of low power consumption of integrated circuits can be made more obvious. A reduction in the number of transistors can help decrease the power consumption, consequently reducing the area consumption. The XOR/XNOR circuits are fundamental digital blocks in a wide range of circuits, including adder, multiplier and analog circuits such as comparators and converters [2-3]. Among different circuits, adders are important blocks which have numerous applications in digital circuits. Many studies have been conducted to optimize these circuits [4-7]. A 1-bit full adder takes three inputs A, B and gives two outputs (sum and carry out), which can be implemented by equation (1).

$$\begin{aligned} sum &= a \oplus b \oplus c_{in} \\ c_{out} &= a.b + c_{in}\left(a \oplus b\right) \end{aligned} \quad (1)$$

The emerging new generation of transistors such as CNTFET (Carbon Nano Tube Field Effect Transistor), has helped in overcoming some limitations of CMOS technology. Therefore, many of these full adders are designed using this new technology [8-13]. CNTFET transistors have better performance compared to CMOS transistors. One of the advantages of CNTFET in comparison with CMOS its ability to control the threshold voltage which can be calculated with equation (2) [10].

$$v_{th} \approx \frac{0.43}{d_{cnt}} \quad (2)$$

D_{CNT} is the nano tube diameter which can be calculated by integer pair chirality vector $\left(n_1, n_2\right)$ in equation (3) below:

$$D_{cnt} = \frac{\alpha\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \quad (3)$$

Where α is lattice constant which is equal to 2.49 A. The use of different logic styles in designing full adder blocks enhances speed, power consumption and size. The speed is determined by the number of transistors connected in series, in a critical way. The speed is majorly dependent on the width of transistors and internal capacity of capacitors. The number of transistors and complexity of wires determine the size of the circuits. Power consumption depends on the switching activity, capacitance of nodes and circuit sizes. It is therefore an obvious fact that lower power consumptions can be achieved by decreasing the source voltage, but reducing the voltage power supply may increase delay and can have a negative effect on drivability. Therefore, the total performance of full adders can be improved by some designs. This paper focused on reducing the power consumption and the area consumption of the full adder by reducing the number of transistors without affecting any of the other critical parameters. Various conventional and new full adder blocks with the same logic style are selected to show better performance of the proposed full adder.

2. THEORETICAL PART

2.1 CNTFET

A Carbon Nanotube (CNT) is a graphite sheet rolled. A CNT has two types based on the number of cylinders, single-wall (SWCNT) and multi-wall (MWCNT). The Chirality vector can define the SWCNT is metallic or semiconducting. In the Chirality vector, if the SWCNT is a semiconductor and other modes it is a metal [14]. A MOS-like CNTFET is made by the SWCNT which is replaced by channel in a CMOS transistor.

There are three types CNTEFTs, Schottky Barrier CNTFET(SB-CNTFET), MOSFET-like CNTFET and band-to-band tunneling CNTFET (T-CNTFET). Schottky Barrier CNTFET tunnels directly throughout Schottky Barriers at the source/drain-channel junctions which is direct between metal and semiconducting

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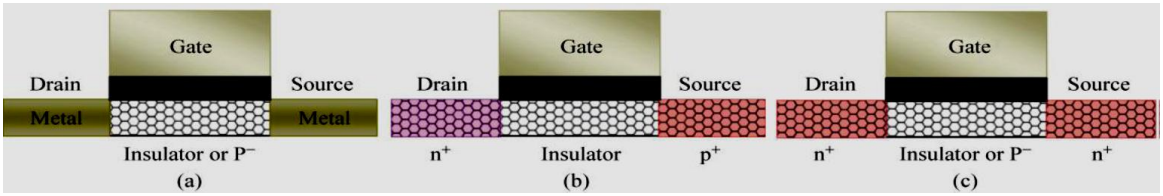


Fig. 1 – Different types of the CNFET device. (a) SB-CNFET (b) T-CNFET (c) MOSFET-like CNFET [15]

CNT. This kind of CNTFET has an ambipolar characteristic which limits its application in CMOS logic.

It is shown in Fig. 1(a). In a MOS-like CNTFET, source and drain regions are doped heavily by CNTs and this kind of CNTFETs has unipolar characteristics and highly ON current. It is shown in Fig. 1(b). T-CNTFET or band-to-band tunneling CNTFET is the best features in low voltage, so it is the best kind of CNTFET at sub-threshold circuits. It is shown in Fig. 1(c) [15]. In this paper, the MOS-like CNTFET model is used for proving the better proposed full adder. The MOS-like CNTFET model has near ideal I-V characteristics at the nanoscale.

2.2 Previous Work

Full adder circuits are designed using various logic styles. The 23T full adder can be designed by the combination the pass transistor logic and transmission gate as it is shown in Figure 2. Two XOR and XNOR functions are used to generate outputs [16]. This logic style was also used to design the 18 transistor full adder. In this paper, the 23T circuit is designed based on CNTFET technology for the better performance.

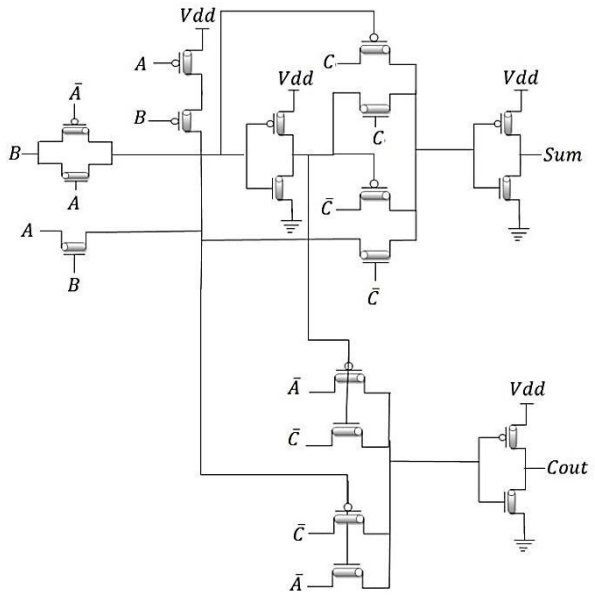


Fig. 2 – The 23T Full Adder Cell based on CNTFET

Another logic style of full adder design is the Hybrid [17], which is based on the CMOS technology. In this paper, however, this full adder is designed based on the CNTFET technology, which is shown in Figure 3. In the Hybrid full adder, two separated sub circuits are used to produce Sum and Cout output signals. To generate a Sum signal, two cascaded XOR/XNOR circuits are used. The first sub circuit is a pseudo-DCVS circuit while the second sub circuit is a high speed DCVS circuit which does not require compulsory inputs, hence the number of used transistors reduces. However, the

DCVS structure of full adder deceased the operating speed and also had a low driving capability. To improve driving capability, an inverter was set in the output nodes. To generate Cout signal, the Bridge structure [18] was used in the Hybrid full adder.

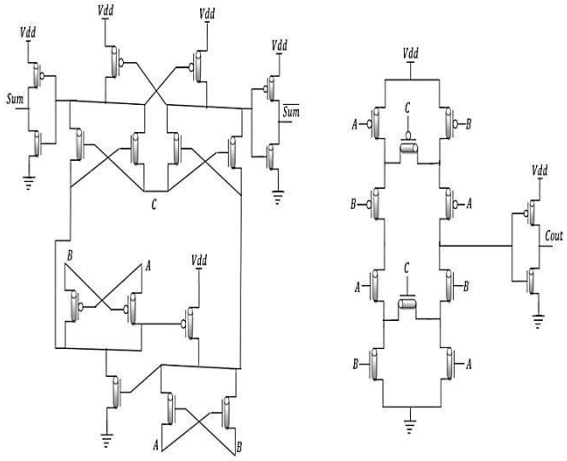


Fig. 3 – The Hybrid Full Adder circuit is based on CNTFET

The CNTCPL is another logic style for full adder, which is shown in figure 4 [19]. This circuit has a characteristic low delay because the critical path has only two very small pass transistors. In this circuit, speed is very high because of the reducing effects of full-swing nodes, but this full adder cannot drive very well as a result of the use of transmission gates.

In order to solve this problem, an inverter included in output nodes can increase the driving, but putting an inverter in the output nodes can damage some unique characters.

Also, another kind of full adder based on intermediate XOR or XNOR logic and transmission gate is the CNTFA which is designed based on CNTFET technolgy [20]. This CNTFA full adder is shown in Figure 5. The XOR or XNOR gate creates signals for the second stage which is a multiplexer to produce the SUM signal. In the second stage, both SUM and CARRY OUT signals can be produced simultaneously. This full adder circuit has a great deal of advantages, including full swing output signals and low power consumption.

The final full adder designed based on XOR logic is the 24T full adder, which uses CNTFET technology [9]. This full adder is depicted in Figure 6. In this full adder, a 2 - input exclusive-or is used for implementation of a XOR logic. In output nodes, there are inverters

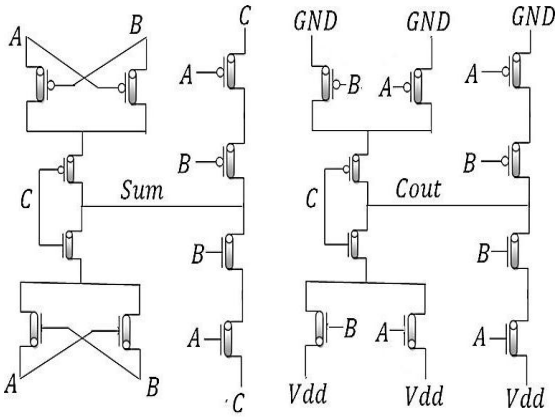


Fig. 4 – The CNT-CPL Full Adder suggested in [19]

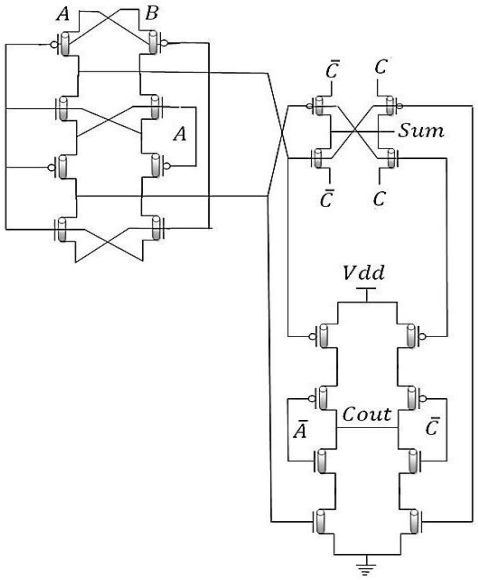


Fig. 5 – The CNTFA Cell proposed in [20]

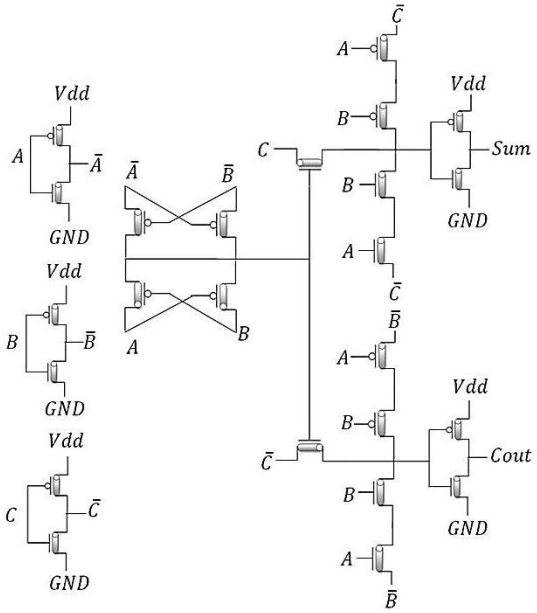


Fig. 6 – The 24T full adder suggested in [9]

which account for the speed of the ineffective high load capacitors in this full adder operation. For two output signals, approximately one structure was used to produce the same delays for both output signals, thereby simplifying the implementation [9].

To simulate the 24T full adder, the number of carbon nano tubes are changed to provide better output setting signals, but the fabrication processes become complicated.

2.3 Proposed Full Adder

This full adder is designed by a XOR logic. By paying attention to the truth table of , the output of follows the following rules. If input A is equal to "0", is equal to input B. If input A is equal to "1", is equal to inverse of input B.

Table 1 - The truth table of $a \oplus b$

A	B	$a \oplus b$
0	0	0
0	1	1
1	0	1
1	1	0

This logic equation can be implemented as shown in the circuit in Fig. 7.

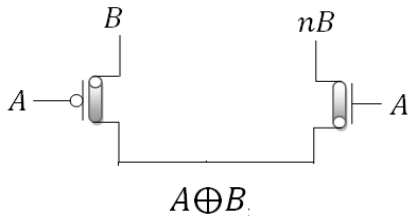


Fig. 7 – Proposed XOR circuit

The truth table of input and output signals of a full adder can be organized as seen in Table 2. This table is designed based on the binary logic of $a \oplus b$. If $a \oplus b$ is equal to "0", SUM signal is equal to c_{in} input. In another condition, if is equal to "1", the SUM signal is equal to the inverse of input or nc_{in}. Also, these relationships can be applied for CATTY OUT signal. If is equal to "0", CARRY OUT signal is equal to the A or B input. If is equal to "1", CARRY OUT signal is equal to the input. A circuit which can produce these equations is shown in figure 8. The input and output signals of the proposed full adder is shown in Figure 9.

3. EXPERIMENTAL PART

All five previous full adders and a proposed full adder were simulated based on 32 nm-MOS-like CNTFET model technology. The parameters of the MOS-like CNTFET model and their values are presented in Table 3. The 24T-based XOR, CNTCPL and CNTFA full adders were designed based on 32nm-CNTFET technology, while others,

Table 2 - The full adder truth table.

A	B	Ci	$a \oplus b$	Sum	Carry out
0	0	0	0	0	0
0	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	0	1	1	0	1

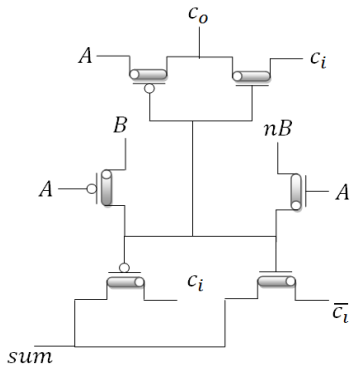


Fig. 8 – The proposed full adder

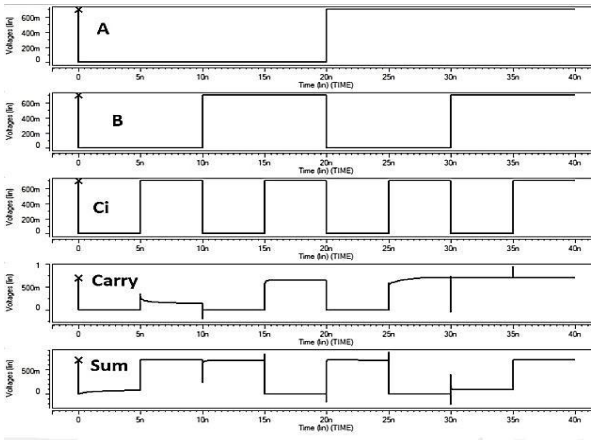


Fig. 9 – The input and output signals of the proposed full adder

such as the 23T and Hybrid Full Adders were based on CMOS technology. In this study, a comparison was made between the 23T and the Hybrid full adders designed based on CNTFET technology and new full adder based on CNTFET technology. The main parameters of full adder are delay, power consumption and power-delay product (PDP) and for the purpose of this study, these three parameters were obtained in a three-volt supply source for 100MegHz input frequency at room temperature. Table 4 shows the results.

Table 3 - MOSFET-like CNTFET model parameters

Parameters	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of the doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of the high-k top gate dielectric material	16
T_{ox}	The thickness of the high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	40 pF/m
E_{fo}	The Fermi level of the doped S/D tube	0.6 eV

Table 4 - Delay, power consumption and power-delay product of proposed full adder and pervious works in a three-volt supply source

vdd	0.7v	0.8v	0.9v
Delay (psec)			
Proposed	0.938	0.83	0.764
24T-based XOR	51.5	36.1	23.2
23T	5.08	4.16	3.64
Hybrid	410	378	468
CNTCPL	0.860	0.719	0.622
CNTFA	4.75	4.13	3.78
Power()			
Proposed	1.04E-02	1.30E-02	1.83E-02
24T-based XOR	6.75E-02	1.15E-01	1.57E-01
23T	1.74E-02	2.53E-02	3.35E-02
Hybrid	9.74E-01	1.07	1.44
CNTCPL	4.43E-02	5.13E-02	5.87E-02
CNTFA	1.57E-02	2.20E-02	2.95E-02
PDP(aJ)			
Proposed	9.80E-3	1.08E-2	1.40E-2
24T- based XOR	3.47	4.15	3.65
23T	8.86E-02	1.05E-01	1.22E-01
Hybrid	399	403	672
CNTCPL	3.81E-02	3.69E-02	3.65E-02
CNTFA	7.46E-02	9.09E-02	0.112

From the table, delay, power consumption and Power-Delay Product experienced a considerable improvement in comparison with other pervious works. In the proposed full adder, there was no change in the standard parameters for CNTFET, but for the better delay, n1, the first parameter for chirality vector changed in two CNTFET transistors connected to the SUM output node, resulting in a slight change in the diameters of two CNTFET transistors.

To test the driving capability of many circuits, some different load capacitors were connected to the output nodes. The value of capacitors in two output nodes changed from 2ff to 10ff. These full adders, pervious full adders and proposed full adder, had the same voltage power supply at 0.7 V and 100 MegHz input frequency. Various full adder delays in different load capacitors are shown in Figure 10.

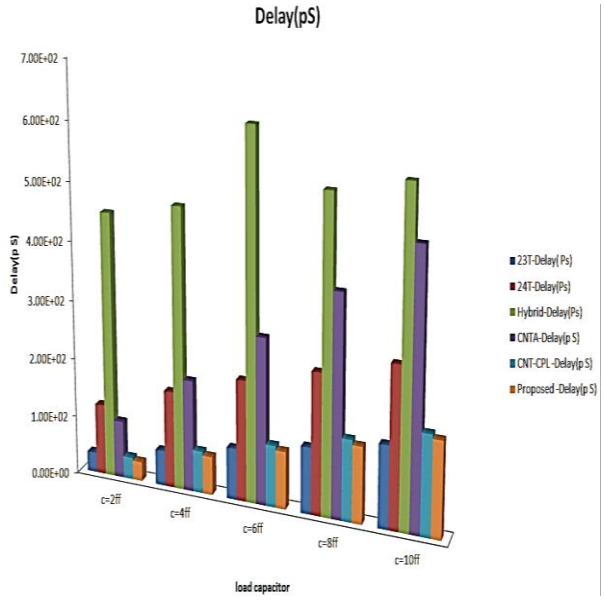


Fig. 10 - Various delays of full adders in different load capacitors

The last orange column was responsible for delaying the proposed full adder. Delays of proposed full adder in different load capacitors improved slightly in comparison with other full adders. Also, this full adder was simulated using standard parameters of CNFET without changing a great deal of them as a result of its fabrication process.

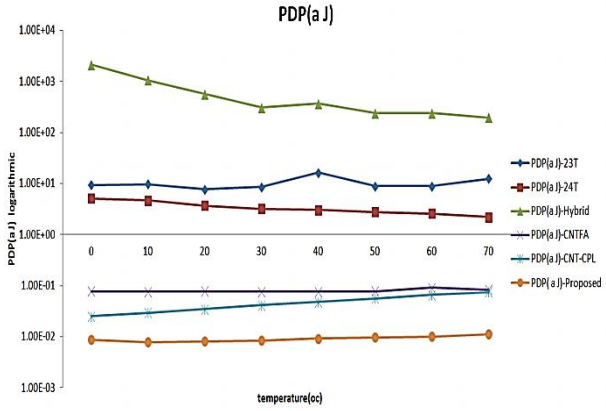
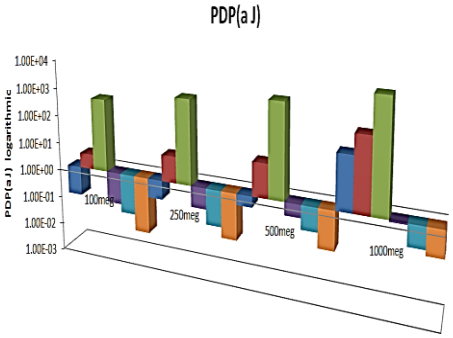


Fig. 11 – PDP of different full adders at various temperatures

The immunity of accurate operation of full adder at various temperatures cannot be over emphasized, therefore, all full adders were simulated within a great range of temperature from 0 °C to 70 °C by increasing temperature with 10 °C in each step. The results of these simulations are presented in Figure 1.

Different line charts are presented in logarithmic scale, in order to clearly show the PDP differences of all full adders. The PDP for the proposed full adder has a minimum value which is in the latest line in the negative direction. This shows that the proposed full adder has a normal performance at the temperature variations.

Better designed VLSI circuits can make these circuits work under high frequencies. All full adders and proposed full adder were simulated at high frequencies, such as 1000 and 500 MHz. Figure 12 shows the PDP of all full adders at four frequencies on a logarithmicscale, to show the differences very clearly.



	100meg	250meg	500meg	1000meg
PDP(a J)-23T	8.86E-02	2.11E-01	4.12E-01	7.80E+01
PDP(a J)-24T	3.47	8.8	1.57E+01	3.83E+02
PDP(a J)-Hybrid	4.18E+02	1.04E+03	2.07E+03	7.58E+03
PDP(a J)-CNTFA	7.46E-02	1.81E-01	3.57E-01	8.85E-01
PDP(a J)-CNT-CPL	3.81E-02	5.32E-02	1.47E-01	1.80E-01
PDP(a J)-Proposed	9.80E-03	2.28E-02	4.40E-02	1.18E-01

Frequency

Fig. 12 – PDP of all full adders in four high frequecies

As can be observed, the PDP of the proposed full adder has the largest value in the negative direction of the logarithmic scale which shows the minimum PDP value at various frequencies. The minimum value of PDP indicates better performance at different frequencies.

4. CONCLUSION

A novel full adder is designed based on the XOR logic, which is simulated based on CNTFET technology. This full adder is designed based on the minimum number of transistors which reduces the area consumption and power consumption without losing any important parameters such as driving capability and delay. Also, this full adder works in different conditions, including various temperatures and frequencies without suffering from changing main parameters such as delay, power consumption and PDP.

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