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J. Nano- Electron. Phys.
3 (2011) No1, P.162-169

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PACS numbers: 64.70.kg, 65.40.gh

EFFECTS OF INTERFACIAL CHARGES ON DOPED AND UNDOPED HfO_x STACK LAYER WITH TIN METAL GATE ELECTRODE FOR NANO-SCALED CMOS GENERATION

***S. Chatterjee*[1], *Y. Kuo*[2]**

[1] ECE Department, Techno India,
EM-4/1, Sector-V, Salt Lake, Kolkata, 700091, India
E-mail: somenath@gmail.com

[2] Thin Film Nano & Microelectronics Research Laboratory,
Texas A&M University,
College Station, TX 77843-3122, USA

A comparison of the interfacial charges present in the high-k stacked gate dielectrics for Zr-doped HfO_x and undoped HfO_x samples with titanium nitride (TiN) metal gate electrode is reported here. The metal gate work function value (4.31 eV) for TiN gate electrode was extracted from the TiN/SiO_2 /p-Si capacitor. The calculated charge densities in both doped and undoped films are of the order of 10^{12} cm^{-2}. The interfacial charge present in the high-k/SiO_2 interface is negative for ALD deposited pure HfO_2 samples; where as the charges are positive for RF-sputter deposited pure HfO_2 and Zr-doped HfO_x samples. The existence of positive interface charges may be due to the fabrication process.

Keywords: *DOPED HIGH-K GATE DIELECTRICS, NANOELECTRONICS, MOSFET, WORK FUNCTION, OXIDE-DEFECTS.*

(*Received 04 February 2011*)

1. INTRODUCTION

Fabrication of smaller and faster metal-oxide-semiconductor (MOS) field effect transistors and superior memory devices dictate the usage of new materials and chemical processes to make nano-electronics a reality. The high gate leakage current, doping penetration and gate depletion effect will limit the use of SiO_2 (as gate dielectrics) and poly-Si (as gate electrodes) for sub-65 nm technology node. Alternative dielectric materials such as Si_3N_4, HfO_2, [1] ZrO_2, [2] their silicates and transition metal doped high-k dielectrics [3, 4] have been suggested as candidate materials. The amorphous-to-polycrystalline phase transition temperature of the film can be increased by adding a third element into the oxide, e.g. Zr doped in the HfO_x, because of the polycrystalline high-k film degraded the device reliability due to the uneven distribution of grains in the channel region [3]. Furthermore, the doped element can control the fast diffusion of oxygen vacancies in high-k films, which is mainly responsible for the formation of uncontrolled interfacial layer thickness, lower breakdown field and higher leakage current density [3-5]. There is no literature so far concerning the gate dielectrics with Zr^{4+} doped HfO_x. It is well known that Zr and Hf are both 4-valence elements, so Zr doped HfO_x would not exhibit any increase in oxygen voids in the film.

In contrast to the high-k dielectric selection that is nearing consensus, the searching of metal gate electrode for CMOS is in its infancy. One of the requirements for the integration issues of a new metal gate electrode is the proper set of work function values. In the PMOS (NMOS) transistor, heavily p-type (n-type) doped poly-Si is used as gate electrode and the work function is about 5.2 eV (4.1 eV). So, the substituting metals or metal compounds should have the work function, i.e. the gate fermi level for PMOS (NMOS) devices is 0.2 eV above (below) the band edge E_v (E_c), in order to reduce the transistor's threshold voltage [6]. The metal gate work functions depend on bulk and surface material properties, crystalline orientation and the permittivity of the dielectric interfacing with the metal. The work function of a metal at a dielectric interface is different from its value in vacuum. This may be explained either by metal induced gap states (MIGS), as the interface provides the possibilities such as metal-insulator transition or by the formation of a dipole layer at the metal-dielectric interface [7]. Again the defects/charges present in the high-k gate dielectrics stack are different than the defects present in the conventional SiO_2 gate dielectrics in SiO_2/Si system. Moreover, the present of charges will lead to large shift in transistor threshold voltage. Columbic scattering from excess charge in the high–k film will most certainly cost degradation in channel carrier mobility to unacceptable levels. Therefore, an investigation of the impact of interfacial charges on the metal gate's work function with doped high-k dielectric stack is technically important and timely.

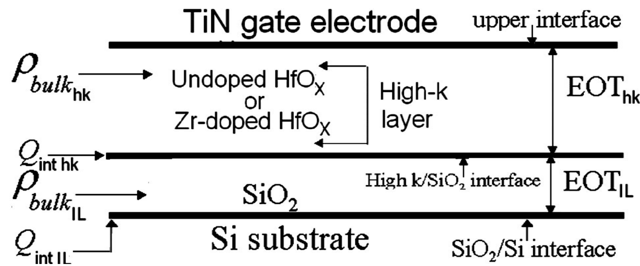

Fig. 1 *– The high-k gate dielectric consists of the stacked structure and the charges are situated at 1) upper interface, i.e. between the gate electrode and high-k gate dielectrics, 2) bulk high-k layer, 3) interface between the high-k and SiO_2-rich dielectrics, 4) bulk SiO_2 dielectrics layer, and 5) between the SiO_2 and substrate interface. The EOT_{hk} and EOT_{IL} are the equivalent oxide thicknesses for High-k and SiO_2 layer, respectively*

Fig. 1 shows a schematic diagram of MOS structure with stacked gate dielectrics (detail descriptions are given in the figure caption). $\rho_{bulk\ hk}$ and $\rho_{bulk\ IL}$ are the bulk oxide charges per unit volume in the bulk of high-k and SiO_2 layer, respectively. Similarly, $Q_{int\ hk}$ and $Q_{int\ IL}$ are the fixed sheet charge (charge/area) at the high-k and SiO_2 interface and SiO_2 and Si (substrate) interface. The location of different bulk and interfacial charges, e.g. $\rho_{bulk\ hk}$, $\rho_{bulk\ IL}$, $Q_{int\ hk}$, and $Q_{int\ IL}$, are shown in the Fig. 1.

In this paper, authors have reported the work function for TiN metal nitride gate electrodes with the conventional SiO_2 gate dielectrics, comparison of the different interface charges located in the HfO_2 and Zr-doped HfO_x gate dielectric stacks with TiN gate electrodes.

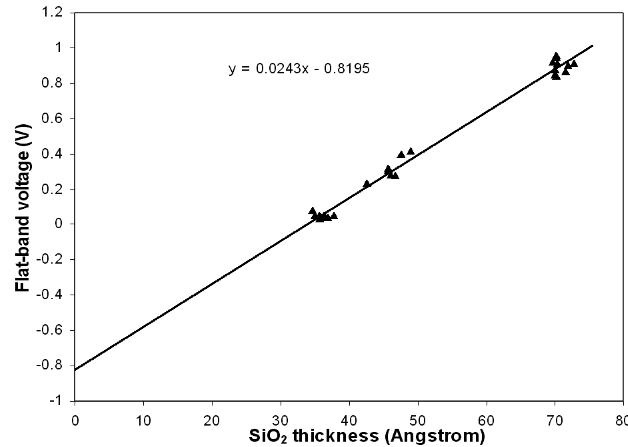

Fig. 2 *– Flat band voltage versus EOT for extraction of metal gate work function using TiN/SiO_2/p-Si MOS capacitor structure.*

2. EXPERIMENTAL

Extraction of the proper work function requires minimization of charges in the oxide, which could vary from wafer to wafer when oxidized to different thicknesses. To avoid such issue, wafer with thick oxide can be partially wet etched in a solution of buffered HF in steps across the wafer in order to achieve the multiple oxide thicknesses (for example 2, 4, 6 nm). The variable thermally grown SiO_2 thicknesses on p-type Si substrate (terraced oxide) and the fixed HfO_2 film thickness using atomic layer deposition (ALD) on the terraced oxide were provided by Sematech [8]. The Zr doped HfO_2 films were deposited by magnetron reactive RF co-sputtering technique using Zr (24 W) and Hf (60 W) metal targets in Ar/O_2 ambient for 20 sec on the terraced oxide substrate. Process parameters such as the reaction time, gas flow rate, and sputtering power were investigated under various conditions to stabilize and optimize process conditions. The post deposition annealing (PDA) was performed for every sample with 700°C in N_2 ambient for 10s using a high temperature substrate heater. TiN metal nitride gates were deposited on the dielectrics by magnetron reactive RF sputtering system in a mixture of Ar and N_2 (50:1) at 5 mTorr for 25 minutes. Post metal annealing (PMA) was done at 425 °C in forming gas (pressure 10 Torr) for 10 mins. For comparison, the undoped HfO_2 films were deposited by magnetron reactive RF sputtering technique on the terraced oxide substrate (20 sec, O_2/Ar mixtures, pressure 5 mTorr). The gate electrode area was defined by photolithography and etched with a mixture of NH_4OH, H_2O_2 and H_2O (5:1:1). For a good ohmic contact of the MOS capacitor, aluminum (Al) film was deposited (using DC Sputter technique) on the backside of the Si after removal of native oxide with HF solution. The capacitance-voltage (C-V) of the MOS capacitor was measured at high frequency (100 kHz) using Agilent 4284A precision LCR meter. The flat-band voltage (V_{FB}) and the equivalent oxide thickness (EOT) of the MOS capacitor were calculated by fitting the high-frequency C-V measurements using a C-V simulation program, developed by NCSU [9].

3. RESULTS AND DISCUSSION

The metal-semiconductor work function difference, ϕ_{ms}, can be estimated using the following equation for TiN metal gate electrodes with different SiO_2 gate dielectrics thicknesses,

$$V_{FB} = \varphi_{ms} - \frac{Q}{C_i} = \varphi_{ms} - \frac{Q\, d_{ox}}{\varepsilon_0 \varepsilon_{SiO_2}} \tag{1}$$

Here, the Q represents the equivalent oxide charge per unit area present in the dielectrics. C_i is the oxide capacitance/area, ε_{SiO2} is the dielectric constant of SiO_2 (~ 3.9), ε_0 is the permittivity of the free space ($8.85 \cdot 10^{-12}$ F/m) and d_{ox} is the SiO_2 thickness.

Fig. 2 shows a V_{FB} versus SiO_2 thickness plot for TiN/SiO_2/p-Si MOS structure. The experimental data points of Fig. 2 are fit to a straight line using "least square fit". The intercept of the straight line is the value of φ_{ms} for TiN metal gate electrode. To obtain the TiN work function (φ_m), the following equation was used

$$\varphi_m = \varphi_{ms} + \varphi_s = \varphi_{ms} + \left(\chi + \frac{E_g}{2q}\right) + \left(\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)\right), \tag{2}$$

where χ is the Si electron affinity (4.05 eV), E_g is the band gap of the Si (1.12 eV), n_i is the intrinsic carrier concentration in Si and Na is the channel doping levels (~ 10^{18} cm^{-3}). In this study, the φ_m for TiN metal gate electrode is found to be 4.31, which is consistent with the reference [10].

However, the values of φ_m for TiN increase with increasing of the N_2 partial pressure during deposition process. To achieve higher φ_m value, the diffusion of N_2 towards the dielectric/electrode interface is necessary as it is produced in a more stoichiometric TiN metal gate electrode [10].

When characterizing high-k gate stacks, it is important to be aware of the charges in the different interfaces and layers that the stack comprises. The dielectric layers in the high-k gate stacks consist of the bi-layer structure, as shown in Fig. 1. Different types of charges are located at the different dielectric layer as well as interface.

The fundamental equation that relates the V_{FB} to the gate dielectric charge distribution per volume, $\rho(x)$, φ_{ms} and EOT of the MOS stack structure, can be expressed as,

$$V_{FB} = \varphi_{ms} - \frac{1}{\varepsilon_{SiO_2}}\left[\int_0^{EOT} x\, \rho(x)\mathrm{d}x\right] \tag{3}$$

Considering the bi-layer stack structure [11], the equation (3) can be rewritten as,

$$V_{FB} = \varphi_{MS} - \frac{1}{\varepsilon_{sio_2}}\left[\int_0^{EOT_{hk}} x\,\rho(x)dx\right] - \frac{1}{\varepsilon_{OX}}\left[Q_{\mathrm{int}\,IL}\,\mathrm{EOT}\right] - \\ - \frac{1}{\varepsilon_{OX}}\left[\frac{1}{2}(\rho_{bulkhk}\mathrm{EOT})^2\right] + \frac{1}{\varepsilon_{OX}}\left[\frac{1}{2}(\rho_{bulkhk}\mathrm{EOT})^2\right] \tag{4}$$

If EOT_{hk} is fixed and the total EOT ($EOT = EOT_{hk} + EOT_{IL}$) is varied only by changing EOT_{IL},one can get the expression for V_{FB} with EOT as a polynomial of order two [11].

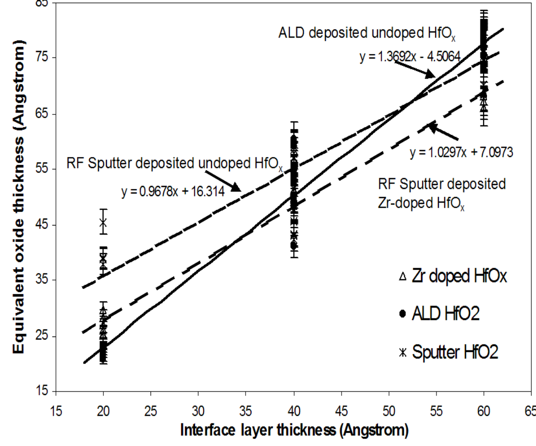

Fig. 3 *– Plot of EOT versus the interface layer physical thickness to determine the physical thickness of high-k layer for different stack layer*

Based on recent reports [11-13], the bulk charge in both layers is usually much less than the interface charge (i.e. $\rho_{bulk\ hk}.EOT_{hk} << Q_{int\ hk}$). Therefore, the equation 4 can be simplified and V_{FB} can be expressed in terms of EOT,

$$V_{FB} = \varphi_{ms} - \frac{1}{\varepsilon_{SiO_2}}\left[Q_{int\,hk} \cdot EOT_{hk}\right] - \frac{1}{\varepsilon_{SiO_2}}\left[Q_{int\,IL}\right] \cdot EOT \quad (5)$$

To find the values of $Q_{int\ IL}$ and $Q_{int\ hk}$ charges present in the different location of the stacked dielectrics (as shown in Fig. 1), the φ_{ms} and EOT_{hk} can be extracted properly. According to equation (1), the Y-axis interception in the V_{FB}-SiO_2 thickness plot represents φ_{ms}, while according to equation (5); the Y-axis interception in the V_{FB}-EOT plot represents the φ_{ms} plus the effect of the HfO_2/SiO_2 interface charges. We have calculated the φ_{ms}values using the TiN/SiO_2/p-Si MOS capacitor system and the equation (1), as there is no interfacial layer. However to calculate EOT_{hk}, we can use the following equation,

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{IL}} d_{IL} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{hk}} d_{hk} \quad (6)$$

where the first term is the contribution of EOT for SiO_2 rich dielectric layer and second term is the EOT for high-k dielectric layer. The ε_{IL}, ε_{hk}, d_{IL} and d_{hk} are the dielectric constant of interfacial layer, high-k layer, the physical thickness of the interfacial layer and the physical thickness of the high-k layer, respectively. We have considered the ε_{IL} is the dielectric constant of SiO_2 rich layer and we have used the fixed Zr-doped HfO_x and undoped HfO_x

film on terraced oxide samples. The EOT_{hk} value for doped and undoped films can be calculated from the intercept on the EOT axis when EOT is plotted against the SiO_2 thicknesses, as shown Fig. 3.

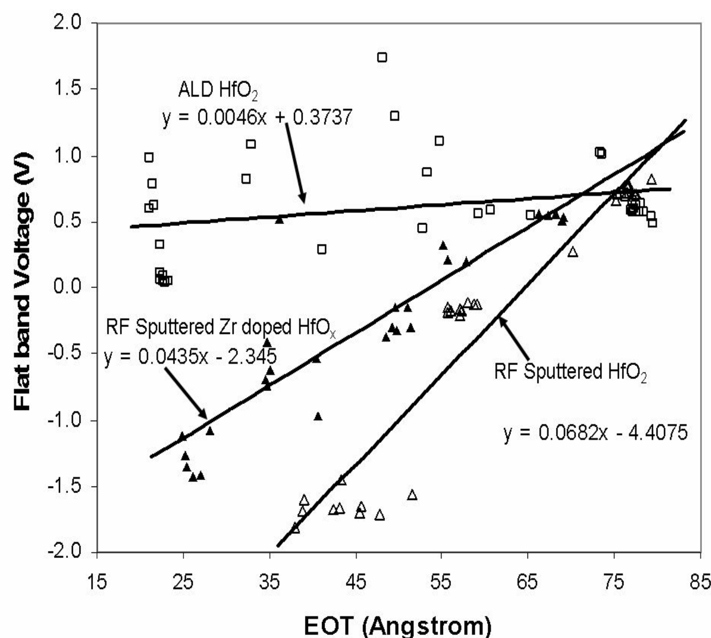

***Fig. 4** – Plot of flat band voltage versus EOT (by changing the Interfacial layer thickness) for determination of the different charges located at different interfaces using ALD and RF-sputter deposited HfO_2, and RF-sputter deposited Zr doped HfO_x with TiN gate electrode MOS capacitor structure*

After knowing the values of φ_{ms} (from equation 1) and EOT_{hk} (from equation 6), one can extract the values of $Q_{int\ hk}$ and $Q_{int\ IL}$ using equation 5 for stacked MOS capacitor with undoped HfO_2 and Zr-doped HfO_2 (shown in Table 1) films.

From Fig. 2, it is observed that the V_{FB} has shifted toward the positive direction as the SiO_2 thickness increases supports that the negative Q is primarily located in the SiO_2 near to the Si/SiO_2 interface. The positive drift of V_{FB} with increasing SiO_2 thickness was caused by negative electric centers. The probable causes to form the negative electric centers are the trapping of electrons by the unsaturated bonds, e.g. Si-O in the SiO_x film and absorbed impurities (i.e. Na^+, K^+) [14]. The SiO_4^{4-} tetrahedral network is the basic structure of SiO_2 film despite whether it is crystalline or amorphous. There are always unsaturated bonds of oxygen in the surface layer and interfacial layer of SiO_2/SiO_2. Thermal treatment causes continuous oxygen diffusion from the surface to the SiO_2/SiO_2 interface. Hence, rich oxygen anions accumulate in these surface and interfacial layer, forming negative electric centers. From Table 1, it is seen that as long as the high-k film has an inserted thermal SiO_2 interface, the interfacial charges near SiO_x/Si interface are negative, same as $TiN/SiO_2/Si$ system independent of the high-k film's deposition method or its doping level.

Table 1 *– Comparison of different charges located in the high-k/SiO$_2$ interface and Si/SiO$_2$ interface for different gate dielectrics are tabulated here*

Sample	$Q_{int\ hk}$ (cm^{-2})	$Q_{int\ IL}$ (cm^{-2})
TiN//SiO$_2$/p-Si	---	$-5.24\cdot10^{12}$
TiN/ALD deposited HfO$_2$/SiO$_2$/p-Si	$-5.71\cdot10^{13}$	$-9.92\cdot10^{11}$
TiN/RF-Sputter deposited Zr-doped HfO$_2$/SiO$_2$/p-Si	$4.6\cdot10^{13}$	$-9.38\cdot10^{12}$
TiN/RF-Sputter deposited HfO$_2$/SiO$_2$/p-Si	$4.7\cdot10^{13}$	$-1.29\cdot10^{13}$

with EOT for ALD deposited undoped HfO$_2$ on SiO$_2$/Si samples compared to the other samples, e.g. thermally grown SiO$_2$ on Si samples, and sputter deposited Zr-doped and undoped HfO$_2$ gate dielectrics on SiO$_2$/Si samples. This can be explained as the formation of more negative interfacial charges in the high-k/SiO$_2$ interface for ALD deposited samples. However, the higher slope value is observed for sputter deposited undoped HfO$_2$ samples (in Fig. 4), which signifies that more positive $Q_{int\ hk}$ are present compared to Zr doped HfO$_x$ samples also shown in Table1. The existence of positive $Q_{int\ hk}$ can be explained considering the gate sputtering process. The sputtering process can cause two kinds of damages: the surface damage and bulk damage [15]. The surface damage is mainly caused by the ion bombardment. The plasma radiation is responsible for bulk damage of the dielectrics. The plasma radiation, for example, UV and the high energy photons could create traps in the gate dielectrics or at the interface. These damages may generate lots of positive interface charges near the high-k/SiO$_x$ interface. Recently, Tewg et al. has also reported the existence of positive charge defects in Zr doped TaO$_x$ dielectric films [16]. The high negative charge values of $Q_{int\ hk}$ for ALD deposited undoped HfO$_2$ samples agree with the literature reports [13, 17]. Again from Table 1, it is seen that the interface charges present in both high-k/SiO$_x$ and SiO$_x$/Si interface are less due to insertion of the Zr atoms in HfO$_x$ gate dielectrics which is due to the reduction of dangling or unsaturated bonds of excess oxygen in HfO$_x$ [5].

4. CONCLUSIONS

We have found out the metal gate work function value (4.31 eV) for TiN gate electrode using the TiN/SiO$_2$/p-Si capacitor structure. The different types of charges present in the gate dielectrics are reported here. The polarity of interfacial charges at the Si/SiO$_2$ interface is the same for SiO$_2$, ALD and RF sputter deposited undoped HfO$_2$ and also RF sputter Zr doped HfO$_x$ samples. The increasing slope of the V_{FB} versus EOT plot (in Fig. 2 and 4) indicate the shifting from negative to positive charge quantities present at the high-k/SiO$_2$ interface. The influence of Zr doping in HfO$_x$ gate dielectrics on the interfacial charge defects found the suitability of the doping element in HfO$_x$ dielectrics for future CMOS generation.

This research was partially supported by NSF project DMI-0300032 and SEMATECH project 309366.

REFERENCES

1. C.K. Maiti, S.K. Samanta, S. Chatterjee, G.K. Dalapati, L.K. Bera, *Solid-State Electron.* **48**, 1369, (2004).
2. S. Chatterjee, S.K. Samanta, H.D. Banerjee, C.K. Maiti, *Thin Solid Films* **422**, 33 (2002).
3. J.-Y. Tewg, Y. Kuo, J. Lu *Electrochem. Solid St.* **8**, G27, (2005).
4. Y. Kuo, J. Lu, J. Yan, S. Chatterjee, T. Yuan, H.C. Kim, J. Peterson, M. Gardner, *208th meeting of the Electrochemical. Society, Abs. # 548*, (Los Angeles, California, USA: 2005).
5. L. Manchanda, M.D. Morris, M.L. Green, R.B. van Dover, F. Klemens, T.W. Sorsch, P.J. Silverman, G. Wilk, B. Busch, S Aravamudhan, *Microelectron. Eng.* **59**, 351 (2001).
6. I. De, D. Johri, A. Srivastava, C.M. Osburn, *Solid-State Electron.* **44**, 1077 (2000).
7. Y. Yeo, P. Ranade, T. King, C. Hu, *IEEE Electron Dev. Lett.* **23**, 342 (2002).
8. G.A. Brown, G. Smith, J. Saulters, K. Matthews, H.C. Wen, P. Majhi, B.H. Lee, IEEE SISC (San Diego: 2004).
9. J.R. Hauser, K. Ahmed, *AIP Conf. Proc.* **449**, 235 (1998).
10. J. Westlinder, G. Sjoblom, J. Olsson, *Microelectron. Eng.* **75**, 389 (2004).
11. R. Jha, J. Gurganos, Y.H. Kim, R. Choi, J.C. Lee, V. Misra, *IEEE Electron Dev. Lett.* **25**, 420 (2004).
12. A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H.E. Maes, U. Schwalke, *IEEE Electron Dev. Lett.* **24**, 87 (2003).
13. G.D. Wilk, M.L. Green, M.-Y. Ho, B.W. Busch, T.W. Sorsch, F.P. Klemens, B. Brijs, R.B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, J.M. Hergenrother, *IEEE VLSI Symp. Tech. Dig.* 88 (2002).
14. L.K. Bera, W.K. Choi, C. S. Tan, S.K. Samanta, C.K. Maiti, *IEEE Electron Dev. Lett.* **22**, 387 (2001).
15. Y. Kuo, *Appl. Phys. Lett.* **61**, 2790 (1992).
16. J.-Y. Tewg, Y. Kuo, J. Lu, B.W. Schueler, *J. Electrochem. Soc.* **152**, G617 (2005).
17. Z. Zhang, M. Li, S.A. Campbell, *IEEE Electron Dev. Lett.* **26**, 20 (2005).