Dynamics of Threshold Voltage Shifts in Organic and Amorphous Silicon Field-Effect Transistors

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Progress in environmental stability and processability, and the increase of the field-effect mobility of organic semiconductors has triggered their use as the active element in microelectronic devices. The advantages of their application are the easy processing, for example, spin-coating and ink-jet printing, without a temperature hierarchy, and their mechanical flexibility. Applications are foreseen in the field of large-area electronics where numerous devices are integrated on low-cost substrates such as plastics. The first flexible, even rollable, quarter video graphics array (QVGA) active matrix displays based on organic semiconductors have already been reported.[1]

In present commercial displays, amorphous silicon, *a*-Si, is used as the active semiconductor. In order to be competitive, organic transistors should exhibit the same performance with respect to current modulation and electrical reliability. The field-effect mobility of organic transistors is already comparable to that of *a*-Si-based transistors. Values of unity have been demonstrated not only for evaporated organic semiconductors,[2] but also using solution-processed semiconductors.[3,4] In this paper we discuss the electrical instability of organic transistors. We observe that the threshold-voltage shift shows a stretched-exponential time dependence under an applied gate bias. The relaxation time is observed to be in the order of 10^7 s (ca. 4 months) at room temperature and is comparable to the best values reported for *a*-Si-based transistors. The activation energy is common for all other organic transistors reported so far. The constant activation energy supports charge trapping by residual water as the common origin. Quantitative analysis shows that differences in reliability of organic transistors are due to differences in the frequency prefactor.

The electrical instability of practical transistors is a device parameter. It can be due to ionic displacements in the gate dielectric; photo-oxidation under applied bias in an ambient atmosphere; or charge trapping at interfaces or at impurities in the bulk, due to defect creation or water at the gate-dielectric–semiconductor interface. Here we focus on the intrinsic electrical instability. We use thermally grown SiO_2 as gate dielectric and determine the dynamics of the electrical instability of organic transistors as a function of time and temperature in a vacuum and in the dark.

We used polytriarylamine (PTAA) as a model compound. This organic semiconducting polymer is amorphous and air stable, with a highest occupied molecular orbital (HOMO) energy level of about –5.1 eV (1 eV = 1.602×10^{-19} J), and yields reproducible transistors with a mobility of about 10^{-3}–10^{-2} cm^2 V^{-1}s^{-1}.[5] The chemical structure is depicted in the insert of Figure 1, where X and Y are short chain alkyl groups. The transistors were fabricated using heavily doped *p*-type Si wafers as the common gate electrode with a 200 nm thermally oxidized SiO_2 layer as the gate dielectric. Gold source and drain electrodes were defined by using photolithography with a channel width (*W*) and length (*L*) of 1000 μm and 10 μm, respectively. A 10 nm titanium layer was used for adhesion. The SiO_2 layer was passivated with hexamethyldisilazane (HMDS) prior to semiconductor deposition. PTAA films were spin-coated from toluene with a layer thickness of 80 nm. To compare the reliability of PTAA transistors with that of other organic semiconductors we investigated regioregular poly(3-hexylthiophene) (P3HT) (Merck, UK), poly(9,9′-dioctyl-fluorene-co-bithiophene) (F8T2) (American Dye Source, Canada) and 3-butyl *a*-quinquethiophene (3-BuT5) (Syncom B.V., The Netherlands) transistors. These

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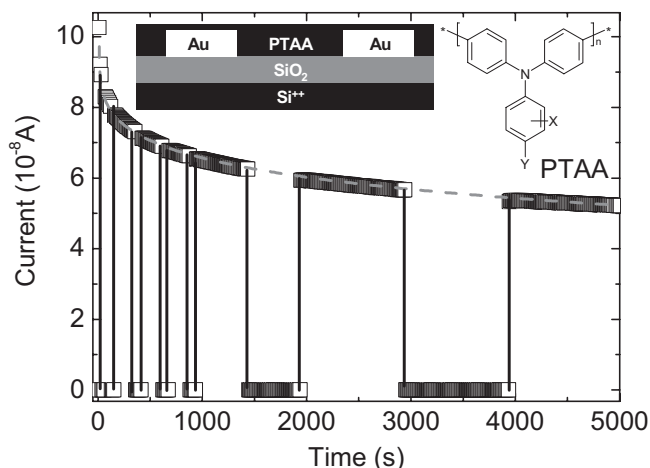University Parkway
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Figure 1. Drain current of a PTAA field-effect transistor as a function of time under an applied gate bias of –20 V. The temperature was 100 °C. The dashed curve is measured using a continuous drain bias of –2 V. The squares present the currents measured when the drain bias is temporarily grounded. The insert shows the schematic cross section of the transistor and the chemical structure of PTAA.

organic semiconductors provide a variety of morphologies; from the polycrystalline film forming oligomer 3-BuT5 with large grain sizes and pronounced grain boundaries, a highly crystalline polymer P3HT with domains in the nanometer scale, a liquid crystalline glassy copolymer F8T2, and an amorphous polymer PTAA. The materials also exhibit a range of HOMO energy levels, from the electron rich, planar and highly conjugated P3HT with a high lying HOMO, to the more electron deficient, fluorene-containing F8T2 polymer. Films were spin-coated from dichlorobenzene and chloroform. Electrical-transport measurements were performed in high vacuum, 10^{-5} mbar (1 bar = 100 000 Pa), in the dark, using a HP 4155C semiconductor parameter analyzer. Prior to the measurements the transistors were annealed for 2 h at 150 °C.

We first investigated the influence of the drain bias on the stress behavior. The drain current of a PTAA transistor under an applied gate bias, V_g, of –20 V as a function of time is presented in Figure 1. The dashed line shows the drain current using a continuous drain bias, V_d, of –2 V. The current slowly decreases with time. The measurement was performed in vacuum at 100 °C. After recovery of the transistor the measurement was repeated, but for certain periods of time the drain was grounded. The measured drain currents are presented in Figure 1 as squares. Irrespective of the previous drain biasing, the currents are identical. Hence, the gate-bias stress was further investigated using a drain bias of 0 V.

Stress was measured as a function of time and temperature. As a typical example, linear transfer curves are presented in Figure 2a as a function of stress time. The applied gate bias during stress was –20 V and the temperature was 140 °C. The transfer curves were measured at a drain bias of –1 V by sweeping the gate bias from 5 V to –35 V and back. No significant hysteresis was observed. The transfer curves shift with
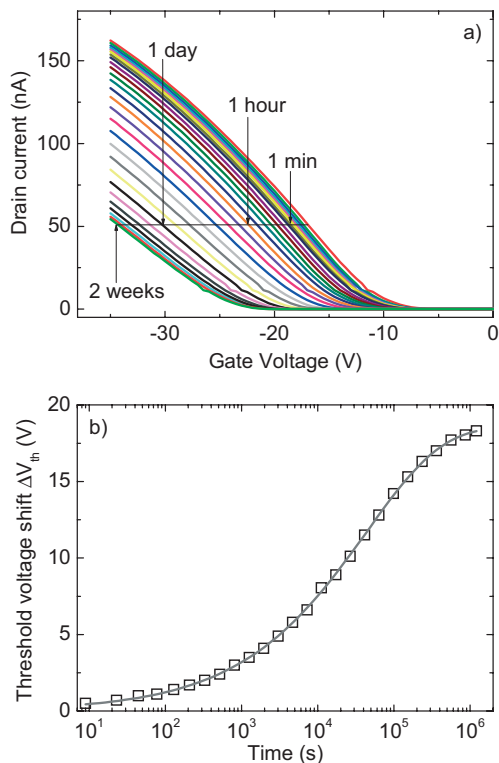

Figure 2. a) Linear transfer curves of PTAA transistors as a function of stress time. The gate bias during stress was –20 V and the temperature 140 °C. The arrows indicate transfer curves measured after 1 min minute up to 2 weeks. b) The threshold voltages obtained from Figure 2a presented as a function of time on a logarithmic scale. The fully drawn curve is a fit with a stretched-exponential time dependence.

stress time in the direction of the applied gate bias; in Figure 2a to the left. Arrows indicate transfer curves measured after 1 min up to 2 weeks. It shows that the magnitude of the shift decreases exponentially with stress time. Figure 2a also shows that the shape of the transfer curves hardly changes. The transfer curves are parallel. The main effect of gate bias stress is a shift of the threshold voltage, V_{th}, which is empirically defined as the intercept of the extrapolated transfer curve with the voltage axis.

We assume that the threshold-voltage shift is due to trapped charges with surface density N_{tr}. The threshold voltage shift, ΔV_{th}, is then given by $\Delta V_{th} = eN_{tr}/C_{ox}$ where C_{ox} is the capacitance of the gate dielectric and e the elementary charge. In other words, the trapped charges create an electric field that has to be compensated by the gate bias before an accumulation layer can be formed. The rate at which the charges are trapped depends on the free-carrier density N_f. For an exponential distribution of trap states, characterized by a temperature T_0, the trap rate is given by[6–8]

$$\frac{dV_{th}}{dt} \propto \frac{dN_{tr}}{dt} \propto N_f(t)\frac{t^{\beta-1}}{\tau^\beta} \qquad (1)$$

where τ is a characteristic time constant and the dispersion parameter β equals T/T_0. Solving Equation 1 with the bound-

ary condition that the threshold voltage at infinite stress time is equal to the applied gate bias, yields a stretched-exponential decay for the threshold voltage with time

$$\Delta V_{th}(t) = V_0 \left\{ 1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\} \qquad (2)$$

with $V_0 = V_g - V_{th,0}$, where $V_{th,0}$ is the threshold voltage at the start of the experiment. The relaxation time τ is thermally activated as

$$\tau = v^{-1} \exp\left(\frac{E_a}{k_B T}\right) \qquad (3)$$

where E_a is the mean activation energy for trapping, and where v is a frequency prefactor.

The threshold voltages are obtained from Figure 2a and presented as a function of time on a logarithmic scale in Figure 2b. The threshold voltage saturates with time. The maximum shift is equal to the applied gate bias. The fully drawn curve is a fit of the stretched exponential to the data. Perfect agreement is obtained for a relaxation time τ of 2×10^4 s and a dispersion parameter β of 0.44, yielding a characteristic temperature of the trap states, T_o, of 9×10^2 K. A similar agreement was found for stress measurements at other temperatures, and when using different values for the gate bias. We note that at times smaller than the relaxation time, τ, the stretched exponential can be approximated by a power law. This representation is used in the literature to analyze reliability measurements on a time scale too short to observe saturation.[9]

Reliability measurements on a-Si transistors and MIS (metal–insulator–semiconductor) diodes show a small deviation from a stretched exponential, especially close to saturation. A better agreement is obtained using a stretched hyperbola.[6,10,11] Mathematically the hyperbola is obtained when raising the trapped charge density, N_{tr}, in Equation 1 to a certain power a. The underlying physics is not well understood. For our measurements, the introduction of a parameter a different from unity does not improve the agreement and, therefore, is disregarded.

To further investigate the trapping dynamics, stress measurements on the PTAA transistors were performed at various temperatures. The threshold voltage shifts were fitted with a stretched exponential. The characteristic relaxation times, τ, are presented as a function of reciprocal temperature in Figure 3. A straight line is obtained showing that the relaxation time is thermally activated. The activation energy was determined to be 0.6 eV and the frequency prefactor, v, 10^3 s^{-1}. The insert of Figure 3 shows the values of the dispersion parameter, β, as a function of temperature. From the linear dependence we re-obtain the characteristic temperature of the trap states, T_o, of 9×10^2 K. For a-Si transistors, a modified temperature dependence has been suggested. An additional constant β_0 has been introduced by taking β equal to $T/T_o - \beta_0$. This refinement is beyond the accuracy of our measurements. Each data point in Figure 3 already required more than a week of measuring time.
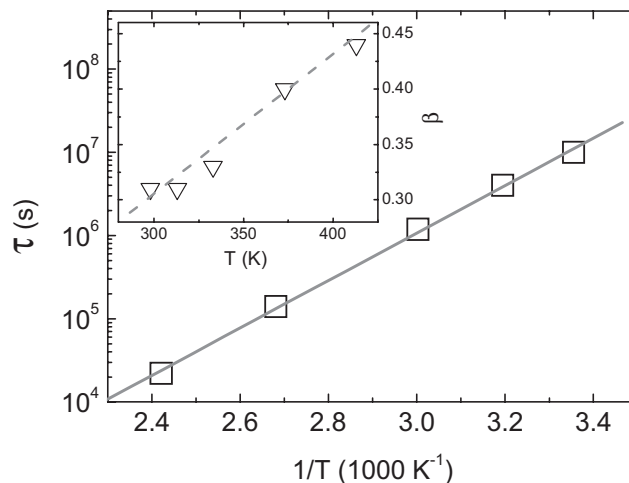

Figure 3. Relaxation times, τ, as a function of reciprocal temperature. The dashed line shows that the relaxation time is thermally activated with an activation energy of 0.6 eV. The inset shows the corresponding dispersion parameters, β, as a function of temperature. From the linear dependence, a characteristic temperature of the trap states of 9×10^2 K is obtained.

PTAA is an amorphous semiconductor. The transport is by hopping, that is, phonon-assisted tunneling, of charge carriers between localized states. The electrical transport of the PTAA transistors in accumulation can be fitted by using an exponential density of transport states with a characteristic temperature of 450 K. This value is significantly lower than that determined for the trap states of 9×10^2 K. This implies that charge transport states and trapping states have a different physical origin. The trapping for instance could be dominated by the interfaces. Therefore we varied both the thickness of the PTAA semiconducting film and the passivation of the SiO$_2$ interface. However, preliminary stress measurements did not yet unambiguously allow identification of the trap states.

Similarly, there is no explanation yet for the values of the activation energy and, especially, for the frequency prefactor. The activation energy is related to the microscopic nature of the trap site. The trap itself is unknown but a value of about 0.6 eV is not unrealistic. The value derived for v is about 10^3 Hz. It cannot be related to a simple phonon-mediated escape-to-attempt frequency; in that case values of around 10^{12} Hz would be expected.[12] We note however, that a stretched-exponential decay, or Kohlrausch relaxation, fits many relaxation processes in disordered electronic and molecular systems.[13] It holds for all dispersive transport processes in an exponential distribution of trap states. The prefactor can vary by orders of magnitude. Here we use the prefactor only to phenomenologically compare the reliability of organic transistors.

Apart from PTAA we investigated the reliability of polythienylenevinylene (PTV), P3HT, F8T2, 3-BuT5 field-effect transistors as a function of gate bias, stress time, and temperature. The experimental threshold-voltage shifts were fitted with a stretched exponential. Values derived for the prefactor

v and the activation energy E_a are presented in Table 1. Reported literature data on sexithiophene (T6), copper-hexadecafluoro-phthalocyanine (FCuPc) and single-crystalline pentacene are included as well. Our data, as well as the litera-

Table 1. Activation energy, E_a, frequency prefactor, v, and relaxation time at room temperature for investigated organic transistors as well as for amorphous and microcrystalline silicon transistors. Semiconductors comprise PTAA, PTV, P3HT, F8T2, and 3-BuT5. The table contains both our data as well as literature data. Values are presented for gate-bias stress in accumulation and recovery.

	Semiconductor	v [Hz]	E_a [eV]	τ @ RT [s]	Reference
STRESS	PTAA	10^3	0.6 ± 0.1	$1\,10^7$	This work
	PTV	10^6	0.62	$6\,10^4$	[17]
	T6	10^5	0.52	10^4	[19]
	FCuPc	–	0.51	–	[20]
	Pentacene (single crystal)	10^8	0.67	$4\,10^3$	[21]
	F8T2	–	0.52	$1.5\,10^4$	E_a: [22] τ: This work
	3-BuT5	10^7	0.6 ± 0.1	$3\,10^3$	This work
	P3HT	10^3	0.6 ± 0.1	$4\,10^7$	This work
	α-Si	10^9	0.98	$8\,10^7$	[12]
	μc-Si	10^6	1.07	10^{12}	[16]
RECOVERY	PTAA	4	0.3 ± 0.1	$1\,10^7$	This work
	α-Si	10^{13}	1.1-1.5	$5\,10^9$	[12]

ture data, show that the threshold voltage shift of organic transistors in accumulation is characterized by a common activation energy of around 0.6 eV. Differences in reliability are mainly due to differences in the value for the prefactor, v.

All measurements were performed at a high vacuum of 10^{-5} mbar. We observe that, in vacuum, a coverage of the SiO_2 gate dielectric with HMDS ranging from 0% to approximately 70% does not influence the threshold-voltage shift. However, the relaxation time in air decreases by an order of magnitude with respect to the measured value in vacuum. This indicates that the threshold voltage shift is due to residual water. This interpretation is confirmed by reported stress and temperature-dependent current measurements on organic transistors deliberately exposed to water vapor.[14,15,17] Table 1 shows that differences in the reliability are due to the difference in the frequency prefactor that ranges from 10^3 s^{-1} to 10^9 s^{-1}.

To benchmark the reliability of organic transistors we have included in Table 1 the typical frequency prefactor and activation energy for a-Si transistors. As a figure of merit we have calculated the relaxation time, τ, at room temperature. As shown in Table 1, the relaxation time of PTAA transistors is comparable to that of a-Si transistors. In the case of silicon-based transistors the frequency prefactor, v, ranges from 10^6 s^{-1} to 10^{10} s^{-1} depending on the silicon crystallinity. The activation energy is constant. The higher stability for microcrystalline-based transistors results mainly from the fact that v is more than three orders of magnitude lower.[16] Due to the high activation energy of a-Si transistors, at higher temperatures PTAA transistors are much more stable than their a-Si

counterparts. We note that the measurements were performed in a vacuum in the dark. The numbers derived are device parameters and represent state-of-the-art intrinsic electrical reliability.

In practical applications such as integrated circuits and active matrix displays, the transistor is only temporarily switched on. The generated threshold-voltage shift relaxes in the off state. Recovery of stress is therefore as important as stress in accumulation. We investigated the recovery by grounding both the drain and gate bias of stressed transistors and measuring the transfer curves as a function of time and temperature. The threshold-voltage shift in PTAA transistors is completely reversible and follows a stretched-exponential time decay. The relaxation times are presented in Figure 4 as a function of reciprocal temperature. The frequency prefactor is 4 s^{-1} and the activation energy is 0.3 eV. The dispersion parameter as a function of temperature is presented in the insert of Figure 4.
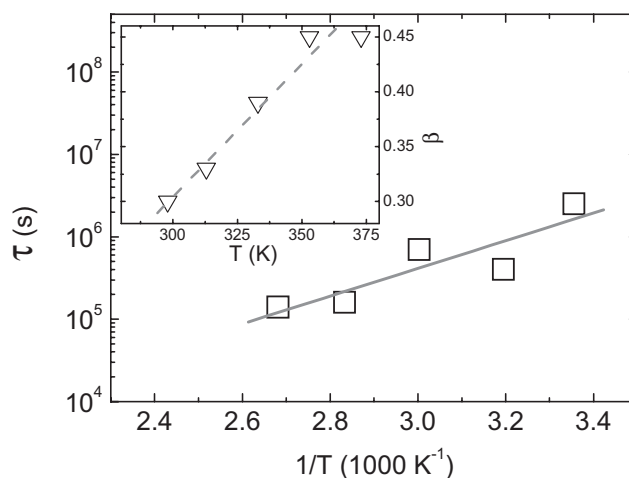

Figure 4. Recovery relaxation times as a function of reciprocal temperature. The stressed PTAA transistors were recovered by grounding both gate and drain electrodes. The dashed line shows that the relaxation time during recovery is thermally activated with an activation energy of 0.3 eV. The inset shows the corresponding dispersion parameters as a function of temperature. From the linear dependence a characteristic temperature of the trap states of 9×10^2 K is obtained.

From the linear dependence we derive a characteristic temperature of the trap states of 9×10^2 K, within experimental accuracy similar to the value derived from the stress measurements in accumulation. This is expected when probing the same density of states. The activation energy and prefactor in accumulation are different from those obtained in recovery. The differences are addressed by, for example, the defect-controlled relaxation model proposed by Crandall.[18] Verification requires measuring the activation energy in recovery as a function of stress time in accumulation.

Table 1 shows that for PTAA transistors at room temperature the relaxation times for stress and recovery are comparable. This is typical for organic transistors and completely different from a-Si transistors where stress is orders of magni-

tude faster than recovery. Finally, we stressed the PTAA devices at a positive gate bias where the transistor was in depletion. Quantitative analysis is hampered by the occurrence of hysteresis. However, the preliminary measurements show that the dynamics are at least an order of magnitude slower than at gate-bias stress in accumulation. The limited voltage shift in depletion indicates the high purity of the PTAA semiconductor.

In summary, we have investigated the reliability of organic field-effect transistors using PTAA as a model semiconductor. Electrical instabilities are due to threshold voltage shifts under applied gate bias. The drain bias can be disregarded. The threshold-voltage shifts with time according to a stretched exponential. The relaxation times in accumulation are thermally activated with activation energy of 0.6 eV. This value has been found to be typical for all other organic transistors. The origin is charge trapping at residual-water-related trap sites. Differences in the reliability of organic transistors are due to differences in the frequency prefactor that varies between 10^3 s^{-1} to 10^9 s^{-1}. The stress is completely reversible with comparable time constants. The measurements were performed in a vacuum and in the dark. The numbers derived here show the present status on the intrinsic reliability. The reliability of PTAA transistors is already comparable to that of a-Si transistors. There is on-going progress in the materials science of organic semiconductors and materials technology of transistors. Mobility values around unity have been demonstrated. Combined with the present reliability measurements it can be expected that organic transistors will soon outperform their a-Si counterparts.

Experimental

Field-effect transistors were fabricated using heavily doped p-type Si wafers as the common gate electrode with a 200 nm thermally oxidized SiO$_2$ layer as the gate dielectric. Using conventional photolithography, gold source and drain electrodes were defined in a bottom-contact device configuration (Fig. 1, inset) with a channel width (W) and length (L) of 1000 μm and 10 μm, respectively. A 10 nm layer of titanium was used acting as an adhesion layer for the gold on SiO$_2$. The SiO$_2$ layer was treated with the primer HMDS prior to semiconductor deposition in order to passivate its surface. PTAA films were spun from a toluene solution at 2000 rpm. for 20 s resulting in a film thickness of 80 nm. P3HT films were spun from a dichlorobenzene solution (7 mg mL^{-1}), 3-BuT5 and F8T2 films from a chloroform solution with a concentration of 10 mg mL^{-1} and 5 mg mL^{-1}, re-

spectively, also resulting in film thicknesses of around 80 nm. Freshly prepared devices were annealed in a vacuum of 10^{-5} mbar at 150 °C for 2 h. All electrical measurements were performed in a high vacuum (10^{-5} mbar) using a HP 4155C semiconductor parameter analyzer.

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