Physics

Nuclear Physics fields

Okayama University   *Year* 2005

Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracke

F Campabadal, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
C Fleta, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
M Key, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
M Lozano, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
C Martinez, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
G Pellegrini, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
J M. Rafi, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
M Ullan, *Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain*
L G. Johansen, *University of Bergen, Bergen, Norway*
B Mohn, *University of Bergen, Bergen, Norway*
O Oye, *University of Bergen, Bergen, Norway*
A O. Solberg, *University of Bergen, Bergen, Norway*
B Stugu, *University of Bergen, Bergen, Norway*
A Ciocio, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

R Ely, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

V Fadeyev, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

M Gilchriese, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

C Haber, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

J Siegrist, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

H Spieler, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

C Vu, *Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA*

P J. Bell, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

D G. Charlton, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

J D. Dowell, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

B J. Gallop, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

R J. Homer, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

P Jovanovic, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

G Mahout, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

T J. McMahon, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

J A. Wilson, *School of Physics and Astronomy, The University of Birmingham, Birmingham, UK*

A J. Barr, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

J R. Carter, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

M J. Goodrick, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

J C. Hill, *Cavendish Laboratory, Cambridge University, Cambridge,*

UK

C G. Lester, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

M A. Parker, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

D Robinson, *Cavendish Laboratory, Cambridge University, Cambridge, UK*

F Anghinolfi, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

E Chesi, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

P Jarron, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

J Kaplon, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

A Macpherson, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

H Pernegger, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

T Pritchard, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

S Roe, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

A Rudge, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

P Weilhammer, *CERN, European Organization for Nuclear Research, Geneva, Switzerland*

W Bialas, *Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland*

W Dabrowski, *Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland*

M Dwuznik, *Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland*

B Toczek, *Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland*

S Koperny, *Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland*

P Bruckman, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

S Gadomski, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

E Gornicki, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

P Malecki, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

A Moszczynski, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

E Stanecka, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

R Szczygiel, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

M Turala, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

W Wolter, *The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland*

L Andricek, *Max-Planck-Institut fur Physik, Munchen, Germany*

S Bethke, *Max-Planck-Institut fur Physik, Munchen, Germany*

D Hauff, *Max-Planck-Institut fur Physik, Munchen, Germany*

J Kudlaty, *Max-Planck-Institut fur Physik, Munchen, Germany*

G Lutz, *Max-Planck-Institut fur Physik, Munchen, Germany*

H -G Moser, *Max-Planck-Institut fur Physik, Munchen, Germany*

R Nisius, *Max-Planck-Institut fur Physik, Munchen, Germany*

R Richter, *Max-Planck-Institut fur Physik, Munchen, Germany*

J Schieck, *Max-Planck-Institut fur Physik, Munchen, Germany*

A-P Colijn, *NIKHEF, Amsterdam, The Netherlands*

T Cornelissen, *NIKHEF, Amsterdam, The Netherlands*

G W. Gorfine, *NIKHEF, Amsterdam, The Netherlands*

F G. Hartjes, *NIKHEF, Amsterdam, The Netherlands*

N P. Hessey, *NIKHEF, Amsterdam, The Netherlands*

P de Jong, *NIKHEF, Amsterdam, The Netherlands*

R Kluit, *NIKHEF, Amsterdam, The Netherlands*

E Koffeman, *NIKHEF, Amsterdam, The Netherlands*

A J. M Muijs, *NIKHEF, Amsterdam, The Netherlands*

S J. M Peeters, *NIKHEF, Amsterdam, The Netherlands*

B van Eijk, *NIKHEF, Amsterdam, The Netherlands*

I Nakano, *Physics Department, Okayama University, Okayama, Japan*

R Tanaka, *Physics Department, Okayama University, Okayama, Japan*

O Dorholt, *University of Oslo, Oslo, Norway*

K M. Danielsen, *University of Oslo, Oslo, Norway*

T Huse, *University of Oslo, Oslo, Norway*

H Sandaker, *University of Oslo, Oslo, Norway*

S Stapnes, *University of Oslo, Oslo, Norway*

N Kundu, *Department of Physics, Oxford University, Oxford, UK*

R B. Nickerson, *Department of Physics, Oxford University, Oxford, UK*

A Weidberg, *Department of Physics, Oxford University, Oxford, UK*

J Bohm, *Academy of Sciences of the Czech Republic (ASCR), Prague, Czech Republic*

M Mikestikova, *Academy of Sciences of the Czech Republic (ASCR), Prague, Czech Republic*

J Stastny, *Academy of Sciences of the Czech Republic (ASCR), Prague, Czech Republic*

Z Broklova, *Charles University, Prague, Czech Republic*

J Broz, *Charles University, Prague, Czech Republic*

Z Dolezal, *Charles University, Prague, Czech Republic*

P Kodys, *Charles University, Prague, Czech Republic*

P Kubik, *Charles University, Prague, Czech Republic*

P Reznicek, *Charles University, Prague, Czech Republic*

V Vorobel, *Charles University, Prague, Czech Republic*

I Wilhelm, *Charles University, Prague, Czech Republic*

P Cermak, *Czech Technical University, Prague, Czech Republic*

D Chren, *Czech Technical University, Prague, Czech Republic*

T Horazdovsky, *Czech Technical University, Prague, Czech Republic*

V Linhart, *Czech Technical University, Prague, Czech Republic*

S Pospisil, *Czech Technical University, Prague, Czech Republic*

M Sinor, *Czech Technical University, Prague, Czech Republic*

M Solar, *Czech Technical University, Prague, Czech Republic*

B Sopko, *Czech Technical University, Prague, Czech Republic*

I Stekl, *Czech Technical University, Prague, Czech Republic*

R J. Apsimon, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

L E. Batchelor, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

J P. Bizzell, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

N G. Falconer, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

M J. French, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

M D. Gibson, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

S J. Haywood, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

R M. Matson, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

S J. McMahon, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

M Morrissey, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

W J. Murray, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

P W. Phillips, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

M Morrissey, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

W J. Murray, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

P W. Phillips, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

M Tyndel, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

E G. Villani, *Rutherford Appleton Laboratory, Chilton, Didcot, UK*

D P. Cosgrove, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

D E. Dorfan, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

A A. Grillo, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

S Kachiguine, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

F Rosenbaum, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

H F. -W Sadrozinski, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

A Seiden, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

E Spencer, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

M Wilder, *Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA*

T Akimoto, *Institute of Physics, University of Tsukuba, Tsukuba, Japan*

K Hara, *Institute of Physics, University of Tsukuba, Tsukuba, Japan*

K Tanizaki, *Institute of Physics, University of Tsukuba, Tsukuba, Japan*

N Bingefors, *Department of Radiation Sciences, Uppsala Universit,*

Uppsala, Sweden

R Brenner, *Department of Radiation Sciences, Uppsala Universit, Uppsala, Sweden*

T Ekelof, *Department of Radiation Sciences, Uppsala Universit, Uppsala, Sweden*

L Eklund, *Department of Radiation Sciences, Uppsala Universit, Uppsala, Sweden*

J Bernabeu, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

J V. Civera, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

M J. Costa, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

J Fuster, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

C Garcia, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

J E. Garcia-Navarro, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

S Gonzalez-Sevilla, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

C Lacasta, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

G Llosa, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

S Marti-Garcia, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

P Modesto, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

F J. Sanchez, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

L Sospedra, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

M Vos, *Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain*

Design and Performance of the ABCD3TA ASIC for Readout of Silicon Strip Detectors in the ATLAS Semiconductor Tracker

F. Campabadal, C. Fleta, M. Key, M. Lozano, C. Martinez, G. Pellegrini, J.M. Rafi, M. Ullan

Instituto de Microelectronica de Barcelona, IMB-CNM, CSIC, Barcelona, Spain

L.G. Johansen, B. Mohn, O. Oye, A.O. Solberg, B. Stugu

University of Bergen, Bergen, Norway

A. Ciocio, R. Ely, V. Fadeyev, M. Gilchriese, C. Haber, J. Siegrist, H. Spieler, C. Vu

Lawrence Berkeley Laboratory and University of California, Berkeley, California, USA

P.J. Bell, D.G. Charlton, J.D. Dowell, B.J. Gallop, R.J. Homer, P. Jovanovic, G. Mahout, T.J. McMahon, J.A. Wilson

School of Physics and Astronomy, The University of Birmingham, Birmingham, UK

A.J. Barr, J.R. Carter, M.J. Goodrick, J.C. Hill, C.G. Lester, M.A. Parker, D. Robinson

Cavendish Laboratory, Cambridge University, Cambridge, UK

F. Anghinolfi, E. Chesi, P. Jarron, J. Kaplon, A. Macpherson, H. Pernegger, T. Pritchard, S. Roe, A. Rudge, P. Weilhammer

CERN, European Organization for Nuclear Research, Geneva, Switzerland

W. Bialas, W. Dabrowski, M. Dwuznik, B. Toczek, S. Koperny

Faculty Physics and Applied Computer Science, AGH University Science Technology, Krakow, Poland

P. Bruckman, S. Gadomski, E. Gornicki, P. Malecki, A. Moszczynski, E. Stanecka, R. Szczygiel, M. Turala, M. Wolter

The Henryk Niewodniczanski Institute of Nuclear Physics, Polish Academy of Sciences, Krakow, Poland

L. Feld, C. Ketterer, J. Ludwig, J. Meinhardt, K. Runge

Fakultat fur Physik, Albert-Ludwigs-Universitat, Freiburg, Germany

A.G. Clark, M. Donega, M. D'Onofrio, D. Ferrere, D. La Marra, D. Macina, M. Mangin-Brinet, B. Mikulec, A. Zsenei

Section de Physique, Université de Genève, Geneva, Switzerland

R.L. Bates, A. Cheplakov

Department of Physics Astronomy, University of Glasgow, Glasgow, UK

Y Iwata, T. Ohsugi

Department of Physics, Hiroshima University, Higashi-Hiroshima, Japan

Y. Ikegami, T. Kohriki, T. Kondo, S. Terada, N. Ujiie, Y. Unno

Institute of Particles and Nuclear Studies, KEK, Tsukuba, Japan

R. Takashima

Kyoto University of Education, Fukakusa, Fushimi-ku, Japan

P.P. Allport, A. Greenall, J.N. Jackson, T.J. Jones, N.A. Smith

Department of Physics, Oliver Lodge Laboratory, University of Liverpool, Liverpool, UK

G.A. Beck, A.A. Carter, J. Morris, J. Morin

Department of Physics, Queen Mary and Westfield College, University of London, London, UK

V. Cindro, G. Kramberger, I. Mandić, M. Mikuž

J. Stefan Institute and Department of Physics, University of Ljubljana, Ljubljana, Slovenia

I.P. Duerdoth, J.M. Foster, J. Pater, S.W. Snow, R.J. Thompson

School of Physics and Astronomy, The University of Manchester, Manchester, UK

T.M. Atkinson, B. Dick, F. Fares, G.F. Moorhead G.N. Taylor

School of Physics, University of Melbourne, Parkville, Victoria 3010, Australia

L. Andricek, S. Bethke, D. Hauff, J. Kudlaty, G. Lutz, H.-G. Moser, R. Nisius, R. Richter, J. Schieck

Max-Planck-Institut fur Physik, Munchen, Germany

A-P. Colijn, T. Cornelissen, G.W. Gorfine, F.G. Hartjes, N.P. Hessey, P. de Jong, R. Kluit,
E. Koffeman, A.J.M. Muijs, S.J.M. Peeters, B. van Eijk

NIKHEF, Amsterdam, The Netherlands

I. Nakano, R. Tanaka,

Physics Department, Okayama University, Okayama, Japan

O. Dorholt, K.M. Danielsen, T. Huse, H. Sandaker, S. Stapnes

University of Oslo, Oslo, Norway

N. Kundu, R.B. Nickerson, A. Weidberg

Department of Physics, Oxford University, Oxford, UK

J. Bohm, M. Mikestikova, J. Stastny

Academy of Sciences of the Czech Republic (ASCR), Prague, Czech Republic

Z. Broklova, J. Broz, Z. Dolezal, P. Kodys, P. Kubik, P. Reznicek, V. Vorobel, I. Wilhelm

Charles University, Prague, Czech Republic

P. Cermák, D. Chren, T. Horazdovský, V. Linhart, S. Pospísil, M. Sinor, M. Solar, B. Sopko, I. Stekl

Czech Technical University, Prague, Czech Republic

R.J. Apsimon, L.E. Batchelor, J.P. Bizzell, N.G. Falconer, M.J. French, M.D. Gibson, S.J. Haywood,
R.M. Matson, S.J. McMahon, M. Morrissey, W.J. Murray, P.W. Phillips, M. Tyndel, E.G. Villani

Rutherford Appleton Laboratory, Chilton, Didcot, UK

D.P. Cosgrove, D.E. Dorfan, A.A. Grillo, S. Kachiguine, F. Rosenbaum, H.F.-W. Sadrozinski,
A. Seiden, E. Spencer, M. Wilder

Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, California, USA

T. Akimoto, K. Hara, K. Tanizaki

Institute of Physics, University of Tsukuba, Tsukuba, Japan

N. Bingefors, R. Brenner, T. Ekelof, L. Eklund

Department of Radiation Sciences, Uppsala Universit, Uppsala, Sweden

J. Bernabeu, J.V. Civera, M.J. Costa, J. Fuster, C. Garcia, J.E. Garcia-Navarro, S. Gonzalez-Sevilla, C. Lacasta, G. Llosa, S. Marti-Garcia, P. Modesto, F.J. Sanchez, L. Sospedra, M. Vos

Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia-CSIC, Valencia, Spain

Abstract

The ABCD3TA is a 128-channel ASIC with binary architecture for the readout of silicon strip particle detectors in the Semiconductor Tracker of the ATLAS experiment at the Large Hadron Collider (LHC). The chip comprises fast front-end and amplitude discriminator circuits using bipolar devices, a binary pipeline for first level trigger latency, a second level derandomising buffer and data compression circuitry based on CMOS devices. It has been designed and fabricated in a BiCMOS radiation resistant process. Extensive testing of the ABCD3TA chips assembled into detector modules show that the design meets the specifications and maintains the required performance after irradiation up to a total ionising dose of 10 Mrad and a 1-MeV neutron equivalent fluence of 2×10^{14} n/cm^2, corresponding to 10 years of operation of the LHC at its design luminosity. Wafer screening and quality assurance procedures have been developed and implemented in large volume production to ensure that the chips assembled into modules meet the rigorous acceptance criteria.

Table of contents

1. Introduction

The Semiconductor Tracker (SCT) together with the Pixel Detector and the Transition Radiation Tracker (TRT) form the Inner Detector (ID) system in the ATLAS experiment being built for the Large Hadron Collider (LHC) at the CERN laboratory [1]. The SCT is built of double-sided modules, each one consisting of two pairs of daisy chained silicon strip sensors. The strips on the two sides are tilted by a small stereo angle of 40 milliradian, which provides the third space coordinate with a moderate resolution, i.e. z in the barrel part and r in the endcap parts. In the barrel part the strips are 12.8 cm long with a constant pitch of 80 μm. In the endcap discs of the SCT there are five different designs of the silicon strip sensor used. The electrical parameters of the barrel and the endcap sensors are very similar and the same front-end electronics can be used for the sensor of each type.

Each module comprises 1536 strips to be read out by means of twelve 128-channel front-end ASICs, which are assembled into a hybrid circuit and attached to the sensor assembly. The complete SCT detector will consist of 4088 silicon strip detector modules comprising approximately 6.3 million readout channels.

There are two aspects that influence strongly the design of all components of the SCT, and of the front-end ASIC in particular, namely the bunch crossing frequency in the LHC of 40 MHz and the required radiation resistance. The design specifications for the SCT front-end electronics, assuming 10 years operation of the LHC at the design luminosity scenario, are: 10 Mrad of total ionising dose and 2×10^{14} n/cm^2 of 1-MeV neutron equivalent fluence, including 50% uncertainty. The front-end ASIC must maintain the specified performance parameters after irradiation up to the above total ionising dose and 1-MeV equivalent fluence. In order to meet these requirements a special radiation hard integrated circuit technology has to be used.

The moderate spatial resolution requirement of the SCT can be achieved with strip pitch of 80 μm and binary readout architecture that guarantees resolution of 23 μm rms. The main advantage of the binary readout system is a drastic reduction of data to be read out as only addresses of channels that have recorded hits above the threshold are transmitted off the detector. For a big tracking system like the SCT this is an important aspect resulting in lower cost, a reduction of the material required for the data transmission system, and simplified off-detector readout electronics. On the other hand, in order to perform data sparsification in the front-end electronics a very robust front-end readout system is required. Besides the usual requirements concerning noise, speed and power dissipation, the channel-to-channel matching of gain, and discriminator threshold become very critical issues.

Another aspect, particularly important for the binary readout architecture, is the immunity of the overall system, and so of each component of the system, to external and internal interference, usually referred to as common mode noise. If one takes into account irreducible noise sources present in the front-end system, i.e. the parallel and series noise sources of the preamplifier and the shot noise of the detector leakage current, an achievable signal-to-noise ratio is about 15 at the beginning of the experiment and about 10 after irradiation of silicon strip detectors and front-end electronics up to the levels as expected after 10 years of LHC operation. With these signal-to-noise ratios there is very little room for setting the discrimination threshold in such a way that the detector is fully efficient and the noise occupancy is much lower than the physical data rate. Thus, any degradation of the signal-to-noise ratio will lead to either a drastic reduction of efficiency or increase of noise occupancy.

The ABCD3TA design is a single chip implementation of the binary readout architecture using the DMILL technology - a radiation resistant BiCMOS process comprising CMOS devices with 0.8 μm minimum gate length and bipolar devices with the cut-off frequency of 5 GHz. The final design is an outcome of several prototyping steps. The actual implementation of the required architecture and functionality depends strongly on the available technological options. At the beginning of the project a version based on two separate chips: CAFE [2] - a front-end chip realised in the MAXIM bipolar process and ABC [3] - a binary pipeline chip realised in the Honeywell bulk CMOS process, have been developed. The DMILL process [4], which became available at a later stage, permits combining all required functionality in a single chip. The ABCD3TA design follows closely the first prototype developed in the DMILL process, the SCT128B chip [5].

The first ABCD prototype chip met most of the requirements, however, the spread of the discriminator threshold in the front-end exceeded the acceptable level. Analysis of the problem led us to a conclusion that given the matching parameters of the DMILL technology we could not achieve the required performance following the original circuit concept. Therefore, the design was upgraded and in the ABCD2T chip threshold correction on a channel basis was implemented by adding a 4-bit digital-to-analogue converter (TrimDAC) per channel [6,7]. Extensive radiation testing performed for that prototype showed that matching performance degraded significantly after irradiation. In particular, after proton irradiation up to the full fluence the discriminator offset spread exceeded the range of the TrimDAC. Therefore, in the final version ABCD3TA the TrimDAC range adjustment was added to ensure that the offset spread is covered even in the case of a very large increase after irradiation, up to a factor of 5.

2. Requirements and specification for the front-end ASIC

2.1. Basic functionality

The ABCD3TA chip must provide all functions required for processing signals from 128 strips of a silicon strip detector and transmitting data off the detector module in the SCT. The basic functions are the following:

- charge integration,
- pulse shaping,
- amplitude discrimination,
- latching data either in the edge sensing mode or in the level sensing mode,
- storage of data in the pipeline for the first level (L1) trigger latency,
- derandomisation and compression of data,

- transmission of data from the chip via serial daisy chained outputs.

The ABCD3TA is required to provide reporting of some of the errors that may occur:

- attempt to read out data from the chip when no data is available,

- overflow of the derandomising buffer,

- derandomising buffer is no longer able to keep track of the data held in it (chip reset required).

- configuration error.

It is a system requirement that the fraction of data, which can be lost due to the readout buffer on the chip overflowing, will remain less than 1% for an occupancy up to 2% and an average trigger rate of 100 kHz. This includes a large safety factor as the expected worst case strip occupancy averaged over strips and time is about 1%. Furthermore, the chip shall incorporate features that will enable the system to continue operating in case of a single chip failure.

In addition to the requirements concerning basic functions related to receiving, storing and compressing the signals from the silicon strip detectors the ABCD3TA chip must be equipped with functions that allow full testability at various steps of module production, commissioning and running the experiment.

2.2. Parameters of silicon strip detectors

The SCT is built with single-sided AC coupled p-on-n silicon strip detectors with polysilicon bias resistors. The strip pitch is 80 μm and every strip is read out. A detailed description of the design and performance of the sensors can be found elsewhere [8]. Here we recall only the electrical parameters that are important for designing the front-end electronics. It is worth noting that the specifications for the electronics and for the sensors have been elaborated as a common project so that the electronics is optimised for this particular detector design and the design of the strip detectors is optimised for the binary readout scheme.

The electrical parameters of the SCT silicon strip detectors are listed in Table1.

2.3. Front-end basic requirements

Parameters and characteristics of the front-end circuit are driven mainly by the parameters of silicon strip detectors used in the SCT, in particular by the total strip capacitance and by the LHC machine beam crossing rate of 40 MHz. The noise performance is driven by the requirements regarding detection efficiency and noise occupancy. In order to ensure that detection efficiency is above 99% for each individual module, taking into account the Landau distribution of the charge generated in silicon strip detectors, smearing of charge by the magnetic field and charge division due to diffusion, the signals from the silicon strips must be discriminated at a

level corresponding to 1 fC. On the other hand, the noise occupancy is required to be kept below 5×10^{-4}. Combination of these two constraints leads to a requirement on the maximum Equivalent Noise Charge (ENC) of 1500 electrons rms for the nominal parameters of the silicon strip detectors and of the ASICs as measured on a fully populated unirradiated module. Degradation of the ENC is expected during the lifetime of the experiment due to unavoidable radiation damage to the silicon strip detectors as well as to the readout ASICs. After receiving nominal SCT fluence the ENC of a typical module is required to stay below 1800 electrons rms.

Since the discrimination threshold is common for all 128 channels in one chip, the above requirements translate into a requirement concerning the channel-to-channel spread of threshold. The threshold variation in one ABCD3TA chip must be much lower, by a factor of at least 5, than the signal fluctuations due to noise in order to ensure that the channel-to-channel threshold variation will not affect significantly the detection efficiency and the noise occupancy.

Regarding the timing performance, there is a basic requirement that each signal recorded in the silicon detectors is uniquely associated with the beam crossing from which it originated. This translates into a requirement that the timewalk be less than 16 ns allowing some margins for time jitter of the discriminator response and of the clock signals. The timewalk is defined as the maximum time variation in the output signal of the comparator over an input signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC. Associated with this is a requirement on double pulse resolution to be less than 50 ns for a 3.5 fC signal followed by another 3.5 fC signal. Note that we allow for pile-up of signals corresponding to two consecutive beam collisions, i.e. separated by 25 ns. Due to finite charge collection time in the silicon strip detectors and requirements on the noise it is impossible to shape the signals in the front-end circuit with the peaking time much shorter than 25 ns, which would be required to obtain double pulse resolution of 25 ns. On the other hand probability of finding the signals in the same channel for two consecutive beam collisions is low given the expected worst case strip occupancy in the SCT detectors of about 1%.

2.4. Data compression and readout

The data from silicon strip detectors has to be kept in the front-end chips for a time period corresponding to the ATLAS L1 trigger latency. A L1 trigger latency of 3.3 µs is assumed, including some margins for unknown fibre lengths, which requires a 132 cells deep pipeline clocked at 40 MHz. If the data corresponding to a given beam collision arrives at the end of the pipeline at the same time as the L1 trigger signal the data corresponding to three beam collisions, the given one, one before and one after, are stamped as valid and transferred to the derandomising buffer. Otherwise the data is considered as non-valid and is discarded at this point. This is a first

step at reducing the amount of data to be transmitted off the detector. In the second step only the addresses of channels with valid hits are encoded and transmitted off the detector. For an occupancy of 1%, i.e. hits in 1-2 channels of each chip, this provides another level of data compression. The third step is that the data is encoded such that only one address is transmitted for clusters of adjacent hit channels since pairs of hit channels are quite common.

The L1 trigger is generated with a Poissonian distribution in time at a mean rate of 100 kHz for the accelerator working at the nominal design luminosity. In order to keep the number of optical links for transmission as low as possible it is required that the maximum data rate transmitted off the detector corresponds to the average trigger rate and not the peak value of the trigger rate. In order to allow for such a solution the data has to be derandomised in the front-end chip. It is required that the derandomising buffer is eight events deep, which was found by Monte Carlo simulation to guarantee that less than 1 % of the data will be lost due to overflow in the derandomising buffers.

The SCT modules are designed to be read out via two optical links each, i.e. the data from six ABCD3TA chips have to be multiplexed and routed serially into one link. The transmission rate of 40 Mbit/s will be sufficient with a factor of 2 safety margin assuming the occupancy of the silicon strip detectors of 1% and the L1 trigger rate of 100 kHz. Note that there is no additional readout IC on the module to take care of organising and transmitting the data off the detector. Such an extra readout IC would require additional space on the modules and add material in the tracker volume. Instead the readout control has to be integrated in the ABCD3TA chips. The compressed data are routed via a token ring for six chips daisy chained on each side of the module.

2.5. System reliability

The SCT will operate within the large ATLAS detector. Any maintenance of the SCT will require removing several of the outer sections of the other ATLAS components, a task requiring more than one month. Therefore, maintenance opportunities are expected to be at most once per year. For this reason, the electronics is designed for high reliability and low maintenance. Minimizing system complexity improves reliability by reducing the number of components that can fail, which also improves the detector performance by minimizing material in the detector volume. Providing redundancy where possible minimises the effects of single point failures.

Each SCT module processes data from 1536 channels. In order to maximize system reliability, several design features are employed to minimize the chance for the loss of a total module in the event of single device or single component failure. One is the choice of a serial data path rather than a parallel data bus. The failure of a single driver on a parallel bus can disable the entire bus thus making the entire module non-functional. The failure of a

driver in a serial daisy chain will only break one link. To prevent the breakage of one link from disabling the entire chain, each ABCD3TA chip is required to have an alternate data path, which will bypass the non-functioning chip. In case of failure of one of the two optical links, the data from both sides of the module should be routed through the single functioning link.

To facilitate the serial data flow without the use of a separate readout IC, a data format was defined which allows a variable data length packet per L1 trigger but does not require the length to be specified at the beginning of the packet. Such a length field at the beginning of the packet requires extra data buffering to hold the data while the length is determined. Instead, the data format makes use of a trailer field, which is a unique pattern to denote the end of the packet.

In addition to a small number of single purpose control lines, the ABCD3TA is controlled via commands sent to one of the two serial command inputs. To minimize system complexity, the L1 trigger commands as well as other calibration and configuration commands are received via the same serial input. To accomplish this, a hierarchical command protocol is defined which allows frequent L1 triggers to be distinguished from longer, infrequently used commands without incurring any trigger deadtime. A 3-bit code identifies either an L1 trigger or some other command. The 3-bit code takes 3 clock cycles to be transmitted, which is the shortest time window allowed for consecutive L1 triggers by the ATLAS experiment, i.e. no more than 1 trigger every 75 ns. If the 3-bit code identifies a non-L1-trigger command, then a longer command string is assumed and some deadtime is assumed. The longer control commands are further divided into "Fast Control Commands" requiring a fixed 4-bit code length and "Slow Control Commands" of arbitrary variable length. The fast commands include those, which require synchronization with a specific clock sequence. The slow commands are intended for loading configuration registers. Care is taken in choosing the specific 3-bit and 4-bit patterns for these command codes to require more than a single bit flip to cause misidentification of a command. Rather, a single bit flip creates an invalid command, which is ignored.

Another design feature to enhance reliability is the requirement of two clock inputs and two command inputs. One control line, by maintaining either a high or low state, is used to specify whether the chip should use the normal clock and command inputs or the alternate two inputs. This allows the chip to continue to operate even if one of the clock or command lines, provided via optical links in the SCT system, fails during the life of the experiment.

2.6. Testability

Particular requirements regard testability of the ABCD3TA chip. Given very large numbers of chips that are needed for construction of the SCT detector it is important that all the components used are fully tested before being assembled into detector modules. This aspect is particularly important for the ABCD3TA chips as each module comprises twelve of them and failure of one chip or a large number of defective channels found after module assembly will disqualify the module resulting in loss of other expensive components, silicon sensors and hybrids. Therefore the ABCD3TA chips have to undergo very rigorous quality assurance tests, which can be implemented effectively provided that sufficient testability functions are built in the ABCD3TA design. However, significant amount of chip area cannot be devoted to special testability functions since space and allowed material on the detector module is extremely limited. Extra test time is accepted rather than adding extra test circuits, which would reduce test time.

Full electrical functionality tests and measurements of all important analogue parameters of the front-end have to be performed at the following steps: (1) wafer testing, (2) testing after assembly of chips on hybrids, (3) hybrid testing after burn-in, (4) testing of complete modules after assembly with silicon sensors. These tests have to provide data for calibration of the discriminator threshold scale with respect to the input charge as well as for offset corrections in the discriminators. In order to enable measurements of analogue parameters the front-end has to be equipped with circuitry that can inject charge signals into the preamplifier inputs, which are equivalent to the physical signals from the silicon strip detectors. The amplitude and the delay of the calibration signal with respect to the phase of the master clock has to be adjusted via the control logic. Furthermore, since in the binary readout architecture the basic analogue parameters are extracted from the discriminator threshold scans and the delay scans of the calibration signals, these scans have to be managed via the control logic.

The functionality and parameters of the digital part of the chip have to be tested by supplying test vectors to the inputs of the digital part of chip. These test vectors have to be delivered via the control logic.

3. Overview of the ABCD3TA design

The block diagram of the ABCD3TA chip is shown in Fig. 1. It comprises all blocks of the binary readout architecture, the front-end circuitry, discriminators, binary pipeline, derandomising buffer, data compression logic and the readout control logic.

The preamplifier-shaper circuit delivers signals with peaking time of 25 ns. This peaking time is sufficient for keeping the discriminator timewalk within the range of 16 ns and the double pulse resolution below 50 ns. It also

provides a reasonable optimum for relative contributions of the series and parallel noise sources, given total strip capacitance in a range 15 – 20 pF. The preamplifier-shaper circuit is followed by a discriminator with a common threshold for all 128 channels, which is controlled by an internal 8-bit DAC. In the ABCD3TA design, in addition to the threshold control common for all channels we have implemented individual threshold correction per channel using a 4-bit DAC (TrimDAC). The TrimDACs are used only for correction of the threshold offsets and are kept at fixed settings whereas the common threshold is adjusted to the required value. Similarly, the threshold scans which are used for extracting the basic analogue parameters of the front-end circuit are performed employing only the main 8-bit DAC common for all channels in the chip.

The binary data from the discriminator output are latched in the input register either in the edge sensing mode or with the level sensing mode with a time resolution of 25 ns and clocked into a 132-cell pipeline. The edge sensing mode puts a more rigorous constraint on the timing performance compared to the level sensing but minimises the rate of data to be transmitted off the detector.

Upon receiving a trigger signal the data are transferred from the pipeline to the second level buffer, which is a dual-port static RAM array 128-bits wide and 24-words deep. For each L1 trigger signal three columns from the pipeline are stored in this derandomising buffer, so that the buffer is effectively eight events deep. It compensates for rate fluctuations of the L1 trigger. The hit patterns from three consecutive bunch crossings corresponding to each L1 trigger signal are held in the buffer pending readout. The data is then compressed in the data compression logic according to one of four possible criteria (hit mode, level mode, edge mode, test mode) and read out via a token ring daisy chaining six chips into one optical fibre.

In addition to the basic functional blocks mentioned above, the ABCD3TA chip comprises calibration circuitry for internal generation of calibration pulses. The amplitudes of calibration pulses are set by an 8-bit DAC and the delay of calibration pulses relative to clock phase is controlled by a delay buffer of 5-bit resolution.

The chip has been designed to work with two power supply voltages: 3.5 V for the analogue part and 4.0 V for the digital part, although the nominal power supply voltage for the DMILL technology used is 5 V. A requirement to reduce the power supply voltages was driven by the constraint on the power consumption. The measured power consumption per chip is 260 mW for the analogue section and 140 mW for the digital section at a clock frequency of 40 MHz, resulting in an average power less than 3 mW/channel.

The die area of the ABCD3TA chip is equal to 6550×8400 μm^2. The front-end part is built mainly of bipolar devices and comprises about 30,000 components, while the digital part comprises about 200,000 CMOS devices.

The pitch of the input pads is 50 μm so that a pitch adapter is needed to match the detector strip pitch of 80 μm. The layout drawing of the ABCD3TA chip is shown in Fig. 2.

3.1. Front-end

The binary front-end circuit comprises the preamplifier, shaper and the discriminator. The diagram of the circuit implemented in the ABCD3TA chip is shown in Fig. 3. The preamplifier is based on a transimpedance configuration using a bipolar transistor with emitter area of (1.2×10) μm^2 as the input device. For a bipolar input transistor the dominant noise source, i.e. the equivalent voltage noise, depends, in the first approximation, on the value of the collector current and is independent of the transistor size. The size of the input transistor has been optimised taking into account two other effects, namely the series noise contribution from the base spread resistance and the parallel shot noise of the base current. The latter one increases after irradiation due to a decrease of the current gain factor β.

In order to optimise the size of the input transistor radiation effects in DMILL, bipolar transistors of various emitter areas have been studied [9]. Similar behaviour of β as observed for other bipolar technologies has been found, i.e. the degradation of β due to radiation effects scales with the collector current density. Therefore, in order to minimise the effect of radiation on the β factor for a given collector current, the minimum geometry input transistor would be preferable, however, noise of the base spread resistance would be too high for such a transistor. For the chosen geometry the base spread resistance is relatively low, of the order 100 Ω, and β is expected to be not less than 40 after irradiation up to a total dose of 10 Mrad and an equivalent neutron fluence of 2×10^{14} n/cm^2, as expected for the SCT detector.

The input stage is followed by a single-ended voltage amplifier built of two gain stages closed with a resistive feedback loop, which determines the gain. This stage introduces a pole in the preamplifier transfer function that is responsible for the integration time constant. Following the gain stage there is an ac coupled differential stage converting the single-ended signal into a differential one, which is then applied to the discriminator. Although the ac coupling is not an ideal solution as it may lead to a shift of the baseline for high rate of pulses, this configuration is driven by the critical aspect of the binary readout architecture, i.e. matching of the gain, noise and dc levels at the shaper output since a common threshold for all 128 channels in the chip is applied. The required uniformity is obtained by (i) suppressing the dc gain by ac coupling between the amplifier and the discriminator, (ii) sufficiently high gain in the preamplifier-shaper circuit, of the order of 50 mV/fC, and (iii) a differential scheme for setting the discriminator threshold. Both stages following the preamplifier, i.e. the single-

ended stage and the differential one, provide additional poles so that the overall shaping function of the circuit is equivalent to a CR-$(RC)^3$ filter with a peaking time of about 20 ns. The peaking time becomes closer to 25 ns if one takes into account the charge collection time in silicon strip detectors, which is about 10 ns for the bias voltage above 300 V, as foreseen to be applied in the SCT detectors.

3.1.1. Discriminator

The discriminator is designed as a differential comparator in the Schmitt trigger configuration with capacitive positive feedback. The threshold voltage as well as the input signal are applied differentially. In this simple solution the timewalk, an important parameter, is determined directly by the rise time of the signal at the shaper output. The requirement concerning the timewalk suits well to the requirement concerning the shaper peaking time which is driven by the three other issues: (i) relative contribution from the parallel noise and the series noise sources, (ii) ballistic deficit, and (iii) double pulse resolution. For the SCT detector it is required that, for the nominal threshold setting corresponding to an input charge of 1 fC, the timewalk is below 16 ns for an input signal range from 1.25 fC to 10 fC.

The discriminator threshold is controlled by the differential voltage applied to the discriminator inputs via the differential amplifier preceding the discriminator. Scanning of the threshold is a main tool for measuring the analogue parameters. Therefore, the threshold voltage that is common for all 128 channels in the chip is generated by an internal DAC with 8-bit resolution, which is set via the control logic. The threshold setting covers a range from 0 mV to 640 mV with steps of 2.5 mV, which for the nominal gain of the front-end circuit of 50 mV/fC corresponds to the range of input signals from 0 fC to 12.8 fC with a step size of 0.05 fC.

In this configuration with a common threshold voltage for all 128 channels the actual threshold for each individual channel depends on the discriminator offset as well as on the gain in the front-end circuit for that particular channel. The discriminator offset is determined only by the offset and gain of the differential pair preceding the discriminator. Initially it was assumed that the required uniformity of the discriminator threshold could be achieved by proper sizing of the devices that contribute the offset in each channel, i.e. the transistors and resistors in the differential pair preceding the Schmitt trigger and the transistors of the Schmitt trigger. Both stages are based on bipolar devices, for which adequate matching of the V_{be} voltages was expected. Good matching of the V_{be} was confirmed in the first prototype, however, at the same time it was found that matching of the resistors was much worse compared to the expected values. As a result the threshold spread was determined mostly by matching of the resistors used as the load devices of the differential amplifier.

Furthermore, irradiation tests showed that the matching of those resistors degraded significantly after irradiation with charged particles, by a factor of about 4.

Thus, in order to guarantee the required uniformity in the final ABCD3TA version, the threshold correction on a channel basis has been introduced. In each channel there is a 4-bit DAC, named TrimDAC, which is used to compensate the threshold offset. In addition, the range of the TrimDAC can be set by two additional bits. For a given step of the TrimDAC the expected rms value of the threshold spread is step/$\sqrt{12}$. The TrimDAC ranges, corresponding steps and expected relative spreads of the threshold for the nominal setting of 50 mV, corresponding to an input charge of 1 fC, are summarised in Table 2. The minimum range (range 0) covers the expected threshold spread at the beginning of the experiment before significant radiation damage occurs. With accumulated radiation damage the offset spread in the discriminator will increase so it will require a larger range to make sure that all the channels can be trimmed. Of course, the resulting spread of the threshold will be higher for higher ranges used, however, the signal-to-noise ratio will also decrease. In order to introduce a safety margin for possible unexpected effects that can occur in the experiment, the maximum range has been chosen to be a factor of 2 higher compared to the worst case offset spread measured after proton irradiation up to the nominal fluence of 3×10^{14} p/cm^2 (see section on radiation effects).

The discriminator output current is converted into a full swing signal in the output inverter. The stage of the Schmitt trigger and the output inverter is supplied from the digital power supply so that one avoids large voltage swings in the front-end part connected to the analogue power supply. For the positive current signal from p-on-n silicon strip detectors the output inverter is HIGH when there is no signal and is switched to LOW in response to a signal.

3.1.2. Calibration circuit

Each channel has an internal calibration capacitor of 100 fF connected to its input allowing injection of test charges. The voltage step pulses are generated by an internal chopper circuit, which is triggered by a command. Every fourth channel can be tested simultaneously with group selection determined by a 2-bit binary coded calibration address. The strobe and the address signals are delivered from the control circuitry. The amplitude of the voltage steps applied to the calibration capacitors by the chopper is determined by a resistor and the current that is controlled by an internal 8-bit digital-to-analogue converter (calibration DAC). The amplitude of the calibration pulse can be set within a range from 0 to 160 mV with 8-bit resolution, i.e. 0.625 mV/step. For the calibration capacitor of 100 fF the charge range and the resolution is 16 fC and 0.0625 fC/step respectively.

The duration of the strobe signal is fixed and equal to 200 ns whereas the delay with respect to the clock phase is controlled by a delay register and can be tuned within a range of 50 ns with 5-bit resolution, i.e. 1.56 ns/step. Since the delay circuit is realised as a series of inverters, in order to minimize circuit complexity, the overall delay is directly dependent on the process variation and, therefore, has to be cross-calibrated using the external clock signal. It is therefore required that in an extreme case of process variation the overall delay covers at least one clock period of 25 ns, which is the basic requirement for full characterisation.

The four calibration bus lines, each one connecting the calibration capacitors of every fourth channel, are also brought out to pads that can be directly driven from an external signal generator. These pads are foreseen for cross checking of the internal calibration circuitry and are not used on the detector modules. The features of the internal calibration circuit enable to test and calibrate the ASICs either at the wafer level or in situ.

3.2. Data buffering

The binary data produced at the discriminator output has to be latched synchronously with the clock and then buffered on the chip until the chip receives a L1 trigger. Latching and buffering the data is performed in three blocks: input register, pipeline and derandomising buffer.

3.2.1. Input register

A simplified schematic diagram of single channel of the input register is shown in Fig. 4. It comprises three blocks: edge detecting circuit, masking logic and mask register cell. The input register latches the incoming data, delivering to the pipeline a pulse of well defined width. In the basic mode of operation the data is latched in edge sensing mode. The circuit detects a HIGH to LOW transition in the discriminator output signal and, for each such transition found, the circuit generates a pulse of duration equal to one clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single "1" is written into the pipeline for every hit detected regardless of the response time of the discriminator. This circuitry can be turned on or off by setting the appropriate bit in the configuration register. If the edge sensing function is turned off the data is latched in the level mode, in which a "1" is produced for each coincidence of the low level at the discriminator output and the rising edge of the clock signal. For discriminator outputs longer than one clock period the circuit produces multiple responses written into the pipeline.

A trade-off between the edge sensing and the level sensing modes is the efficiency vs. readout occupancy. An important parameter of the detector module is the in-time efficiency defined as the probability for a hit to be correctly associated with a given LHC beam crossing. In the level sensing mode one can avoid in-time

inefficiency, however, the occupancy of readout channels is substantially higher compared to the hit occupancy. Since for most of the hits the response of the discriminator will be longer than 25 ns the average rate of data written into the pipeline in the level sensing mode will be about a factor of 2 higher than the rate of data at the discriminator output. In the edge sensing mode the occupancy in the readout channels is the same as the hit occupancy but the in-time efficiency becomes a critical parameter.

A part of the input register is the mask register, which serves a dual purpose. Firstly, the channel mask register can be used to turn off any bad or noisy channel thus preventing increase of data rate due to false hits. Secondly, it can be used for chip testing to apply a set of test patterns to the pipeline input. The contents of this register can be changed by sending the appropriate control command to the chip. In the test mode the digital part of the ASIC, from the input register up to the output, can be tested separately without using the signals from the front-end.

3.2.2. Pipeline

The binary pipeline is realised as a multiplexed FIFO circuit. The operational principle of a single pipeline channel is shown schematically in Fig. 5. An array of $m \times n$ memory cells is controlled by m non-overlapping clock signals. The input data in a single channel is multiplexed into m rows. In each clock cycle only one cell per row is switched. After $m \times (n-1)$ clock cycles the data is shifted to the end of the row and de-multiplexed to the output. As a result only m out of $m \times n$ cells are switched in each clock cycle while the effective delay provided by such a block is equal to $m \times (n-1)$ clock cycles which is equivalent to $m \times (n-1)$ memory cells. In our case each pipeline channel is built of a memory block of 12×12 cells resulting in an effective depth of 132 cells since for each clock cycle the data is copied from one column to the following one. This way the data corresponding to a given time bin is always stored in two adjacent columns.

The basic memory cell shown in Fig 5b is realised as a semi-static circuit. A particular feature of this circuit is provided by the feedback transistor, which maintains the output state independently of leakage in the pass transistor and threshold voltage shifts in the inverter, which may appear after irradiation. In Fig. 5c the structure of the output demultiplexing cell is shown.

The applied architecture results in two additional very valuable features: low power consumption and a very compact layout, which is particularly important as the circuit is implemented in a 0.8 μm CMOS process of relatively low density. The pipeline block of 128 channels, each 132 bits deep, occupies an area of 9 mm^2 only. The expected power consumption for this block is of the order of 140 μW/channel at a clock frequency of 40 MHz and does not depend on the data rate.

3.2.3. Derandomising readout buffer

The ABCD3TA chip contains a second level readout buffer, which is realised as a dual port static RAM array, 128 bits wide by 24 bits deep, allowing simultaneous write and read operations. Three bits of data are stored in this buffer for each channel per L1 trigger. These bits represent the three beam crossings centred on the L1 trigger time and are set if the input was above threshold during the corresponding crossings. The task of this buffer is to remove the time fluctuations from the L1 trigger distribution. The hit patterns corresponding to each L1 trigger are stored in the second level buffer pending a readout strobe. Up to 8 events can be stored in the readout buffer, which assures that the dead time will be less than 1% at the maximum first level trigger rate of 100 kHz, provided that the strip occupancy is less than 2%.

A block diagram of the readout buffer is shown in Fig. 6. The RAM block is addressed by two cycling pointers, a write pointer and a read pointer. Once the pointer has reached the end of the RAM, it returns to the beginning the next time it is incremented. The write pointer is allowed to go past the read pointer and over-write data that has not yet been read out. However, if this happens the Overflow flag is set to indicate that data has been over-written. The read pointer is not allowed to pass the write pointer and if the read pointer should catch up with the write pointer the Empty flag is set. This is to prevent attempts to readout the buffer when there is no data in it.

An overflow counter is used to track the number of events that have been overwritten in the buffer. This counter is incremented every time an event is written into the buffer while the buffer is full. The output from this counter represents the number of events from which data has been lost. This counter is decremented every event that is readout of the buffer, until its value reaches zero. In this state all the events from which data have been lost are cleared and none of the data in the buffer represents overwritten events. Should this counter overflow, the Error flag is set and it remains set until either a software reset or a power-up reset has been issued to the readout buffer and associated logic.

3.2.4. Data compression

Given the foreseen worst case strip occupancy of 1% on any event, very few channels will contain hits. Therefore, compressing of data will result in a significant reduction of the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each group of 3 bits is compared against one of the four selectable criteria. If the pattern meets the criteria, then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This

process is repeated until the hit patterns from all 128 channels have been examined. Table 3 shows the four selection criteria.

The data compression circuit operates as follows. After receiving a L1 trigger the three 128-bit words that constitute an event are written into the readout buffer. The flag on the readout buffer is set, indicating that there is data to be processed. The data compression logic monitors the state of this flag until it finds that there is data available. Providing that the circuit is not already processing data, it then proceeds to read in the three 128-bit words that constitute an event from the readout buffer. In the next step the data compression logic rearranges the order of the data from being three 128-bit words into one hundred twenty eight 3-bit words because the data compression algorithm requires all three samples of an event to be examined in parallel.

The data compression logic then starts to scan through all the channels in turn until it finds one, which has a pattern of hits that matches the chosen data selection criteria. If it finds such a pattern of hits, it validates the data and attaches the 7-bit channel address to the hit pattern. The logic then waits until the readout logic signals it to proceed by asserting the next input. If the next hit found is on the next adjacent channel, the ADJ bit is asserted with the data from the previous channel. If no more hits are found, the END signal is asserted.

3.3. Data readout

The SCT module has twelve ABCD3TA chips, six on each side. The compressed data is read out from six chips via a token ring daisy chaining the chips on each side. The chips can be configured as a Master (M), Slave (S) or End (E) chip. On each side the chips are configured as follows: one Master, four Slaves and one End. The interconnections between the chips on the module are shown in Fig. 7. The black lines show the primary connections and grey lines show the redundant connections. Each chip has a pair of token and data inputs/outputs, normal (N) and redundant (B) used for bypass connections. The data output of the Master chip is connected to the optical fibre interface.

After reception of a L1 Trigger, the Master chip initiates a readout cycle by sending the preamble bits at the start of each data block to the optical link driver. It then appends its data bits to the output stream sent to the optical link driver. Once the last bit of data has been sent, the Master chip sends a token to the Slave chip on its right. The Slave chip on the right responds by sending its data packet to the Master, which in turn is appended to the preamble and data bits from the Master already sent to the optical link driver. Once this Slave chip has finished sending its data, it also passes on the token to the next chip on the right. The next chip on the right passes its data onto the previous chip on the left, which in turn passes it back to the Master chip for transmission to the link driver. This process continues until the last chip in the chain has sent its data. A bit is set in the End

chip in the chain to define it as the last chip. When this chip has sent its data it appends a trailer to the end of the data stream. While the Master chip is outputting data, it is constantly looking for the trailer pattern that has been carefully chosen to be distinct from the data. Once it finds the trailer pattern, it knows that all the data from the event has been sent and it can start processing the next event.

In the event of the failure of one of the Slave chips, the previous and next chips in the chain are programmed to route their data and tokens around the failed chip using the redundant connection on the hybrids. If the End chip in the chain should fail, then the last Slave chip in the chain is programmed to perform the operation of the End chip. In the event of the failure of a Master chip in the chain, the data and tokens from the chain with the failed Master chip are routed to the working Master chip on the other side of the hybrid.

3.3.1. Readout circuitry

The readout control circuitry is responsible for capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives. On arrival of the token, it checks if any hits have been found by the data compression logic. If so, it then outputs the appropriate header pattern, the address of the hit channel together with the data from that channel. Once the readout circuitry has finished sending the data from one channel, it proceeds to output the data from the next channel. In the situation where one or more neighbouring channels are to be read out, only the address of the first channel is output, but the data from all hit channels is sent. This process continues until the data compression logic indicates that all channels have been examined by asserting the End code. Once all the data corresponding to a single event has been read out, a token is sent out to the next chip in the readout chain. If the chip has no data to be read out, circuitry sends out the No-Hit-Data code and passes the token on to the next chip in the chain. In the case of an error condition occurring, e.g. attempt to readout data while no data available, the appropriate error code is sent by the readout logic. If the chip is in the Send-Id mode of operation, no data or error codes are output from the chip but instead a special packet of data containing information about the chip's current configuration is sent.

The building blocks of the readout circuitry are:

- **Readout Controller Block** - this block is enabled by placing the chip in the Master mode and has to detect L1 trigger, issue a token, collect all the data from the chips and tag the data with the beam crossing number from which it came and the number of the L1 Trigger.

- **L1 Counter** - is a 4-bit binary counter that is incremented every time the chip receives an L1 trigger.

- **Beam Crossing Counter** - is an 8-bit binary counter that is incremented on every clock cycle.

- **Event FIFO** - is a 24 location deep, 12-bit wide FIFO. Each time the chip receives an L1 trigger, the output of the L1-Counter and the Beam Crossing Counter are loaded into the FIFO prior to the counters being incremented. These values are read from the FIFO every time an event is read out and are used to tag the data with 12-bits of information about the trigger number and beam crossing number from which the data came.

- **Token Generation Logic** - detects when the chip has received an L1 trigger and when to generate a token to initiate the readout of data from that L1 trigger. This logic waits until the Event FIFO becomes not empty and it then issues a token. It then monitors the data passing through it from all the chips in the chain looking for a "Trailer" bit pattern.

- **Data Formatting Logic** - attaches the header information to the packets of data output from the chip on the Serial Data Output.

- **Serial Data Output Driver** - outputs the data to the DAQ system.

3.4. Chip control

The command and control information all comes into the chip on the command input pins. The Command Decoder block decodes the command and sends the relevant instruction and data to other parts of the chip. There are two main classes of information which arrive here, L1 Trigger Commands and Control Commands. These are distinguished by a 3-bit code. Furthermore two types of Control Commands are possible, Fast Control Commands and Slow Control Commands. The two classes of Commands and two types of Control Commands are:

- **L1 Trigger Command** - in response the control logic writes 3 samples from the pipeline into the Readout Buffer.

- **Fast Control Commands** - this type of command is sent when a command has to be issued to the chip more quickly than can be achieved by sending a slow command. There are only two commands of this type: the Soft Reset and Beam Crossing Counter Reset. These commands will be sent to the chip at regular intervals during periods of time when no L1 Triggers will be sent to the chip in order to perform a limited reset of the chip.

- **Slow Control Command** - these are long packets that enable the configuration of all internal registers of the chip and operation of the chip in various test modes. All chips that receive the command must decode it, even if they do not act on it. This is to avoid un-addressed chips erroneously decoding parts of the data field as the start of another command. To ensure that the chip does not respond to erroneous commands the chip will be placed out of data taking mode for any command it receives which affects the configuration of the chip.

Hence, it will be necessary to issue a command to the chip to enable data taking after issuing a command to change its configuration. When the chip is not in data taking mode, it will send its ID instead of real data in response to a L1 Trigger.

3.5. Input/Output circuits

The input/output circuits in the ABCD3TA chip are designed to ensure compatibility with the design of the overall readout system of the SCT detector in the ATLAS experiment. In particular, robust operation and low noise performance should be maintained when the detector modules are operated in the electrical environment of the experiment. The signal receivers should provide robust reception of signals and high rejection of noise, which may be generated by other components of the readout system. At the same time the noise generated by the output signal drivers of the ABCD3TA chips should be minimised. Since the fast signals, clock, commands and data, are transmitted to and from the detector module comprising 12 ABCD3TA chips by means of optical links the noise considerations due to switching of fast signals can be limited mostly to a single detector module.

In order to guarantee robust reception of signals and low noise generation, all fast signals from and to the chip are transmitted in the differential mode. In the ABCD3TA design the LVDS standard, which has become the most popular differential data transmission standard in the industry, has been adopted. The LVDS is a low swing, differential signalling technology, which allows data transmission at hundreds or even thousands of Megabits per second over distances of tens of metres, provided that proper cables are used.

On the SCT modules the distances of traces are much shorter and the nominal required speed of 40 Mbit/s is relatively slow compared to the capability of standard LVDS circuits, however, the reduced noise generated by them minimizes interference to the front-end amplifiers allowing simultaneous data acquisition and I/O operation. The receivers of the clock and command signals are designed to meet the specification of the LVDS standard. The driver circuits, which transmit the data to the optical link driver is designed as an LVDS type but with driving capability adjusted to the requirement of the SCT detector module thus minimizing power consumption. The output data is sent to the optical link driver only by the Master chip and the output driver is not used in the Slave and the End chips. In order to avoid dissipating unnecessary power on the module, the driver circuit is set in a power off mode when the chip is configured as a Slave or an END chip, which reduces the power consumption per chip from 64 mW in active state to 4 mW when disabled.

The LVDS-like input/output circuits are used also for passing the data and token between neighbouring chips on the module. The driving capability of these circuits is much reduced compared to the driver used for sending the data off the Master chip as the distances to transmit the signals are much shorter and the capacitive loads of

the traces do not exceed 10 pF for primary connections on the hybrid and 50 pF for redundant connections on the hybrid.

4. Design for large volume production

The full SCT requires 49,056 conforming ASICs, not counting the spares. Obviously, given the requirements for the overall efficiency of the SCT to be better than 99%, use of any out-of-spec chips would result in a degradation of the tracking performance of the ATLAS detector. In addition some losses are unavoidable through the full construction process. A loss model was established for losses that may occur in various steps starting from receiving the wafers from the foundry, through wafer saw, hybrid and module assembly and test culminating with installation of complete modules. The assumed model resulted in a requirement of 61,000 conforming chips.

Based on the yield of 26% guaranteed by the foundry vendor we ordered 961 6-inch wafers which amounts to 250,000 chips to be tested. The number of ordered wafers implied that wafer fabrication would span 12-18 months and about 40 fabrication lots. Over this period of time the wafers could display the full range of process variations. Therefore, as a part of the design procedure and preparation for production, extensive simulations were made using corner model parameters supplied by the vendor, including post-rad conditions, combined with the assumed variation of temperature and power supply voltages.

In order to illustrate the issue let us recall a few parameters from the corner models provided by the vendor:

- the current gain factor β of bipolar transistors may vary between production lots from 90 to 350; for the worst case, after neutron irradiation, one has to accept β as low 40.

- the threshold voltage for the PMOS transistor may vary between production lots from −0.69 V to −1.15 V; in addition the maximum expected drift after irradiation is up to −200 mV

- the threshold voltage for the NMOS transistor may vary between production lots from 0.69 V to 1.05 V; in addition the maximum expected drift after irradiation is up to −200 mV

- the resistor value may vary between production lots by ±25%; in addition the resistor value increases by 25% after irradiation.

On top of these variations, the design specification also required that the IC meets the functional specifications over the temperature range of 0 to 40°C and for power supply voltages differing by ±200 mV from the nominal values.

In the light of the above numbers it is clear that particular effort was needed to make the design insensitive to the variations of process parameters, temperature, power supply voltages and to radiation effects. In order to validate the design extensive corner simulations have been performed for all combinations of the corner models, temperature and power supply voltages. As an example the results of corner simulations for the gain of the front-end circuits are shown in Fig. 8. Each point on the plot represents one combination of the device corner parameters, temperature and bias voltage. There are nine corners for parameters of MOS transistors (PSET: $0 \div 8$) combined with four values of resistors, three values of power supply voltage and two temperatures. Given very wide ranges of variation of all these parameters some variations of the circuit parameters are unavoidable, but the fabricated chips must still meet specifications. Although the corner parameters resulting from process variations are specified by the vendor at the 3σ level deviation from the nominal values and the probability of occurrence of some combinations is very low, it was decided to require that for the simulations the circuit should be fully functional for any combination of process, temperature and power supply voltage variation. This conservative approach was taken to provide an additional safety margin with respect to unexpected situations that may appear in the experiment.

For the digital blocks the following design strategy has been applied. The standard cell library has been parameterised for different corner parameters, power supply voltages and temperatures. It was required that the digital circuits should operate correctly at the nominal clock frequency of 40 MHz over the temperature range of 0 to 40°C and for the power supply voltage differing by ± 200 mV from the nominal value of 4 V. It is worth noting that we have set the nominal digital power supply voltage for the ABCD3TA design at 4 V, although the nominal power supply voltage for the DMILL technology is 5 V and the foundry parameterisation is valid for 5 V power supply. Reduction of the power supply voltage was required to keep the power consumption as low as possible.

Taking into account the corner parameters resulting in the slowest operation of the digital circuitry, degradation of the digital speed due to reduced power supply voltage, increased temperature and radiation effects, it has been found that all these factors combined together may result in the speed of the digital circuitry being reduced by a factor of 2 lower compared to the speed for nominal foundry parameters, power supply and temperature 0°C. For practical reasons most of the digital simulations have been performed for the nominal parameters and nominal conditions, while requesting that all digital circuitry should be fully functional at the doubled clock frequency, i.e. 80 MHz.

5. Module performance

Requirements for the analogue parameters and characteristics of the ABCD3TA ASICs are specified for given parameters of the silicon strip detectors. Therefore, the performance of the ASICs should be validated by demonstrating that the requirements are met for a fully loaded module designed according to the SCT specification. It is important to note that some design aspects can be demonstrated only in the final fully loaded modules. This applies in particular to parameters like phase margin of the preamplifier, input impedance of the preamplifier, power supply and common mode noise rejection ratio, immunity to digital noise.

In this section we present examples of basic electrical characteristics of the barrel SCT modules being now produced in series. A photograph of the barrel module is shown in Fig. 9. The details on the module design and on the construction steps can be found in [10]. The basic analogue parameters are: gain, noise (ENC), threshold spread, noise occupancy at a given threshold and timewalk.

5.1. Gain offset and noise

Given the binary architecture of the ABCD3TA chip, the parameters of the front-end channel can be extracted from the threshold scans performed for different amplitudes of test pulses. For each value of the test charge the result of the threshold scan is a complementary error function of which the 50% point corresponds to the signal amplitude at the discriminator input and the transition width contains information on noise spread. The calibration circuitry built in the ABCD3TA design enables the testing of all the channels in the ASICs mounted in a module without necessity of using external test signals. As a result of the threshold scans one obtains a response curve for each individual channel, i.e. the discriminator threshold as a function of the input charge. From the response curve one then extracts the gain of the front-end circuit and the discriminator offset for each individual channel. From the error functions one extracts the rms value of noise at the discriminator input, which then can be translated into the equivalent ENC at the input. Typical distributions of gain offset and noise for 762 channels on one side of the module are shown in Fig. 10.

The ENC for a fully populated module is below 1500 electrons rms and is consistent with the value measured for a single channel with equivalent input capacitance. The measurements shown correspond to the hybrid temperature of 25 °C. The ENC increases with increasing temperature by about 5 electrons rms per degree.

Comparison of the channel-to-channel and chip-to-chip spread of the gain and of the offset shows that for a threshold of 1 fC the offset spread will dominate the effective threshold spread.

5.2. Uniformity of threshold

Good channel-to-channel uniformity of the nominal 1 fC threshold is essential for operation of the binary readout system. The effective discrimination threshold in terms of the input charge is determined by the discriminator offset as well as by the gain of the front-end circuit of a given channel. The uniformity of the effective 1 fC threshold is ensured through the ASIC threshold correction circuit, where each channel is provided with a trim DAC of 4-bit resolution with four selectable ranges. The first range (0 mV – 60 mV) is used pre-irradiation, which gives channel-to-channel alignment at the 4 mV bin level with a threshold of ~ 100 mV for all channels. This is to be compared with the noise value of ~ 12.5 mV. Therefore, the channel-to-channel threshold spread effectively contributes less than 1% to the pre-irradiation module noise values.

Figure 11 shows the distribution of 1 fC threshold before and after the trimming procedure. One can notice that the spread of the threshold before trimming is at the same level as the spread of the discriminator offset shown in Fig. 10. This proves that the offset spread dominates the uniformity of the effective threshold.

5.3. Noise occupancy at 1fC threshold

The SCT design goal is to set the ASIC single-strip binary readout threshold at 1fC in order to ensure high tracking efficiency for particles traversing the silicon at inclined angles, depositing charge on more than one readout strip. The mean noise occupancy for all channels of a module is shown in Fig. 12. The noise occupancy of the individual unirradiated modules at 1 fC, even if operated at room temperature, is typically $<1\times10^{-5}$, which is well below the level of 5×10^{-4} required for correct operation of the SCT.

5.4. Timewalk

The requirement is that the timewalk should be less than 16 ns. Here, timewalk is defined as the maximum time variation in the comparator output over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC. Figure 13 shows measured data for one chip on a barrel module. The top plot shows the delay of the comparator response (in strobe delay units) versus injected charge (fC) and the bottom plot shows the timewalk distribution in nanoseconds measured for input charges from 1.25 to 10 fC as defined above. The specification is met for all channels with an additional safety margin of about 4 ns.

6. Radiation effects

The detector together with its readout electronics will be located close to the interaction point and so exposed to high levels of radiation. The highest accumulated radiation levels expected in the ATLAS SCT after 10 years

of operation, including 50% uncertainty, will be 10 Mrad of total ionising dose and a 1 MeV neutron equivalent fluence of 2×10^{14} n/cm^2, causing displacement damage. The ABCD3TA chip is realised in a BiCMOS technology so it is built of MOS transistors, which are primarily susceptible to ionising radiation, and bipolar transistors using oxide-isolation structures, which are susceptible to both displacement damage and ionising radiation. High energy particles present in the SCT radiation field will cause single event effects (SEE), which have to be taken into account as well. To validate the design of the chips with respect to radiation hardness, an extensive irradiation program has been performed in which about 300 chips in total have been irradiated with various radiation sources.

In the ABCD3TA design there are some particularly critical parameters and characteristics that are affected by radiation: noise of the front-end, matching in the front-end circuit, in particular the offset spread of the discriminator, speed of the front-end and the speed of the digital CMOS circuitry. Increase of power consumption after irradiation is another critical aspect because of the limited capability of the cooling system to remove the heat from the active volume of the detector and because of limited capability of the power supply system to deliver the power.

Given the particular composition of the radiation field in the SCT detector and the complexity of radiation effects in the basic devices and in the complete integrated circuit, ideally, one would prefer to perform radiation tests in the field identical or similar to the one expected in the experiment. Such a source of radiation is, however, not available. Therefore irradiations of the ABCD3TA chips were performed using different available facilities:

- 24 GeV proton beam at CERN [11],
- 200 MeV pion beam at PSI, Villigen, Switzerland,
- neutrons from the TRIGA reactor in Ljubljana, Slovenia [12],
- ^{60}Co source at different sites in California, USA,
- X-ray source at CERN.

The proton beam and the pion beam deliver both the ionising dose and the displacement damage as expected in the SCT detector. In order to study and to factorise the ionising effects and the displacement damage, the devices were tested separately with X-rays and gamma photons causing primarily ionisation damage and with neutrons causing primarily displacement damage. The devices in the SCT detector will be exposed to neutrons with a broad energy spectrum, from thermal up to tens of MeV of energy, so one should verify whether

displacement damage caused by neutrons is of the same nature as the displacement damages caused by charged particles.

In addition to the commonly known and usually considered radiation effects in semiconductor devices, there are two particular effects in the ABCD3TA chips, which have been studied in detail, namely the low dose rate effect in bipolar transistors and the damage of bipolar transistors caused by thermal neutrons.

Chips irradiated with charged particles and neutrons were mounted on hybrids and were biased, configured and clocked during irradiation. Analogue parameters were measured using the internal calibration circuit of the ABCD3TA.

6.1. Analogue performance under irradiation

The front-end stage of the ABCD3TA chip is built as a transimpedance amplifier using a bipolar input transistor. One of the noise sources, which contribute to the total ENC, is the shot noise of the base current of the input transistor, which is increased due to the decrease of the current gain factor β. In bipolar transistors β is degraded by ionisation effects as well as by displacement damage. Irradiation with protons and neutrons were therefore performed to study the noise performance of the chips.

In the binary readout scheme precise control over channel-to-channel threshold matching is one of the most critical issues. Tests of the chip prototypes showed that matching of the resistors is the limiting factor for the offset spread in the discriminator and that resistor matching degrades significantly after irradiation with neutrons or protons. Threshold spread was therefore also a matter of concern after irradiation with protons and neutrons.

6.1.1. Proton irradiation results

Irradiation with 24 GeV proton beam at the CERN PS were performed in conditions most similar to those expected in the experiment. The radiation environment provided by the PS beam was close to what is expected in the ATLAS experiment, except for the neutron field, and it allowed for testing the components with respect to total ionising dose, bulk damage due to charged particles and single event effects. Therefore, the PS facility was used as the standard irradiation test bed for SCT electronics.

During irradiation hybrids were kept inside a cold box flushed with nitrogen at a temperature of about 2 °C, which will be the operating temperature of the chips in the ATLAS experiment. At this temperature the annealing of radiation damage in bipolar and CMOS structures is negligible. The proton beam with a spot size of 1×2 cm^2 was scanned across the hybrid. Chips received the total fluence of 3×10^{14} p/cm^2 during a period of about

10 days. The displacement damage of this proton fluence is equivalent to 1.8×10^{14} n/cm^2 [13]. The total ionisation dose delivered with this proton fluence was 10 Mrad.

Evolution of noise with fluence measured in proton irradiation is shown in Fig. 14. The noise increase after full fluence agrees with expectations. The noise shown in Fig. 14 was measured with open inputs so that the capacitance at the preamplifier input was negligible. In an SCT module, i.e. with strips connected to inputs, the total noise will be dominated by the voltage noise contribution due to the strip capacitance. As the input voltage noise of preamplifier is determined by the transconductance of the input transistor, it is not influenced directly by the radiation effects. However, due to decrease of β one has to reduce the collector current in the input transistor in order to keep the base current and so the shot noise within an acceptable range. As a result the transconductance of the input transistor will be respectively lower and the voltage noise higher. Irradiation of full modules with protons proved that required efficiency and noise occupancy could be maintained also after irradiation [14].

An example of the evolution of untrimmed threshold spread with fluence for six chips is shown in Fig. 15. One can notice that the spread increases rapidly after initial radiation and then saturates above 1×10^{14} p/cm^2. One can also notice some spread between the chips. Therefore, as discussed in sec. 3.1.1, an additional safety factor has been foreseen in the range of the TrimDAC to make sure that one can correct the threshold for all the channels with peak-to-peak spread of up to 240 mV. It is expected, however, that for a majority of the chips trimming at range 1, i.e. 120 mV, will be sufficient after receiving the full expected fluence and the threshold spread after trimming will be negligible compared to noise.

6.1.2. Neutron irradiation results

Hybrids were irradiated with neutrons by inserting them into the reactor core through an irradiation tube. The neutron energy spectrum in the irradiation tube spans from thermal energies to about 10 MeV [15]. From the measured flux the NIEL equivalent flux of 1 MeV neutrons was determined [16] using the neutron damage function for silicon from [17]. The equivalent fluence of 2×10^{14} n/cm^2, was delivered to the chips within 440 s. During this time chips received also about the same fluence of thermal neutrons and about 400 krad of ionisation dose from gamma background. Temperature of the chips during irradiation was about 30°C.

Figure 16 shows evolution of noise with fluence of 1 MeV equivalent neutrons measured during irradiation in the reactor. One can note a slightly larger noise increase at the same NIEL fluence (note that the proton fluence in Fig. 14 should be multiplied by 0.6 to get the fluence in units of 1 MeV neutrons) in chips irradiated with

neutrons as compared to protons. This effect was seen also in other irradiation tests of SCT readout chips [8] including the irradiation of basic DMILL bipolar test structures.

Recent irradiation results indicate that this effect can be explained by additional damage in bipolar transistors caused by thermal neutrons, which are present in the reactor channel [18]. These are not present in the PS and also do not contribute to the 1 MeV equivalent fluence, however, they will be present in the SCT detector. Displacement damage is enhanced in this case by the energetic products of the nuclear reactions of thermal neutrons and boron atoms used as doping in the base of the bipolar transistors. The thermal neutrons are captured by boron isotope ^{10}B resulting in a reaction ^{10}B $+ n \rightarrow ^{7}$Li $+ \alpha$. Although doping concentration of boron in the base is relatively low, of the order of 10^{18} cm^{-3}, and abundance of ^{10}B in natural boron is only about 10% the fluence of α-particles and lithium ions becomes significant due to the particularly high cross section of boron to capture thermal neutrons which reaches 3840 barns. The total energy of 2.3 MeV released in this reaction is divided between the α-particle and the lithium ion and deposited in a very short range of a few microns from the interaction point. In addition, there are heavily doped p^{+} regions below the base contacts and energetic α-particles and Li ions originating from boron capture reactions in these regions can contribute to the damage in the transistor base.

6.1.3. X-ray irradiation results

Comparison of the results from proton and neutron irradiation does not provide a definitive answer whether ionisation effects present in proton irradiation contribute significantly to degradation of the current gain factor β in bipolar transistors. In order make an estimate of ionisation effect on bipolar transistors the ABCD3TA chips were irradiated with X-rays of 10 keV energy. The irradiation was performed at a dose rate of 36 krad/min up to a total dose of 10 Mrad. The measurements were taken immediately after irradiation so that no significant annealing took place.

Figure 17 shows the noise as a function of the collector current of the input transistor before and after the X-ray irradiation. After the X-ray irradiation one can see a small increase of noise as predicted, since in this case only limited degradation of the beta parameter is expected.

6.1.4. Low dose rate tests

All the irradiation tests reported above have been performed with dose rates 2-3 orders of magnitude higher than those expected in the ATLAS experiment. Therefore, one should address a question about validity of such tests performed on a time scale of days or weeks when used for making predictions for 10 years of operation of

the ATLAS experiment. Typically, the effects caused by ionising radiation undergo some annealing and irradiation at high dose rate results in larger effects compared to irradiation up to the same total dose but performed at low dose rate. For CMOS devices and circuits a well established annealing procedure has been elaborated that allows one to convert high dose rate irradiation results to irradiation conditions at low dose rate [19].

Recently several reports have been published on the Low Dose Rate Effect (LDRE) observed in modern bipolar transistors using oxide isolation technique when irradiated with ionising radiation [20,21]. The effect is opposite to what is typically observed in CMOS devices, i.e. irradiation with a low dose rate leads to larger degradation of β compared to irradiation with a high dose rate up to the same total dose. This effect may lead to underestimation of the radiation damage when performing radiation tests with a high dose rate, which is the only practical way to achieve a full ATLAS dose. The ATLAS experiment is intended to operate for ten years, including periodic breaks. In the SCT detector an average dose rate of 0.05 rad(SiO_2)/s is expected [1].

Many different approaches have been tried to test dose rate effects on bipolar technology, and recent studies have shown that high temperature irradiation at high dose rates can mimic the effects of low dose rate irradiation [22-24]. It has been seen that these effects are strongly technology dependent, which means that each new technology has to be tested. Since the DMILL technology uses oxide isolation technique in the structure of bipolar transistors it is potentially susceptible to the LDRE. Therefore, a dedicated irradiation experiment has been performed in order to understand whether bipolar transistors in the DMILL technology are susceptible to LDRE [25].

All irradiations have been done using three different ^{60}Co sources. A Pb+Al shielding box has been used together with geometrical considerations in order to avoid dose enhancement effects according to standards [26,27], guaranteeing less than a 20% systematic error in the dosimetry. The dosimetry was performed using thermoluminiscent devices (TLD), also according to standards [28]. Since the net results of ionisation effects depend on the bias conditions during irradiation, the transistors were kept biased in forward directions as used in analogue circuits. The tests were performed in two steps.

In the first phase of the experiment the transistors were irradiated at a very wide range of dose rates, all reaching a total dose of 1 Mrad(SiO_2) in order to obtain data even for the very low dose rates in a reasonable period of time. The dose rates chosen covered a range of four decades and the values were: 0.05, 0.28, 1.33, 31.1, 112, 575 rad(SiO_2)/s. The relative decrease of beta ($\Delta\beta/\beta$) in all these experiments was in the range 10 - 15% and there was no indication of LDRE in these transistors.

However, in order to prove that the LDRE does not appear at high doses at low dose rate, irradiation should be performed up to a total dose of 10 Mrad at dose rate of 0.05 rad/s, which would correspond to the real conditions in ATLAS-SCT. Such an experiment would take too long to provide meaningful results. A solution to the problem is to map out the damage on the transistors vs. the total dose taking intermediate measurements for increasing total doses up to 10 Mrad. In this way one can perform low dose rate irradiation up to a certain achievable total dose, and then estimate the damage at the final total dose by extrapolation. Furthermore, one can see if irradiations done at different dose rates lead to divergence of curves corresponding to different dose rates. The conditions of the four different mapping experiments that have been performed for this purpose can be seen in Table 4.

The results of this experiment for the DMILL transistors are shown in Fig. 18. One can notice that for all dose rates there is no significant dependence on the dose rate. A somewhat larger effect observed for the dose rate of 1.24 rad/s and for the total dose above 2 Mrad is, however, much smaller compared to effects reported in the literature for processes that exhibit LDRE. Based on these results we have concluded that there is no significant LDRE that would have to be taken into account for evaluating radiation hardness of bipolar transistors in the DMILL technology.

6.2. Digital performance under irradiation

6.2.1. Digital speed

The primary radiation effect in the digital CMOS circuitry of the ABCD3TA is a decrease of the maximum clock frequency at which the chip correctly performs all operations. Since the speed of the CMOS circuits depends on the power supply there are two parameters which provide information about the speed margins of the chip:

- maximum speed measured at the nominal supply voltage of 4 V

- minimum supply voltage at which the chip works correctly at 40 MHz.

Figure 19 shows the degradation of speed of the ABCD3TA chip after X-ray irradiation up to a total dose of 10 Mrad. The results are shown for the following digital tests:

- TEST 1 - L1/BC counters check, which tests the functionality of the two counters by reading out several even records;

- TEST 2 - configuration check, which validates write and read-back of the configuration register;

- TEST 3 - L1 overflow check, which validates the error flags by forcing an overflow of the derandomising buffer;

- TEST 4 - data taking, which tests the full data path from pipeline through readout buffer.

We observe a degradation of speed almost by a factor of 2, nevertheless, after 10 Mrad the chip still meets the requirement of 40 MHz operation at the nominal supply voltage. It is worthy to note that the results shown in Fig. 20 do not include any annealing so that they represent worst case post-radiation conditions.

Radiation resistance of the digital circuitry has also been proven in proton irradiation tests. During typical irradiations with a total fluence of 3×10^{14} p/cm^2 the chips also received an ionising dose of about 10 Mrad. Although the primary goal of this irradiation was testing the radiation resistance of the front-end circuitry, the measurements of analogue parameters were performed at the nominal clock frequency of 40 MHz. Thus, this required that all the digital blocks involved in the readout of data operated correctly after receiving the full dose of 10 Mrad.

After delivering an ionising dose to the chips, an increase of current consumption in the digital part of the chips was observed. This current increase was identified as the leakage current between MOS transistors. The excess current did not influence the digital performance of the chips. However the power consumption must comply with the limitations imposed by the power distribution and cooling systems of the SCT. It should be noted that all measurements showed that the current increase (on average 50 mA/chip) would be manageable in the ATLAS experiment.

6.2.2. SEU test results

The SCT readout chips in the experiment will be exposed to high energy particles. A maximum of 3×10^{14} hadrons/cm^2 with energy greater than 20 MeV will cross the ABCD3TA chips during their lifetime. Study of the sensitivity of the chips to Single Event Effects (SEE) was therefore equally important as the study of the cumulative effects.

There are two major types of digital blocks in the ABCD3TA chip that may be affected by SEE: the pipeline and the static registers that contain information about chip configuration and settings of operating points. A bit flip in the pipeline causes a single data error and does not require intervention. The rate of such events has to be compared with the noise hit rate from the front-end. Errors in the static registers may lead to changes in the operating mode and will require reloading of the chip configuration.

Measurements of the SEE have been done with the 24 GeV proton beam at the CERN PS and the 200 MeV pion beam at the PSI. Beam structures at these two sites are quite different. At the PS the beam is structured in

short spills of very high intensity whereas at the PSI the pion beam is quasi-continuous with 50 MHz structure. Nevertheless results of measurements at the two sites are rather consistent. This is expected since the cross section for SEE is expected to saturate well below 200 MeV [29].

The scheme of measurement was to write to a memory cell in the device, let a certain fluence traverse the device and then read the content of the cell. From the number of differences observed between the written and read-back values and known fluence the probability for a bit flip in such cells was calculated. Measurements were done with pipeline and mask register cells. The latter were used as the estimate of SEE rate also of other static register cells in the chip. Results of measurements using the proton and the pion beam are summarised in Table 5.

The numbers in Table 5 are used to estimate the impact of SEE on the performance of the SCT. To make a conservative estimation it can be taken that the sensitivity of pipeline cells is 10^{12} particles/cm^2/flip and of static registers 5×10^{13} particles/cm^2/flip. During 10 years of LHC operation the machine will be running at high luminosity for about 1/3 of the time i.e. about 10^8 sec. To estimate the worst case SEE rate it can be taken that maximum of 3×10^{14} fast particles/cm^2 will cross the chips during this time giving the maximum flux of 3×10^6 particles/(cm^{2}s). With 132 bits per channel in the pipeline one expects an SEE rate of 10^{-11} per bunch collision (every 25 ns) per channel. This number is negligible compared to the expected noise occupancy of 5×10^{-4}.

Similar consideration for static cells gives the SEE rate of 6×10^{-8} bit-flips/s per cell. With 10 critical bits per chip and 6 chips daisy chained for one link and 96 links per off-detector readout crate, the expected SEE rate is 3×10^{-4} /crate/s. Such an error rate can easily be handled by reloading chip configurations in regular intervals from the off detector readout electronics.

7. Large volume production

As already stated, the full SCT requires 49,056 conforming ASICs installed but our model for losses in assembly and installation created a requirement for 61,000 good chips. Given the expected yield of 26% based upon the foundry's guarantee, the production plan was made for 961 wafers or roughly 250,000 ICs.

The production plan included the following steps:

- Receipt of wafers from the foundry vendor with visual inspection.

- Full functional test of each IC in wafer form

- Wafer saw and selection of good ICs

- Assembly of ICs into hybrid circuits containing 12 ICs each.

- Test of full hybrid circuit including long-term test.

The resources of the ATLAS-SCT collaboration are such that the testing and assembly work needed to be shared by several institutions. The testing of wafers was conducted at three sites: the CERN laboratory in Switzerland, the Rutherford Appleton Laboratory in the UK and the University of California, Santa Cruz in the US. The good chips were then sent to several other institutes for assembly into hybrids and long term testing. Given that bare, not packaged dice are assembled into the hybrids, the hybrid test was the first practical point where long term testing could be performed. The material flow for the ASIC production is shown in Fig. 20.

7.1. Wafer testing

The assembly procedure of the SCT modules requires that the ASICs be fully tested at the wafer level. These tests should provide not only information about basic functionality but also full characterisation of the analogue parameters. The requirements to measure precisely the analogue parameters at the wafer testing stage demanded development of a custom wafer testing system since the program of measurements could not be realised using a standard IC tester. The basic measurements performed for the ABCD3TA chips include:

- analogue front-end performance (gain, noise and comparator offsets for every channel),

- digital functions (control register, addressing, communication, pipeline, output buffer),

- sensitivity of digital functionality to clock frequency and supply voltage,

- internal DACs linearity,

- I/O signal properties (timing, amplitudes, duty cycles),

- power consumption

7.1.1. System overview

The block diagram of the wafer testing system is shown in Fig. 21. The system is based on the VME standard and consists of several custom designed boards and control software. The system is controlled by a GUI written in Visual C++, which runs in a PC under Microsoft Windows (W95/NT/2000). The GUI is based on the code for the previous version of the test system [31]. The PC communicates with the VME crate using the NI-VXI interface from National Instruments.

The crate houses a custom-designed VME board equipped with an ORCA3T FPGA. The FPGA operates at 40 MHz and interprets the VME commands, communicates with the ASIC under test, and controls most critical parameters in the system. The data between the VME board and the probe card are transmitted as differential

signals. Two intermediate boards, named Pin Driver and Connector Board, have been designed to transfer and control the signals between the VME crate and the probe station. The Connector Board contains high current, high speed drivers AD53040 with variable output signal levels to test ABCD3TA inputs. It contains also window comparators discriminating on the upper and lower ABCD3TA output signal levels. The signal delays and the window comparator levels are controlled by the FPGA through the DACs.

The probe card has been designed using a standard probe card technology combined with a custom designed printed circuit board following the rules required for low-noise analogue measurements.

The standard procedure of measuring the analogue parameters of the ABCD3TA chips requires the transmitting of large amounts of data between the chip and the data acquisition system. The transmission is one of the factors that drive the testing time. Therefore, the VME board has been designed to perform the low-level data processing that reduces the amount of data to be transferred to the PC. The FPGA was programmed to be able to issue a sequence of ABCD3TA input commands, which can be looped over a given number of times. Furthermore, a dedicated data-stream-decoding algorithm was conceived to interpret the data from the chip and to extract the numbers of channels having hits. The count of the number of hits for each channel is stored in a memory chip on the VME board. The number of hits per channel, together with the decoding algorithm error codes, is the only information from the test to be read out. This scheme greatly reduces the amount of information transferred from the VME board to the PC.

The functions of the digital circuitry of the IC are verified using test vectors, which define the sequence of the IC's control line values for consecutive clock cycles. The IC's output signals are transmitted to the FPGA and compared with the expected data corresponding to that particular test vector. Only the binary result of the comparison is read out. Both the stimulus test vector and the expected chip response are stored in memory chips on the VME board, which makes it possible to run the test vector multiple times without reloading. This allows repetitive testing to detect soft errors. The expected chip response was obtained with Verilog simulation of the ABCD3TA chip design. The FPGA algorithms do not interfere with the test vector content, which allowed for rapid test vector development without firmware changes.

Digital tests can be performed at frequencies higher than the nominal 40 MHz. This capability is achieved by buffering the signals in IDT72V2113 FIFOs, which are able to perform the read/write operations at different frequencies. The FIFOs can hold the data for up to 262,000 clock cycles. The data exchange between the FPGA and the FIFOs is done at 40 MHz, and the data flow between the FIFOs and the probe card can be done at a different frequency in the range between 40 and 100 MHz.

The data taken required substantial, post-test analysis to extract the analogue performance from the binary ASIC data. This was done initially at the testing sites and then at CERN for all the data. This ensured consistent treatment of data from different sites, allowed archiving of all data and uploading to a common database. These results were used to make the final selection of good ASICs.

7.1.2. Testing procedures

7.1.2.1. Analogue Tests

The basic method for the characterisation of the analogue circuitry of the ABCD3TA relies on scanning the threshold while injecting a fixed calibration charge. This measures the integral of the Gaussian distribution of noise superimposed on the signal. Repeating these scans for several amplitudes of calibration charges one extract the gain, offset, noise and the trim DAC performance. For each scanning point 200 triggers are sent to the chip under test. With the test parameters chosen for production testing, the accuracy of noise measurement is dominated by the 9% statistical uncertainty. The precision of the gain and trim DAC linearity measurements is dominated by 5% error on the calibration pulse amplitude. Their statistical uncertainty is less than 1%.

7.1.2.2. Digital Tests

The test vectors have been developed to characterise the performance of different parts of the digital circuit. The following set is used in the test:

- Configuration register R/W test - a value is written to the ABCD3TA configuration register, then the chip is set to present the content of the register on the output, and the values are compared. All bits of the ABCD3TA configuration register are scanned.

- Addressing, beam counter and the error code test – the chip possesses an addressing scheme to distinguish different chips on a module. The counter of the LHC beam crossings is embedded in the output data to separate the information from different events. The bits of both counters are scanned. In addition, abnormal conditions are created and the chip response is verified.

- Data compression logic test - functionality of different criteria for data sparsification is verified. Hits are placed in different time slices relative to the trigger.

- Dynamic digital pipeline test - the digital data are supplied to the input register of the digital circuit according to channel mask. Time structure of the pipeline is scanned.

- Static digital pipeline test - the digital data are supplied directly to the pipeline, avoiding the input register.

- Redundant command line test - the dynamic pipeline test is performed using the redundant input command and clock lines.

- Data and token by-passing circuitry test - the inter-chip communication functions are tested.

The test vectors are run at a set of frequencies from the nominal 40 MHz up to 90 MHz to ensure sufficient performance margin for radiation damage. The test vectors are also scanned over the digital supply within $\pm5\%$ of the nominal 4.0V. The lower range of the scan is extended to monitor the quality of the probe card contact with the chip pads. The problems with the contact are revealed by non-monotonic dependence of test vector efficiency on the voltage.

7.1.2.3. Power Consumption

We determine the power consumed by the chip by measuring the currents, separately for the digital and analogue parts. We calibrated each test system to within 1% in this measurement. To simulate the conditions of the experiment, the 100 kHz trigger rate is set while a random 3% of channels have hits. The measurement is done separately for the "master" and "slave" modes. Chips with power consumption outside of a 30% margin from the wafer mean value are rejected.

7.1.2.4. Internal DACs

We verify the performance of comparator threshold voltage, input transistor bias current and shaper current DACs by doing a full scan of the respective DAC bits and measuring the voltage values with the test system ADC. The linearity of the DACs is extracted and compared with specifications. The error on each measurement is 1%. It stems from the uncertainty of the resistor values in the amplifiers used to match the signal ranges with the ADC inputs.

7.1.2.5. I/O Signals Tests

We test the properties of ABCD3TA input or output signals by using test vectors, stimulating the calibration signal and varying the test conditions. We test the phases of the input signals relative to the input clock by scanning their delays. Setup and hold time requirements for inputs are verified in this way. We test the phases of the output signals, relative to the input clock, by scanning the delay for the data receiving register latching clock and using the measurements of the signal propagation times in the system. We vary the swing of the input differential signals to measure the minimal working value. We vary the thresholds of the window comparators, placed after differential operational amplifiers, to measure the swing of the output differential signals. Finally,

we vary the duty cycles of the input clocks from 40 to 60% to ascertain the stability of the chip performance against the clock shape variation.

7.1.2.6. Test Specification

The test specification requires that chips pass the digital tests at frequencies of 40 and 50 MHz and simultaneously at digital voltages between 3.8 and 4.2 V. All chip channels must respond to the calibration pulses. We further select on the following criteria:

- channel noise and the average chip noise

- the average chip gain

- the trim DAC linearity

- the average trim DAC ranges for a chip

- channel offset

- Threshold DAC linearity

- bias and shaper current DACs linearity

- the chip power consumption

7.2. Quality assurance

A full quality assurance program has been applied to the ABCD3TA ASICs at the following stages:

- qualifying good dice on wafers as described in the previous section,

- checking for infant mortality in ASICs assembled onto hybrids,

- monitoring radiation resistance on a sampling basis, as these are destructive tests.

7.2.1. Infant mortality

A long duration test was performed for ABCD3TA chips assembled on hybrids. The aim of this test was to catch infant mortality problems in the ASICs. The test was therefore performed at the first stage where it was feasible and practical and where replacing ASICs was still possible. The test consisted of a long duration run at elevated temperature, initially for 90 hours at a temperature of 55 °C, measured on the hybrid.

7.2.2. Radiation hardness quality assurance

With respect to total ionising dose a first step of quality assurance procedure was radiation hardness verification performed at the foundry as part of the acceptance criteria. Ten Mrad (SiO_2) radiation tests were

done on a sampling basis to control radiation hardness stability and to statistically measure the process capability to satisfy radiation sensitive parameter drift tables as given in the DMILL electrical specification document. Each production lot was controlled according to the sampling plan defined by the in-house procedure. After irradiation, in case one parameter exhibited larger drift or greater absolute value than expected, a deeper analysis was performed and, when failure was confirmed, wafers were rejected.

Since some radiation effects are associated with particular circuit configurations, in addition to the foundry tests of the process control monitors, the ABCD3TA chips have been checked for radiation resistance on a sampling basis. From each production lot four chips have been sampled randomly from four different wafers and irradiated with X-rays. After irradiation the chips were tested for digital functionality and power consumption of the digital part.

In order to determine the speed margin of the digital part, the complete digital test procedures were run for a clock frequency of 50 MHz at different values of the power supply voltage. Figure 22 shows the minimum power supply voltage required for correct digital operation at 50 MHz clock frequency for samples irradiated with a dose of 10 Mrad at a high dose rate of 36 krad/min. The measurements were performed immediately after irradiation before any annealing took place. The continuous shaded area at the bottom of the plot shows the minimum power supply voltages for those lots before irradiation. One can see that for a majority of production lots there is a significant safety margin with respect to the nominal power supply voltage of 4 V and clock frequency of 40 MHz. Only two lots that showed an increase of the minimum Vdd above 4.5V after irradiation have been rejected.

High dose rate X-ray irradiation was performed to screen for anomalous increase of the power consumption in the digital part of the chip caused by radiation. The source of this current has been identified as a leakage current between neighbouring NMOS devices. Detailed study of the nature of this leakage current showed that (i) this current does not influence at all the functionality and the speed of the digital circuitry and (ii) it anneals with a relatively short time constant of about 30 days at a temperature of 25 °C. Based on the study of long term annealing, a maximum excess current allowed after high dose rate X-ray irradiation has been set at 120 mA.

In a first step a sample chip per lot was irradiated at the vendor facility with a dose of 10 Mrad in 3 hours and power consumption of the chip measured. If the result complied with the limit, the production lot was accepted. If the result exceeded the limit, additional irradiation was done and if the high current was confirmed the whole lot was rejected. This was performed by the vendor on all lots prior to being shipped and was in addition to the

normal irradiation of process control structures that the vendor was performing on each lot to certify the lot as radiation-hard.

In the second step, the power consumption was monitored in the chips that were sampled and irradiated for monitoring radiation resistance with respect to digital functionality. Figure 23 shows the excess currents measured immediately after X-ray irradiation with a dose of 10 Mrad for the same samples as shown in Fig. 22. No lot has been rejected due to the post radiation excess digital current.

To screen for unexpected process changes that would influence the radiation hardness with respect to bulk damage, three chips from each lot were irradiated with neutrons in a reactor to a fluence of 2×10^{14} n/cm^2 of 1 MeV equivalent neutrons. Irradiations were done with chips mounted on hybrids. Full functionality of chips was tested before and after irradiation with a focus on performance of the analogue part.

8. Summary

The ABCD3TA ASIC developed for binary readout of silicon strip detectors meets the requirements of the ATLAS Semiconductor Tracker. The performance of the chip has been demonstrated through extensive evaluation of the prototypes as well as in the series production of the SCT detector modules.

For a fully populated module built with silicon strip detectors of a total length of 12.8 cm, an ENC below 1500 electrons rms and a noise occupancy below 1×10^{-4} are systematically achieved. After irradiation up to full SCT doses, an ENC below 1800 electrons rms and a noise occupancy below 5×10^{-4} are maintained.

The required threshold uniformity in the amplitude discriminator has been achieved by implementing threshold trimming on a channel basis. The equivalent input threshold spread is lower by a factor of 5 compared to the ENC and it does not contribute significantly to the noise occupancy and efficiency loss.

The chip design meets the timing requirements achieving discriminator timewalk below 16 ns, which ensures correct associations of all hits above a threshold of 1 fC with the corresponding beam crossing number.

The ABCD3TA chip design provides data storage for the first level trigger latency, data derandomising and zero suppression so that only addresses of hit strips are transmitted to the off detector electronics. As a result the module comprising 1536 readout channels is read out via two optical links at 40 MHz rate. The readout control logic is built into the ABCD3TA architecture so that no additional control chip is required on the module.

The ABCD3TA design has been optimised for low power consumption. The chip operating at the nominal bias conditions and the nominal clock frequency of 40 MHz typically dissipates a power of 3.1 mW/channel. This number complies with the requirements of the SCT power supply and cooling systems.

The radiation resistance of the ABCD3TA design has been verified in numerous dedicated irradiation tests specific for ionisation effects, displacement damage and Single Event Effects. Moreover, the radiation resistance has been monitored on a sampling basis through the entire production. The results of the irradiation tests and radiation hardness quality assurance program ensure that the chips will maintain required performance during the lifetime of the ATLAS experiment.

The production and acceptance testing of 270,000 chips has been completed yielding a sufficient number of chips to build the Semiconductor Tracker for the ATLAS experiment.

Acknowledgements

References

[1]   ATLAS Inner Detector Technical Design Report, Vol. 2. pp. 427-439, CERN/LHCC/97-17, ATLAS TDR 5, 30 April, 1997.

[2]   T. Dubbs, et al., The development of the CAFE-P/CAFE-M bipolar chips for the ATLAS Semiconductor Tracker, Proceedings of the Fifth Workshop on Electronics for LHC Experiments (CERN 99-09 – CERN/LHCC/99-33), CERN, 1999, pp. 123-7.

[3]   D. Campbell, et al., The development of a rad-hard CMOS chip for the binary readout of the ATLAS Semiconductor Tracker, Proceedings of the Fifth Workshop on Electronics for LHC Experiments (CERN 99-09 – CERN/LHCC/99-33), CERN, 1999, pp. 152-6.

[4]   DMILL, a Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics, RD29 Status Report, CERN/LHCC/97-15, CERN, 1997.

[5]   W. Dabrowski, J. Kaplon, R. Szczygiel, Nucl. Instr. and Meth. A 421 (1999), 303.

[6]   W. Dabrowski, et al., Progress in Development of the Readout chip for ATLAS Semiconductor Tracker, Proceedings of the Sixth Workshop on Electronics for LHC Experiment, (CERN 2000-010 - CERN/LHCC/2000-041) CERN, 2000, pp. 115-9.

[7]   W. Dabrowski, et al., IEEE Trans. Nucl. Sci., NS-47 (2000) 1843.

[8]   D. Robinson, et al., Nucl. Instr. and Meth. A 485 (2002) 84.

[9]   F. Anghinolfi et al.., Development of Front-End Electronics for Silicon Strip Detectors Using the DMILL BiCMOS Rad-Hard Process, Proceedings of the Second Workshop on Electronics for LHC Experiments (CERN/LHCC/96-39), CERN, 1996, pp. 483-7.

[10]   T. Kondo, et al., Nucl. Instr. and Meth. A 485 (2002), 27.

[11]   M. Glaser, et al., Nucl. Instr. and Meth. A 426 (1999) 72.

[12]   M. Ravnik, R. Jeraj, Nucl. Sci. Eng. 145 (2003) 145.

[13]   G. Lindström, et al., Nucl. Instr. and Meth. A 466 (2001) 308.

[14]   Y. Unno, et al., IEEE Trans. Nucl. Sci., NS-49 (2002) 1868.

[15]   E. Krištof, Proceedings of the conference Nuclear Energy in Central Europe '98, Terme Čatež, Slovenia, 1998, pp. 43-8.

[16]   D. Žontar, et al., Nucl. Instr. and Meth. A 426 (1999) 51.

[17]   A.M. Ougang, et al., IEEE Trans. Nucl. Sci., NS-37 (1990) 2219.

[18]   I. Mandić et al., IEEE Trans. Nucl. Sci. NS-51 (2004) 1752.

[19]   P.S. Winokur, et al., IEEE Trans. Nucl. Sci., NS-41 (1994) 538.

[20]   E.W. Enlow, et al., IEEE Trans. Nucl. Sci., NS-38 (1991) 1991.

[21]   R.D. Schrimpf, IEEE Trans. Nucl. Sci., NS-43 (1996) 787.

[22]   S.C. Witczak, et al., IEEE Trans. Nucl. Sci., NS-43 (1996) 3151.

[23]   O. Flament, et al., IEEE Trans. Nucl. Sci., NS-45 (1998) 1420.

[24]   S.C. Witczak, et al., IEEE Trans. Nucl. Sci., NS-44 (1997) 1989.

[25]   M. Ullán, et al., IEEE Trans. on Nucl. Sci., NS-49 (2002) 1106.

[26]   Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources, Annual Book Of ASTM Standards, American Society For Testing And Materials (ASTM), E 1249–93, 1993.

[27]   Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices, Annual Book Of ASTM Standards, American Society For Testing And Materials (ASTM), F 1892–98, 1998.

[28]   Application of Thermoluminiscence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices, Annual Book Of ASTM Standards, American Society For Testing And Materials (ASTM), E668–97, 1997.

[29]   M. Huhtinen, F. Faccio, Nucl. Instr. and Meth. A 450 (2000) 155.

[30]   L. Eklund, et al, Nucl. Instr. and Meth. A 515 (2003) 415.

[31]   F. Anghinolfi, et al., IEEE Trans. on Nucl. Sci., NS-49 (2002) 1080.
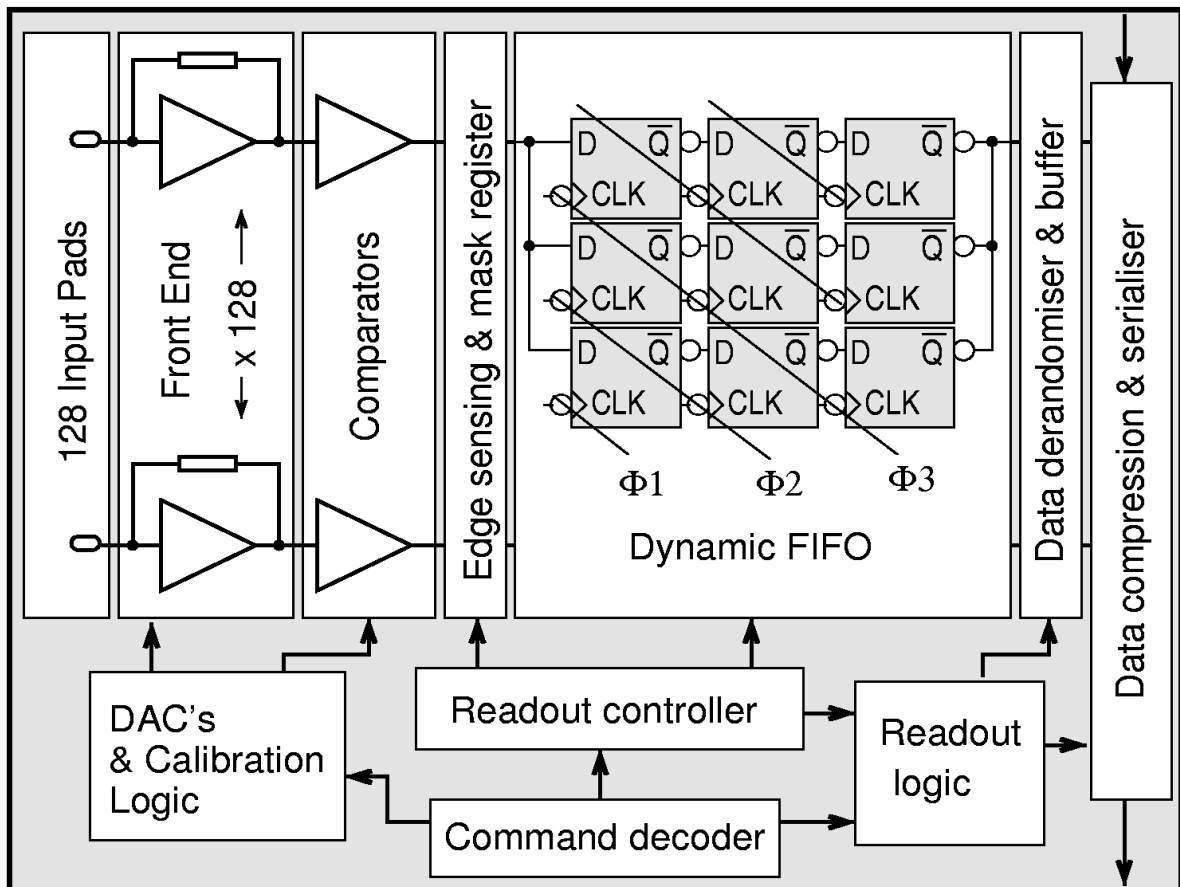
Figure captions

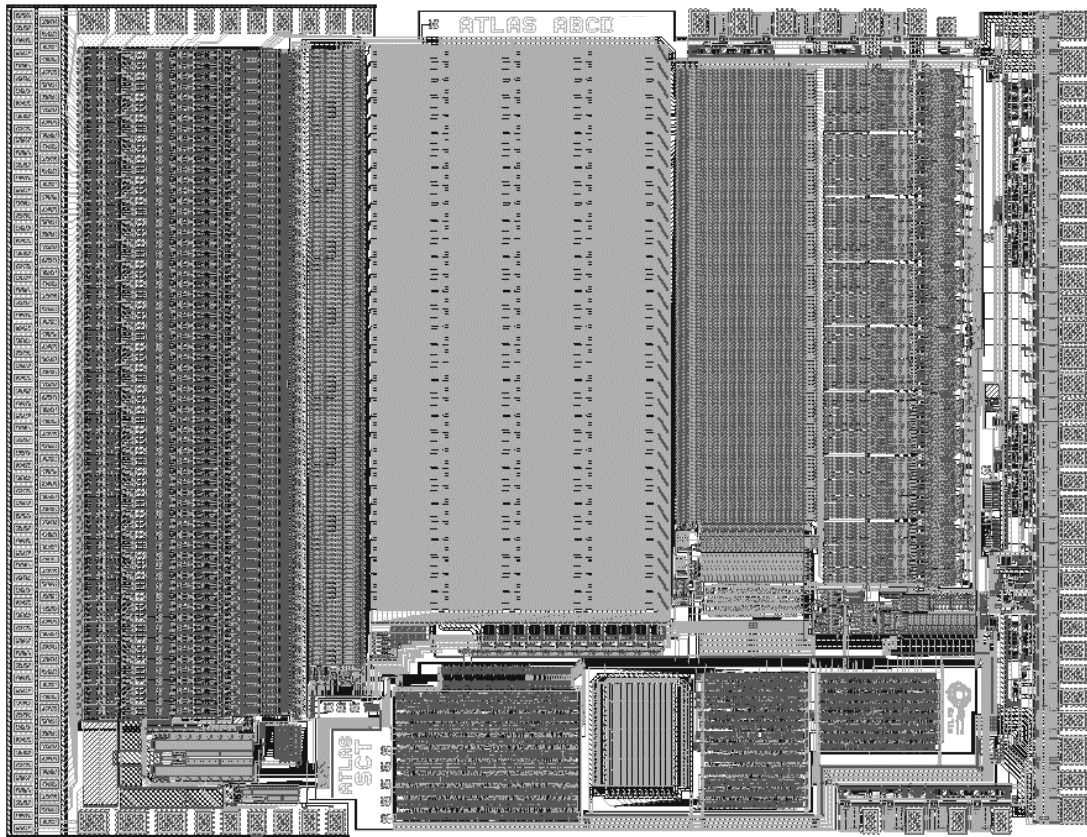Fig. 1. Block diagram of the ABCD3TA chip.
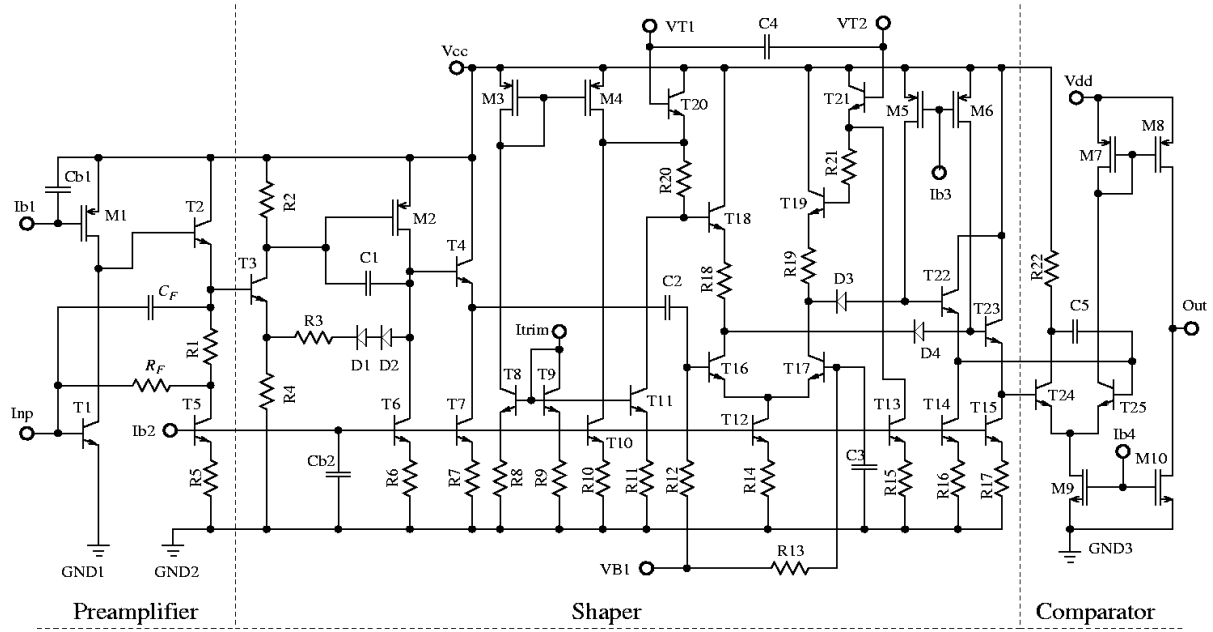
Fig. 2. Layout drawing of the ABCD3TA chip.

Fig. 3. Schematic diagram of the front-end circuitry implemented in the ABCD3TA chip.
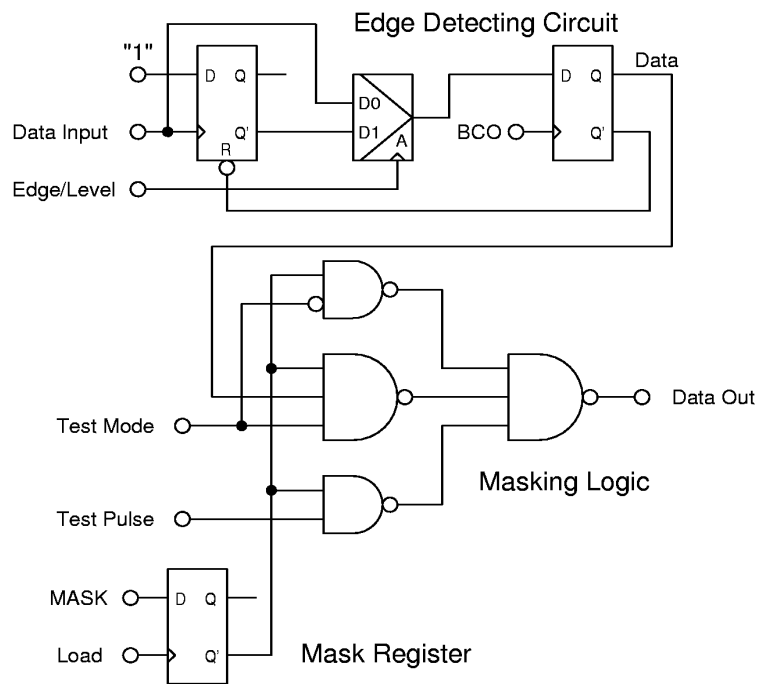
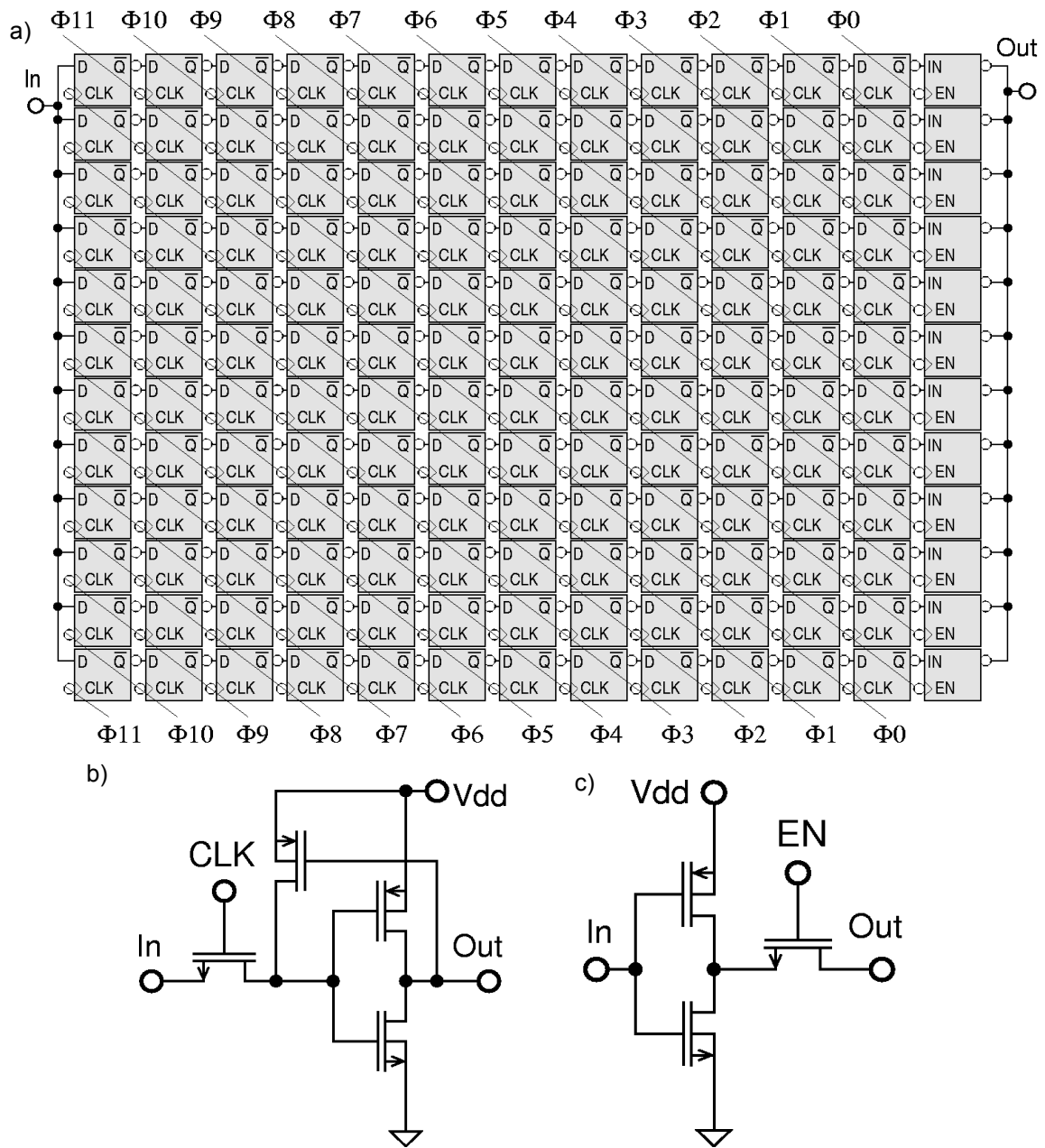Fig. 4. Schematic diagram of the input register.

Fig. 5. (a) array of 12 × 12 memory cells, (b) structure of the storage cell, (c) structure of the output demultiplexing cell.
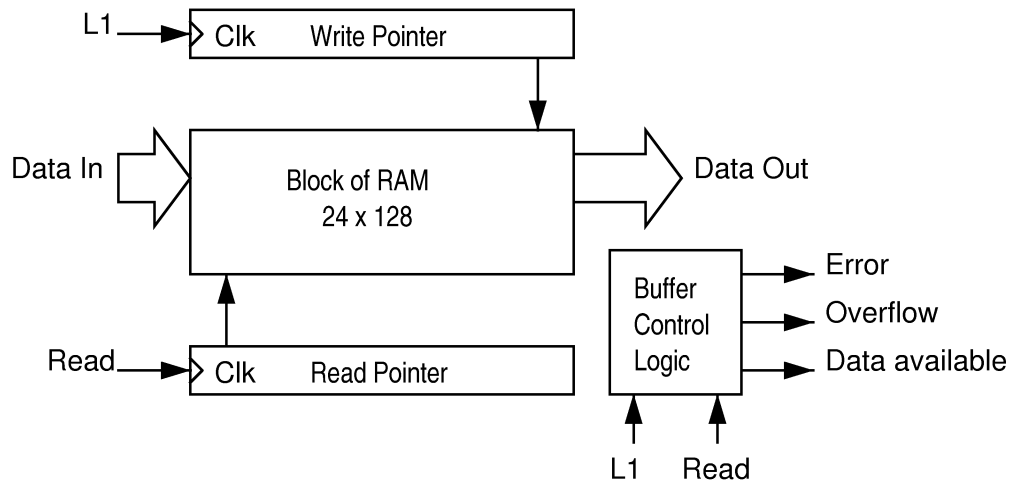
Fig. 6. Block diagram of the readout buffer.

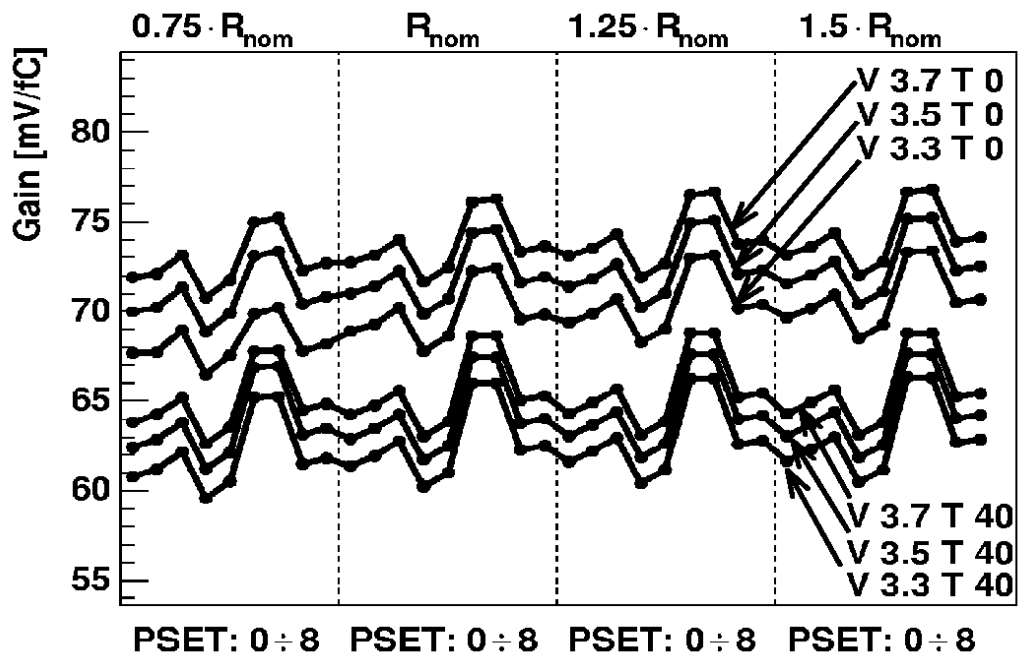Fig. 7. Interconnection of ABCD3TA chips on a 12-chip detector module.

Fig. 8. Simulation of pulse gain of the full analogue chain as a function of process parameter variations (resistors from -25% to +50% (RSET from -1 to 2), CMOS corner parameters (PSET from 0 to 8), temperature 0 and 40°C, power supply ±200mV).
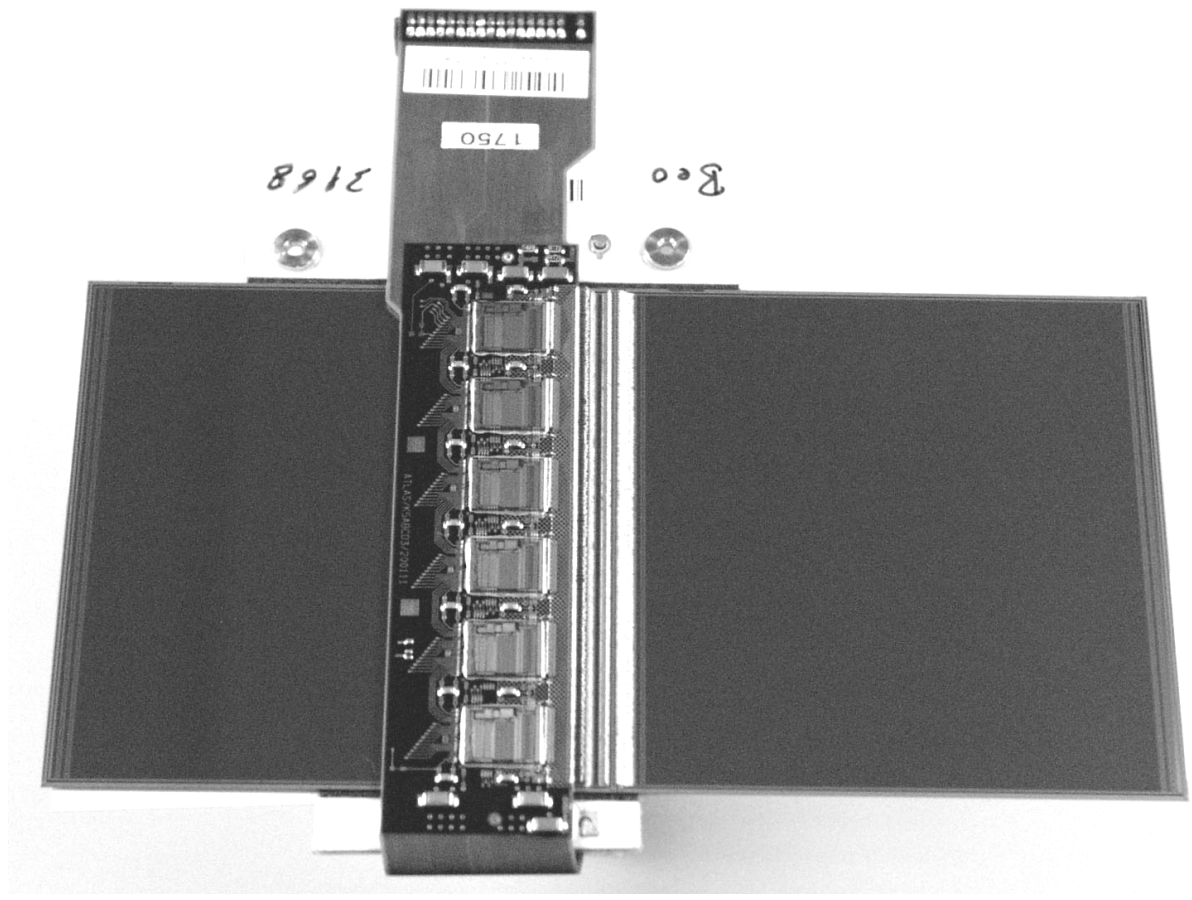
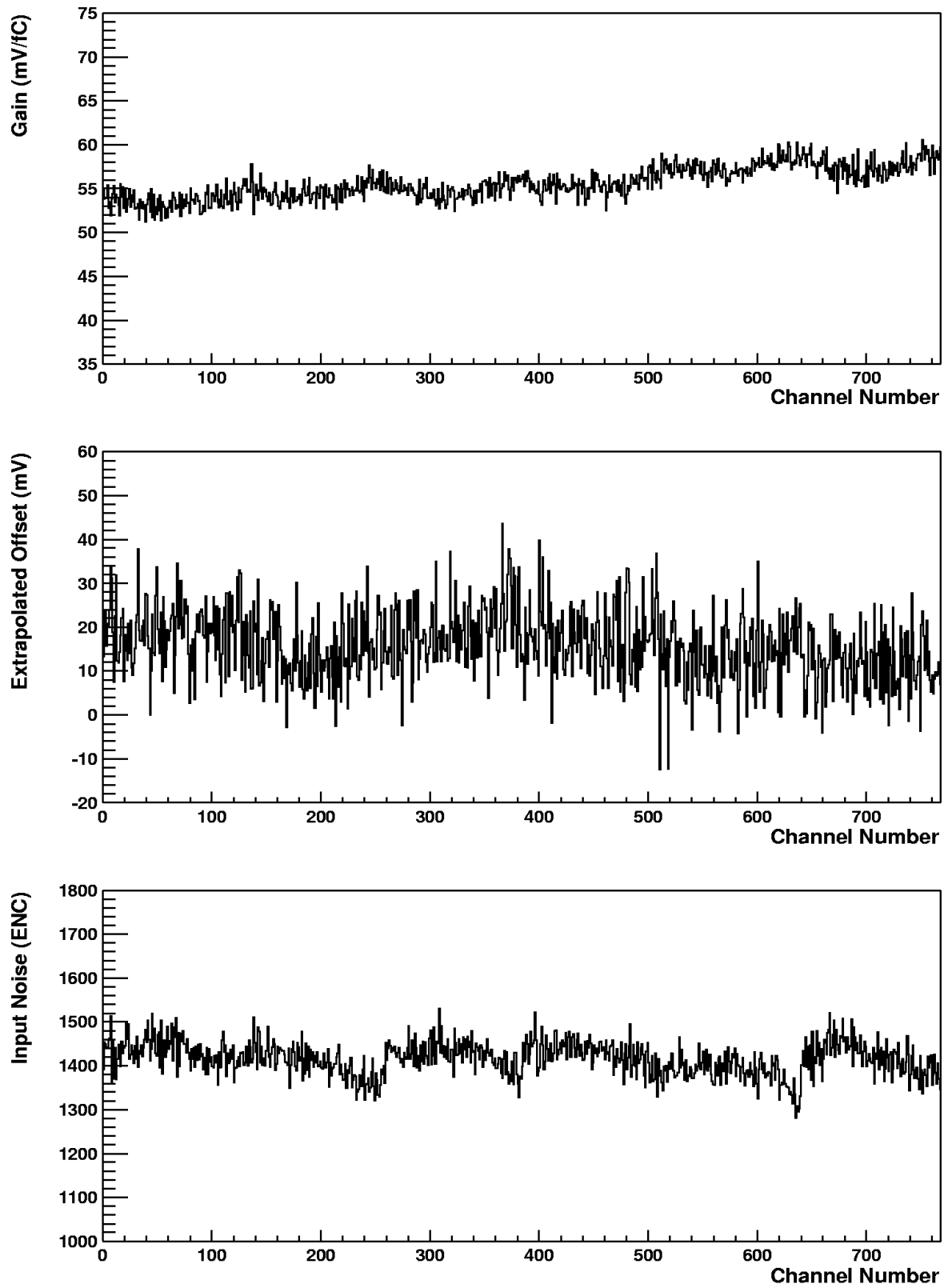Fig. 9. Barrel module. Six ABCD3TA chips on one side of the module are visible.

Fig. 10. Distributions of gain, offset and noise for 6 chips (762 channels).
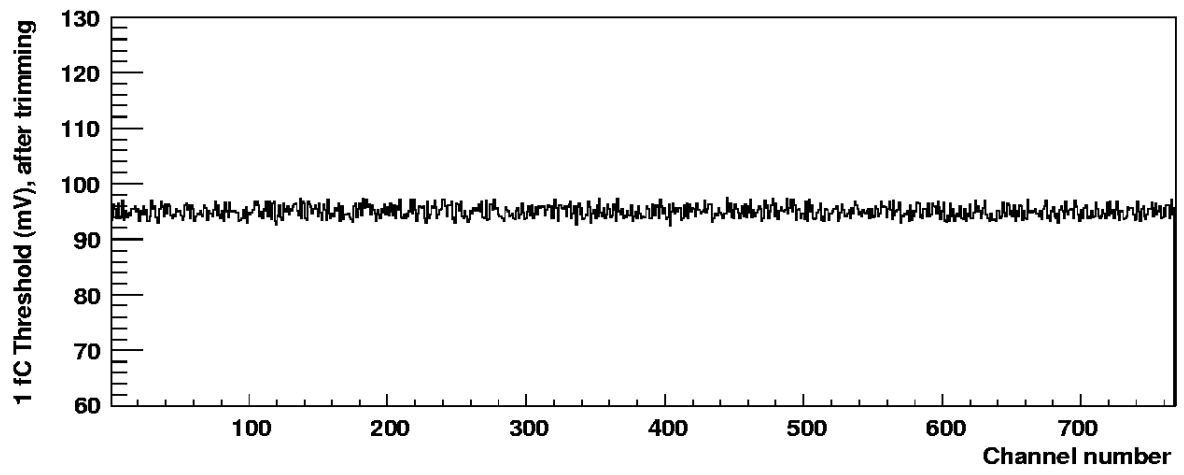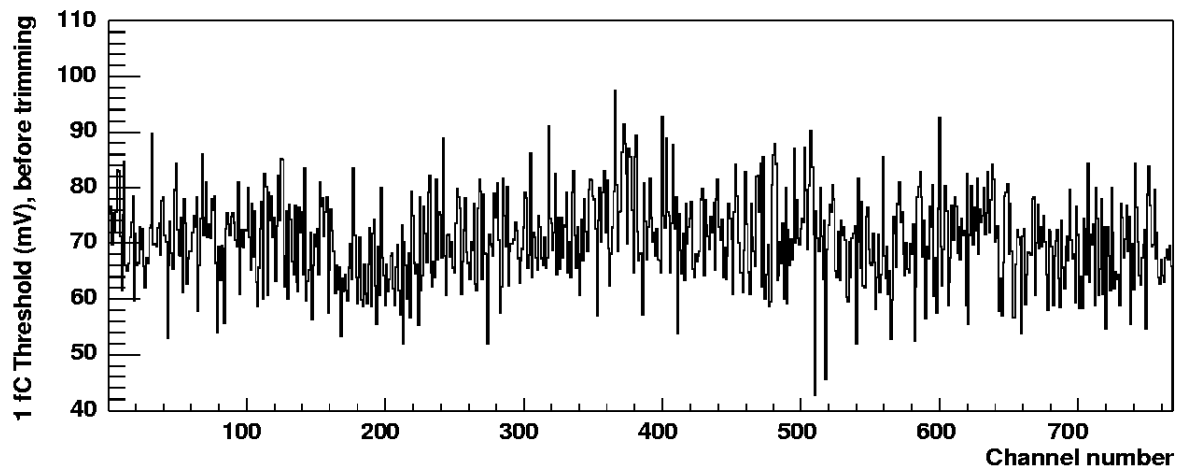
Fig. 11. 1 fC threshold spread for 6 chips on one side of the module before and after trimming.
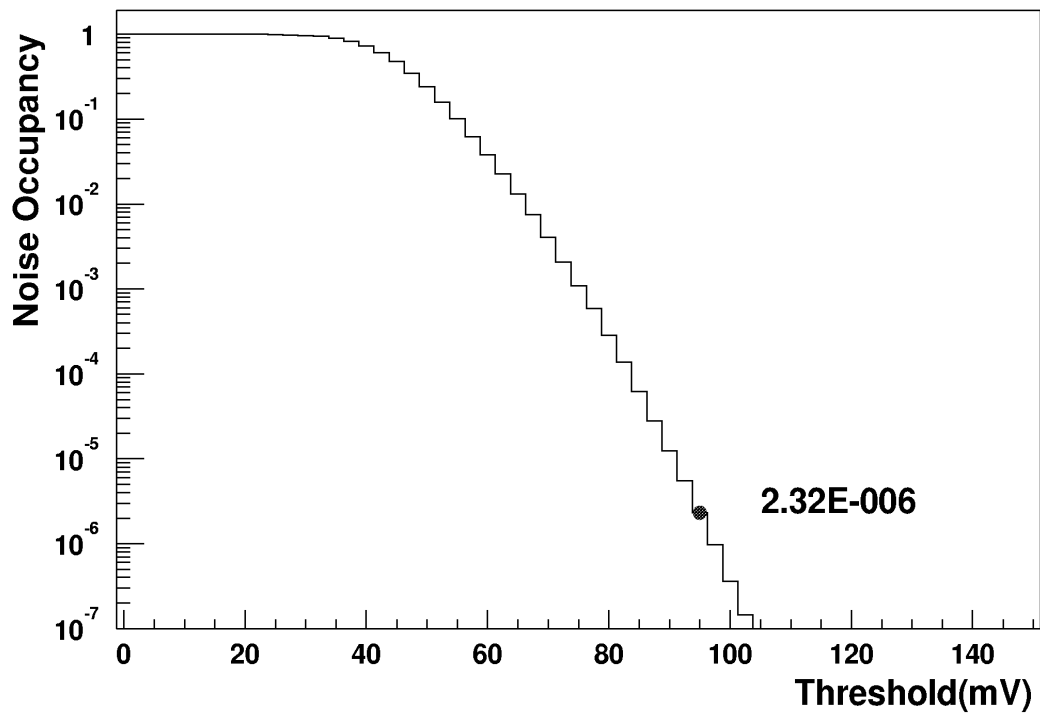
Fig. 12. Measured mean noise occupancy for all channels of a module. At 1 fC threshold the noise occupancy is 2.32×10^{-6}.
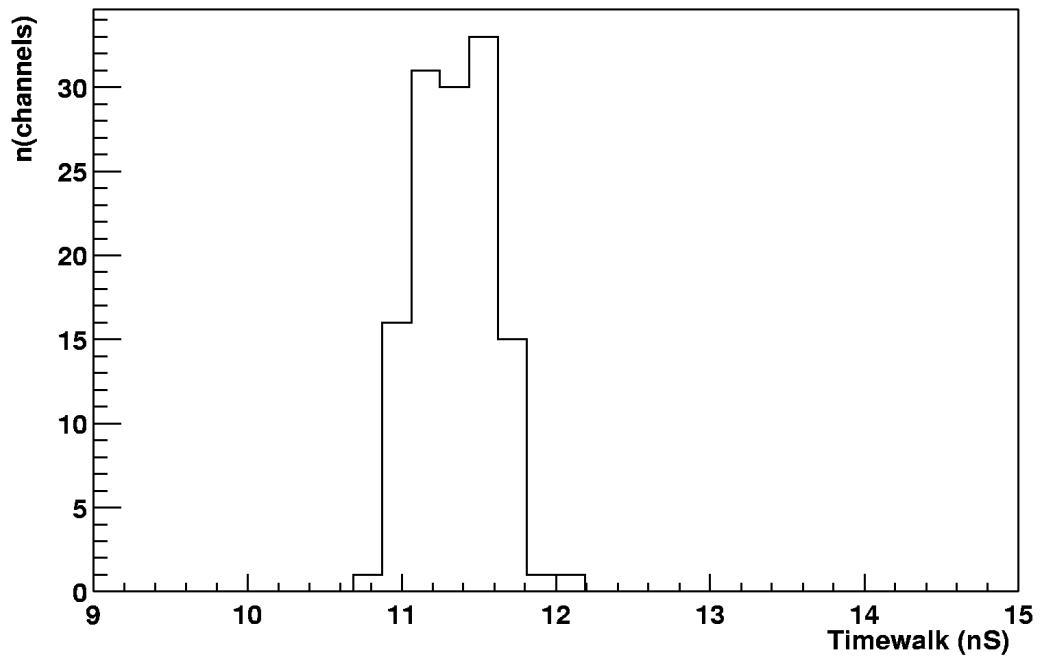
Fig. 13. Timewalk measurements for 128 channels in one chip on a barrel module.

Fig. 14. Evolution of noise with fluence of 24 GeV protons for six chips irradiated on a hybrid. Noise is expressed in the number of electrons of ENC.

Fig. 15. Evolution of the rms value of threshold spread at 1 fC input charge with proton fluence. No threshold trimming was performed for these measurements.

Fig. 16. Evolution of noise with 1 MeV equivalent fluence of reactor neutrons for 6 chips irradiated on a hybrid. Noise is expressed in the number of electrons of ENC.

Fig. 17. Noise as a function of the current in the input transistor before and after X-ray irradiation.

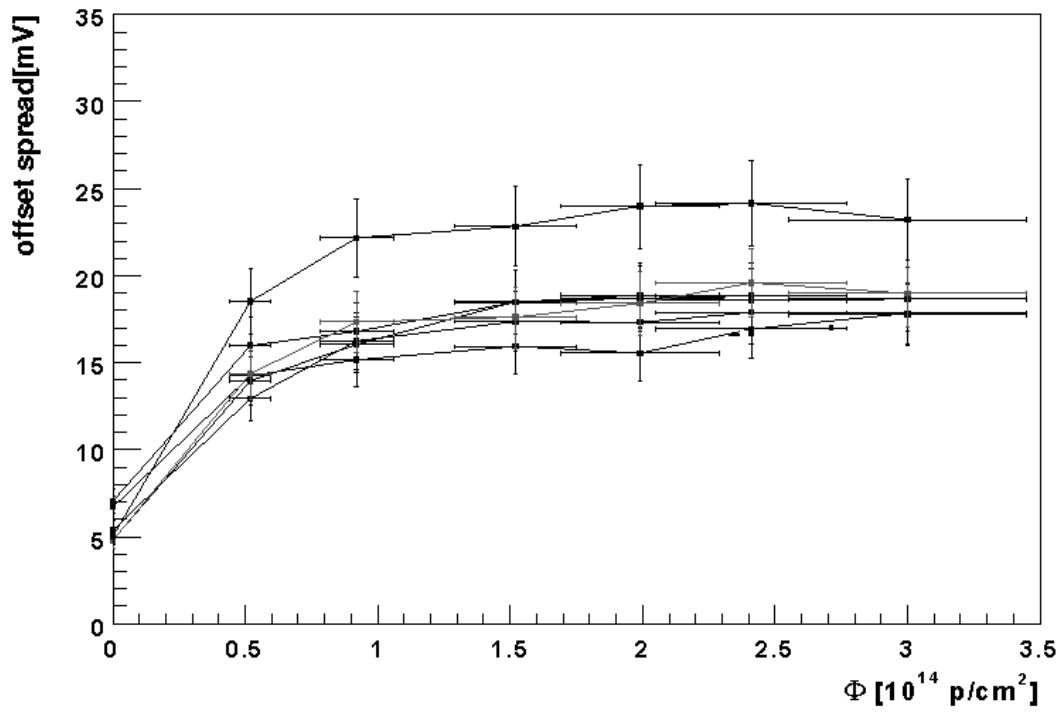Fig. 18. Mapping of the common emitter current gain change for DMILL transistors irradiated at different dose rates up to 10 Mrad total dose.

Fig. 19. Maximum speed at supply voltage of 4 V (a) and minimum supply voltage at 40 MHz (b) as a function of total ionising dose.

Fig. 20. ABCD3TA production flow.

Fig. 21. The architecture of the ASIC wafer test system. All hardware parts of the system and their communication are shown.

Fig. 22. Minimum power supply voltage for correct digital operation at 50 MHz clock frequency for samples irradiated with a dose of 10 Mrad. Minimum power supply voltage before the irradiation is shown as continuous grey area.

Fig. 23. Excess current measured after 10MRad X-ray irradiation for ABCD3TA chips from selected wafers of consecutive production lots. Data is presented without annealing.

Fig. 1. Block diagram of the ABCD3TA chip.

Fig. 2. Layout drawing of the ABCD3TA chip.

Fig. 3. Schematic diagram of the front-end circuitry implemented in the ABCD3TA chip.

Fig. 4. Schematic diagram of the input register.

Fig. 5. (a) array of 12 × 12 memory cells, (b) structure of the storage cell, (c) structure of the output demultiplexing cell.

Fig. 6. Block diagram of the readout buffer.

Fig. 7. Interconnection of ABCD3TA chips on a 12-chip detector module.

Fig. 8. Simulation of pulse gain of the full analogue chain as a function of process parameter variations (resistors from -25% to +50% (RSET from -1 to 2), CMOS corner parameters (PSET from 0 to 8), temperature 0 and 40°C, power supply ±200mV).

Fig. 9. Barrel module. Six ABCD3TA chips on one side of the module are visible.

Fig. 10. Distributions of gain, offset and noise for 6 chips (762 channels).

Fig. 11. 1 fC threshold spread for 6 chips on one side of the module before and after trimming.

Fig. 12. Measured mean noise occupancy for all channels of a module. At 1 fC threshold the noise occupancy is 2.32×10^{-6}.

Fig. 13. Timewalk measurements for 128 channels in one chip on a barrel module.

Fig. 14. Evolution of noise with fluence of 24 GeV protons for six chips irradiated on a hybrid. Noise is expressed in the number of electrons of ENC.

Fig. 15. Evolution of the rms value of threshold spread at 1 fC input charge with proton fluence. No threshold trimming was performed for these measurements.

Fig. 16. Evolution of noise with 1 MeV equivalent fluence of reactor neutrons for 6 chips irradiated on a hybrid. Noise is expressed in the number of electrons of ENC.

Fig. 17. Noise as a function of the current in the input transistor before and after X-ray irradiation.

Fig. 18. Mapping of the common emitter current gain change for DMILL transistors irradiated at different dose rates up to 10 Mrad total dose.

Fig. 19. Maximum speed at supply voltage of 4 V (a) and minimum supply voltage at 40 MHz (b) as a function of total ionising dose.
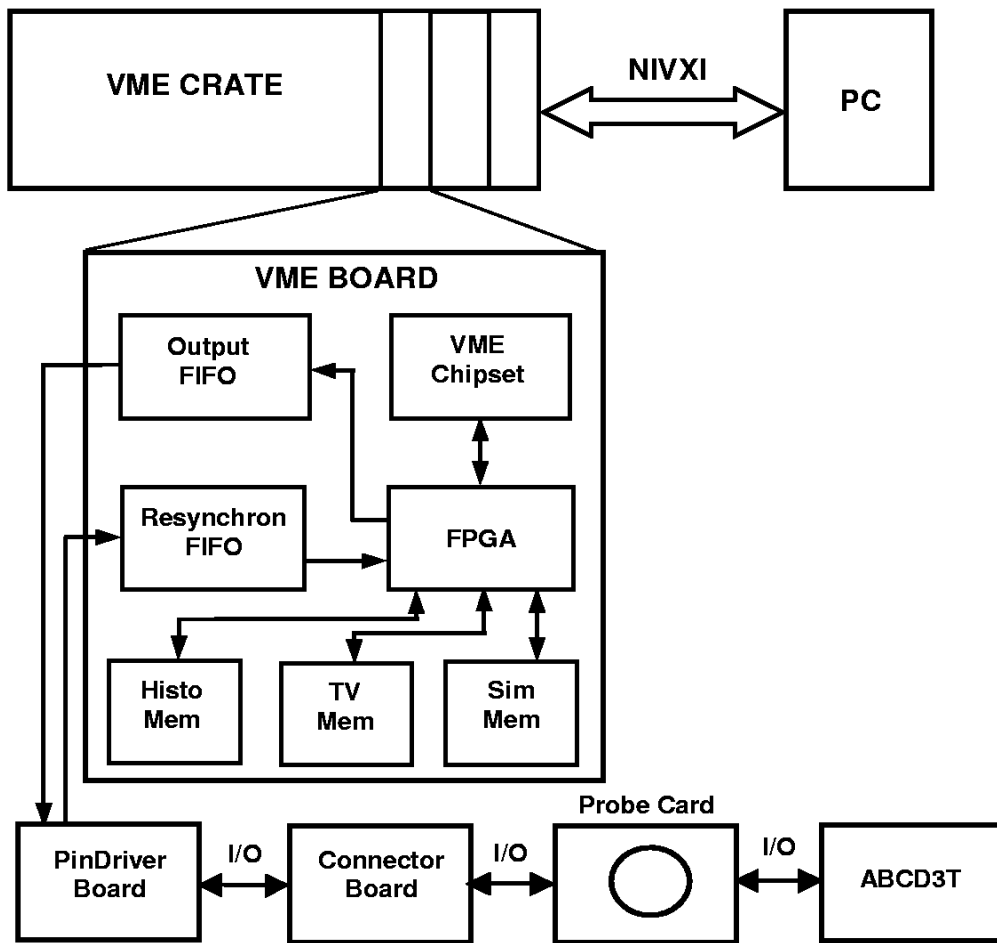
Fig. 20. ABCD3TA production flow.

Fig. 21. The architecture of the ASIC wafer test system. All hardware parts of the system and their communication are shown.
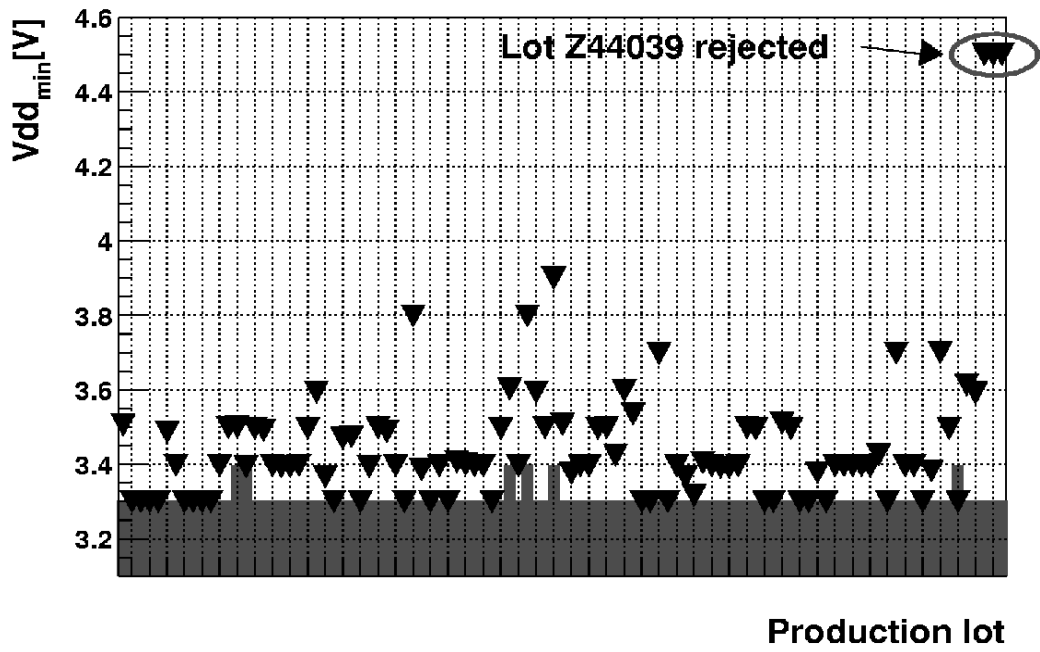
Fig. 22. Minimum power supply voltage for correct digital operation at 50 MHz clock frequency for samples irradiated with a dose of 10 Mrad. Minimum power supply voltage before the irradiation is shown as continuous grey area.
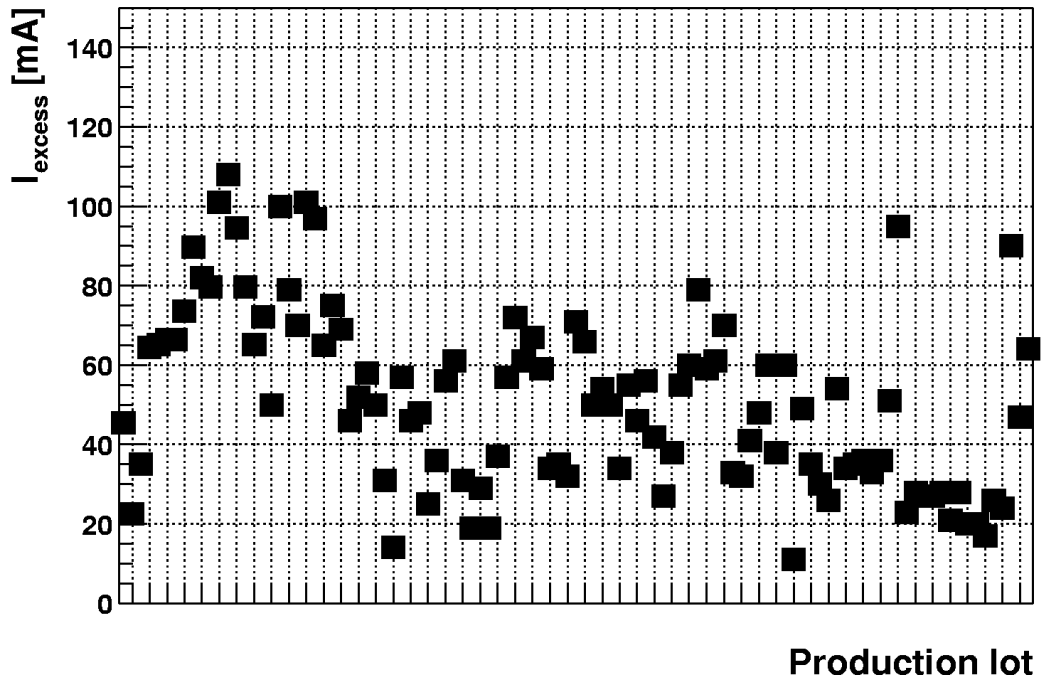
Fig. 23. Excess current measured after 10MRad X-ray irradiation for ABCD3TA chips from selected wafers of consecutive production lots. Data is presented without annealing.

Table 1: Assumed detector electrical parameters.

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbour strips	1.03 pF/cm	1.40 pF/cm
Capacitance of strip to backplane	0.30 pF/cm	0.30 pF/cm
Metal strip resistance	15 Ω/cm	15 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise	2.0 nA	2.0 μA
Charge collection time	< 10 ns	< 10 ns

Table 2: Trim DAC range selection

TrimDAC range	TrimDAC step	Relative threshold spread for the nominal threshold setting of 50 mV (1 fC) (1 sigma)
0 mV - 60 mV	4 mV	2.3%
0mV -120 mV	8 mV	4.6%
0mV -180 mV	12 mV	6.9%
0mV -240 mV	16 mV	9.2%

Table 3: Data Compression Criteria.

Name of Selection Criteria	Hit Pattern	Usage
Hit	1XX or X1X or XX1	Detector alignment
Level	X1X	Normal Data Taking
Edge	01X	Normal Data Taking
Test	XXX	Test Mode

Table 4: Dose rates and total dose samples taken in the different irradiation of mapping experiment.

Exp #	Dose rate [rad/s]	Total dose [Mrad]								
1	112	1	3	5	7	10				
2	112	0.5	1							
3	1.24	1	1.4	2.2	2.4	3.2	5.2	6.2	6.8	7.8
4	0.05	0.06	0.10	0.16	0.25	0.35	0.50	0.67	0.81	0.90	1.0

Table 5: SEE sensitivity and corresponding cross-section measured at PS and PSI facilities. The sensitivity is given in units of fluence of particles traversing the device which will cause one bit flip in one cell. Errors are statistical only.

	PS (24 GeV/c protons)		PSI (200 MeV/c pions)	
	SEE sensitivity [(p/cm^2)/flip]	SEE cross-section [cm^2/bit]	SEE sensitivity [(π/cm^2)/flip]	SEE cross-section [cm^2/bit]
Pipeline cell	$(1.2 \pm 0.3) \times 10^{12}$	$(8.3 \pm 2.0) \times 10^{-13}$	$(3.1 \pm 0.4) \times 10^{12}$	$(3.2 \pm 0.4) \times 10^{-13}$
Mask register cell	$(7.0 \pm 6.0) \times 10^{13}$	$(1.4 \pm 1.2) \times 10^{-14}$	$(4.7 \pm 1.7) \times 10^{13}$	$(2.1 \pm 0.7) \times 10^{-14}$