A Hybrid Test Compression Technique For Efficient Testing Of Systems-On-A-Chip

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Summary

One of the major challenges in testing a System-on-a-Chip (SOC) is dealing with the large test data size. To reduce the volume of test data, several efficient test data compression techniques have been recently proposed. In this paper, we propose hybrid test compression techniques that combine the Geometric-Primitives-Based compression technique with the frequency-directed run-length (FDR) and extended frequency-directed run-length (EFDR) coding techniques. Based on experimental results, we demonstrate the effectiveness of the proposed hybrid compression techniques in increasing the test data compression ratios over those obtained by the Geometric-Primitives-Based compression technique.