Topology of 2 input subnanowatt XOR gate in 65nm CMOS technology

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Abstract- **Exclusive OR (XOR) gate is highly utilized in various digital system applications such as full adder, comparator, parity generator and encryption processor, which leads to increased in the interests to enhance the performance of XOR gate. A novel design of low power and high performance XOR gate using six transistors application are proposed in this paper. The new XOR gate has been compared with previous design in term of power, delay and power-delay product (PDP). The XOR gate is simulated using Cadence Spectre with 65nm Complementary Metal Oxide Semiconductor (CMOS) technology at different supply voltages with a range of 0.6V to 1.2V. The area of the core circuit is approximately 48 μm2. The critical path propagation delay is 1.585 ns with power dissipation of only around 3.256 fW at 0.8V supply voltage .The results demonstrate that the proposed design achieve a lowest power consumption and high speed with respect to other designs.**

Keywords-XOR gate, low power, VLSI

I. INTRODUCTION

With the growth of integrated circuit towards very high integration density and high operating frequencies, it is crucial to design a logic circuit that can contribute a low power and high speed to overall system. Low power design has become major design forethought with the enormous growth of portable applications. Various low power techniques have been explored and one of it is improving the circuit level including enhancing the basic gate such as XOR gate which influence the overall power system. Optimization of XOR circuit design to achieve low power, small size and delay is needed due to the important role played by XOR gate in various circuits especially in arithmetic circuits such as full adder, parity generator and cryptography circuits. As XOR gate is use in a critical path in most of the system, it significantly affects the overall performance of larger and complex circuits.

Over the years, various 2-input XOR gate designs have been reported to enhance the performance for various applications [3-15]. By designing XOR gate, consideration must be made in power consumption and delay in the critical path and full output voltage swing with low number of transistors to implement it. One of the useful methods to reduce power consumption is by voltage scaling. In the other hand, reducing the voltage will reduce the speed. Another effective method is by avoiding non-full swing nodes connected to the gate of the other transistors especially to the input of inverters.

In this paper, we present a novel low-power design for 2-input XOR gate using six transistors implemented using 65nm CMOS technology. The paper is organised as follows: in Section II, previous work is reviewed. Subsequently, in section III, the proposed design of XOR gate is presented. In section IV, the simulation results are given and discussed. The comparison and evaluation for proposed and existing designs are carried out. Finally a conclusion will be made in the last section.

II. PREVOIUS WORK

Traditional XOR gate design based on eight transistors static CMOS can operate with full output voltage swing with the drawback of acquires large amount of transistors [1]. XOR gate based on transmission gate [2] is used to overcome the signal degradation cause by the PMOS and NMOS. It offer a better quality but with the drawback of loss of driving capability and need complementary signal value to control gates of PMOS and NMOS which require more transistors and area. Cross-coupled (CC) XOR gate based on the pass transistor logic have been reported in [3] claims to have better speed and power consumption and works well under a lower supply voltage than six transistors XOR gate.

The XOR gate realization of the circuit using six transistors can be found in [4] after modifying their four by transistors XOR gate design cascading a standard inverter as a driving output. This design has improved the poor signal output for a certain input signal by using this topology. Powerless XOR gate (P-XOR) in [5] is proposed using the set of four transistors circuit with no power supply connection consumes less power than other design but with a large delay. Other four transistors XOR design was reported in [6] based on Gate-Diffusion-Input (GDI) cell. XOR gate with three transistors can be found in [7] using CMOS inverter and PMOS pass transistor. It provide less power-delay product but have a voltage degradation when the input A=1 and B=0. Elgamel et al. [8] also proposed three transistors XOR gate but consumes high power when A=1 and B=0 which produce poor logic '1'.

III. PROPOSED NEW XOR GATE TOPOLOGY

We previously reported in [15] an XOR gate using six transistors which provides full output swing for all input combinations and enables low voltage operation with small propagation delay. Here we propose a further low-power constrained novel 2-input XOR gate using six transistors including inverter. The proposed XOR circuit is based on the concept of pass transistor logic and inverter for complementary input. Pass transistor design enables small transistor count along with smaller input loads (with signal input to source/drain instead of gate) offering very low-power operation with high-performance. Since a nMOS device passes a strong '0', but a weak '1' while a pMOS device passes a strong '1', but a weak '0', the complementary pass transistors are organized to pass a strong output logic level for all input combinations of '1' and '0'.

Fig. 1 shows the circuit schematic of the proposed XOR circuit. It performs a perfect full swing operation for every input pattern. The output Y generates '0' corresponding to $A=B=0$. For this condition, transistor M1, M2 and M4 are ON, but the transistor M4 will pass a strong '0' to the output Y. When $A=0$, $B=1$, transistor M2, M3 and M4 are ON and a '1' is generated at the output Y with transistor M2 passing the strong '1'. For $A=1$, $B=0$, only the device M1 is ON and a strong '1' is passed to the output Y. With $A=B=1$, only transistor M3 is ON and a strong '0' is passed to the output. The transistor sizes are carefully chosen for optimal power-delay performance under various operating conditions. This pass transistor XOR thus does not suffer from signal level deteriorations like other pass-transistor XOR gates.
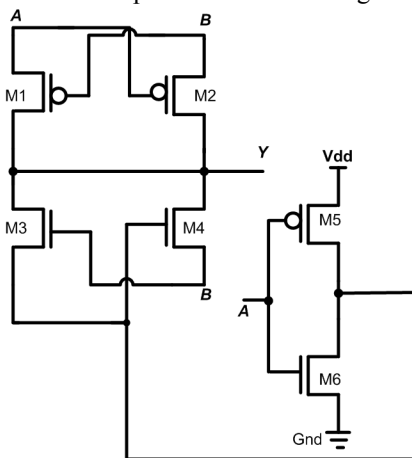

Fig. 1. Circuit diagram of the proposed XOR circuit for low-power application.

IV. RESULT AND ANALYSES

The complete circuit simulation, optimization, layout and parasitic extraction were carried out using Cadence tools. The mask layout of the XOR gate illustrated in Fig. 2 was customized (with manual *placement* and *routing*) in 65nm IBM CMOS. Minimum channel length is used for all the devices and optimum channel width is carefully chosen for each device to achieve verified functionality with low power

dissipation and smallest possible propagation delay. The silicon-area of the XOR gate is approximately 48 μm^2 using the 65nm CMOS process.

Comparative studies and extensive simulation on the proposed XOR gate and five existed XOR gates found in literature have been realized using 65nm IBM CMOS technology in order to analyze the performance comparison with the proposed XOR gate. Fig. 3 displays the functional full-swing operations of the chip for several computation cycles verified by Cadence Spectre. The simulations were carried out using the same testing condition on Cadence Spectre platform to measure the propagation delay and the power dissipation in each case. All the simulation were carried out using the same 65nm IBM CMOS technology with a 0.6V to 1.2V supply voltage range, a load capacitance of 50fF, and, a throughput (clocking) rate of 500MHz. Propagation delay is evaluated from 50% of voltage level of input to 50% of voltage level of output. Power delay product (PDP) is calculated from production of worst case delay and average power consumption. In order to have closer analysis, several input pattern have been applied to cover all the input cases and simulation results verified the correct functionality for every input combination with a supply voltage of 0.8V. Table 1 summarizes the measured performance of the proposed XOR gate and provides a comparison of the circuit with recently reported designs.

From the simulation results, it is clear that the proposed new XOR gate has the lowest propagation delay as well as the lowest power consumption. The improvement attained by the proposed circuit is clearly evident when compared to these other XOR gate circuits. The worst circuit in term of speed is six transistor XOR gate in [4]. It has the highest propagation delay against voltage scaling. Power consumption increased as the supply voltage is increased. The proposed XOR circuit design worked successfully in low voltage supply of 0.8V with 3.256 fW which is the lowest power dissipation when compared to the six transistors in [4] and [15].
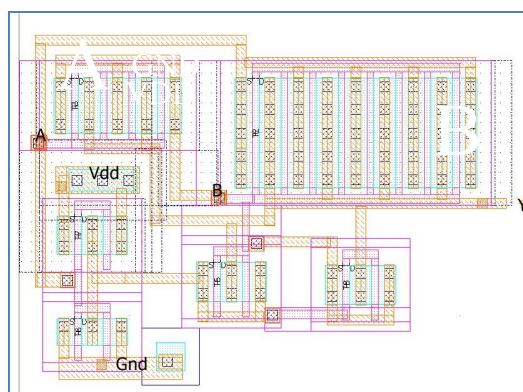

Fig. 2. Layout of the 2-input XOR gate.

TABLE I
SIMULATION RESULTS OF XOR GATE

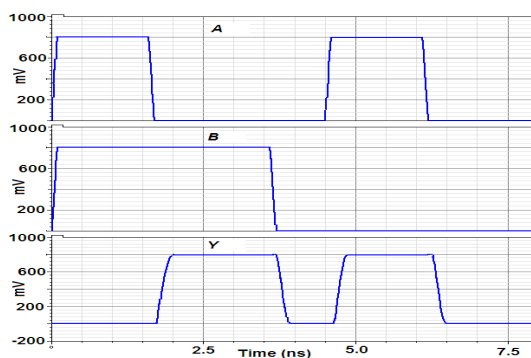|	V(v)	Proposed 6T	6T[15]	4T [4]	3T [7]	6T [4]
Delay (ns)	0.6	1.69	2.81	2.66	3.08	5.01
	0.8	1.59	2.75	2.99	2.06	3.25
	1.0	1.56	2.64	2.09	2.05	2.11
	1.2	1.55	2.09	2.07	2.04	2.08
Average power	0.6	1.82	2.31	4.19	8.70	14.66
	0.8	3.26	6.07	7.61	16.25	89.57
(fW)	1.0	15.02	22.77	12.12	25.36	238.90
	1.2	17.14	25.00	18.81	34.96	463.30
PDP (yJ)	0.6	3.08	6.49	11.13	26.81	73.36
	0.8	5.16	16.68	22.79	33.49	291.20
	1	23.45	60.16	25.38	51.86	504.20
	1.2	26.63	52.48	38.91	71.15	961.50

Fig. 3.   Full-swing logic of the novel pass-transistor XOR gate

I. CONCLUSIONS

This paper presents a new 2-input XOR gate topology with a full-swing voltage output in 65nm CMOS process for low-power application in order to reduce the power dissipation and delay for the overall circuit. The performances of the proposed XOR gate was compared to other peer designs in various conditions and the results show that there are improvements in term of power consumption, propagation delay and PDP compared to others design. It has a good driving capability with good output signal in all input combinations and better performance especially in low supply voltage The proposed XOR gate has a much less delay and hence much less PDP than its peer designs. It give better performance which can operate at low voltages which is the best choice for low-power and low-voltage application with requires small area and low power consumption such as RFID tags.

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