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A New Design of XOR-XNOR gates for low power application

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***Abstract*—XOR and XNOR gate plays an important role in digital systems including arithmetic and encryption circuits. This paper proposes a combination of XOR-XNOR gate using 6-transistors for low power applications. Comparison between a best existing XOR-XNOR have been done by simulating the proposed and other design using 65nm CMOS technology in Cadence environment. The simulation results demonstrate the delay, power consumption and power-delay product (PDP) at different supply voltages ranging from 0.6V to 1.2V. The results show that the proposed design has lower power dissipation and has a full voltage swing.**

Keywords-XOR-XNOR gate, low power, delay

I. INTRODUCTION

Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. Due to the important role played by XOR and XNOR gate in various circuits especially in arithmetic circuits, optimized design of XOR and XNOR circuit to achieve low power, small size and delay is needed. The primary concern to design XOR-XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with low number of transistors to implement it.

In this paper, we propose a new design of XOR-XNOR gate using 6 transistors. The paper is organized as follows: in Section II, previous work is reviewed. Subsequently, in section III, the proposed design of XOR-XNOR gate is presented. In section IV, the simulation results are given and discussed. The comparison and evaluation for proposed and existing designs are carried out. Finally a conclusion will be made in the last section.

II. PREVIOUS WORK

Numerous designs were reported to realize the XOR-XNOR functions using different number of circuit techniques and approaches [1], [2], [3], [4], [5], [6], [7]. They vary in methodologies and transistor count to improve the circuit performance in term of speed and density. Among these, the conventional design of XOR-XNOR circuit using static CMOS network can be found in [4]. Each input is connected to both an NMOS transistor and a PMOS transistor. It provide a full output voltage swing but with a large number of transistors.

Complementary pass transistor logic (CPL) is used in [1]. Wang et al. [2] report the XOR-XNOR circuits based on transmission gates. It uses eight transistors and complementary inputs and has a drawback of loss of driving capability. Wang et al. also designed XOR-XNOR circuits based on inverter gates. It does not require a complementary inputs but it has no driving capability because there is no direct connection to Vdd and Gnd. The improved version of this circuit has been designed by adding a standard inverter to the output. This modified circuit provides a good driving capability but uses twelve transistors for XOR-XNOR circuits.

Shiv et al. [3] proposed two of XOR-XNOR circuits (Figure 1 and 2) and claimed to have lower PDP, less power dissipation and faster compared to design in [5] with a low supply voltage. However both of the circuits give a poor signal output voltage in certain input combination. In [6], the XOR and XNOR circuit based on Pass Transistor Logic (PTL) using 6 transistors is reported as shown in Figure 3. It has a full output voltage swing and better driving capability by using Vdd and Gnd connection.

Elgamel et al. [7] proposed an improved version of [6] in Figure 4 and has better power-delay product and higher noise immunity. In [5], the XOR-XNOR circuit adds a forward and backward feedback between the XOR and XNOR gate and additional transistors to rectify the degraded logic level problem. This configuration shown in Figure 5 provides a better performance of the circuit.

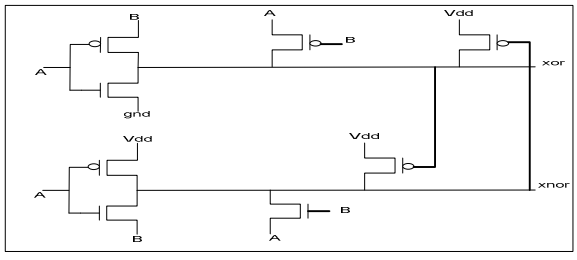

Figure 1. XOR-XNOR gate using 8 transistors in [3]

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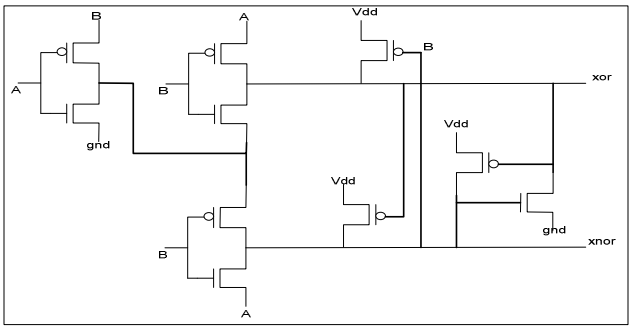

Figure 2. XOR-XNOR gate using 10 transistors in [3]

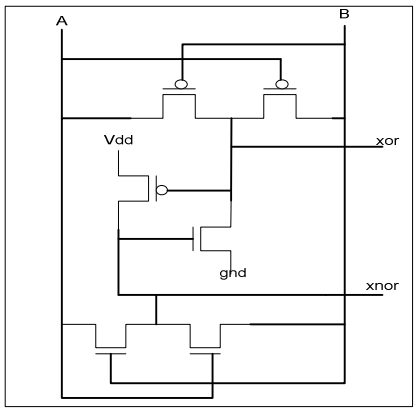

Figure 3. XOR-XNOR gate using 6 transistors in [6]

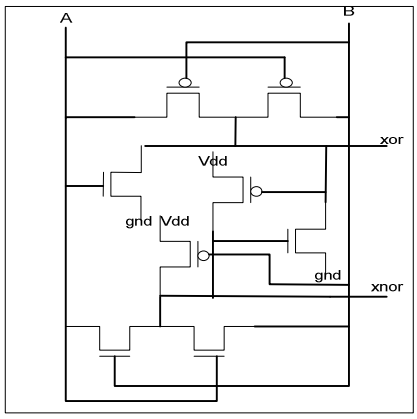

Figure 4. XOR-XNOR gate using 8 transistors in [7]

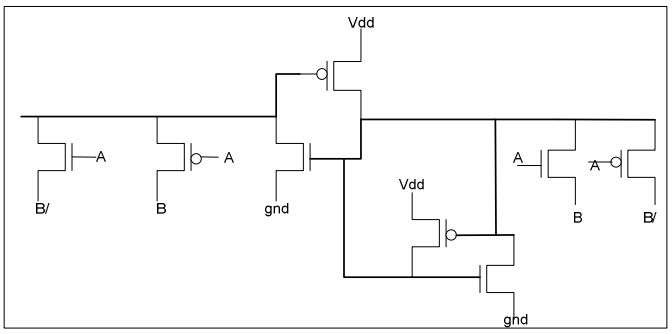

Figure 5. XOR-XNOR gate using 8 transistors in [5]

III. PROPOSED XOR-XNOR GATE CIRCUIT

The XOR and XNOR gate functions are shown in Table 1 and denoted by $\oplus$ and $\odot$ respectively. The logic expression for XOR and XNOR are

$$A \oplus B = A'B + AB' \quad (1)$$

$$A \odot B = A'B' + AB \quad (2)$$

TABLE I. XOR AND XNOR GATE FUNCTION

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

The proposed design of XOR-XNOR gate using six transistors is shown in Figure 6. It uses a concept of pass transistor and CMOS inverter. The inverter is used as a driving output to achieve a perfect output swing. Vdd connection to transistor M3 and M4 are use to drive a good output of '1'. Transistor M4 is used to drive the output signal when XOR output '0' when input signal A=B=1. In this condition, when transistor M1 or M2 is ON, it will pass a poor signal '1' with respect to the input to the inverter. The output XOR will also be degraded and to achieve a good output signal, transistor M4 is ON when output Xor is '0', then it will pass the perfect signal '1' from Vdd to the output XOR.

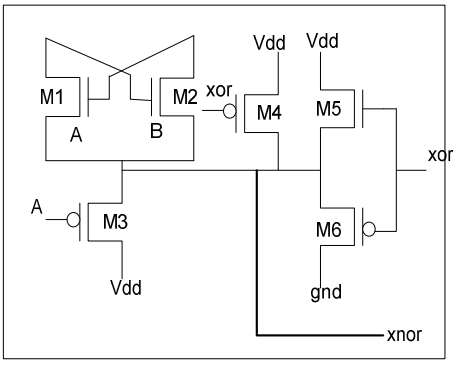

Figure 6. Proposed XOR-XNOR gate using 6 transistors

IV. SIMULATION RESULTS OF 6-TRANSISTOR XOR-XNOR GATE

The XOR-XNOR gate is simulated using Spectre Cadence in the voltage range of 0.6V to 1.2V using 65nm CMOS technology. Simulation is performed at varying supply voltages to show the effect of different voltages to the power dissipation of XOR-XNOR circuit. Comparative analysis has been carried out on the different types of combination XOR-XNOR based on the best previous design. The transient analysis of the circuits were performed with a load capacitance of 50fF at 500MHz and simulated using the same conditions to measure propagation delay and power dissipation. The delay has been computed between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of

voltage level for both rising and fall transition. The power-delay product (PDP) is measured as the product of the average delay and the average power.

The comparisons of output value for XOR-XNOR circuits for each input combination are shown in Table 2. The results of simulation which included a delay, power dissipation and power delay product are listed in Table 3 and also are represented in Figure 7, 8, 9, 10 and 11. The results indicate that the delay of the proposed XOR-XNOR circuit is smaller than previous circuit in Figure 2[3], [6] and [5], and nearly similar to circuit in Fig 1[3] and [7]. But in terms of power consumption, the proposed circuit consumes less power compared to other design except for the circuit in [6] which consumes less power than other circuits but [6] offer slowest speed at a low voltage. The overall PDP for the proposed circuit have been improved more than 50% from other circuit except from the circuit in [6], but nearly similar at the low supply voltage. Regarding to the simulation results, the proposed XOR-XNOR circuit are the most energy efficient and very well suited to low voltage applications.

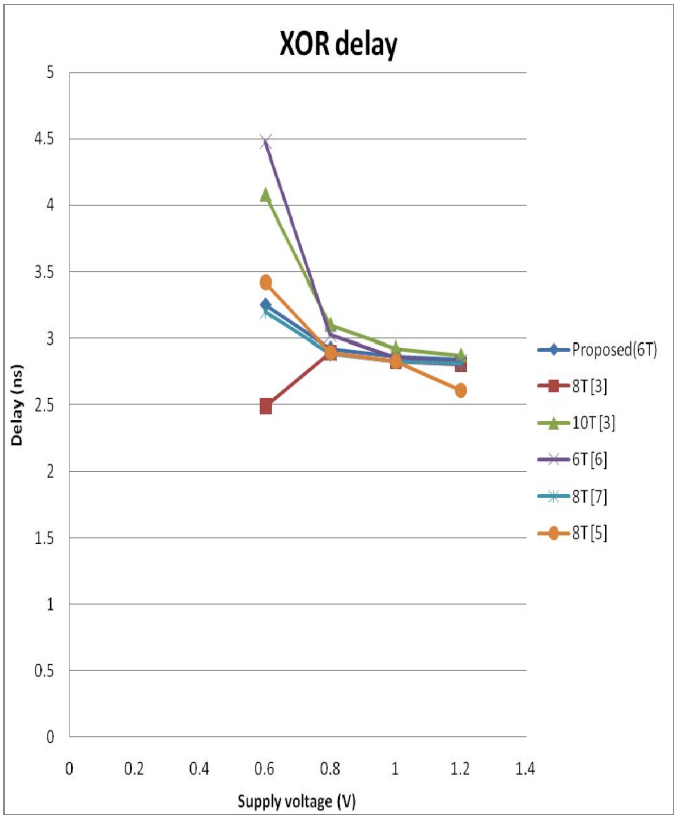

Figure 7. Worst case delay of different XOR circuit

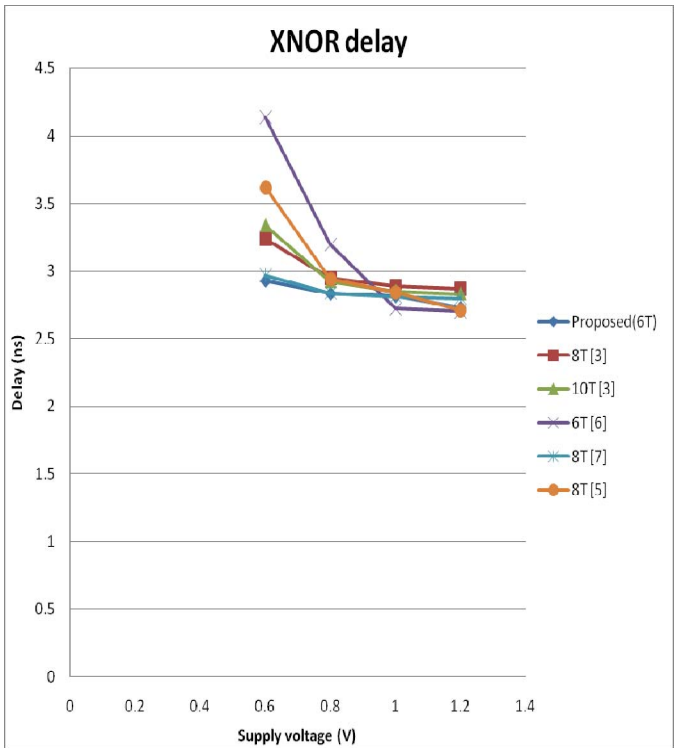

Figure 8. Worst case delay of different XNOR circuit

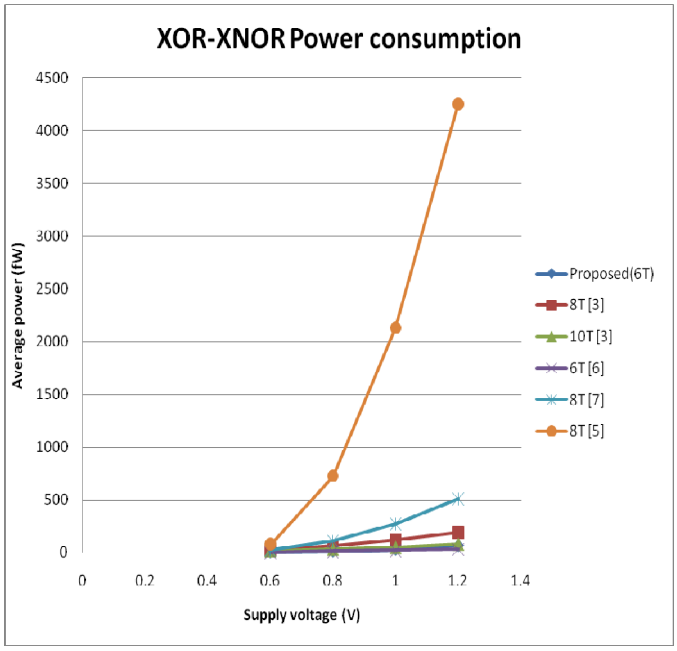

Figure 9. Power consumption of different XOR-XNOR circuit

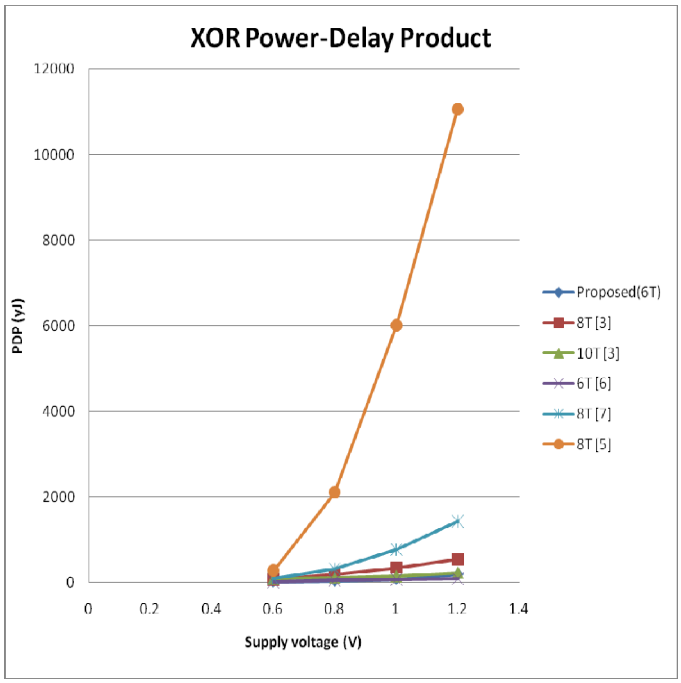

Figure 10. Power-delay products (PDP) of different XOR circuit

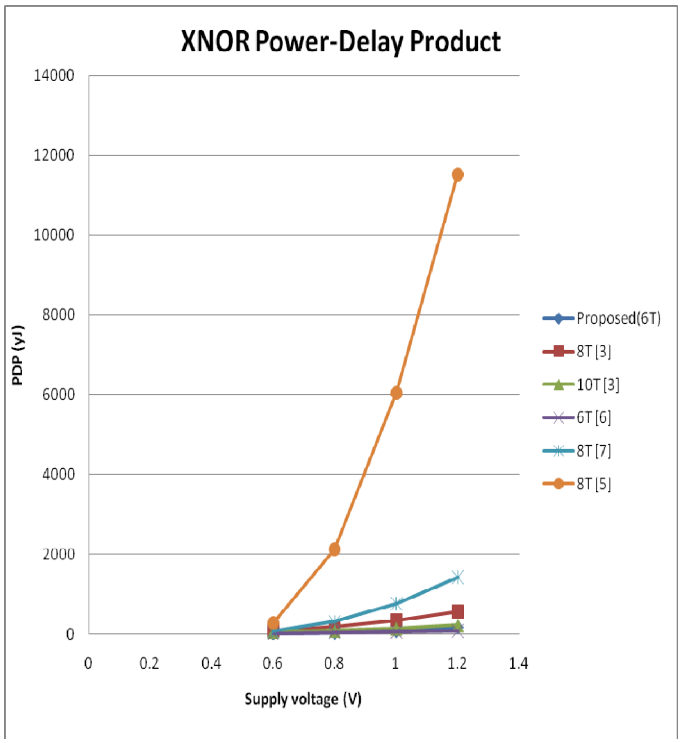

Figure 11. Power-delay products (PDP) of different XNOR circuit

CONCLUSIONS

In this paper, we proposed the new design of combination XOR-XNOR circuit configuration. The performances of this circuit have been compared to previous reported XOR design based on delay, power dissipation and PDP. According to the simulation results, the proposed circuit offers a better and more competitive than other design. It offers the lowest power dissipation at a low supply voltage. It has a good driving capability with good output signal in all input combinations and better performance especially in low supply voltage compared to the previous designs. Thus, the proposed circuit is suitable for low-voltage and low-power application.

ACKNOWLEDGMENT

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TABLE II. COMPARISON OF OUTPUT VALUE FOR XOR-XNOR GATE

Inputs		Proposed (6T)		8T [3]		10T [3]		6T [6]		8T [7]		8T [5]	
A	**B**	**XOR**	**XNOR**	**XOR**	**XNOR**	**XOR**	**XNOR**	**XOR**	**XNOR**	**XOR**	**XNOR**	**XOR**	**XNOR**
0	0	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Good 0	Good 1
0	1	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Bad 0	Good 1	Good 0	Good 1	Bad 0
1	0	Good 1	Good 0	Bad 1	Good 0	Good 1	Bad 0	Good 1	Good 0	Bad 1	Bad 0	Bad 1	Good 0
1	1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Good 1	Good 0	Bad 1

TABLE III. SIMULATION RESULT OF XOR-XNOR GATE

	V(v)	Proposed(6T)	8T [3]	10T [3]	6T [6]	8T [7]	8T [5]
Delay for XOR (ns)	0.6	3.252	2.484	4.083	4.483	3.205	3.422
	0.8	2.925	2.892	3.101	3.025	2.886	2.891
	1	2.865	2.825	2.928	2.86	2.828	2.824
	1.2	2.843	2.802	2.874	2.823	2.81	2.603
Delay for XNOR (ns)	0.6	2.926	3.239	3.339	4.136	2.966	3.62
	0.8	2.832	2.947	2.922	3.195	2.835	2.942
	1	2.813	2.89	2.852	2.72	2.81	2.844
	1.2	2.731	2.867	2.831	2.701	2.798	2.711
Average power for XOR-XNOR (fW)	0.6	6.379	27.7	19.93	2.251	25.69	77.46
	0.8	12.62	64.36	33.65	13.75	109.4	726
	1	28.78	121.4	50.19	21.36	270.5	2129
	1.2	65.04	196.2	79.98	30.55	510.3	4254
PDP for XOR (yJ)	0.6	20.75	68.8	81.38	10.09	82.34	265.07
	0.8	36.91	186.1	104.35	41.53	315.73	2099
	1	82.46	343	146.96	61.09	764.97	6012.3
	1.2	184.9	549.8	229.86	86.24	1433.94	11073
PDP for XNOR (yJ)	0.6	18.66	89.721	66.55	9.31	76.2	280.41
	0.8	35.74	189.67	98.33	43.87	310.15	2135.89
	1	80.96	350.85	143.14	58.1	760.11	6054.88
	1.2	177.62	562.51	226.42	82.52	1427.82	11532.6