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Design of FPGA Based SPWM Single Phase Inverter

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***Abstract*—**Nowadays power inverter serves as an important emergency power supply system in events of mains power supply failure. The AC output voltage of a power electronic inverter is usually non-sinusoidal and hence has a high harmonic content. Sinusoidal Pulse Width Modulation (SPWM) scheme is normally used to convert the DC power supply into AC power supply by comparing the reference voltage waveform with the triangular waveform known as carrier. SPWM provides a way to reduce the total harmonic distortion of load current. The objective of this paper is to demonstrate a SPWM switching by using Altera DE2 board. In this SPWM, a sinusoidal reference voltage waveform is compared with the triangular carrier voltage to generate the on and off switching scheme. These switching schemes will trigger the gate of the power switch. In this paper, the SPWM switching strategies will be develop using Altera DE2 (Cyclone II EP2C35F672C6) with 16 bit serial configuration devices. The switching between reference and carrier waveforms of SPWM is obtained by using Matlab software. Simulation on the design pulses is conducted using Quartus II software tools provided by Altera. The output frequency of SPWM is 50 Hz and the design is limited to two levels of modulation index which are 0.5 and 0.75.

***Keywords*:** SPWM-Sinusoidal Pulse Width Modulation, FPGA-Field Programmable Logic Array, VHDL- Very High Description Language.

I. INTRODUCTION

Pulse width modulation (PWM) is the most popular switching method used to several types of converter with an appropriate switching scheme to produce a desired switching pattern. PWM is one of the switching techniques used for converter to produce an AC output signal fed from DC input [1]. PWM makes the inverter output waveforms made up of many pulses with certain rules and goals through supplying DC voltage for the inverter [2]. The on and off scheme based on the intersection of the carrier signal (triangular) and reference signal (constant DC). PWM still contains a harmonics and another approach is SPWM switching technique [3]. This paper presents work carried out in developing control signal using bipolar SPWM to produces a switching scheme which only a single sinusoidal waveform (reference) used with the triangular (carrier) [4]. In SPWM a fixed triangular is compared with sinusiodal waveform and the amplitude can be varied from [1]. The on and off switching scheme will be produce when the instantaneous value of the reference signal is larger than the triangular carrier, the output is at positive and when the reference is less the carrier output is at negative as shown in figure 1. In order to demonstrate SPWM switching using Altera DE2 board, the switching interval between each crossing obtained using Matlab software. The crossover of the signal then transferred into a table. The switching scheme should be able to be implemented to the four switches at the inverter with a different timeline.

This project presents the implementation of FPGA technology in designing the SPWM switching signal. Altera Cyclone II FPGA is used in this project. It aslo provide a wide range of density, memory, embedded multiplier, and packaging options in a customer-defined FPGA feature set optimized for low-cost applications. Besides that, Cyclone II FPGA also supports a wide range of common external memory interfaces and I/O protocols common in low-cost applications. The use of FPGA will produce better control signal for single phase full bridge inverter. The modulation index, number of pulses over a period and the output frequency can easily changed using the program. The designed of the switching pulse can be altered without any changes in hardware. This is the main advantages of this project that applied the FPGA technology where there is the flexibility of any changes on the switching parameter and directly eliminates the complexity of the hardware.

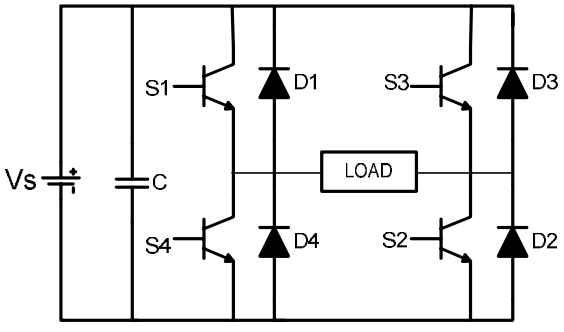

Figure 1: Single phase full-bridge inverter.

II. MATLAB PROGRAMMING

A program is developed from the fundamental concept of the SPWM switching technique by using Matlab M-File. The programming is capable to produce the SPWM waveform characteristic from the several ranges of frequencies, modulation and number of pulses for half period of reference signal. The input data will be processed through a mathematical programming and the intersection between reference signal and carrier signal generates PWM pulses for the period of α_n to β_n in each pulse as shown in figure 2. According to figure 2, n is the number of pulse for half cycle of reference signal. This strategy is implemented using Matlab/M-file programming and can be fulfilled through six steps as demonstrated in figure 3.

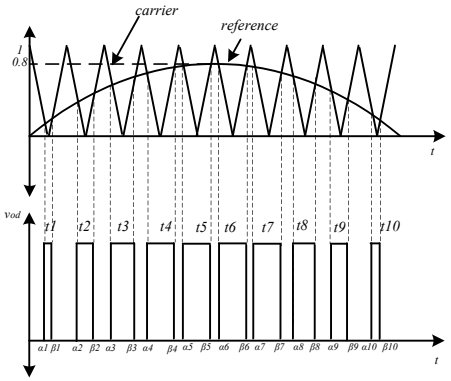

Figure 2: Generation of SPWM switching scheme.

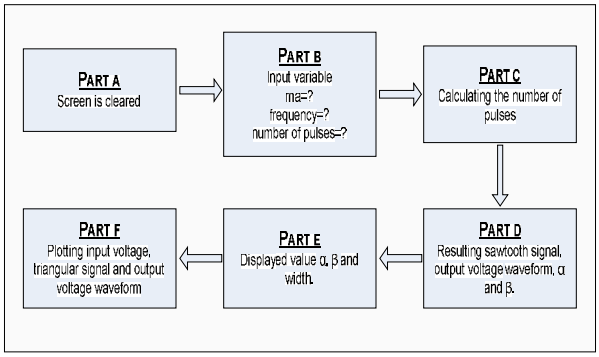

Figure 3: Block diagram of Matlab Programming.

In this paper, the proposed frequency of the output inverter is 50Hz with two modulation index which is 0.75 and 0.5. The output of PWM signal is recorded based on time scale and degree scale. These data are used to produce the SPWM switching scheme whereas the time will be digitized.

III. SWITCHING STRATEGIES

The proposed converter is use an IGBT as a switching device. The IGBT's have simpler driving circuits than other power transistors devices and used due to its popularity among researchers that could lead to high-power application. The converter consists of four IGBTs. The data of the reference frequency of 50Hz with the modulation index of 0.5 and 0.75 are obtained from Matlab software then depicted in Table 1 (a) and (b) respectively. The recorded data are taken over one complete cycle of reference signal. For the first, the data recorded are in degree scale and then converted to time scale. Thus it can be used easily to generate PWM signal digitally and implemented using Quartus II software. From the table, it can be observed that the width of each pulse at the beginning and end for every half cycle of reference signal have the same scale. For instant, in the positive half cycle of reference signal the width of the pulse t_1 is equal with the pulse of t_{20}.

The period of the reference input frequency is

$$T = \frac{1}{f_{ref}} \tag{1}$$

For the half cycle

$$\frac{T}{2} \tag{2}$$

The value of α_n, β_n and the width of the pulses expressed in term of time can be determined by equations (3), (4), and (5) respectively.

$$\alpha_n(t) = \alpha_n(^\circ) \times \frac{T/2}{180^\circ} \tag{3}$$

$$\beta_n(t) = \beta_n(^\circ) \times \frac{T/2}{180^\circ} \tag{4}$$

$$Width = \beta_n - \alpha_n \tag{5}$$

All the intersection value for α and β is recorded in Table 1(a) and (b). The last intersection between the reference signal and carrier signal is occurs at β_{40} which is equal to 19.76ms and this is happen at the last pulse over one cycle of 20ms.

Switching time	α(°)	ß(°)	Width(°)	α(t)	ß(t)	Width(t)
t1	4.32	4.68	0.36	0.000240	0.000260	0.000020
t2	12.96	14.04	1.08	0.000720	0.000780	0.000060
t3	21.69	23.40	1.71	0.001205	0.001300	0.000095
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t10	83.25	87.75	4.50	0.004625	0.004875	0.000250
t11	92.25	96.75	4.50	0.005125	0.005375	0.000250
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t18	156.60	158.31	1.71	0.008700	0.008795	0.000095
t19	165.96	167.04	1.08	0.009220	0.009280	0.000060
t20	175.32	175.68	0.36	0.009740	0.009760	0.000020
t21	184.32	184.68	0.36	0.010240	0.010260	0.000020
t22	192.96	194.04	1.08	0.010720	0.010780	0.000060
t23	201.69	203.40	1.71	0.011205	0.011300	0.000095
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t30	263.25	267.75	4.50	0.014625	0.014875	0.000250
t31	272.25	276.75	4.50	0.015125	0.015375	0.000250
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t39	345.96	347.04	1.08	0.019220	0.019280	0.000060
t40	355.32	355.68	0.36	0.019740	0.019760	0.000020

(a)

Switching time	α(°)	ß(°)	Width(°)	α(t)	ß(t)	Width(t)
t1	4.23	4.77	0.54	0.000235	0.000265	0.000030
t2	12.78	14.31	1.53	0.000710	0.000795	0.000085
t3	21.24	23.85	2.61	0.001180	0.001325	0.000145
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t10	82.17	88.92	6.75	0.004565	0.004940	0.000375
t11	91.17	97.83	6.66	0.005065	0.005435	0.000370
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t18	156.15	158.76	2.61	0.008675	0.008820	0.000145
t19	165.69	167.22	1.53	0.009205	0.009290	0.000085
t20	175.23	175.77	0.54	0.009735	0.009765	0.000030
t21	184.23	184.77	0.54	0.010235	0.010265	0.000030
t22	192.78	194.31	1.53	0.010710	0.010795	0.000085
t23	201.24	203.85	2.61	0.011180	0.011325	0.000145
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t30	262.17	268.92	6.75	0.014565	0.014940	0.000375
t31	271.17	277.83	6.66	0.015065	0.015435	0.000370
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t39	345.69	347.22	1.53	0.019205	0.019290	0.000085
t40	355.23	355.77	0.54	0.019735	0.019765	0.000030

(b)

Table 1: (a) and (b): Data obtained from Matlab for modulation index 0.5 and 0.75.

IV. VHDL PROGRAMMING USING QUARTUS II

By using Quartus II 8.0 sp1 software provided by Altera, the data obtained from the Matlab are digitized to be able to implement in Quartus II environment. Figure 4 illustrate the block diagram of the complete SPWM generator for modulation index 0.5 and 0.75. The block diagram consists of altpll which be able to generate 25 MHz clock output from 50 MHz internal clock of Altera DE2 board. The altpll megafunction can be used to reduce the clock delay and generate another internal clocks to be operates at multiples of system frequency. The clock divider is applied to divide the the internal clock of Altera DE2 board into several frequency ranges. As an example the internal clock frequency can be divided to 25 MHz, 1 MHz, 100 kHz, 1 kHz and etc. Then, the 1 MHz of the output frequency of clock divider is connected to the lpm_counter which will be counting from 0 to 19999 over one complete cycle. This means, one cycle of this frequency represent the period of 1 µs. The lpm_counter megafunction is actually a binary counter that either can be count up, down, or up and down together. The on and off signal is created by VHDL programming and then converted into block diagram. The VHDL for 0.75 and 0.5 modulation index are created by employing four switches which are operate in pair for a time (S1-S2 and S3-S4).

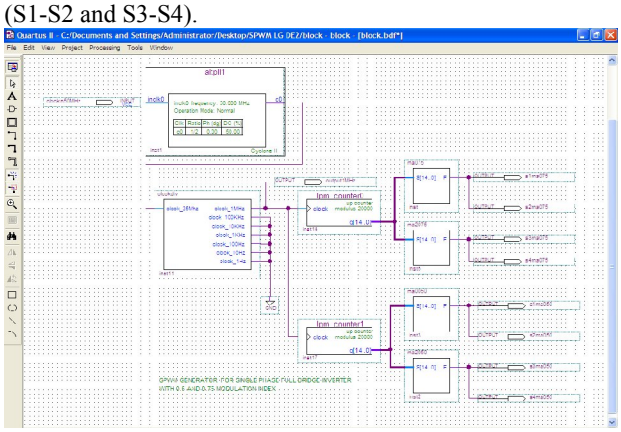

Figure 4: Block diagram of SPWM generator.

Before the programming can be uploaded into the DE2 board, the simulation using Waveform Editor of Quartus II is implemented to perform the SPWM signal. Figure 5 present the output waveform from the clock divider while figure 6 presents the output SPWM signal to trigger switches for 0.5 and 0.75 modulation indexes. In this stage, the measured velue of the estimated difference between the observed or calculated value of the timing compared to its true value. The behavior of the SPWM at high speeds for short interval can be observed by using compress option to compress the waveform.The output of the SPWM then assigned to the expansion header of the DE2 board through Pin Planner. The expansion headers connect directly to 36 pins of the Cyclone II FPGA. Table 2 show the output of the control signal which connected to expansion header pins.

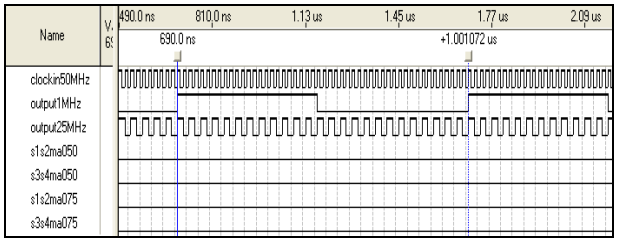

Figure 5: Output from the clock divider.

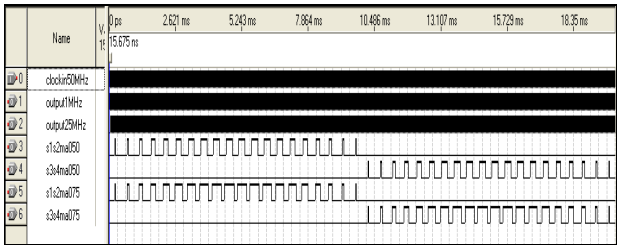

Figure 6: Control signal for 0.5 and 0.75.

Modulation Index (ma)	Switch	Expansion Header
0.5	S1	PIN N_24
	S2	PIN N_29
	S3	PIN M_22
	S4	PIN M_21
0.75	S1	PIN N_21
	S2	PIN N_22
	S3	PIN L_21
	S4	PIN L_22

Table 2: Output of SPWM connected to expansion header DE2 board.

The Assembler which is the compiler module that completes project processing will generate a device programming image. For the FPGAs, this programming image is in the form of one or more Programmer Object Files (.pof) and SRAM Object Files (.sof). With the Active Serial programming interface, programming hardware used to download the configuration data for programming serial configuration devices. The voltage level of the input and output on the expansion header can be adjusted to 3.3V, 2.5V or 1.8V.

V. RESULTS

Tektronix four channel digital oscilloscope TDS3054B is used to measure the experimental result from the DE2 board. The experiment also conducted for two modulations which is 0.5 and 0.75. Figure 7 and Figure 8 demonstrate the width difference for modulation 0.5 and 0.75 respectively. Practically the above signal of figure 7 and figure 8 are used to control the turning on/off of the power switch S1S2 while the below is to control power switch of S3S4 of the inverter. The width of both pulses from t_1 to t_{40} is analyzed and compared with the simulated signal using Quartus II software. From the simulation results and experiment results its give the acceptable ranges of PWM signal between design and practical. Thus it can be said that the accuracy of the internal clock of the DE2 board is very precise.

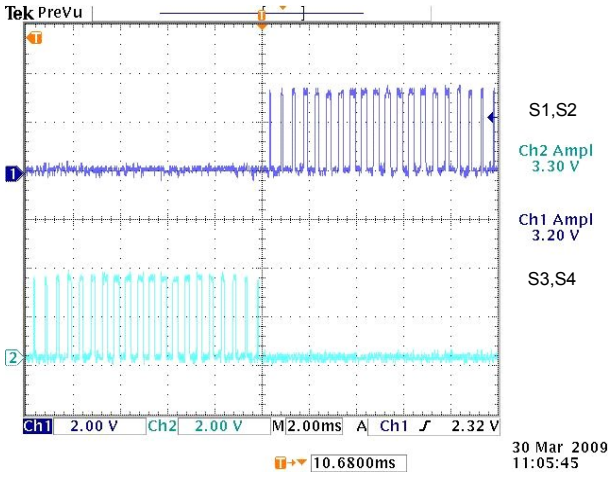

Figure 7: Output signal for modulation index 0.5.

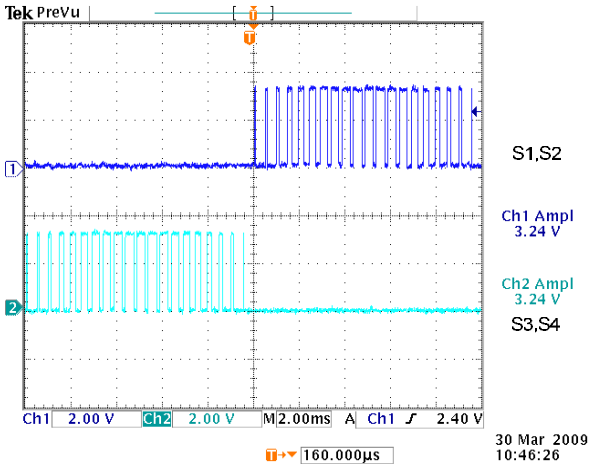

Figure 8: Output signal for modulation index 0.75

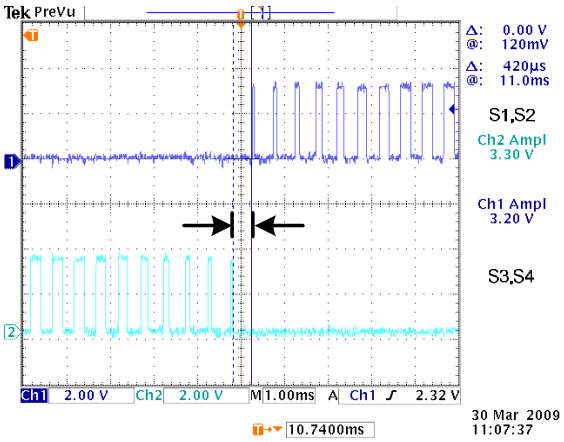

Figure 9: Dead time for 0.5 modulation index.

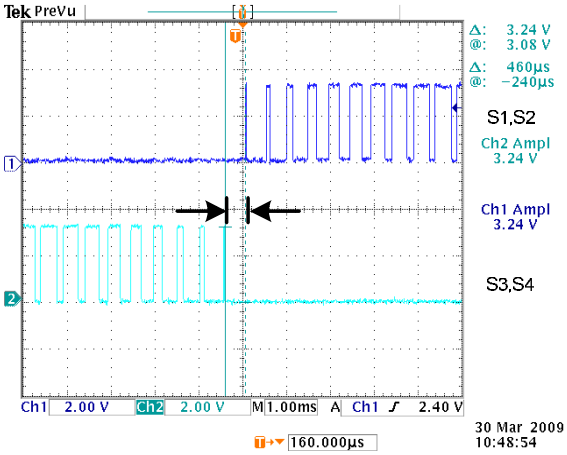

Figure 10: Dead time for 0.75 modulation index.

Figure 9 and figure 10 show the dead time applied between switch S1S2 and S3S4 for the modulation index of 0.5 and 0.75 respectively. From these figure it can be observed that the dead time for modulation index 0.5 and 0.75 is 420µs and 460µs respectively. The occurs of dead time between the S1S2 and S3S4 shows that the signal are possible to be implemented to control the IGBTs switch of the inverter. The SPWM signal with the modulation index of 0.5 and 0.75 has the amplitude of 3.3 V and 3.24 V respectively and demonstrated in Figure 11 and Figure 12.

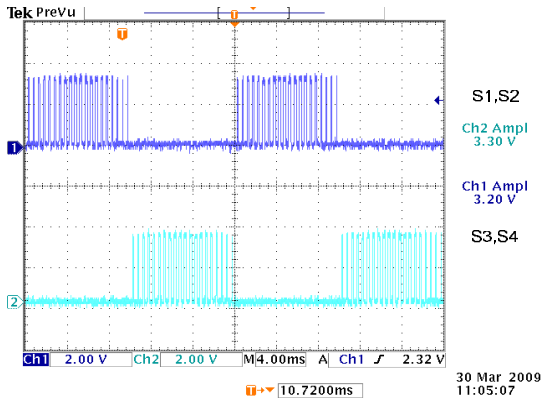

Figure 11: Output signal for S1S2 and S3S4 with modulation index= 0.5

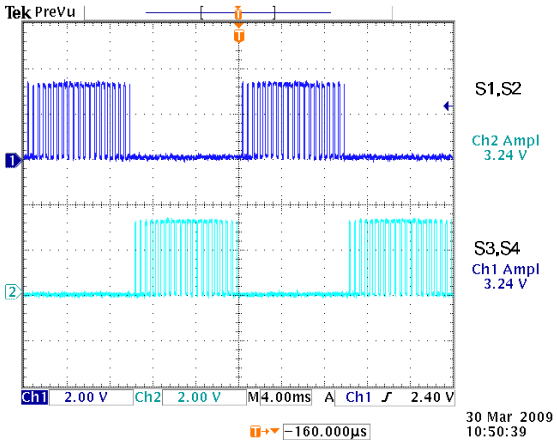

Figure 12: Output signal for S1S2 and S3S4 with modulation index= 0.75

VI. CONCLUSIONS

This paper outlined and illustrated a method to obtain the switching strategies in generating a SPWM signal for a single-phase inverter. The SPWM signal has been developed and tested successfully using Quartus II software and implemented on Altera DE2 Board. The developed SPWM is uploaded on a single chip of Altera Board and it is capable to provide flexibility, relibitily and ease to program in order to control a single-phase inverter.

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REFERENCES

[1] Muhammad, H. Rashid. *Power Electronics Circuits, Devices and Application*. Upper Saddle River, NJ: Prentice Hall, 2004.

[2] Huo B., Zhao Z., Meng S., Liu J. and Sun X, "Comparison of Three PWM Strategies-SPWM, SVPWM & One-cycle Control". Dept. of Electrical Engineering, Tsinghua University, Beijing, China, IEEE Explore, 2003.z

[3] M. N. Md Isa, M.I. Ahmad, Sohiful A.Z. Murad and M. K. Md Arshad, "FPGA Based SPWM Bridge Inverter", American Journal of Applied Sciences 4 (8), 2007, pp 584-586.

[4] Mohan, Undeland and Robbins. *Power Electronic converters, applications and design*, 2nd ed. Canada: John Wiley & Sons Inc, 1995.