A Simple Approach of Space-vector Pulse Width Modulation Realization Based on Field Programmable Gate Array

TOLE SUTIKNO,1,2 WONG JENN HWA,1 AUZANI JIDIN,1,3 and NIK RUMZI NIK IDRIS1

1Department of Energy Conversion, Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), Johor, Malaysia
2Department of Electrical Engineering, Faculty of Industrial Technology, Universitas Ahmad Dahlan, Yogyakarta, Indonesia
3Department of Power Electronics and Drives, Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Melaka, Malaysia

Abstract Employing a field programmable gate array to realize space-vector pulse width modulation is a solution to boost system performance. Although there is much literature in the application of three-phase space-vector pulse width modulation based on field programmable gate arrays, most is on conventional space-vector pulse width modulation with designs that are complicated. This article will present a simple approach to realize five-segment discontinuous space-vector pulse width modulation based on a field programmable gate array, in which the judging of sectors and the calculation of the firing time are simpler with fewer switching losses. The proposed space-vector pulse width modulation has been successfully designed and implemented to drive on a three-phase inverter system that is loaded by an induction machine of 1.5 kW using the APEX20KE Altera field programmable gate array (Altera Corporation, San Jose, California, USA).

Keywords electric drives, field programmable gate array applications, motor controls, power converters, space-vector pulse width modulation

1. Introduction

The space-vector pulse width modulation (SVM) method is an advanced pulse width modulation (PWM) method and is the best among all the PWM techniques in the application of variable frequency drives. SVM provides a better fundamental output voltage, better harmonic performance, and is easy to implement [1–13]. In recent years, the SVM method has gradually obtained widespread application in power electronics and electrical drives due to its superior performance characteristics. Compared with sinusoidal pulse width modulation (SPWM), SVM is more suitable for digital implementation because the obtainable DC voltage utilization ratio can highly be increased. As the
result, a better voltage total harmonic distortion (THD) factor can be obtained [1, 2, 10–12, 14]. A comparison of switching losses $P_L$, junction temperature of the insulated-gate bipolar transistor (IGBT) $T_J$, and weighted THD of the different modulation schemes are shown in Table 1 [15]. From the comparison, the discontinuous SVM shows the lowest switching losses and the lowest junction temperature of the IGBT compared with SPWM and conventional SVM, although it has a slightly higher weighted THD compared with the conventional SVM method.

In most engineering practices, the SVM algorithm is mainly implemented through software based on microcontroller or digital signal processors (DSPs) [16–18]. From here, designers must sequentially perform the control procedure by exploiting their mathematically oriented resources. The instructions of different procedures need to be executed one after the other. Thus, the purely software-based technique is not an ideal solution. The field programmable gate array (FPGA) is an appropriate alternative over analog and software solutions (DSP and microcontroller) [19–24], and its architecture offers a significant integration density [25] within a flexible programmable environment. Designers can get a new degree of freedom by applying the FPGA in SVM, because the dedicated hardware architectures of the FPGA matches all of the requirements in terms of control performance as well as the implementation constraints [19]. Employing the FPGA in SVM strategies provides many advantages, such as shorter design cycle, fair cost, rapid prototyping, simpler hardware and software design, and higher switching frequency. Differing with the software implementation, the FPGA performs the entire procedure with a concurrent operation (allowing parallel processing by means of a hardware mode and not occupying) by using its reconfigurable hardware. With its powerful computation ability and flexibility, an FPGA is quite mature in the application of electrical drives, and it is considerable as a solution to boost the system performance when including the SVM algorithm [6, 19, 26–29].

The digital hardware FPGA-based solution has been widely implemented in many control applications, including SVM realization [6, 19, 26–29]. However, conventional SVM suffers from drawbacks such as computational burden, inferior performance at high modulation indices, and high switching losses of the inverters. Hence, to reduce the switching losses and to improve the performance in the high-modulation region, several discontinuous SVM methods have been proposed [5, 15, 30–32].

Literature on the implementation of three-phase conventional SVM and discontinuous SVM based on the FPGA is not lacking. However, most of the designs are based on conventional SVM without consideration of the hardware-resource saving and are more complex. In this article, new approaches of FPGA-based SVM will be discussed, where the judging of sectors and the calculation of the firing time to generate the

<table>
<thead>
<tr>
<th>Table 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparison of switching losses, temperature, and weighted THD of the different modulation schemes [15]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>SPWM</th>
<th>Conventional SVM</th>
<th>Discontinuous SVM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching losses $P_L$ (per unit of SPWM)</td>
<td>1.00</td>
<td>1.33</td>
<td>0.83</td>
</tr>
<tr>
<td>$T_J$ (increase, °C)</td>
<td>35</td>
<td>45</td>
<td>32</td>
</tr>
<tr>
<td>Weighted THD (%)</td>
<td>4.0</td>
<td>1.8</td>
<td>2.9</td>
</tr>
</tbody>
</table>
SVM waveform is simple with low switching losses and hardware-resource saving. A novel five-segment discontinuous SVM design based on the basic idea from [33] and [18] is proposed, and the scheme with lower switching losses and a simpler algorithm is implemented through the APEX20KE Altera FPGA (Altera Corporation, San Jose, California, USA).

2. Novel Method of SVM Algorithm

The conventional principle of the SVM algorithm relies too much on the judging of sectors, and firing time (duration of active vectors) calculation and the method of switching sequence generation is too complex. As a solution to overcome the problems from the conventional SVM algorithm, this article proposes the principle of a symmetrical five-segment discontinuous switching sequence that has not yet been revealed as a novel method of SVM algorithm.

2.1. Proposed SVM Switching Pattern (Five-segment Discontinuous Switching Sequence)

Many discontinuous SVM patterns have been reported [5, 6, 30, 31, 34]. However, these patterns performed with high switching losses and used a complicated algorithm that is not easily implemented based on an FPGA. In this article, a novel symmetric five-segment discontinuous SVM is proposed, the design of which mainly originated from the ideas of [33] and [18]. The pattern has been successfully implemented by Yu based on DSP [18]. This pattern resulted in lower switching losses, a simpler algorithm, and easy implementation. Therefore, this article will focus on implementation of a discontinuous SVM pattern based on an FPGA in order to boost system performance. In this proposed pattern, there is always a leg that stays constant for the entire PWM period. The state sequence in this pattern is X-Y-Z-Y-X, where Z

\[ Z^{D} \] in Sectors I, III, and V; Z

\[ Z^{D} = 0 \] in the remaining sectors. Thus, the number of switching times for this pattern is less than the conventional pattern, and the obvious result is reduced switching losses.

2.2. Proposed Identification of the Sector

There are many different methods to judge the sector where the reference space voltage vector lies. Zhi-pu [35] compared the reference space vector’s angle with 0°, 60°, 120°, 180°, 240°, and 300° to obtain the number of the sector where \( V_{ref} \) is Yu et al. [36], Jiang et al. [37], and Xing and Zhao [7] obtained the sector number by analyzing the relationship between \( V_{\alpha} \) and \( V_{\beta} \). To determine the sector, the inverse Clark transformation is used for the calculation of projections \( V_{a} \), \( V_{b} \), and \( V_{c} \) of \( V_{\alpha} \) and \( V_{\beta} \) in the \((a, b, c)\)-plane, as follows:

\[
\begin{align*}
V_a &= V_{\beta} \\
V_b &= \frac{\sqrt{3} V_{\alpha} - V_{\beta}}{2} \\
V_c &= \frac{-\sqrt{3} V_{\alpha} - V_{\beta}}{2}
\end{align*}
\]
Then, based on Eq. (1), $N = \text{sign}(V_a) + 2 \times \text{sign}(V_b) + 4 \times \text{sign}(V_c)$, mapping $N$ to the actual sector of the output voltage reference by referring to the following relationship:

$$
\begin{array}{c|cccccc}
\text{Sector} & I & III & IV & V & VI & VII \\
\text{Vector} & 0 & 1 & 1 & 0 & 0 & 0 \\
\text{angle} & (0^\circ, 60^\circ) & (60^\circ, 120^\circ) & (120^\circ, 180^\circ) & (180^\circ, 240^\circ) & (240^\circ, 300^\circ) & (300^\circ, 360^\circ) \\
\end{array}
$$

Note: 1: satisfied; 0: not satisfied.

In [38], Zeliang et al. adopted two new intermediate vectors $X_\alpha$ and $X_\beta$, whereby $X_\alpha = \frac{3}{2}V_\alpha$ and $X_\beta = \sqrt{3}V_\beta$. Decomposing the conventional SVM will properly counteract the redundant calculations to identify sector location, but it results in complicated matrix calculations. In this article, by analyzing on the principle of SVM in [7, 36–38] and to reduce the burden of computation, a new method to determine the sectors of voltage vectors based on a comparison between $V_\beta$, $\sqrt{3}V_\alpha$, $-\sqrt{3}V_\alpha$, and 0, as shown in Figure 1, is proposed. Through the comparison, sectors of voltage vectors, as shown in Table 2, can be determined.

### 2.3. Determination of the Duration of Active Vectors

The space-vector technique synthesizes a desired vector $V_{ref}$ from two adjacent actives, $V_\alpha$ and $V_\beta$ (among $V_1$ and $V_2$, as shown in Figure 1) during time interval $T_a$ and $T_b$. The
null vectors (V and V7) are also applied to reduce the inverter switching frequency. In the proposed design, only one null vector is inserted in a PWM period, whereby V7 is used for odd sectors and V for even sectors:

\[ V_{\text{ref}} = V_a + jV_\beta = \frac{2T_a}{T}V_a + \frac{2T_b}{T} \],

(2)

\[ \frac{T}{2} = T_a + T_b + T_0. \]

(3)

Hence, the half PWM period T is composed of the switching times T_a, T_b, and T. The total time of the null vectors can be expressed as

\[ T_0 = \frac{T}{2} - T_a - T_b. \]

(4)

In this design, the switching times of the active vectors for each sector can be calculated as shown in Table 3.

### Table 3
Switching time of the active vector for each sector

<table>
<thead>
<tr>
<th>Sector</th>
<th>( T_a )</th>
<th>( T_b )</th>
<th>( T_a + T_b )</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>( \frac{3T}{4} \left( \frac{V_a - V_\beta}{V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a + V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
</tr>
<tr>
<td>II</td>
<td>( \frac{3T}{4} \left( \frac{V_a}{V_{dc} + \sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a + V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
</tr>
<tr>
<td>III</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a - V_\beta}{V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a + V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
</tr>
<tr>
<td>IV</td>
<td>( \frac{3T}{4} \left( \frac{V_a}{V_{dc} + \sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a + V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
</tr>
<tr>
<td>V</td>
<td>( \frac{3T}{4} \left( \frac{V_a - V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a - V_\beta}{V_{dc} - \sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{V_{dc} - \sqrt{3}V_{dc}} \right) )</td>
</tr>
<tr>
<td>VI</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{\sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{V_a - V_\beta}{V_{dc} - \sqrt{3}V_{dc}} \right) )</td>
<td>( \frac{3T}{4} \left( \frac{2V_\beta}{V_{dc} - \sqrt{3}V_{dc}} \right) )</td>
</tr>
</tbody>
</table>

2.4. Proposed SVM Switching Sequence Generating Method Based on Calculation of the Duration of Active Vectors

In this article, a new method of SVM switching sequence is proposed, whereby the PWM signal for odd sectors are realized through comparison between the triangle waveform with \( T_a \) and \( T_a + T_b \). A high signal will be generated when the triangle waveform is higher than signal A or B, and another leg is always set to 1. For even sectors, the generation of the PWM signal is a complement to the odd sectors, whereby the signal will be set high when the triangle waveform is lower than signal A or B and another leg is set to 0.
To simplify the design process, the term $2m/T$ will set to 1 so that $y$ will be always equal to $x$ ($x = T_0 = T_a$, then $y = x = T_a$; and if $x = T_1$, then $y = T_1 = T_b$). Obviously if $x = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$, then $y = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$. Therefore, the generation of PWM for $S_b$ and $S_c$ legs in Sector I can be obtained by comparing the triangle waveform with $T_a$, and $T_a + T_b$, respectively, and the $S_a$ leg is set to 1 due to the odd sector position, as shown in Figure 2.

3. FPGA Implementation of Proposed Novel SVM

After the discussion on the principle of SVM generation, this section focuses on the implementation of an FPGA in SVM. The overall proposed SVM design is shown in Figure 3. It can be seen from this figure that the design consists of five blocks or modules, namely $ajust\_freq$, $Vbeta\_Valpha$, $find\_sector$, $SVM\_generator$, and $deadtime\_sytem\_module$. Each of these modules is explained in the following subsections.

3.1. First Module: $ajust\_freq$

From Figure 3, the function of $ajust\_freq$ is to generate a suitable clocking frequency. In the proposed SVM design, this module functions as a frequency divider by generating a carrier frequency of 20 kHz and a fundamental frequency of 50 Hz from the FPGA board, which have a clocking signal of 33.33 Mhz. Since the triangle signal generator in this design is sampled to be 32 times per period, in order to get a carrier frequency of 20 kHz, the main clock generator from the FPGA board was divided by 13 (33.33 MHz: $(13 \times 32) = 20$ kHz).
Figure 3. Overall of the proposed SVM design.

3.2. Second Module: Vbeta_Valfa

In the proposed method, $V_{alpha}$ and $V_{beta}$ are generated based on sine and cosine functions through the look-up table (LUT) with a memory mapping of 360 addresses. There are three lines, categorized as lower, base, and upper, that are represented with 96, 224, and 352, respectively, into 9 unsigned bits. With the memory mapping of 360 addresses, the counter mod-360 will be used to count the LUT of $V_{alpha}$ and $V_{beta}$.

3.3. Third Module: find_sector

Due to the different switching time equations, a reference voltage sector is necessary. The sector finder (SF) module in this design is used to judge the reference vector sector by referring to Table 2. This module determines the number of sectors and simplifies the truth table by comparing the above-mentioned results.

3.4. Fourth Module: SVM_generator

This module was divided into four sub-modules, namely Triangle, Duration_Ta, Duration_TaTb, and SVM pattern modules. The Triangle module functions as a triangle signal generator. In the proposed SVM design, one period of triangle signal generation is sampled 32 times and is represented in the digital number of 9 unsigned bits with lower (in this case, it is the same with the base number) and upper numbers of 224 and 352, respectively. The Duration_Ta and Duration_TaTb modules are digital solutions for each second and fourth column, respectively. Finally, the SVM pattern module is used to generate the SVM sequence as described in Section 2.4.

3.5. Fifth Module: deadtime_system

A dead-time of at least 2 $\mu$s is required to avoid short circuit within a leg. A combination
of a 16-bit counter and a 16-bit comparator is used to construct the dead-time generator for each leg.

4. Results and Discussions

In this research, the proposed SVM generator with different carrier frequencies was successfully carried out using the APEX20KE Altera FPGA. Figure 4 shows the results from hardware implementation with this proposed SVM generating method at carrier frequency of 20 kHz. Probes 1, 2, and 3 in Figures 4(a) and 4(b) are represented as switching states of $S_a$, $S_b$, and $S_c$, respectively, whereby probe $M$ is a $(S_a + S_b)$ line-to-line switching state with its frequency spectrum. The harmonics due to the 20 kHz switching frequency are clearly visible in Figure 4(b).

A similar condition is shown in Figure 5. In this case, the carrier frequency is set to 40 kHz, although the result in Figure 5(b) shows 38.5 kHz (an error of 3.75%).

Figure 4. Hardware implementation of proposed SVM generator at carrier frequency 20 kHz: (a) the switching state and its line to line and (b) the signal gating and its frequency spectrum.

Figure 5. Hardware implementation of proposed SVM generator at carrier frequency 40 kHz: (a) the switching signals and line-to-line switching and (b) the signal gating and its frequency spectrum.
three-phase inverter system together with an induction machine of 1.5 kW is used to test the performance for the proposed SVM-generator-based FPGA design.

Figure 6 shows the practical result for output stator current ($I_a$), output phase-to-phase voltage ($V_{ab}$), frequency spectrum, output three-phase current, and output voltage line-to-neutral ($V_{an}$). The results show that this proposed SVM-generator-based FPGA design is successful when implemented through a hardware platform.

Furthermore, a comparison of current and voltage THD between the proposed SVM and other SVMs is shown in Table 4. From the table, the proposed SVM shows a lower percentage in current and voltage THD compared with other SVMs. However, the current THD from the proposed SVM (6.4%) is slightly higher than the hybrid type IV proposed by Zhao et al. [40], which is 6.34%. In addition, the voltage THD is 11.10% and is slightly higher than the pattern III proposed by Bharatiraja et al. [34] with 9.90%.

5. Conclusion

This article mainly presents the design and realization of a simple five-segment discontinuous SVM based on the application of an FPGA. The judging of sectors and the calculation of the firing time to generate the SVM waveform become simpler, and switching losses can also be reduced by using this new approach of SVM-based
Table 4
Comparison of current and voltage THD between the proposed SVM and other SVMs

<table>
<thead>
<tr>
<th>Strategy</th>
<th>Current THD (%)</th>
<th>Voltage THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed SVM based on FPGA</td>
<td><strong>6.4</strong></td>
<td><strong>11.10</strong></td>
</tr>
<tr>
<td>Bharatiraja et al. [34]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pattern I</td>
<td>15.07</td>
<td>17.60</td>
</tr>
<tr>
<td>Pattern II</td>
<td>19.31</td>
<td><strong>9.90</strong></td>
</tr>
<tr>
<td>Pattern III</td>
<td>23.96</td>
<td>24.27</td>
</tr>
<tr>
<td>Saad et al. [39]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rising-edge aligned sequence scheme (SVM1)</td>
<td>Not reported</td>
<td>54.49</td>
</tr>
<tr>
<td>Falling-edge aligned sequence scheme (SVM2)</td>
<td>Not reported</td>
<td>54.47</td>
</tr>
<tr>
<td>Symmetric aligned sequence scheme (SVM3)</td>
<td>Not reported</td>
<td>54.45</td>
</tr>
<tr>
<td>Alternative sequence scheme (SVM4)</td>
<td>Not reported</td>
<td>39.86</td>
</tr>
<tr>
<td>Zhang and Yu [31]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Three-segment SVM</td>
<td>Not reported</td>
<td>69.38</td>
</tr>
<tr>
<td>Five-segment SVM</td>
<td>Not reported</td>
<td>68.52</td>
</tr>
<tr>
<td>Seven-segment SVM</td>
<td>Not reported</td>
<td>66.59</td>
</tr>
<tr>
<td>Narayanan et al. [32]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conventional SVM</td>
<td>20.29</td>
<td>Not reported</td>
</tr>
<tr>
<td>Discontinuous SVM</td>
<td>15.37</td>
<td>Not reported</td>
</tr>
<tr>
<td>Three-zone hybrid PWM</td>
<td>13.00</td>
<td>Not reported</td>
</tr>
<tr>
<td>Five-zone hybrid PWM</td>
<td>12.72</td>
<td>Not reported</td>
</tr>
<tr>
<td>Seven-zone hybrid PWM</td>
<td>12.58</td>
<td>Not reported</td>
</tr>
<tr>
<td>Zhao et al. [40]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conventional SVM</td>
<td>10.07</td>
<td>Not reported</td>
</tr>
<tr>
<td>Minimum switching loss PWM (MSLPWM)</td>
<td>10.11</td>
<td>Not reported</td>
</tr>
<tr>
<td>Discontinuous SVM</td>
<td>7.64</td>
<td>Not reported</td>
</tr>
<tr>
<td>Hybrid type I</td>
<td>6.43</td>
<td>Not reported</td>
</tr>
<tr>
<td>Hybrid type IV</td>
<td><strong>6.34</strong></td>
<td>Not reported</td>
</tr>
</tbody>
</table>

FPGA. The proposed SVM scheme has been successfully designed and implemented through the APEX20KE Altera FPGA without computing the number and angles of each sector as well as the commutation pattern. A three-phase inverter system loaded by an induction machine of 1.5 kW was successfully driven by the proposed design with a carrier frequency up to 40 kHz.

References


